OAK RIDGE NATIONAL LABORATORY
operated by
UNION CARBIDE CORPORATION
NUCLEAR DIVISION
for the
U.S. ATOMIC ENERGY COMMISSION

ORNL-TM-1638
Part 9
COPY NO. - 69
DATE - March 25, 1968

NUCLEAR INSTRUMENT MODULE MAINTENANCE MANUAL

PART 9

FAST TRIP COMPARATOR, ORNL MODEL Q-2609

J. L. Anderson

ABSTRACT

The circuit, application, maintenance procedures, and acceptance tests for a Fast Trip Comparator are described. The comparator is intended for use in the safety or control systems of nuclear reactors to provide voltage level discrimination of safety or control signal inputs. The circuit is bistable in nature; that is, there is no change in output indication until the predetermined "trip" level is exceeded, at which time the output suddenly changes from one state to the other. Both logic-level and relay outputs are available. By simple jumpering of connector plus, the circuit can be arranged for either positive or negative inputs with either increasing or decreasing sense.

The comparator is packaged in a standard "one-unit" plug-in module of the ORNL Modular Reactor Instrumentation Series, Q-2600.

CONTENTS

1. DESCRIPTION

1.1 General

The Fast Trip Comparator circuit compares the magnitude of two input dc signals having opposite polarities and produces an output voltage having either of two possible values, depending upon which input voltage is larger. Two electronic outputs drive logic circuits external to this unit, and there are also two relay drivers within the unit. The change in voltage from one level to the other is completed in less than 200 μsec after the trip signal occurs. The relays can change states in approximately 10 msec. Each relay has one set of contacts for external connections and one set to perform an indicating function on the front panel. One relay can be connected to hold a trip indication after the trip has cleared, and the other relay indicates the immediate state of the circuit.

Several external connections can be made that allow the circuit to trip for a variety of input conditions. With a reference serving as one signal, the circuit can trip on a positive or a negative input signal and on an increasing or decreasing signal. For the case of two external signals A and B, tripping action can take place when the magnitude of A is greater than or less than that of B, provided A and B have opposite polarities.

1.2 Construction

The Fast Trip Comparator is constructed in a single module 1.40 in. wide, 4.72 in. high, and 11.90 in. deep. It is a standard "one-unit" plug-in module of the Modular Reactor Instrumentation Series depicted on drawings Q-2600-1 through Q-2600-6.

The circuit is constructed on a printed circuit board mounted within a shielding enclosure with removable sides.

1.3 Application

The Fast Trip Comparator is intended primarily to be used as a voltage level discriminator for safety and control functions in a nuclear reactor. For maximum flexibility, the unit has two inputs so that it may be used either to compare two signals or to compare one signal with an external reference. The circuit is bistable in nature; that is, there is no change in output indication until the predetermined "trip" level is exceeded, at which time the output suddenly changes from one state to the other. The trip level is nominally zero volts; that is, the two inputs must be of opposite polarity so that when the magnitude of one input exceeds the magnitude of the other, the circuit will change state. By use of suitable external jumpers, the circuit can be arranged to trip on either net positive or net negative input.

Two types of output are available. The logic output, intended for use in fast safety systems, is -10 v normally and 0 v when tripped. The switching time is less than 200 μsec. Normally, the logic level will revert to normal as soon as the input signal drops below the trip level. However, by use of external jumpers, the circuit can be made to latch, or seal, the logic output in the trip state until manually reset, provided the trip signal persists for 10 msec or more.

The second type of output is provided by two relays. Both relays are driven by the logic signal described previously and respond accordingly. K1 may be arranged to latch if the trip signal persists for more than 10 msec; the relay will go to the trip state and remain there until manually reset, regardless of whether or not the logic level signal is arranged to latch. This arrangement is sometimes called a "scram catcher," in that it allows a momentary trip to be located and identified after it has disappeared. K2 operates directly off the logic signal and will be in the same state. Contacts of both relays are available for actuating external circuits.

1.4 Specifications

1. Trip range: The trip range shall be adjustable from +1 to +10 v or from -1 to -10 v.

2. Trip point accuracy: Once the trip point has been set, variations in temperature from 10 to 55°C and aging of components should not cause the trip point to change more than 50 mv referred to the trip-circuit input signal.

3. Trip point hysteresis: When the signal falls 60 mv below the trip point, the circuit shall reset itself. The circuit shall not reset less than 40 mv below the trip point.

4. Input impedance: 150 kilohms, either input.

5. Logic output: In the normal state, the logic level output shall be -10 ± 1/2 v, 20 ma maximum drain. In the trip state, the logic level output shall be 0 ± 1/2 v.

6. Tripping time-logic level: The change from normal to abnormal condition (-10 to 0 v) shall require at least 100 μsec, but less than 200 μsec.

7. Relay outputs: Type 1 is a DPDT relay having contacts rated 2 amp at 32 v dc and 2 amp at

115 v ac. This relay must change state in less than 100 msec.

Type 2 is a fast-latching relay that will operate in less than 10 msec. The purpose of this relay is to indicate the location of a momentary trip signal.

8.	Power required:	+15 ± 0.25 v dc with regulation of 0.1%. -15 ± 0.25 v dc with regulation of 0.1%. +10 ± 0.1 v dc with regulation of 0.1%. -32 ± 4 v dc, unregulated.
9.	Ambient temperature range:	10 to 55°C.
10.	Indication:	Front-panel indicator lights shall show the immediate state of the trip, that is, "Trip" or "Normal," and also "Latch," which indicates that a momentary trip of 10 msec or more has occurred.
11.	Test and reset:	Front-panel pushbuttons shall cause the circuit to trip regardless of the input signal ("Test") and to reset the latch indication ("Reset").

1.5 Applicable Drawings and Specifications

The following list gives the drawing numbers (ORNL Instrumentation and Controls Division drawing numbers) and subtitles and fabrication specification number for the Fast Trip Comparator:

1.	Q-2609-1	Circuit.
2.	Q-2609-2	Details.
3.	Q-2609-3	Metalphoto Panel.
4.	Q-2609-4	Printed Circuit Board.
5.	Q-2609-5	Assembly.
6.	Q-2609-6	Parts List.
7.	SF-253	Fabrication Specification.

The following list gives the drawing numbers and subtitles for the Plug-In Chassis System:

1. Q-2600-1 Assembly.
2. Q-2600-2 Details.
3. Q-2600-3 Details.
4. Q-2600-4 Details.
5. Q-2600-5 Details.
6. Q-2600-6 Details.

2. THEORY OF OPERATION

2.1 General

The Fast Trip Comparator is composed of three functional parts: a voltage comparator, logic switching circuits, and relay drivers (Fig. 1).

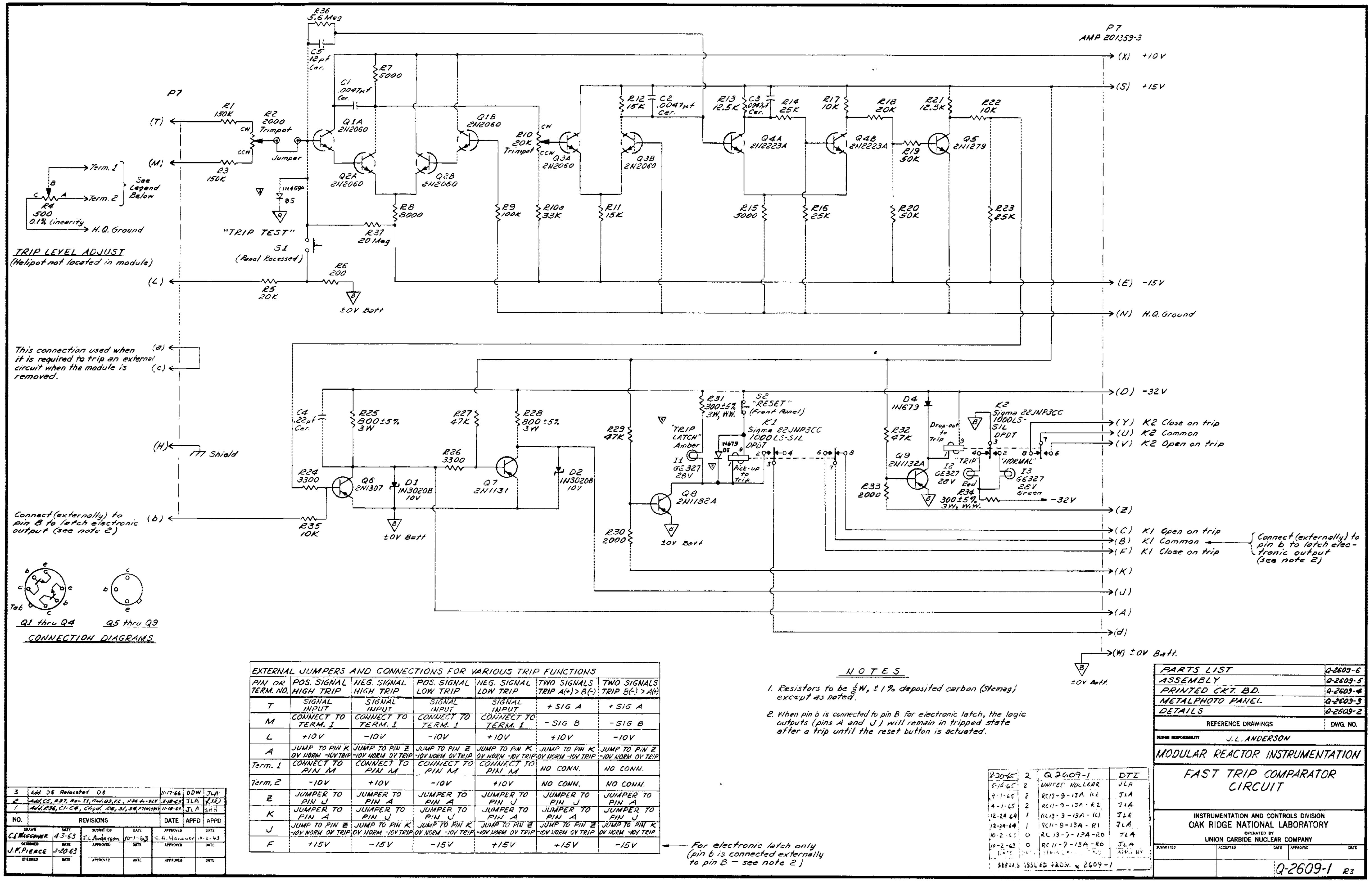
The input stage consisting of Q1 and Q2 is a compound (Darlington) differential amplifier having a high degree of temperature stability and a high input impedance. This stage drives a simple differential amplifier Q3 which, in turn, drives a Schmitt trigger circuit Q4. These three stages make up the voltage comparator.

All transistors after the Schmitt trigger circuit act as switches and are either off (open) or saturated (closed). Transistor Q5 acts as a buffer to prevent the Schmitt trigger circuit from being affected by variations in the load. Electronic output points are located at the collectors of Q6 and Q7.

Two double-pole, double-throw relays K1 and K2 each provide one set of contacts for the operation of external circuits and one set for the operation of indicator lamps on the front panel of the trip circuit. Relay K1 can be connected to hold the "Latch" indicator lamp I1 from the time a trip has occurred until the manual reset switch S2 has been depressed, even if the signal level decreases below the trip point. Relay K2 energizes indicator lamp I2 ("Trip") or I3 ("Normal"), depending upon the existing state of the circuit. Either or both of the relay drivers Q8 and Q9 can be driven from either electronic output. For operational flexibility, the connections to the electronic outputs and the relay drivers are made externally through the rear connector P7. The following sections provide a detailed discussion of the design and operation of the various stages of the circuit.

2.2 The Voltage Comparator

The input stage Q1 and Q2 is a compound differential amplifier. The compounding Q1 provides high input impedance. The two inputs are applied



EXTERNAL JUMPERS AND CONNECTIONS FOR VARIOUS TRIP FUNCTIONS						
PIN OR TERM. NO.	POS. SIGNAL HIGH TRIP	NEG. SIGNAL HIGH TRIP	POS. SIGNAL LOW TRIP	NEG. SIGNAL LOW TRIP	TWO SIGNALS TRIP A(+) > B(-)	TWO SIGNALS TRIP B(-) > A(+)
T	SIGNAL INPUT	SIGNAL INPUT	SIGNAL INPUT	SIGNAL INPUT	+ SIG A	+ SIG A
M	CONNECT TO TERM. 1	CONNECT TO TERM. 1	CONNECT TO TERM. 1	CONNECT TO TERM. 1	- SIG B	- SIG B
L	+10V	-10V	-10V	+10V	+10V	-10V
A	JUMP TO PIN K 0V NORM -10V TRIP	JUMP TO PIN Z -10V NORM 0V TRIP	JUMP TO PIN Z -10V NORM 0V TRIP	JUMP TO PIN K 0V NORM -10V TRIP	JUMP TO PIN K 0V NORM -10V TRIP	JUMP TO PIN Z -10V NORM 0V TRIP
Term. 1	CONNECT TO PIN M	CONNECT TO PIN M	CONNECT TO PIN M	CONNECT TO PIN M	NO CONN.	NO CONN.
Term. 2	-10V	+10V	-10V	+10V	NO CONN.	NO CONN.
Z	JUMPER TO PIN J	JUMPER TO PIN A	JUMPER TO PIN A	JUMPER TO PIN J	JUMPER TO PIN J	JUMPER TO PIN A
K	JUMPER TO PIN A	JUMPER TO PIN J	JUMPER TO PIN J	JUMPER TO PIN A	JUMPER TO PIN A	JUMPER TO PIN J
J	JUMP TO PIN Z -10V NORM 0V TRIP	JUMP TO PIN K 0V NORM -10V TRIP	JUMP TO PIN K 0V NORM -10V TRIP	JUMP TO PIN Z -10V NORM 0V TRIP	JUMP TO PIN Z -10V NORM 0V TRIP	JUMP TO PIN K 0V NORM -10V TRIP
F	+15V	-15V	-15V	+15V	+15V	-15V

Fig. 1. Fast Trip Comparator Circuit.

to a single base, rather than differentially to the two bases, so that no shift in output will occur when the two inputs are of equal magnitude at various levels from -10 to +10 v. The 2-kilohm trimming adjustment R2 is used to balance the input resistors R1 and R3. The output of the first stage appears at the collector of Q2A and is coupled to the second stage through R10 and R10a. Diode D5 provides protection against overvoltage at the input.

The second stage Q3 is a simple differential amplifier that provides additional voltage gain to increase the sensitivity of the amplifier. Overall negative feedback is employed from the collector of Q3B to the base of Q1A (R36) to adjust the sensitivity to the desired level and to improve the temperature-drift characteristics. The dc level is adjusted by Trimpot R10 to establish the correct trip point.

The output of the second stage Q3 is directly coupled to the Schmitt trigger circuit Q4. The Schmitt trigger circuit is a regenerative bistable circuit that provides the actual voltage level discrimination. The output of the Schmitt trigger circuit and all succeeding stages have only two stable states, "Normal" and "Trip."

2.3 Logic Switching Circuits

Loading effects on the Schmitt trigger circuits are buffered by an isolation stage Q5. The bistable signal is then coupled to Q6 where the logic levels are established. When the collector of Q5 (and the base of Q6) is in the "high," or more positive state, Q6 is biased off, allowing Zener diode D1 to be fired through R25. The logic level output at pin A of P7 is then -10 v, as determined by the break-down voltage of D1.

In the "low" state, when the voltage at the base of Q6 is less positive (actually slightly negative), Q6 is saturated, shunting Zener diode D1; and the magnitude of the output at pin A is near zero (less than 0.2 v). The Q7 stage is nearly identical to Q6 and provides an inverted logic level output for maximum flexibility; that is, when the level at pin A is -10 v, Q7 is saturated, producing "zero" level at pin J. Conversely, when the level at pin A is "zero," Q7 is cut off and the output at pin J is -10 v.

The inherent speed of response of the entire electronic circuit, from a sufficient level change at the input pin T to a logic level change at either pin A or pin J, is about 10 μsec. However, this speed of response has been intentionally lessened to about 120 μsec by capacitors C1 - C4 to reduce the tendency to respond to sharp noise spikes.

2.4 Relay Drivers

Either logic output may be connected to either or both of the two relay drivers Q8 and Q9. Normally K1 is intended to pick up when a trip (abnormal) condition exists. To accomplish this, the base of Q8 is connected through R30 and pin K of P7 to a logic output that is at -10 v in the "Trip" state, namely, either pin A or pin J. Note that "Trip" and "Normal" are related to the character of the input signal, and refer to a signal which may be either too large or too small and either positive or negative. The proper connections for a desired signal and function can be determined by referring to the connection table on circuit diagram Q-2609-1 (Fig. 1).

One set of contacts of K1 is used to latch-in the coil of K1 to keep it energized after a trip has occurred and cleared. This optional function is accomplished by connecting pin d of P7 to battery ground (pin W).

Relay K2, driven by Q9, is normally connected so as to drop out in the trip state. This relay is intended to show the immediate state, and no provisions are made to latch it.

One set of form-C contacts is available from each relay to operate external circuits.

The logic level output may be latched in the trip state by using the output contacts of relay K1. Pin b is connected to pin B, and either positive or negative 15 v is connected to pin F, depending upon the nature of the input signal. When this connection is used, K2 also latches, because it is driven by the logic signals.

3. OPERATING INSTRUCTIONS

3.1 Installation

The Fast Trip Comparator Q-2609 is a module in the ORNL Modular Reactor Instrumentation Series. Like the other modules of the series, it has standard connectors and dimensions and has a pin- and hole-code on the rear plate so that the module will not be inserted in a wrong location in a drawer. The module is installed by placing it in its proper location, inserting the module firmly, and tightening the thumb screw. The module may be plugged in with power on without damage.

3.2 Operating Controls

The only integral operating controls are the "Trip Test" pushbutton and the "Reset" pushbutton. The "Trip Test" pushbutton causes the circuit to trip by overriding the input signal. The circuit will remain in the trip position if the screw-driver actuated pushbutton is rotated clockwise after being depressed.

"Reset" is a momentary pushbutton that releases relay K1 and the "Latch" indication.

In a good many applications of the Fast Trip Comparator, a single signal will be compared against a reference. The reference can be fixed by a simple external voltage divider, or it can be adjusted by means of a Helipot located in the drawer into which the trip circuit is plugged. This adjustment is shown on the circuit diagram as R4 and is, in effect, an operating control of the trip circuit.

3.3 Connections

All connections to the Fast Trip Comparator are made through the rear connector P7 when the module is inserted. After initial calibration is completed, there are no adjustments or connections to be made within the module itself. However, a high degree of flexibility is provided through external connections. The various possible modes of operation and the connections required to achieve them are detailed in the connection table on circuit diagram Q-2609-1 (Fig. 1) and in the following section.

3.4 Operating Procedures

3.4.1 Input Signals

The input signals to the trip circuit should be supplied from a low impedance source (500 ohms or less). A single signal may be either positive or negative within the range of ±10 v. The magnitude of two different signals may be compared, but they must be of opposite polarity. The input terminal for a single signal is pin T, and an external reference voltage of opposite polarity is required on pin M. If two signals are compared, the reference voltage is not required, and the second signal is connected to pin M.

3.4.2 Reference Voltage

The external reference voltage is required on pin M when the input is a single signal. This reference must be exactly equal in magnitude to the desired signal trip point and of opposite polarity. The source impedance should be 500 ohms or less. In applications where the trip point is to be changed occassionally, the reference may be derived from a 500-ohm precision potentiometer connected to a 10-v supply. A potentiometer with 0.1% linearity will be sufficiently accurate to allow direct reading of the potentiometer dial as the trip voltage. Such a potentiometer is shown on the circuit diagram as R4.

In applications where infrequent or no changes in trip point are anticipated, the reference should be derived from a 10-v supply and a fixed-voltage divider with a total series resistance of approximately 500 ohms.

It should be noted that, within the accuracy specifications of the trip comparator, the trip point is directly equal in magnitude to the reference voltage, and any drift or inaccuracy of the reference will result in equal error of the trip point. The accuracy specifications do not apply in the range -1 to 0 to +1 v, and adjusting the reference to a trip point in this range should be avoided.

3.4.3 Signal Polarity and Direction

Different external connections are required for different types of input signals to achieve proper output sense. These connections are shown in the table on the circuit diagram. The column headings refer to the nature of the signal; for example, the second column is headed "Pos. Signal, High Trip." This means that the input signal may range from 0 to +10 v, and trip will occur when the signal is greater in magnitude than the reference. The fifth column is headed "Neg. Signal, Low Trip," which means that the signal range is 0 to -10 v, and that trip occurs when the signal is smaller in magnitude than the reference. The column entries under the selected heading show the voltage or destination for the pin or terminal in the same row of column 1 on the left.

The preceding discussion of the second column labeled "Pos. Signal, High Trip," is continued. The first row shows pin T as the signal input. Pin M connects to terminal 1, which is the wiper of the reference potentiometer. Pin M could go instead to the pick-off tap of a fixed divider if a fixed trip point is desired. Pin L connects to +10 v to provide the proper test voltage. Pin A is jumpered to pin K to provide proper drive to Q8. Pin J is jumpered to pin Z to provide proper drive to Q9 and is also the correct logic level output for driving external circuits.

3.4.4 Latching

Latching instructions are not shown in the table, but they are shown at the appropriate connector pins on the circuit diagram. With no latching, K1, K2, and the logic level outputs will all indicate the immediate state of the comparator. Connecting pin d to battery ground causes only K1 to latch, that is, to remain in the trip state, after a trip signal has cleared, until the reset button is pressed.

If it is desired to also latch the logic level outputs in the same manner, it is necessary to jumper pin b to pin B and connect an appropriate voltage to pin F as shown in the table. In this condition, all outputs, K1, K2, and both logic levels will latch and remain in the trip state after a trip-level signal occurs.

3.5 Precautions

3.5.1 Relay Contacts

The contacts of the relays used in the Fast Trip Comparator circuit are rated for resistive loads only. If inductive loads are necessary, appropriate contact-arc-suppression techniques should be employed.

3.5.2 Transistors

Some of the transistors used in the circuit unavoidably have small reverse base-emitter voltage ratings. Most ordinary laboratory-type ohmmeters, such as the Triplett 630 or the Simpson 260, have sufficiently high voltage on some resistance scales to permanently damage these transistors. The common practice of using an ohmmeter to check transistors when troubleshooting should be avoided in this unit.

3.5.3 Trip Point Near Zero Volts

The trip-point accuracy specifications do not apply at trip voltages near zero. Due to possible inaccuracy, trip points between -1 and +1 v should be avoided.

4. MAINTENANCE INSTRUCTIONS

4.1 General

This module is designed to operate continuously with a minimum of maintenance and adjustment. No periodic adjustments are required. The two internal trimming potentiometers should be adjusted only during initial calibration or during subsequent recalibrations after circuit damage or failure has occurred. Should a failure occur, any part listed in the Replaceable Parts List, Sect. 5, may be replaced. The calibration should be checked after any circuit repair.

4.2 Periodic Maintenance

No specific periodic maintenance is required. It is presumed that the accuracy of the trip point (external reference) and the operability of the Fast Trip Comparator will be checked periodically as part of the routine tests of the system, of which the Comparator is a part.

4.3 Calibration

4.3.1 Instruments Required

The following special instruments are required to calibrate the Fast Trip Comparator:

1. Power supplies for +32 ± 4 v dc and -32 ± 4 v dc; and a Power Supply Drawer Q-2626-7A, complete with voltage-regulator modules Q-2619, Q-2620, and Q-2621.

The power supplies of the Modular Reactor Instrumentation Series should normally be used with the Fast Trip Comparator. It is recommended that these supplies be used to calibrate the Comparator; however, the use of these supplies is not absolutely necessary, and the required voltages may be obtained from suitable general purpose supplies. The voltages required are:

a. +10 ± 0.1 v dc, regulation 0.1%;

b. -10 ± 0.1 v dc, regulation 0.1%;

c. +15 ± 0.25 v dc, regulation 0.1%;

d. -15 ± 0.25 v dc, regulation 0.1%;

e. -32 ± 4 v dc, unregulated.

2. Digital voltmeter with sensitivity and absolute accuracy of 1 mv or better, Cubic Corporation, model V-71, or equal.

3. Trip Circuit Tester, a special test jig shown schematically in Figs. 2 and 3.

4.3.2 Calibration Procedure

1. Remove the jumper between the base of Q1A and R2 (2-kilohm Trimpot) wiper. Disconnect the ends of R36 and C5 that are connected to R2. Resolder a short piece of wire to the wiper of R2.

2. Connect the trip circuit tester as diagrammed in Figs. 2 and 3; turn on the power supplies, and adjust the voltages to the desired values as accurately as possible, as measured with the digital voltmeter.

3. Set the reference potentiometer on the tester to exactly 500 divisions.

4. Connect the Fast Trip Comparator to be calibrated to the tester.

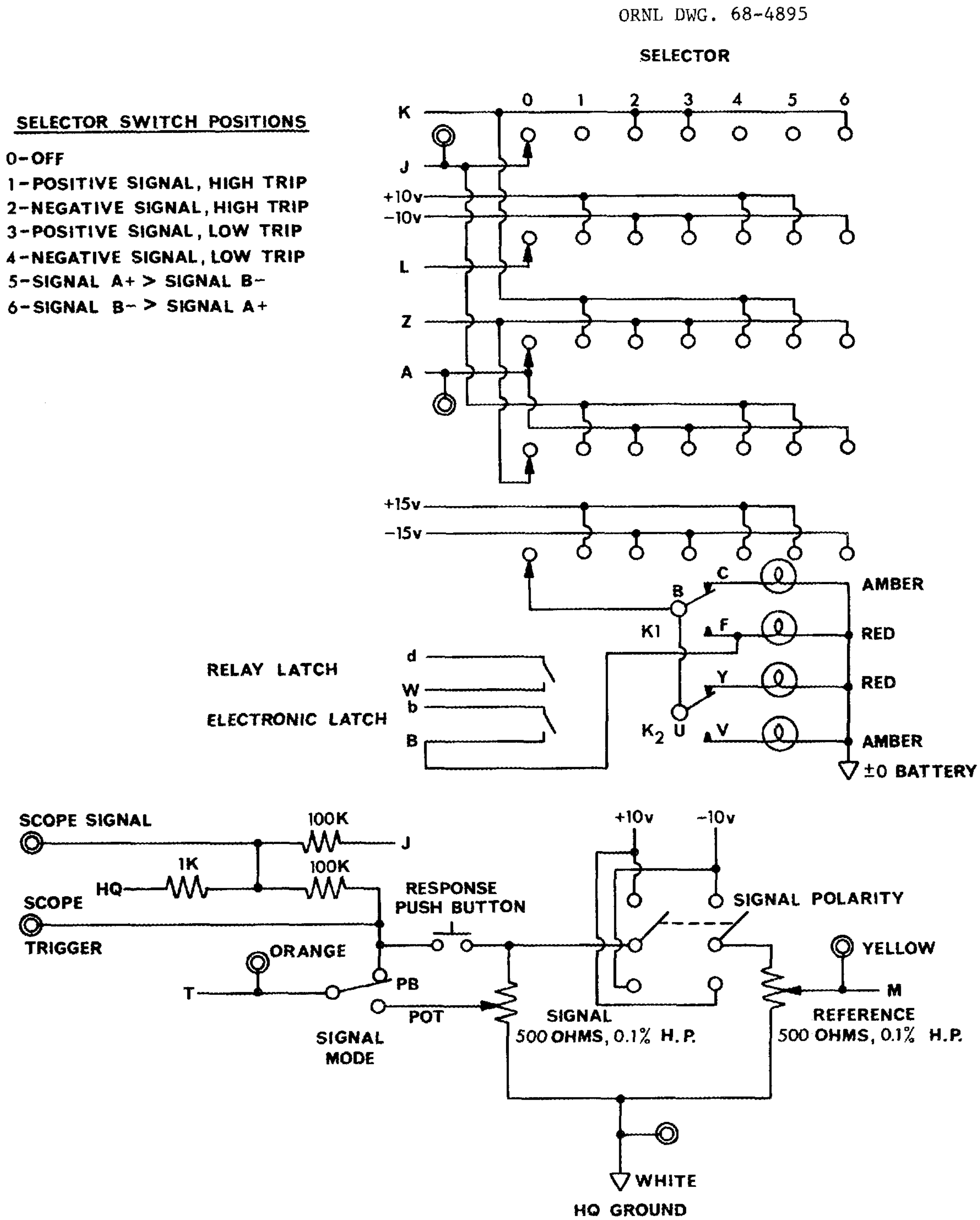


Fig. 2. Circuit for Tester Unit for Fast Trip Comparator, ORNL Model Q-2609.

ORNL DWG. 68-4896

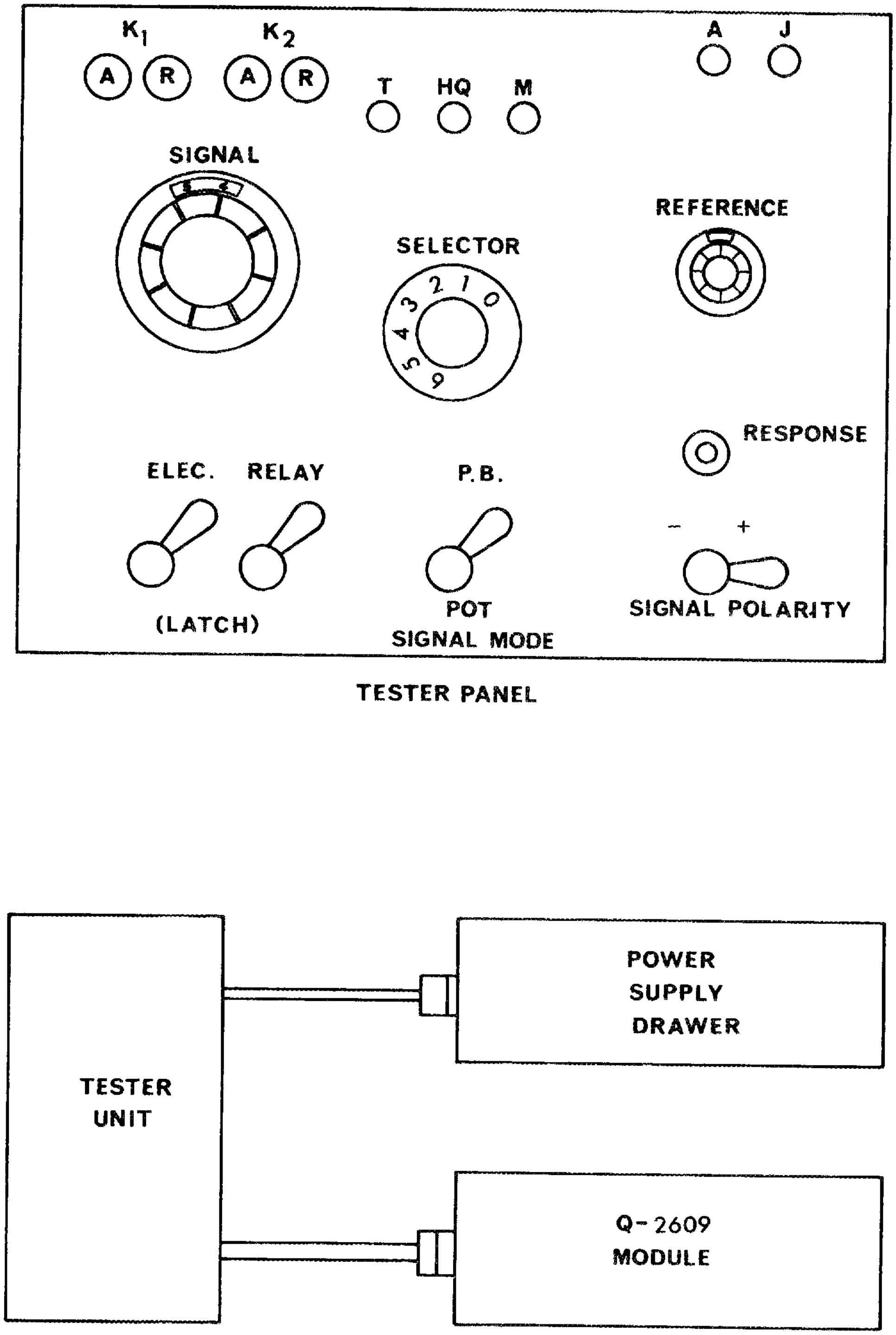


Fig. 3. Tester Unit for Fast Trip Comparator, ORNL Model Q-2609.

5. Connect the digital voltmeter to the test jacks T (orange), and readjust the reference potentiometer until the voltmeter indicates -5.000 v.

6. Move one digital voltmeter lead from test jack T (orange) to jack M (yellow), and adjust the signal potentiometer of the tester until the voltmeter indicates +5.000 v.

7. Connect the voltmeter between the wiper of R2 (short piece of wire provided in Step 1) and HQ ground. Adjust R2 (2-kilohm Trimpot) until the voltmeter indicates 0.000 v.

8. Disconnect the module from the tester, and restore all connections removed in Step 1.

9. Reconnect the module to the tester. Note that, after the jumper has been resoldered, the voltage between the jumper (R2 wiper) and HQ ground will no longer be zero for equal input voltages owing to transistor base current. Do not readjust to zero!

10. Set the selector switch of the tester to position No. 1 (positive signal, high trip), and set the signal switch to positive.

11. Connect the digital voltmeter between test jack T (signal) and HQ ground. Adjust the signal potentiometer until the meter indicates +5.025 v. Adjust R10 (20-kilohm Trimpot) until the comparator just trips, as indicated by the panel lights.

12. Slowly decrease the setting of the signal potentiometer on the tester and observe the signal voltage when the trip just clears. The signal voltage should be +4.975 ± 0.010 v when the trip clears. This represents hysteresis of from 40 to 60 mv.

13. Increase the signal potentiometer until the comparator just trips again. If trip does not occur at 5.025 ± 0.003 v, readjust R10 slightly and recheck. Several readjustments may be required to achieve proper results. There is no adjustment to change the hysteresis, and values less than 40 mv or greater than 60 mv indicate components out of tolerance in the amplifier stages of the comparator.

14. Set the selector switch of the tester to position No. 2 (negative signal, high trip), and set the signal polarity switch to negative.

15. Measure the voltage at test jack M, and readjust if necessary to +5.000 v.

16. Measure the signal voltages (jack T) at trip and untrip as done previously for positive signals. Trip should occur at -5.025 ± 0.010 v. Dropout, or untrip, should occur at -4.975 ± 0.010 v.

This completes the calibration procedure, but it is recommended that the module be given a complete acceptance test (Sect. 6) after calibration and before being placed in service.

4.4 Transistor Voltage Chart

The voltages of all transistors are listed in Table 1.

Table 1. Transistor Voltage Chart[1]

Transistor	Emitter	Base	Collector
Q1A	-0.555/-0.553	-0.023/-0.025	+10.00/+10.00
Q1B	-0.555/-0.554	-0.027/-0.027	+10.00/+10.00
Q2A	-1.184/-1.185	-0.551/-0.553	+4.064/+4.135
Q2B	-1.181/-1.186	-0.552/-0.553	+10.00/+10.00
Q3A	-0.613/-0.603	-0.041/-0.010	+15.00/+15.00
Q3B	-0.612/-0.601	+0.001/+0.001	+3.312/+5.020
Q4A	+4.290/+4.407	+3.312/+5.020	+11.63/+4.542
Q4B	+4.290/+4.407	+4.907/+2.248	+4.408/+10.99
Q5	0/0	-1.115/+0.665	+7.060/+0.153
Q6	0/0	+0.759/-0.279	-9.960/-0.175
Q7	0/0	-0.744/+0.817	-0.325/-10.27
Q8	0/0	-0.874/+0.440	-0.350/-32.00
Q9	0/0	+0.304/-0.829	-32.00/-0.171
Pin T	+5.025/+4.975	-	-
Pin M	-5.000/-5.000	-	-

[1]All dc voltages on Q1-Q5 were measured with respect to HQ ground, and on Q6-Q9 with respect to ±0 battery ground with a digital voltmeter (Cubic Corp., model V-71, or equal). In each case the first value listed is with the input adjusted to just cause "trip." The second value is with the input reduced until the circuit just "untrips."

5. REPLACEABLE PARTS LIST

A description and an ORNL Stores number for replaceable parts are given in Table 2. Since the original group of modules was manufactured the "Stemag," carbon-film resistors have been discontinued as ORNL Stores items. The presently stocked precision metal-film resistors are equal or superior to Stemag resistors and may be substituted.

Table 2. Replaceable Parts List

Parts No.	ORNL Stores No.	Description
Q1, 2, 3	-	Transistor, dual NPN, type 2N2060.
Q4	-	Transistor, dual NPN, type 2N2223A (2N2060 will substitute directly).
Q5	06-996-1880	Transistor, NPN, type 2N1279.
Q6	06-996-1960	Transistor, PNP, type 2N1307.
Q7	06-996-1710	Transistor, PNP, type @n1131.
Q8, 9	-	Transistor, PNP, type 2N1132A.
D1, 2	06-995-7094	Diode, Zener, 10 v ± 5%, type 1N3020B.
D3, 4	06-995-6160	Diode, Silicon, 1N679.
D5	06-995-5860	Diode, Silicon, 1N959A.
C1, 2, 3	06-802-0405	Capacitor, 0.0047 mf ± 20%, 1000 v fixed ceramic disc.
C4	06-802-0095	Capacitor, 0.22 mf, ± 20%, 50 v fixed ceramic, insulated.
C5	06-802-0270	Capacitor, 10 pf ± 10%, 1000 v, fixed ceramic, insulated.
R1, 3	06-932-0195	Resistor, 150 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R2	06-930-8210	Potentiometer, trimmer, 2000 ohms ± 10%, 1-1/2 w, conductive glass resistance element, "Helitrim" series 53 with printed circuit pins, Helipot Division.

Table 2. (continued)

Part No.	ORNL Stores No.	Description
R5, 18	06-932-0155	Resistor, 20 kilohm ± 1%, 1/2 w, Stemag, type SLAK.
R6	06-932-0057	Resistor, 200 ohms ± 1%, 1/2 w, Stemag, type SLAK.
R7, 15	06-932-0133	Resistor, 5000 ohms ± 1%, 1/2 w, Stemag, type SLAK.
R8	06-932-0143	Resistor, 8000 ohms ± 1%, 1/2 w, Stemag, type SLAK.
R9	06-932-0189	Resistor, 100 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R10	06-930-8216	Potentiometer, trimmer, 20 kilohms ± 10%, 1-1/2 w, conductive glass resistance element, "Helitrim" series 53 with printed circuit pins, Helipot Division.
R10a	06-932-0169	Resistor, 33 kilohms ±%, 1/2 w, Stemag, type SLAK.
R11, 12	06-932-0151	Resistor, 15 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R13, 21	06-932-0149	Resistor, 12.5 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R14, 16, 23	06-932-0161	Resistor, 25 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R17, 22, 35	06-932-0147	Resistor, 10 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R19, 20	06-932-0175	Resistor, 50 kilohms ± 1%, 1/2 w, Stemag, type SLAK.
R24, 26	06-932-0127	Resistor, 3300 ohms ± 1%, 1/2 w, Stemag, type SLAK.
R25, 28	-	Resistor, 800 ohms ± 5%, 3 w, ww, vitreous enamel insulation, Ohmite code 7/16-A-54-F.
R27, 29, 32	06-932-0173	Resistor, 47 kilohms ± 1%, 1/2 w, Stemag type SLAK.

Table 2. (continued)

Part No.	ORNL Stores No.	Description
R30, 33	06-932-0113	Resistor, 2000 ohms ± 1%, 1/2 w, Stemag type SLAK.
R31, 34	06-933-6250	Resistor, 300 ohms ± 5%, 3 w, ww, vitreous enamel insulation, Ohmite code 7/16-A-54-F.
R36	06-932-0359	Resistor, 5.6 megohms ± 1%, 1/2 w, Texas Instruments, type CD-1/2-SR.
R37	-	Resistor, 20 megohms ± 5%, 1/2 w, carbon composition.
K1, 2	-	Relay, DPDT, 2 amp at 28 v dc resistive load, 1000-ohm coil resistance, adjustment LS, silver contacts, 5 ma dc operate current, Sigma type 22 JNP 3CC-1000-LS-SIL.
I1	06-918-2150	Lens cap, amber, for use with T1-3/4 incandescent lamp, Dialco No. 101-973.
I2	06-918-2149	Lens cap, red, for use tith T1-3/4 incandescent lamp, Dialco No. 101-971.
I3	06-918-2147	Lens cap, green, for use with T1-3/4 incandescent lamp, Dialco No. 101-972.
I1, 2, 3	06-916-2576	Lamp, incandescent, 28 v at 40 ma, type 327, GE.

6. ACCEPTANCE TEST PROCEDURE

6.1 Test Equipment

The instruments required to perform acceptance tests of the Fast Trip Comparator are the same as those required for calibration and listed in Sect. 4.3.1. In addition, a dc-coupled oscilloscope with calibrated time base and external trigger and a laboratory-type temperature test chamber are required.

6.2 Adjustment Procedure

No adjustments are necessary except those performed during calibration.

6.3 Acceptance Test

6.3.1 Calibration

Calibrate the Fast Trip Comparator according to the procedure of Sect. 4.3.

6.3.2 Output Functions: Positive Signal, High Trip

1. Connect the module to the trip circuit tester and set the selector switch to position 1 and the signal switch to positive. The latch switches should be off and the mode switch at "Pot."

2. Increase the signal (turn potentiometer clockwise) until trip occurs. The red ("Trip") light and the amber ("Latch") light on the module front panel should be on, indicating that relay K1 is picked up and K2 is dropped out. The output contacts of K1 and K2 are monitored by the amber and red lights on the tester. The tester lights are red when the relays are picked up and amber when the relays are dropped out. These should be observed occasionally during the subsequent testing to ascertain that all relay contacts are making and breaking properly.

3. Measure the voltage between test jack A and ground. The voltage should be -10 ± 1/2 v.

4. Measure the voltage between test jack J and ground. The voltage should be 0 ± 1/2 v.

5. Decrease the signal to well below the trip point. Only the green ("Normal") light should be on. It should not be necessary to press the reset button.

6. Again measure the voltages at test jacks A and J. Jack A should now measure 0 ± 1/2 v, and jack J should measure -10 ± 1/2 v.

6.3.3 Relay Latch

1. Switch the "Relay Latch" switch on the tester to on and turn the signal potentiometer clockwise until the trip occurs. The "Trip" and "Latch" lights should be on.

2. Decrease the signal to below the trip point. The amber ("Latch") light should remain on, the red ("Trip") light should be off, and the green ("Normal") light should be on.

3. Measure the voltages at test jacks A and J. At A the voltage should be 0 ± 1/2 v and at J should be -10 ± 1/2 v.

4. Press the reset button S2 on the module, and again measure the voltages at A and J. They should not have changed, but the amber ("Latch") light should now be out.

6.3.4 Electronic Latch

1. Switch the "Electronic Latch" switch to on and the "Relay Latch" switch to off; increase the signal until trip occurs. The "Trip" and "Latch" lights should be on, and the "Normal" light should be off.

2. Measure the voltages at test jacks A and J. At A the voltage should be -10 ± 1/2 v and at J should be 0 ± 1/2 v.

3. Decrease the signal to well below the trip point. No changes should occur in either the state of the lights or of the voltages.

4. Press the reset button on the module. Only the green ("Normal") light should be on, and the voltages should have changed state to A = 0 ± 1/2 v and J = -10 ± 1/2 v.

6.3.5 Trip Test

1. Switch both latch switches to off and adjust the signal to well below the trip point.

2. With a screw driver, depress the "Test Trip" button S1. The "Trip" and "latch" lights should come on.

3. Rotate S1 one-eighth turn clockwise while it is depressed. This should lock the button in the depressed position, causing the trip condition to persist.

4. Release S1 by rotating it one-eighth turn counterclockwise and let it spring back. The circuit condition should revert to normal with only the green light on.

6.3.6 Output Functions: Negative Signal, High Trip

1. Turn the tester selector switch to position 2 and the signal polarity switch to Negative. The latch switches should be off.

2. Increase the signal potentiometer until trip occurs. With the reference potentiometer still set at 5.000, trip should occur at -5.025 ± 0.010 v measured at test jack T. In the trip condition, both the red and the amber lights should be on, and the voltage at test jack A should measure 0 ± 1/2 v.

3. Decrease the signal potentiometer until the circuit just switches to normal (only the green light on). The voltage at jack T should be -4.975 ± 0.010 v. If these trip and recover voltages do not check, repeat the positive-signal high-trip tests and check the trip point accuracy and hysteresis very carefully. If the hysteresis is out of tolerance, circuit repair or transistor substitution is indicated. If only the trip point accuracy is out of tolerance, recalibration should suffice.

6.3.7 Output Functions: Positive Signal, Low Trip

1. Place the tester selector switch in position 3 and the signal polarity switch to Positive. With the signal potentiometer well below 5 v, the circuit should be in the trip condition with 0 ± 1/2 v at test jack A.

2. Slowly increase the signal (turn the potentiometer clockwise) until the circuit untrips. The voltage at test jack T should be +5.025 ± 0.010 v (reference = -5.000 v). The voltage at jack A should be -10 ± 1.2 v.

3. Now decrease the signal (turn counterclockwise) until trip just occurs. The voltage at jack T should be +4.975 ± 0.020 v, and the trip and latch lights should be on.

6.3.8 Output Functions: Negative Signal, Low Trip

1. Place the tester selector switch in position 4 and the signal polarity switch to Negative. With the signal potentiometer well below 5 v, the circuit should be in the trip condition with 0 ± 1/2 v at test jack J.

2. Slowly increase the signal until the circuit untrips. The voltage at test jack T should be -5.025 ± 0.010 v (reference = +5.000 v). The voltage at jack J should be -10 ± 1/2 v.

3. Now decrease the signal until trip occurs. The voltage at jack T should be -4.975 ± 0.010 v, and the trip and latch lights should be on.

6.3.9 Dual Signal Trip

1. Place the tester selector switch in position 5 and the signal polarity switch to Positive. With the signal potentiometer well below 5 v, the circuit state should be normal. In this case the reference potentiometer represents signal B and should be at -5.000 v (jack M).

2. Increase the signal until trip occurs. The voltage at jack T should be +5.025 ± 0.003 v.

3. Place the tester selector switch in position 6 and the signal polarity switch to Positive. The circuit should now be in the normal state.

4. Decrease the signal until trip occurs. The voltage at jack T should be +4.975 ± 0.010 v.

6.3.10 Response Time

1. Connect an oscilloscope with a calibrated time base and external trigger provisions to the terminals on the rear of the tester labeled "Signal" and "Trigger." Set the tester selector switch to position 1; the signal should be on Positive, and the latch switches at Off. Adjust the reference potentiometer to 990.

2. Adjust the oscilloscope to 50 mv/cm sensitivity and 50 μsec/cm sweep, dc coupled. Depress the tester pushbutton repeatedly while adjusting the scope triggering and centering to obtain a display as shown in Fig. 4.

ORNL DWG. 68-4897

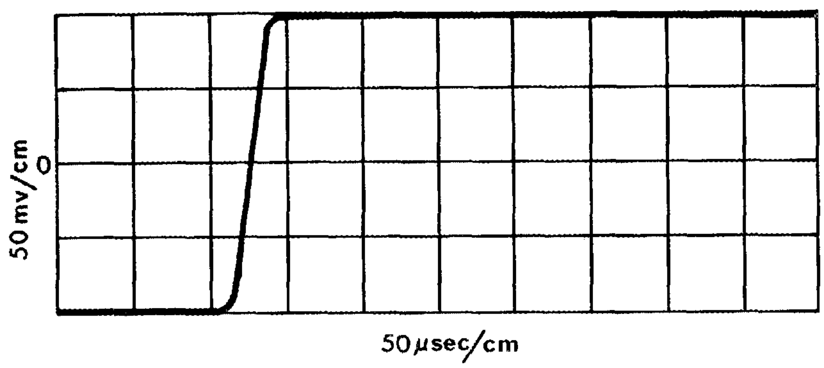


Fig. 4. Oscilloscope Presentation of Time Response.

The trace at approximately -100 mv represents the response or storage display of the amplifier stages of the comparator and is typically about 120 μsec. The transition from -100 to +100 mv represents the switching time of the bistable stages of the comparator, which is typically 10 μsec. The overall time from the beginning of the trace until the +100 mv level is reached represents the overall response time of the electronic, or logic level, output of the comparator and is typically about 130 μsec. This time must be less than 200 μsec.

6.3.11 Temperature and Input Range

1. Set the tester selector switch to position 1 and the signal polarity to Positive. The signal mode switch should be in the Pot position, and the latch switches should be off.

2. Adjust the reference potentiometer until the voltage indicated at jack M is exactly -1.000 v.

3. Increase the signal potentiometer adjustment from 000 until the circuit just trips. Measure and record the signal voltage as measured at test jack T. The voltage should be +1.025 ± 0.003 v.

4. Decrease the signal until the circuit just untrips, and measure and record the signal voltage at jack T. The voltage should be 40 to 60 mv less than the trip voltage.

5. Repeat the preceding procedures at reference voltages of -4.000, -7.000, and -9.500.

6. Place the Fast Trip Comparator module in a temperature test chamber and maintain the ambient air temperature at 55 ± 3°C for at least 15 min.

7. Repeat the trip-point accuracy and hysteresis measurements as described previously and compare them with the room-temperature measurements. Select the largest negative and the largest positive errors with respect to the references and add them together numerically. The total, which represents the total maximum extreme error of the comparator, should be less than 50 mv. The hysteresis at any reference voltage between 1 and 10 v and at any temperature between 0 and 55°C should be more than 40 but less than 60 mv.

ORNL-TM-1638
Part 9

INTERNAL DISTRIBUTION

1-20. J. L. Anderson
21. D. S. Asquith
22. A.E.G. Bates
23. A. L. Boch
24. C. J. Borkowski
25-34. W. D. Brown
35-36. C. T. Carney
37-39. O. C. Cole
40. T. E. Cole
41. B. L. Corbett
42. C. C. Courtney
43. R. A. Dandl
44. J. T. De Lorenzo
45. E. P. Epler
46. C. S. Harrill
47. C. F. Holloway
48. G. A. Holt
49. W. H. Jordan
50. W. E. Lingar
51. C. E. Mathews
52. T. L. McLean
53. R. V. McCord
54. L. C. Oakes
55. G. R. Owens
56. R. W. Peelle
57-59. W. Ragan
60. J. L. Redford
61. P. Rubel
62. J. B. Ruble
63. G. S. Sadowski
64-65. R. W. Tucker
66. D. D. Walker
67. K. W. West
68. H. N. Wilson
69-70. Central Research Library
71. Document Reference Section
72-76. Laboratory Records Department
77. Laboratory Records, ORNL R.C.
78. ORNL Patent Office
79-93. Division of Technical Information Extension
94. Research and Development Division, ORO

EXTERNAL DISTRIBUTION

95. M. Levenson, Argonne National Laboratory