A Binary Linker Tracker Module for the BaBar Level 1 Drift Chamber trigger

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I. INTRODUCTION

The BaBar detector at PEP-II will operate in a high-luminosity e^+e^- collider environment near the $\Upsilon(4S)$ resonance with the primary goal of studying CP violation in the B meson system. In this environment, typical physics events of interest involve multiple charged particles, and can be identified from these tracks in a fast first level (Level 1) trigger system, by reconstructing the tracks in "real time". For this purpose, a Binary Linker Tracker Module (BLTM) was designed and prototyped for the BaBar Level 1 Drift Chamber trigger system. The BLTM is responsible for linking track segments, constructed by other trigger modules, into complete tracks. A single BLTM module processes a 360 MBytes/s stream of segment hit data, corresponding to information from the entire Drift Chamber.

A. Overview of Level 1 Drift Chamber Trigger

The BaBar Level 1 trigger system consists of three subsystems: the Drift Chamber Trigger, the Calorimeter Trigger and the Global Trigger. The Drift Chamber Trigger and Calorimeter Trigger receive information from the Drift Chamber and Calorimeter detectors respectively, process it, and send condensed data to the Global Trigger (GLT). The GLT attempts to match the angular locations of calorimeter towers and drift chamber tracks, and generates Level 1 triggers based on the results of the processing. The Drift Chamber trigger input data is a collection of raw Drift Chamber hits.

The Drift Chamber is a small-hex-cell design and contains 40 layers. The 40 layers are grouped four each in 10 radial superlayers. There are four axial superlayers (A1, A4, A7 and A10), with each pair of axial superlayers separated by two stereo superlayers (U2, V3, U5, V6, U8 and V9). Each superlayer is divided into 32 sectors in the azimuthal (ϕ) direction. A magnetic field of 1.5 T, parallel to the beam axis, forces charged particles on a circular trajectory and facilitates the measurement of their transverse momentum. The Drift Chamber front-end electronics (FEE) system continuously contributes "real-time" information (hit signals) about particle-related activity in each of drift cells to the Drift Chamber Trigger system. A hit signal represents the time during which the voltage on the wire of the cell is above the threshold of a discriminator, which resides in the ELEFANT chip [1] of the Drift Chamber FEE.

The algorithms of the Drift Chamber Trigger System are executed on three types of modules. First, the track segments, i.e., series of hits that are contiguous in space and time within a group, are found by a set of 24 Track Segment Finder Modules (TSFMs). The track segments are then linked into complete tracks by the Binary Link Tracker Module (BLTM). A set of 8 PT Discriminator Modules (PTDMs) determine if the segments are consistent with tracks of particles having a transverse momentum (P_t) greater than a specified minimum.

In this paper, the design and the hardware implementation of the Binary Track Linker Module is described.

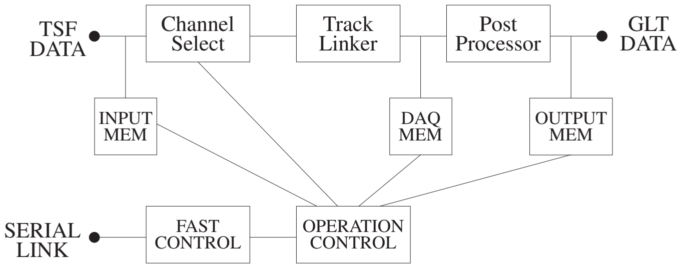

Figure 1: BLT Board Overview

II. BLT MODULE IMPLEMENTATION

A. Algorithm

The algorithm of BLT Module consists of three major sections: the Channel Select, the Track Linker and the Post Processor as shown in Figure 1. Each section is implemented in one Lucent Technologies Orca 2C family Field Programmable Gate Array (FPGA).

The module receives segment hit data from all 24 TSFMs, which corresponds to information from the entire drift chamber. To account for inoperative supercells, a 320 OR gate block is provided in the Channel Select to force ON the segments from such cells. The segment data is then passed to the Track Linker which uses an extension of a simple algorithm, developed for the CLEO II trigger [2], to link the segments into a continuous track. It starts from the innermost superlayer, A1, and moves radially outward. A track is found if (1) there is a segment hit in every layer, and (2) segments in two consecutive superlayers are within a certain number of supercells (three or five depending on the superlayer type) of each other. This allows for track curvature in the magnetic field and dip angle variations. For example, as illustrated in Figure 2, given a hit in superlayer A1, sector 5, the linker will then look for hits at sectors 4, 5, and 6 of superlayer U2 where it finds a hit in sector 4. The linker will continue look for hits in sectors 3, 4, and 5 of superlayer V3 where it finds a hit in sector 4, and so on until it reaches U5 where it finds a hit in sector 5. At this point a 'B' track is considered found. These steps are then continued until either no more hits are found in the next superlayer, or it successfully links all the way to superlayer A10, to form an 'A' track. These radial travel distances impose implicit transverse momentum (P_t) cuts on the A and B tracks of 180 and 120 MeV respectively.

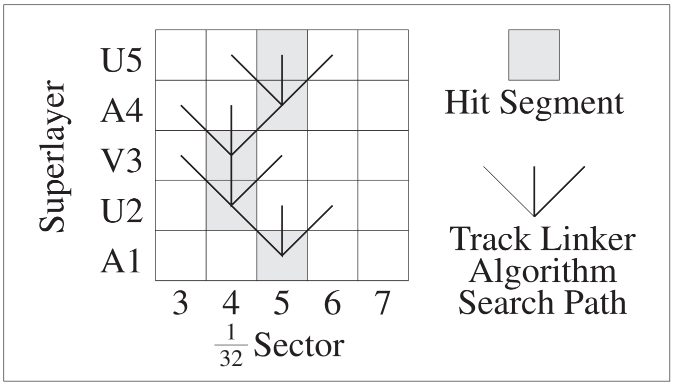

Figure 2: Example of Track Linker Algorithm

To make the BLT robust against cell inefficiencies the first requirement, that there is a segment hit in every layer, is relaxed to include tracks for which hits in one or two superlayers are missing as long as the following criteria are satisfied: (1) Either or both of the U5 and V6 layers must have a hit, (2) Only one of layers A1, U2, V3, A4 and U5 may be missing a hit, and (3) Only one of layers V6, A7, U8, V9 and A10 may be missing a hit.

Two 32-bit words corresponding to A and B tracks are output from the Track Linker, with each bit in a word representing whether or not a track of a given type was linked through the corresponding sector of the given superlayer. This information, which provides the ϕ location in either the A10 or U5 superlayer for each track found, is output to the Post Processor. To account for possible clock jitter, the Post Processor first extends in time each bit by approximately 269 ns, and then compresses the data to 16 bits to match the calorimeter's 20-bit ϕ resolution. The result is then sent to the GLT.

B. Control Logic

The control logic on the board is implemented in two FPGAs, a Fast Control unit and a board Operation Controller. The Fast Control FPGA implements a high speed serial link responsible for remote control and configuration of the board. It is a generic chip common to all the Level 1 trigger modules. The Operation Controller interprets the commands from the Fast Control unit and coordinates the functionality of the board by implementing the control and interface logic specific to the BLTM.

C. Memory Buffers

A DAQ memory circular buffer is used to save data related to a particular Level 1 trigger. The data saved can be read out, allowing for later reconstruction, of the processing that occurred in the BLT module during the creation of the particular Level 1 trigger. The buffer has sufficient storage to hold the history of local data during the time required for the trigger decision to be made.

Additionally, Save and Playback diagnostic memories are attached to the input and output data streams allowing for arbitrarily complex test vectors to be exercised on the board independent of its external connections. This design feature provides for powerful board and system level diagnostic capabilities.

III. Design Methodology

A major fraction of the design effort was dedicated to the implementation of the BLT algorithms and the necessary control logic within FPGAs using the VHDL hardware description language. The design takes full advantage of state-of-the-art Computer Aided Design tools. These sophisticated tools, which include routing algorithms for logical arrays and gate-level simulation greatly streamlined the design process. The finished 9U$\times$400 mm board contains roughly 75,000 gates of programmable logic or about 10,000 lines of VHDL synthesized into five FPGAs.

The BLTM was simulated prior to fabrication to ensure that the connectivity of the board was correct. The simulations also uncovered logic errors that would have been very difficult to find otherwise. The layout of the board emphasizes the careful routing and termination of critical signals such as clock lines. Also the timing of signals on the board contain large safety margins with respect to delays and setup/hold times.

The input/output memories allow all the algorithms and interfaces on the board to be tested. Through application of test vectors of "typical" event data from Monte Carlo simulations, generated from a software model for the complete Level 1 trigger electronics pipeline, one can debug and test the board in a systematic way. The test results are described below.

IV. Test Results And Conclusion

The BLTM prototype has undergone extensive testing of its algorithms using the memory's diagnostic play/record features. It was fed data from simulations of over 15,000 Monte Carlo events, and the results were successfully compared against the software model for the Level 1 trigger. The test bench results were in full agreement with all computer simulations of the BLTM. The Fast Control communication link is fully functional. There were no layout or fabrication errors found on the prototype board, allowing it to serve as the production version for the experiment. A limited system test of the board was also performed in which the BLTM was able to communicate with a TSF board.

The entire trigger system is expected to be installed and commissioned by the end of 1998.

V. References

[1] A. Chan *et al.,* "Electronics for Amplitude and Timing Measurement in Drift Chamber Readout," *IEEE Trans. On Nuclear Science, Vol. 43, No.3, June 1996*.

[2] K. Kinoshita, *Nucl. Instr. Methods A276 (1989)242* .