Development of Fully Depleted, Back-Illuminated Charge Coupled Devices

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ABSTRACT

The status of CCD development efforts at Lawrence Berkeley National Laboratory is reviewed. Fabrication technologies for the production of back-illuminated, fully depleted CCD's on 150 mm diameter wafers are described. In addition, preliminary performance results for high-voltage compatible CCD's, including a 3512×3512, 10.5 μm pixel CCD for the proposed SuperNova Acceleration Probe project, are presented.

Keywords: CCD, fully depleted, back illuminated, 150 mm diameter wafers, refractory metal, MBE

1. INTRODUCTION

We have developed fully depleted, back-illuminated CCD imagers fabricated on high-resistivity, n-type silicon for scientific applications (see Figure 1).[1] Since the first description in 1996[2] the virtues of such a CCD have been well established. The typical thickness of 200–300 μm results in good near-infrared quantum efficiency (QE) and greatly reduces and even eliminates fringing.[3] Point spread function (PSF) is well defined and is determined by the transit time of the photogenerated holes in an electric field that extends throughout the thickness of the device. The PSF is directly proportional to the thickness of the CCD and inversely proportional to the square root of the substrate bias used for full depletion.[1,4,5] The PSF of a relatively thick, fully depleted CCD can be better than that observed with a conventional thinned CCD if the latter has a significant field-free thickness at the backside of the device.[6] Since the CCD is p-channel, the radiation hardness due to bulk damage from protons in the space environment is improved significantly when compared to conventional n-channel CCD's due to the lack of phosphorus-vacancy formation in the CCD channel after proton irradiation.[7–9]

In this work we describe efforts to fabricate fully depleted, back-illuminated CCD's on 150 mm diameter wafers. Three fabrication technologies under investigation to produce high performance CCD's are described. In addition, we report preliminary results on exploratory high-voltage compatible CCD's of interest to the proposed SuperNova Acceleration Probe (SNAP) satellite.

2. CCD FABRICATION ISSUES

The CCD's described in this work have been fabricated both at Lawrence Berkeley National Laboratory (LBNL) and at DALSA Semiconductor. At LBNL, CCD's are fabricated in a Class 10 clean room on 100 mm diameter wafers, and CCD's from this facility are in use at ground-based observatories.[6] Formats as large as 2048×4096, 15 μm pixel have been produced.

In addition, CCD's have been successfully fabricated on 150 mm diameter, high-resistivity wafers at DALSA Semiconductor.[6] The major difference we have noted when comparing high-resistivity 100 mm and 150 mm diameter wafers is a generally lower resistivity achieved to date on the 150 mm material. Typically the range of resistivity seen in 150 mm diameter wafers is 4000–8000 Ω-cm, in contrast to the greater than 10,000 Ω-cm resistivity seen on the 100 mm material. The wafers used in this work were supplied by Wacker Siltronic Corporation.

In order to produce back-illuminated CCD's from the DALSA Semiconductor wafers, three technologies have been under development. The first involves partial processing of the wafers at DALSA Semiconductor with the

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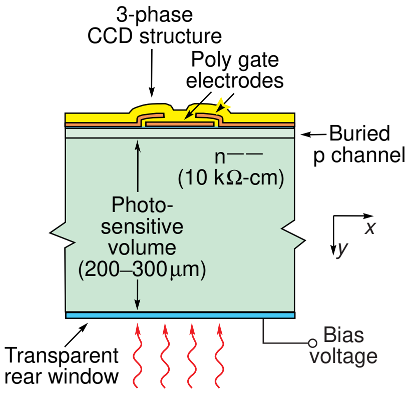


Figure 1. Cross-sectional diagram of the CCD described in this work.

additional steps necessary for back illumination done at LBNL. CCD's are processed up to the contact mask step before metal deposition. The standard thickness wafers (650–700 μm) are mechanically thinned and polished to the final desired thickness, which is typically 200–300 μm. The wafers are then completed at LBNL. The second technology under development involves replacing the standard aluminum metallization used for interconnect in the CCD with a refractory metal.

In both cases the backside ohmic contact is formed by low-pressure, chemical-vapor deposition of in-situ doped polycrystalline silicon (ISDP).[1, 10] This layer can be made thin for good blue response, typically 10-20 nm, and is robust to over-depleted operation that is necessary both to guarantee full depletion across the entire CCD, and to improve spatial resolution.[1, 4, 5]

The ISDP deposition is typically done at 650°C, which is too high for aluminum metallization.[11] Hence in the first fabrication scenario described above the ISDP is deposited before aluminum deposition. This requires photolithography and etching steps be done on non-standard thickness wafers. This is essentially the same fabrication technique used to fabricate CCD's on 100 mm diameter wafers at LBNL. However, in the case of 150 mm diameter wafers, substantial thinning of the wafers is required in order to achieve the desired CCD thickness. Typically more than 400 μm of silicon must be removed, and a significant learning curve was needed in order to achieve good thinning results.

In contrast, in the refractory-metal process the thinning can be done after the wafers are completed at DALSA Semiconductor. Due to the high melting point of refractory metals it is possible to deposit the ISDP on a finished wafer.

The third fabrication technology in development is a backside ohmic contact formed by molecular-beam epitaxy (MBE). This work is being done in collaboration with the Jet Propulsion Laboratory (JPL). All three fabrication technologies are discussed in more detail in the following sections.

2.1. Back-illuminated CCD fabrication on 150 mm diameter wafers

As described above, in one fabrication scenario the wafers are partially processed at DALSA Semiconductor up to the step before contact mask. The wafers are then thinned to the desired CCD thickness after which ISDP is deposited, followed by processing through two photolithography and etch steps. Anti-reflection coatings are deposited at the end of the process.

Thinning of the wafers is a critical step, especially for fully depleted devices where defects on the backside of the wafer can lead to high dark current. In addition, since the wafers must go through photolithography steps, the wafers must be sufficiently flat after the thinning step. We have investigated a backgrinding and polishing process for wafer thinning. This process is common in the integrated circuits industry and is offered as a service at various commercial vendors. Thinning of 150 mm diameter wafers has also been reported for use in power transistor technologies.[12–15]

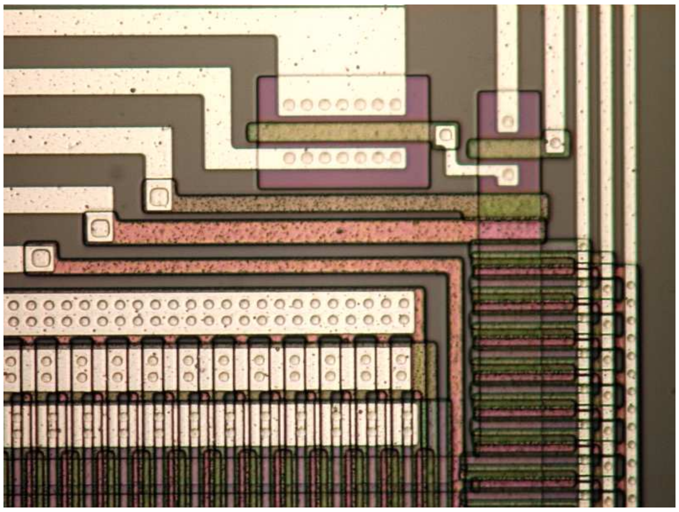


Figure 2. Micrograph showing the output amplifier of a CCD partially fabricated at DALSA Semiconductor with the contact and metal mask photolithography and etch steps done at LBNL. The smallest drawn contact size in this micrograph is 2 μm square.

During the thinning process the front sides of the wafers are protected by the application of wax or a specialized tape, and most of the silicon is removed by a coarse backgrinding step. This is followed by a fine polishing step that is used to remove subsurface damage from the coarse grinding step. At this stage the back surface of the wafer is of comparable quality to the front side of a prime-grade wafer. ISDP is then deposited on this polished, backside surface.

Following ISDP deposition the wafers are processed through the contact and metal photolithography and etch steps. In order to do these steps, 150 mm wafer tooling has been added to the LBNL facility. This includes a 150 mm projection aligner photolithography tool that features a fairly large depth of focus, about 12 μm, which eases the flatness requirements for the thinned wafers. This photolithography tool is a 1$\times$ aligner, i.e. the feature size on the mask is the same as that on the wafer, and allows for large area CCD fabrication without the need for stitching of patterns. The illumination is through a fixed slit and the mask and wafer are scanned past the slit illumination that is projected through the mask and onto the wafer. The minimum linewidth that can be routinely printed is in the range of 1.5–2 μm.

An issue with this fabrication scenario is the ability to register the contact and metal mask patterns with the underlying patterns done at DALSA Semiconductor on similar, but not identical photolithography equipment. Matching of lithography is demonstrated in Figure 2, which shows a micrograph of a CCD amplifier where the contact and metal steps were done at LBNL on wafers that were partially processed at DALSA Semiconductor. The photolithography tool in use at LBNL can correct for registration offsets as well as second order effects such as magnification and skew errors. Typical registration errors are on the order of 0.5 μm and below, which is adequate for most large format, scientific CCD's.

The major challenge in the photolithography steps has been the production of sufficiently flat wafers, although improvements in the wafer thinning process has solved this problem. Beyond that we have found that the most critical step in this fabrication scenario is the etching of contacts through silicon dioxide (SiO_2) layers to make contact to the polycrystalline silicon gate layers and to the implanted layers in the silicon substrate. In order to achieve good control of contact size when etching thick SiO_2 films, plasma etching is required. Contact size is typically at the minimum allowed design rule of the technology, and wet chemical etch of thick SiO_2 would require relaxing of design rules with negative impact on various CCD performance parameters. Contacts as small as 2 μm square are present in typical LBNL CCD designs (see Figure 2).

Initial attempts to etch thinned 150 mm wafers resulted in non-functional CCD's due to plasma damage. We observed that large-area CCD's exhibited damage consisting of clock-to-clock and clock-to-substrate shorts. In

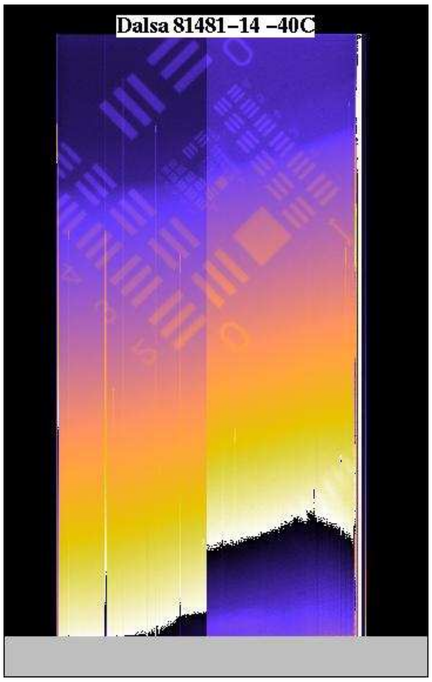


Figure 3. Test pattern image taken at $-40°$C on a 250 μm thick, 2048 $\times$ 4096, 15 μm pixel CCD partially fabricated at DALSA Semiconductor with the contact and metal mask photolithography and etch steps done at LBNL. The contact etch step was done on the dual-frequency etcher described in the text. The top to bottom gradient in the image is due to dark current at this operating temperature. The readout amplifiers are at the top of the image. Measurement courtesy of Kirk Gilmore of Lick Observatory.

addition, significant wafer heating with subsequent failure of the photoresist mask was observed (resist reticulation). We attribute much of this difficulty to the use of thinned wafers, which have significant bow that varies as the inverse square of wafer thickness.[16] Hence it is likely that the thinned wafers are not in good thermal contact with the lower electrode of the etcher, resulting in significant wafer heating and exacerbated plasma damage.[17] In addition, the polycrystalline silicon electrode area in large-format CCD's is quite significant and non-uniform charging of these electrodes during etching steps can lead to dielectric breakdown of the insulators isolating the electrodes from each other and from the substrate.

The initial attempts at etching of 150 mm CCD wafers were done on a capacitively coupled, rf-diode etcher. In the rf-diode etcher technology the plasma ion density is coupled to the bias voltage that the wafer acquires in the plasma.[18] The bias voltage determines the energy of the ions impinging on the wafer during the etch. More modern dielectric etch technologies[19] decouple the ion density from the bias voltage by techniques that include the introduction of a magnetic field in the etch chamber[20] or the use of a dual-frequency discharge.[21] In the latter case the high frequency rf source (27 MHz) results in an increased ion density, about ten times that achieved in a single-frequency 400 kHz etcher, while the low frequency rf source (2 MHz) determines the bias voltage.

Given the difficulties etching large area CCD's with the rf-diode technology, a dual-frequency dielectric etch system was recently acquired at LBNL. In addition to the decoupling of ion density and bias voltage described above, this etcher has additional design features to minimize plasma damage. This includes the use of a small electrode gap that allows for electron neutralization of charge imbalances on the wafer during each rf cycle, and reduction in the voltage needed to initiate the plasma as a result of the higher degree of ionization with the high frequency rf source.[22] In addition, an electrostatic chuck with backside He cooling is used to minimize wafer heating and to hold the wafers flat during the etch.[23]

Preliminary results indicate excellent etching performance on 200 and 250 μm thick test wafers. Etch rate uniformities of less than 3.3% have been achieved for both thermally grown and deposited SiO_2. Electrostatic chucking has been verified for the thinned wafers with similar results to those observed on standard thickness wafers. Figure 3 shows a test pattern image taken on a 250 μm thick, 2048 × 4096, 15 μm pixel CCD at −40°C on a cold wafer prober system at Lick Observatory. At this operating temperature saturation near the bottom of the image due to dark current is observed. No plasma damage is obvious from Figure 3 although detailed testing of packaged CCD's is necessary to verify this.

2.2. Refractory-metal technology

An alternative fabrication technology using a refractory metal in place of the standard aluminum interconnect was proposed.[24] The essential idea is that the refractory metal and metal contacts to the silicon and polycrystalline silicon electrodes might withstand the 650°C temperature of the ISDP deposition. Hence the ISDP layer could be deposited after metal masking thereby minimizing the need to handle thinned wafers. The processing steps required on the thinned wafers consist of only the ISDP deposition, removal of the frontside ISDP, and deposition of anti-reflecting coatings.

The two major concerns for this technology are possible metallic contamination of the silicon during the ISDP deposition with degradation in the CCD dark current, and the relatively high resistivity of the refractory metal compared to the standard aluminum. The refractory metal chosen, a stack of Ti and TiN, has about 10× higher resistivity than the standard thin film aluminum used at DALSA Semiconductor. A lower resistivity refractory metal such as W would be of interest although that would require specialized equipment for etching.[24]

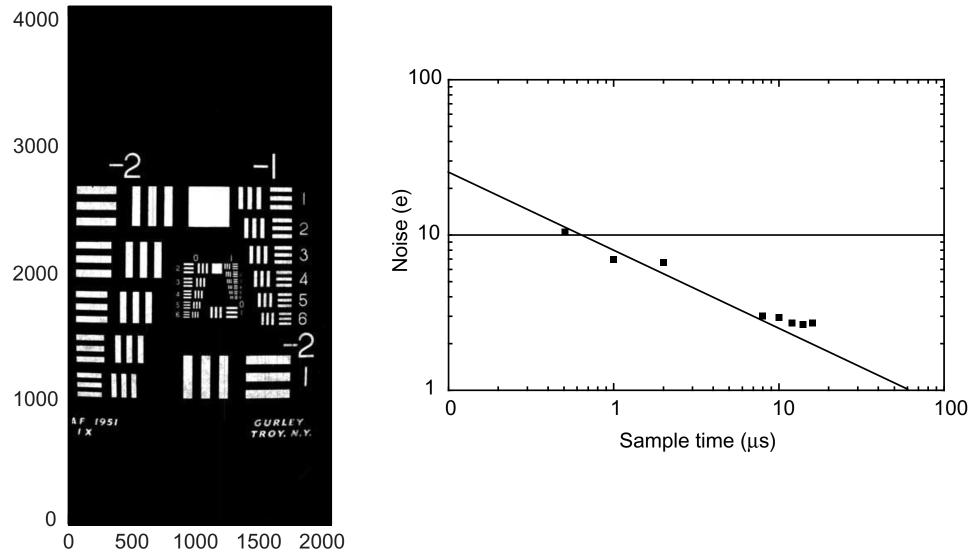
The contamination concern has to do with the extreme sensitivity of silicon devices to trace amounts of metallic contamination with resulting deleterious effects on dark current.[25] This is especially a concern for fully depleted devices where contamination nearly anywhere in the substrate could lead to high dark current. Due to this fact backside in-situ doped (phosphorus) polycrystalline silicon gettering has been employed both at LBNL and at DALSA Semiconductor to minimize dark current in fully depleted CCD's.[26] However, the gettering layer is removed when the wafers are thinned, and therefore metallic contamination is a concern, especially during the high-temperature ISDP deposition.

The refractory metal itself is not believed to be a significant source of contamination due to its low vapor pressure. However, trace contaminants in the refractory metal could be a problem. In addition, proper cleaning of the wafers is necessary before any high-temperature steps given the high mobility of metallic contaminants in silicon at high temperatures.[25] The former issue was addressed with a neutron activation analysis study of Ti/TiN films done at the LBNL Low Background Facility. Since Ti has no stable isotopes convenient for application of the slow neutron activation process, a fast neutron reaction on stable ^{46}Ti producing the radioactive ^{46}Sc (84 day half life) was used as the diagnostic for the presence of Ti in the samples. The only significant trace metal found in the Ti/TiN was Zn in the low ppb range.[27]

The need for ultra-low concentrations of metals in the silicon requires that wafers go through chemical cleaning steps before any high temperature processing. For the refractory-metal process the cleaning of the wafers is complicated by the exposed metal on the front sides of the wafers that would be attacked by the acids used in a typical wafer cleaning step. This was addressed by utilizing a cleaning fixture that exposes only the backside of the wafer during the cleaning steps.[28] A chemically resistant Kalrez o-ring was used to seal the front surface of the wafer from the chemicals used for wafer cleaning.

Figure 4 (a) shows a test pattern image from the first back-illuminated, 2048 × 4096, 15 μm pixel CCD fabricated with the refractory-metal process. The wafer was thinned to 250 μm in this case. Figure 4 (b) shows measured noise versus sample time. The sample time is the integration time used on both the reset and signal in the double-correlated sampling signal processing. The minimum noise is about 3 e^- rms at a readout speed of around 50 kpixels/sec. The straight line drawn in Figure 4 (b) is proportional to the inverse square root of the sample time and is a reasonable fit of the data except at long sample times.[29] Both measurements were done at −120°C.

Figure 5 shows an image taken after exposure of a 200 μm thick, back-illuminated 2520 × 2520, 12 μm pixel CCD to ^{55}Fe x-rays. This is the first 200 μm thick CCD produced at LBNL from a 150 mm diameter wafer. Given the minimal wafer handling in the refractory-metal process, it is felt that even thinner CCD's are possible



(a) (b)

Figure 4. (a) Test pattern image taken on the first back-illuminated, 2048 × 4096, 15 μm pixel CCD fabricated with the refractory-metal process. (b) Measured noise versus sample time. The operating temperature was $-120°$C. Measurements courtesy of Mingzhi Wei of Lick Observatory.

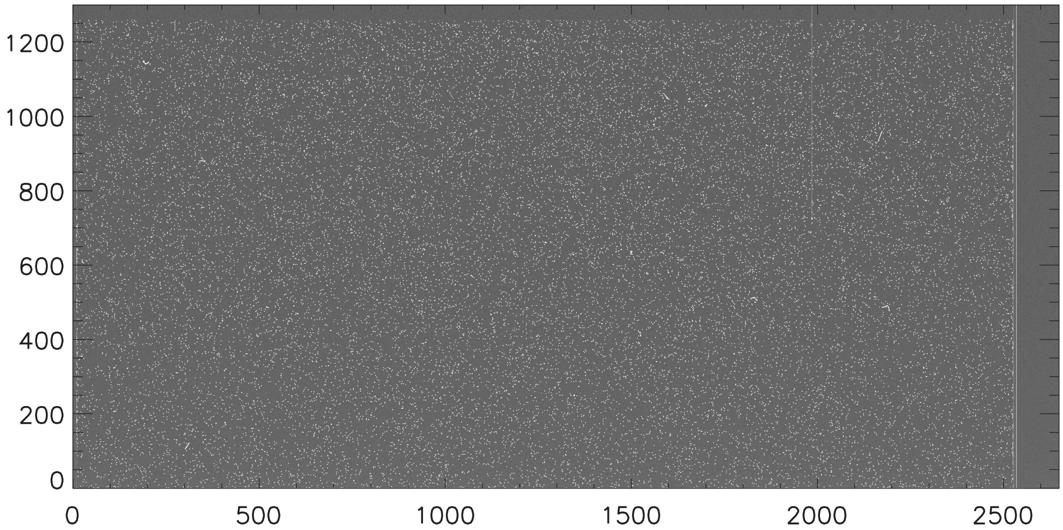


Figure 5. Image taken on half of a 200 μm thick, back-illuminated, 2520 × 2520, 12 μm pixel CCD fabricated using the refractory-metal process. The image was taken after a 45 second exposure to ^{55}Fe x-rays and the operating temperature was $-140°$C.

in this technology. As mentioned previously, power semiconductor devices fabricated on 150 mm diameter wafers with thicknesses in the 70–100 μm range have been reported.[12–15] The dark current measured after a 30 minute integration at $-140°$C for the CCD shown in Figure 5 was 16 e$^-$/pixel-hour, although dark currents as low as 1–2 e$^-$/pixel-hour have been measured on other LBNL refractory-metal CCD's (see Figure 8).

Although more detailed testing on refractory-metal CCD's is required to validate the technology, preliminary results are quite encouraging. Most of the the testing to date has been at relatively slow readout rates, 100 kpixels/sec and below, and testing at higher speed will be necessary in order to determine the operating limits due to the relatively high resistivity of the refractory-metal interconnects.

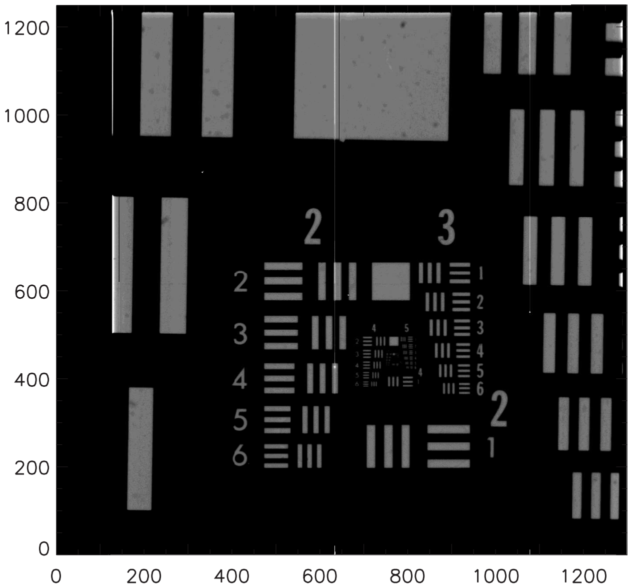


Figure 6. Image taken on a 250 μm thick, back-illuminated, 1230 $\times$ 1170, 12 μm pixel CCD with a backside layer grown by MBE. The substrate bias voltage was 45 V, which was sufficient to fully deplete the CCD. The operating temperature was $-140°$C.

2.3. MBE development

Another technology under investigation at JPL is n-type delta doping, which uses MBE to grow the backside ohmic contact layer. The high quantum efficiency and stability of the delta-doping process has been previously demonstrated in standard n-channel CCD's.[30] By keeping the process temperature below 450°C, backside contacts can be deposited on fully processed devices with the standard aluminum metallization. In this case, MBE enables fabrication of a thin contact by incorporating a high concentration of dopant in a very thin layer of silicon. In addition to the advantages offered by low temperature growth, the thin layers produced by delta doping can also be used to extend the wavelength sensitivity of CCD's into the ultraviolet. For fully depleted p-channel CCD's JPL has developed a low-temperature process for growing thin layers of Sb-doped silicon, in which the device temperature never exceeds 450°C.

Figure 6 shows the first results for a fully depleted, p-channel CCD with a 15 nm thick, Sb-doped MBE backside layer. A fully processed DALSA wafer with aluminum metallization was thinned to 250 μm and processed at JPL. After MBE growth the CCD was packaged and tested at LBNL.

The CCD of Figure 6 had a partial vertical short that limited quantitative testing, although the short was not believed to be related to the MBE step. The substrate bias voltage was 45 V, which was sufficient for full depletion. This was verified by inspection of cosmic ray tracks in long dark exposures. More details on the MBE effort will be presented in a future publication.[31]

3. EXPLORATORY HIGH-VOLTAGE COMPATIBLE CCD'S

There is motivation to be able to operate fully depleted CCD's at fairly large substrate bias voltages. The depletion depth for a simple pn junction is given by

$$y_D = \sqrt{\frac{2\epsilon_{\text{Si}}\left(V_{\text{Appl}} + \phi_{bi}\right)}{qN_D}} \tag{1}$$

where ϵ_{Si} is the permittivity of silicon, V_{Appl} is the applied reverse bias voltage, ϕ_{bi} is the built-in potential of the junction, q is the electron charge, and N_D is the doping density in the lightly doped side of the junction, where

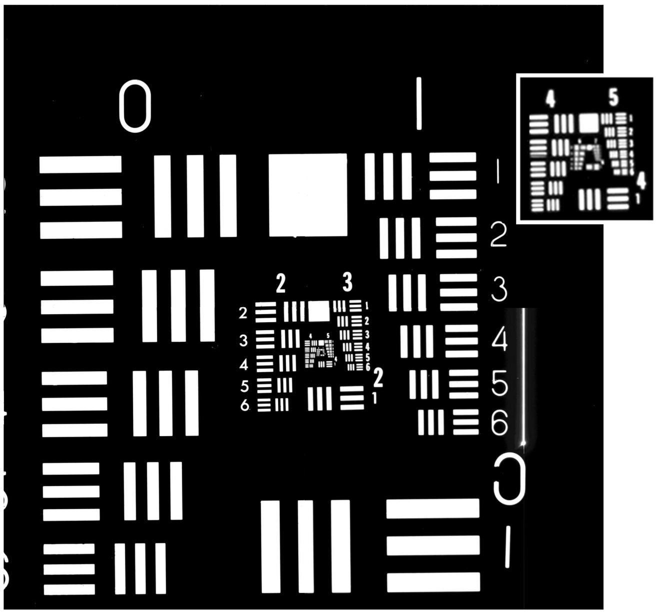


Figure 7. Test pattern image taken on a 250 μm thick, back-illuminated, 3512 $\times$ 3512, 10.5 μm pixel CCD fabricated using the refractory-metal process. The substrate bias voltage was 100 V and the operating temperature was $-140°$C. The test pattern insert shown in the upper right of the figure is an expanded view of the smallest test patterns located near the center of the image.

it is assumed that the doping density on the heavily doped side of the junction is much greater than N_D. Hence the depletion depth varies as the square root of bias voltage. Depending on the doping density N_D and desired depletion thickness, relatively large bias voltages may be required for full depletion. One application area that could benefit from larger depletion depths than needed for near-IR applications is the direct detection of x-rays in the 10–20 keV range.

In addition, operation of fully depleted CCD's at bias voltages larger than that needed for full depletion results in improved PSF. The PSF of a fully depleted CCD for light absorbed at the back surface is approximately given by

$$\sigma_{od} \approx \sqrt{2\frac{kT}{q}\frac{{y_{\rm sub}}^2}{(V_{\rm sub}-V_J)}} \tag{2}$$

where k is Boltzmann's constant, T is absolute temperature, $y_{\rm sub}$ is the substrate thickness, $V_{\rm sub}$ is the applied substrate bias voltage, and V_J is an average potential near the CCD potential wells.[1, 4, 5] For some applications both a high near-IR QE and small PSF are desired. Since the former requires a relatively thick device while the latter implies reducing the device thickness (Equation 2), the ability to improve the PSF via the substrate bias voltage allows one more degree of freedom in device optimization. The CCD's presently being developed for the proposed SNAP space-based mission are an example of CCD's that require both high near-IR QE and good PSF.

Figure 7 shows a test pattern image taken with a 250 μm thick, refractory metal, back-illuminated SNAP prototype CCD at a substrate bias of 100 V. The CCD is 3512 $\times$ 3512 and the pixel size is 10.5 μm. Various techniques have been used in the design to allow for operation at such high substrate bias voltages.[32] Figure 8 shows a 30 minute dark exposure for a 1000 $\times$ 2474, 12 μm CCD also operated at 100 V. This CCD is also 250 μm thick with refractory metal although it was packaged for front illumination. The measured dark current at $-140°$C was 2.1 e$^-$/pixel-hour.

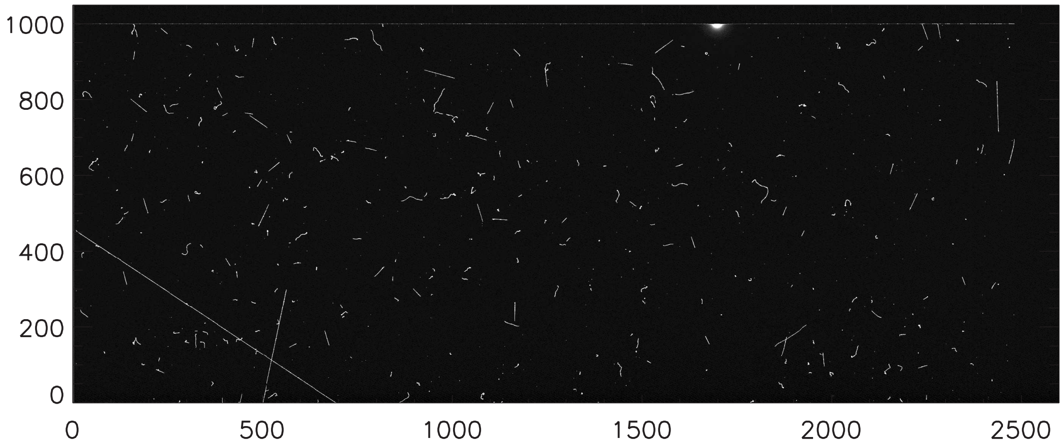


Figure 8. Image taken after a 30 minute dark exposure on a 250 μm thick, front-illuminated, 1000 $\times$ 2474, 12 μm pixel CCD fabricated using the refractory-metal process. The substrate bias voltage was 100 V and the operating temperature was -140°C. The measured dark current was 2.1 e^{-}/pixel-hour. A weak hot pixel region is seen near the top center of the image.

There are concerns with the use of high substrate bias voltages that must be addressed. High voltages near sensitive regions of the CCD, for example the output and reset transistors, could permanently damage the device. An area of major concern would be if for some reason a sufficiently high voltage were impressed between the transistor gate and channel causing catastrophic breakdown of the transistor gate dielectric. A similar concern exists for the CCD imaging area and serial registers. For space applications it has been shown that power MOSFET's can be rendered non-functional by the effects of energetic heavy ions that generate dense electron-hole tracks through the device that can result in a significant fraction of the applied high voltage reaching the surface of the device, where dielectric breakdown can occur.[33,34] This mechanism is referred to as single-event gate rupture (SEGR). Power MOSFET's have similarities with fully depleted CCD's in that both require that a high voltage be applied to the backside of the device. Although initial test results on the high-voltage compatible CCD's are encouraging, more testing is required to study the long-term reliability of such CCD's, especially for space applications.

4. SUMMARY

Technology developments for the fabrication of back-illuminated, fully depleted CCD's on 150 mm diameter wafers have been presented. CCD's have been successfully fabricated via three techniques. Standard thickness wafers partially processed at DALSA Semiconductor have been thinned to 250 μm and back-illuminated CCD's have been successfully processed through photolithography and etching steps on the thinned wafers at LBNL. Plasma etching of contacts on thinned wafers using a dual-frequency dielectric etcher have been described. Also, 200 μm thick, back-illuminated CCD's have been produced using a refractory metal in place of the standard aluminum. In collaboration with JPL an MBE CCD with standard aluminum metallization has been demonstrated. In addition, preliminary results on high-voltage compatible CCD's have been reported. Future efforts include detailed testing of large-format CCD's fabricated with the various technologies, and further investigation of the high-voltage compatible CCD's.

5. ACKNOWLEDGEMENTS

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