# XC2C256 CoolRunner-II CPLD

DS094 (v1.1) May 13, 2002 **Advance Product Specification**

## Features

- Optimized for 1.8V systems
  - As fast as 5.0 ns pin-to-pin delays
  - As low as 25 µA quiescent current
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 100-pin VQFP with 80 user I/O
  - 144-pin TQFP with 106 user I/O
  - 132-ball CP (0.5mm) BGA with 118 user I/O
  - 208-pin PQFP with 173 user I/O
  - 256-ball FT (1.0mm) BGA with 184 user I/O
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
  - Two separate output banks
  - Fast Zero Power™ (FZP) FZP 100% CMOS product term generation
  - DataGATE enable (DGE) signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
    - SSTL2-1, SSTL3-1, and HSTL-1 I/O compatibility
  - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

## Description

The CoolRunner-II 256-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved

This device consists of sixteen Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as "fast input" registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchonous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Circuitry has also been included to divide one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time.

By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is output banking. Two output banks are available on the CoolRunner-II 256-macrocell device that permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 256-macrocell CPLD is I/O compatible with standard LVTTL and LVCMOS18, LVCMOS25, and LVCMOS33 (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

## Fast Zero Power Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that makes use of CMOS technology in both the fabrication and design methodology. FZP design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

## Supported I/O Standards

The CoolRunner-II 256 macrocell features both LVCMOS and LVTTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

*Table 1:* **I/O Standards for XC2C256**

| I/O Types | Output $V_{CCIO}$ | Input $V_{CCIO}$ | Input $V_{REF}$ | Board Termination Voltage $V_{TT}$ |
|---|---|---|---|---|
| LVTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS33 | 3.3 | 3.3 | N/A | N/A |
| LVCMOS25 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| 1.5V I/O | 1.5 | 1.5 | N/A | N/A |
| HSTL-1 | 1.5 | 1.5 | 0.75 | 0.75 |
| SSTL2-1 | 2.5 | 2.5 | 1.25 | 1.25 |
| SSTL3-1 | 3.3 | 3.3 | 1.5 | 1.5 |

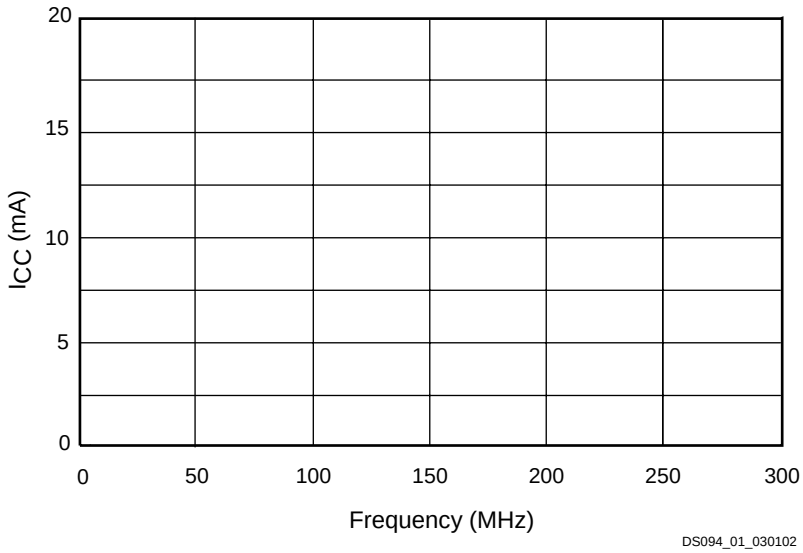



*Figure 1:* **$I_{CC}$ vs Frequency**

*Table 2:* **$I_{CC}$ vs Frequency (LVCMOS 1.8V $T_A$ = 25°C)(1)**

| | Frequency (MHz) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 25 | 50 | 75 | 100 | 150 | 175 | 200 | 225 | 250 | 270 |
| Typical -6, -7.5 $I_{CC}$ (mA) | | | | | | | | | | | |
| Typical -5 $I_{CC}$ (mA) | | | | | | | | | | | |

**Notes:**
1. 16-bit up/down, resettable binary counter (one counter per function block).

## Absolute Maximum Ratings

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to ground | –0.5 to 2.0 | V |
| $V_{CCIO}$ | Supply voltage for output drivers | –0.5 to 4.0 | V |
| $V_{JTAG}$ | JTAG input voltage limits | –0.5 to 4.0 | V |
| $V_{AUX}$ | JTAG input supply voltage | –0.5 to 4.0 | V |
| $V_{IN}$ | Input voltage relative to ground(1) | –0.5 to 4.0 | V |
| $V_{TS}$ | Voltage applied to 3-state output(1) | –0.5 to 4.0 | V |
| $T_{STG}$ | Storage Temperature (ambient) | –65 to +150 | °C |
| $T_{SOL}$ | Maximum Soldering temperature (10s @ 1/16in. = 1.5mm) | +260 | °C |
| $T_J$ | Junction Temperature | +150 | °C |

**Notes:**
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage for internal logic and input buffers | Commercial $T_A$ = 0°C to +70°C | 1.7 | 1.9 | V |
| | | Industrial $T_A$ = –40°C to +85°C | 1.7 | 1.9 | V |
| $V_{CCIO}$ | Supply voltage for output drivers @ 3.3V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers @ 2.5V operation | | 2.3 | 2.7 | V |
| | Supply voltage for output drivers @ 1.8V operation | | 1.7 | 1.9 | V |
| | Supply voltage for output drivers @ 1.5V operation | | 1.4 | 1.6 | V |
| $V_{AUX}$ | JTAG programming | | 1.7 | 3.6 | V |

## DC Electrical Characteristics (Over Recommended Operating Conditions)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{CCSB}$ | Standby current (-6, -7.5) | $V_{CC}$ = 1.9V, $V_{CCIO}$ = 3.6V | - | 100 | µA |
| $I_{CCSB}$ | Standby current (-5) | $V_{CC}$ = 1.9V, $V_{CCIO}$ = 3.6V | | | mA |
| $I_{CC}$ | Dynamic current (-6, -7.5) | f = 1 MHz | | | mA |
| | | f = 50 MHz | | | mA |
| $I_{CC}$ | Dynamic current (-5) | f = 1 MHz | | | mA |
| | | f = 50 MHz | | | mA |
| $C_{JTAG}$ | JTAG input capacitance | f = 1 MHz | | | pF |
| $C_{CLK}$ | Global clock input capacitance | f = 1 MHz | | | pF |
| $C_{IO}$ | I/O capacitance | f = 1 MHz | | | pF |

## LVCMOS 3.3V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Input source voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | High level input voltage | | 2 | $V_{CCIO}$ + 0.3V | V |
| $V_{IL}$ | Low level input voltage | | –0.3 | 0.8 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –8 mA, $V_{CCIO}$ = 3V | $V_{CCIO}$ – 0.4V | - | V |
| | | $I_{OH}$ = –0.1 mA, $V_{CCIO}$ = 3V | $V_{CCIO}$ – 0.2V | - | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 8 mA, $V_{CCIO}$ = 3V | - | 0.4 | V |
| | | $I_{OL}$ = 0.1 mA, $V_{CCIO}$ = 3V | - | 0.2 | V |
| $I_{IL}$ | Input leakage current | $V_{IN}$ = 0V or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $I_{IH}$ | I/O High-Z leakage | $V_{IN}$ = 0V or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $C_{JTAG}$ | JTAG input capacitance | f = 1 MHz | | | pF |
| $C_{CLK}$ | Global clock input capacitance | f = 1 MHz | | | pF |
| $C_{IO}$ | I/O capacitance | f = 1 MHz | | | pF |

## LVCMOS 2.5V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Input source voltage | | 2.3 | 2.7 | V |
| $V_{IH}$ | High level input voltage | | 1.7 | 3.9 | V |
| $V_{IL}$ | Low level input voltage | | –0.3 | 0.7 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –8 mA, $V_{CCIO}$ = 2.3V | $V_{CCIO}$ – 0.4V | - | V |
| | | $I_{OH}$ = –0.1 mA, $V_{CCIO}$ = 2.3V | $V_{CCIO}$ – 0.2V | - | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 8 mA, $V_{CCIO}$ = 2.3V | - | 0.4 | V |
| | | $I_{OL}$ = 0.1mA, $V_{CCIO}$ = 2.3V | - | 0.2 | V |
| $I_{IL}$ | Input leakage current | $V_{IN}$ = 0V or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $I_{IH}$ | I/O High-Z leakage | $V_{IN}$ = 0V or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $C_{JTAG}$ | JTAG input capacitance | f = 1 MHz | | | pF |
| $C_{CLK}$ | Global clock input capacitance | f = 1 MHz | | | pF |
| $C_{IO}$ | I/O capacitance | f = 1 MHz | | | pF |

## LVCMOS 1.8V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Input source voltage | | 1.7 | 1.9 | V |
| $V_{IH}$ | High level input voltage | | 0.7 x $V_{CCIO}$ | 3.9 | V |
| $V_{IL}$ | Low level input voltage | | –0.3 | 0.2 x $V_{CCIO}$ | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –8 mA, $V_{CCIO}$ = 1.7V | $V_{CCIO}$ – 0.45 | - | V |
| | | $I_{OH}$ = –0.1 mA, $V_{CCIO}$ = 1.7V | $V_{CCIO}$ – 0.2 | - | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 8 mA, $V_{CCIO}$ = 1.7V | - | 0.45 | V |
| | | $I_{OL}$ = 0.1 mA, $V_{CCIO}$ = 1.7V | - | 0.2 | V |
| $I_{IL}$ | Input leakage current | $V_{IN}$ = 0 or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $I_{IH}$ | I/O High-Z leakage | $V_{IN}$ = 0 or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $C_{JTAG}$ | JTAG input capacitance | f = 1 MHz | | | pF |
| $C_{CLK}$ | Global clock input capacitance | f = 1 MHz | | | pF |
| $C_{IO}$ | I/O capacitance | f = 1 MHz | | | pF |

## 1.5V DC Voltage Specifications(1)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Input source voltage | | 1.4 | 1.6 | V |
| $V_{IH}$ | High level input voltage | | 0.7 x $V_{CCIO}$ | 3.9 | V |
| $V_{IL}$ | Low level input voltage | | –0.3 | 0.3 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –8 mA, $V_{CCIO}$ = 1.4V | $V_{CCIO}$ – 0.45 | - | V |
| | | $I_{OH}$ = –0.1 mA, $V_{CCIO}$ = 1.4V | $V_{CCIO}$ – 0.2 | - | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 8 mA, $V_{CCIO}$ = 1.4V | - | 0.4 | V |
| | | $I_{OL}$ = 0.1 mA, $V_{CCIO}$ = 1.4V | - | 0.2 | V |
| $I_{IL}$ | Input leakage current | $V_{IN}$ = 0 or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $I_{IH}$ | I/O High-Z leakage | $V_{IN}$ = 0 or $V_{CCIO}$ to 3.9V | –10 | 10 | µA |
| $C_{JTAG}$ | JTAG input capacitance | f = 1 MHz | | | pF |
| $C_{CLK}$ | Global clock input capacitance | f = 1 MHz | | | pF |
| $C_{IO}$ | I/O capacitance | f = 1 MHz | | | pF |

**Notes:**
1. Hysteresis used on 1.5V inputs.

# AC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | -5 | | -6 | | -7 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $T_{PD1}$ | Propagation delay single p-term | - | 4.7 | - | 5.6 | - | 6.7 | ns |
| $T_{PD2}$ | Propagation delay OR array | - | 5.0 | - | 6.0 | - | 7.5 | ns |
| $T_{SUF}$ | Fast input register p-term clock setup time | 1.8 | - | 2.0 | - | 2.3 | - | ns |
| $T_{SU1}$ | Setup time fast (single p-term) | 1.9 | - | 2.4 | - | 2.5 | - | ns |
| $T_{SU2}$ | Setup time (OR array) | 2.2 | - | 2.8 | - | 3.3 | - | ns |
| $T_{HF}$ | Fast input register hold time | 0 | - | 0 | - | 0 | - | ns |
| $T_{H}$ | P-term hold time | 0 | - | 0 | - | 0 | - | ns |
| $T_{CO}$ | Clock to output | - | 3.8 | - | 4.5 | - | 6.0 | ns |
| $F_{TOGGLE}$(1) | Internal toggle rate | - | 416 | - | 250 | - | 168 | MHz |
| $F_{SYSTEM1}$(2) | Maximum system frequency | - | 238 | - | 213 | - | 159 | MHz |
| $F_{SYSTEM2}$(2) | Maximum system frequency | - | 222 | - | 196 | - | 141 | MHz |
| $F_{EXT1}$(3) | Maximum external frequency | - | 175 | - | 145 | - | 118 | MHz |
| $F_{EXT2}$(3) | Maximum external frequency | - | 167 | - | 137 | - | 108 | MHz |
| $T_{PSUF}$ | Fast input register p-term clock setup time | 1.0 | - | 0.9 | - | 1.5 | - | ns |
| $T_{PSU1}$ | P-term clock setup time (single p-term) | 1.1 | - | 1.3 | - | 1.7 | - | ns |
| $T_{PSU2}$ | P-term clock setup time (OR array) | 1.4 | - | 1.7 | - | 2.5 | - | ns |
| $T_{PHF}$ | Fast input register p-term clock hold time | 0.5 | - | 0.9 | - | 0.7 | - | ns |
| $T_{PH}$ | P-term clock hold | 0.4 | - | 0.5 | - | 0.5 | - | ns |
| $T_{PCO}$ | P-term clock to output | - | 4.6 | - | 5.6 | - | 6.8 | ns |
| $T_{OE}/T_{OD}$ | Global OE to output enable/disable | - | 4.8 | - | 5.6 | - | 7.0 | ns |
| $T_{POE}/T_{POD}$ | P-term OE to output enable/disable | - | 5.4 | - | 6.4 | - | 7.3 | ns |
| $T_{MOE}/T_{MOD}$ | Macrocell driven OE to output enable/disable | - | 6.2 | - | 7.2 | - | 9.2 | ns |
| $T_{PAO}$ | P-term set/reset to output valid | - | 6.4 | - | 7.4 | - | 9.1 | ns |
| $T_{AO}$ | Global set/reset to output valid | - | 6.5 | - | 7.3 | - | 9.3 | ns |
| $T_{SUEC}$ | Register clock enable setup time | 2.0 | - | 2.5 | - | 2.6 | - | ns |
| $T_{HEC}$ | Register clock enable hold time | 0 | - | 0 | - | 0 | - | ns |
| $T_{CW}$ | Global clock pulse width High or Low | 1.2 | - | 2.0 | - | 3.0 | - | ns |
| $T_{PCW}$ | P-term pulse width High or Low | 5.0 | - | 6.0 | - | 7.5 | - | ns |
| $T_{DGSU}$ | Set-up before DataGATE latch assertion | 6.0 | - | 7.0 | - | 9.0 | - | ns |
| $T_{DGHO}$ | Hold to DataGATE latch assertion | 6.0 | - | 7.0 | - | 9.0 | - | ns |
| $T_{DGR}$ | DataGATE recovery to new data | - | 6.0 | - | 7.0 | - | 9.0 | ns |
| $T_{DGW}$ | DataGATE high pulse width | 2.0 | - | 2.5 | - | 4.0 | - | ns |
| $T_{CDRSU}$ | CDRST setup time before falling edge GCLK2 | 1.0 | - | 1.3 | - | 2.0 | - | ns |
| $T_{CDRHO}$ | Hold time CDRST after falling edge GCLK2 | 0 | - | 0 | - | 0 | - | ns |
| $T_{CONFIG}$ | Configuration time | | | | | | | µs |

**Notes:**

1. $F_{TOGGLE}$ ($1/2*T_{CW}$) is the maximum frequency of a dual edge triggered T flip-flop with output enabled.
2. $F_{SYSTEM1}$ ($1/T_{CYCLE}$) is the internal operating frequency for a device fully populated with 16-bit resettable binary counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array (one counter per function block).
3. $F_{EXT1}$ ($1/T_{SU2}+T_{CO}$) is the maximum external frequency using one p-term while $F_{EXT2}$ is through the OR array.

## Internal Timing Parameters

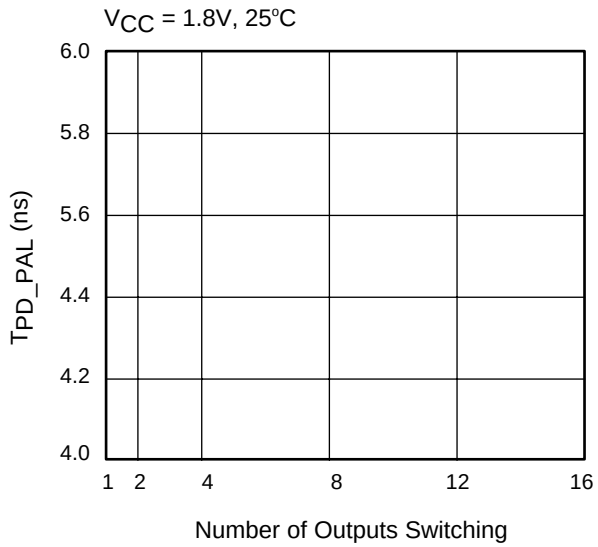
| Symbol | Parameter[1] | -5 | | -6 | | -7 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Buffer Delays** | | | | | | | | |
| $T_{IN}$ | Input buffer delay | - | 1.9 | - | 2.3 | - | 2.4 | ns |
| $T_{FIN}$ | Fast data register input delay | - | 2.2 | - | 2.4 | - | 3.0 | ns |
| $T_{GCK}$ | Global Clock buffer delay | - | 1.6 | - | 1.8 | - | 2.5 | ns |
| $T_{GSR}$ | Global set/reset buffer delay | - | 2.5 | - | 2.8 | - | 3.5 | ns |
| $T_{GTS}$ | Global 3-state buffer delay | - | 1.8 | - | 2.1 | - | 3.0 | ns |
| $T_{OUT}$ | Output buffer delay | - | 2.0 | - | 2.3 | - | 2.8 | ns |
| $T_{EN}$ | Output buffer enable/disable delay | - | 3.0 | - | 3.5 | - | 4.0 | ns |
| **P-term Delays** | | | | | | | | |
| $T_{CT}$ | Control term delay | - | 0.5 | - | 0.6 | - | 0.9 | ns |
| $T_{LOGI1}$ | Single P-term delay adder | - | 0.4 | - | 0.5 | - | 0.8 | ns |
| $T_{LOGI2}$ | Multiple P-term delay adder | - | 0.3 | - | 0.4 | - | 0.8 | ns |
| **Macrocell Delay** | | | | | | | | |
| $T_{PDI}$ | Input to output valid | - | 0.4 | - | 0.5 | - | 0.7 | ns |
| $T_{SUI}$ | Setup before clock | 1.2 | - | 1.4 | - | 1.8 | - | ns |
| $T_{HI}$ | Hold after clock | 0 | - | 0 | - | 0 | - | ns |
| $T_{ECSU}$ | Enable clock setup time | 1.2 | - | 1.4 | - | 1.8 | - | ns |
| $T_{ECHO}$ | Enable clock hold time | 0 | - | 0 | - | 0 | - | ns |
| $T_{COI}$ | Clock to output valid | - | 0.2 | - | 0.4 | - | 0.7 | ns |
| $T_{AOI}$ | Set/reset to output valid | - | 2.0 | - | 2.2 | - | 3.0 | ns |
| $T_{CDBL}$ | Clock doubler delay | - | 0 | - | 0 | - | 0 | ns |
| **Feedback Delays** | | | | | | | | |
| $T_{F}$ | Feedback delay | - | 2.4 | - | 2.4 | - | 3.0 | ns |
| $T_{OEM}$ | Macrocell to global OE delay | - | 1.4 | - | 1.5 | - | 2.0 | ns |
| **I/O Standard Time Adder Delays 1.5V I/O** | | | | | | | | |
| $T_{IN15}$ | Standard input adder | - | 0 | - | 0 | - | 0 | ns |
| $T_{HYS15}$ | Hysteresis input adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| $T_{OUT15}$ | Output adder | - | 0 | - | 0 | - | 0 | ns |
| $T_{SLEW15}$ | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| **I/O Standard Time Adder Delays 1.8V CMOS** | | | | | | | | |
| $T_{IN18}$ | Standard input adder | - | 0 | - | 0 | - | 0 | ns |
| $T_{HYS18}$ | Hysteresis input adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| $T_{OUT18}$ | Output adder | - | 0 | - | 0 | - | 0 | ns |
| $T_{SLEW}$ | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |

## Internal Timing Parameters *(Continued)*

| Symbol | Parameter[1] | -5 | | -6 | | -7 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **I/O Standard Time Adder Delays 2.5V CMOS** | | | | | | | | |
| $T_{IN25}$ | Standard input adder | - | 0.5 | - | 0.8 | - | 1.0 | ns |
| $T_{HYS25}$ | Hysteresis input adder | - | 1.5 | - | 2.5 | - | 3.0 | ns |
| $T_{OUT25}$ | Output adder | - | 1.5 | - | 2.5 | - | 3.0 | ns |
| $T_{SLEW25}$ | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| **I/O Standard Time Adder Delays 3.3V CMOS/TTL** | | | | | | | | |
| $T_{IN33}$ | Standard input adder | - | 0.7 | - | 1.0 | - | 2.0 | ns |
| $T_{HYS33}$ | Hysteresis input adder | - | 1.0 | - | 2.0 | - | 3.0 | ns |
| $T_{OUT33}$ | Output adder | - | 1.0 | - | 2.0 | - | 3.0 | ns |
| $T_{SLEW33}$ | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| **I/O Standard Time Adder Delays HSTL, SSTL** | | | | | | | | |
| SSTL2-1 | Input adder to TIN, TFIN, TGCK, TGSR,TGTS | - | 1.5 | - | 1.8 | - | 2.5 | ns |
| | Output adder to TOUT | - | 0 | - | 0 | - | 0 | ns |
| SSTL3-1 | Input adder to TIN, TFIN, TGCK, TGSR,TGTS | - | 1.5 | - | 1.8 | - | 2.5 | ns |
| | Output adder to TOUT | - | 0 | - | 0 | - | 0 | ns |
| HSTL-1 | Input adder to TIN, TFIN, TGCK, TGSR,TGTS | - | 1.5 | - | 1.8 | - | 2.5 | ns |
| | Output adder to TOUT | - | 0 | - | 0 | - | 0 | ns |

**Notes:**
1. 1.5 ns input pin signal rise/fall.

## Switching Characteristics




DS092_09_121501

## Pin Descriptions

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 1 | 1 | - | - | - | 2 | B3 | 2 |
| 1 | 2 | - | - | - | 208 | B4 | 2 |
| 1(GSR) | 3 | 99 | A3 | 143 | 206 | C4 | 2 |
| 1 | 4 | - | - | 142 | 205 | A2 | 2 |
| 1 | 5 | - | - | - | 203 | A3 | 2 |
| 1 | 6 | 97 | B4 | 140 | 202 | A4 | 2 |
| 1 | 7 | - | - | - | - | - | - |
| 1 | 8 | - | - | - | - | - | - |
| 1 | 9 | - | - | - | - | - | - |
| 1 | 10 | - | - | - | - | - | - |
| 1 | 11 | - | - | - | - | - | - |
| 1 | 12 | 96 | - | 139 | 201 | B5 | 2 |
| 1 | 13 | 95 | - | 138 | 200 | A5 | 2 |
| 1 | 14 | 94 | A4 | 137 | 199 | E8 | 2 |
| 1 | 15 | - | - | - | 198 | B6 | 2 |
| 1 | 16 | - | C5 | - | 197 | C7 | 2 |
| 2(GTS2) | 1 | 1 | A1 | 2 | 3 | D3 | 2 |
| 2 | 2 | - | - | - | 4 | C3 | 2 |
| 2(GTS3) | 3 | 2 | B2 | 3 | 5 | E3 | 2 |
| 2 | 4 | - | B1 | 4 | 6 | B2 | 2 |
| 2(GTS0) | 5 | 3 | C3 | 5 | 7 | D4 | 2 |
| 2 | 6 | - | - | - | 8 | D2 | 2 |
| 2 | 7 | - | - | - | - | - | - |
| 2 | 8 | - | - | - | - | - | - |
| 2 | 9 | - | - | - | - | - | - |
| 2 | 10 | - | - | - | - | - | - |
| 2 | 11 | - | - | - | - | - | - |
| 2(GTS1) | 12 | 4 | C2 | 6 | 9 | E5 | 2 |
| 2 | 13 | - | C1 | 7 | 10 | B1 | 2 |
| 2 | 14 | 6 | D2 | 9 | 12 | E4 | 2 |
| 2 | 15 | 7 | - | 10 | 14 | C1 | 2 |
| 2 | 16 | - | D1 | - | - | E2 | 2 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 3 | 1 | - | - | 136 | 196 | A6 | 2 |
| 3 | 2 | - | B5 | 135 | 195 | D7 | 2 |
| 3 | 3 | - | - | 134 | 194 | B7 | 2 |
| 3 | 4 | - | A5 | - | 193 | E9 | 2 |
| 3 | 5 | 93 | - | 133 | 192 | A7 | 2 |
| 3 | 6 | | C6 | | 191 | D8 | 2 |
| 3 | 7 | - | - | - | - | - | - |
| 3 | 8 | - | - | - | - | - | - |
| 3 | 9 | - | - | - | - | - | - |
| 3 | 10 | - | - | - | - | - | - |
| 3 | 11 | - | - | - | - | - | - |
| 3 | 12 | 92 | - | - | 189 | B8 | 2 |
| 3 | 13 | - | B6 | - | 188 | C8 | 2 |
| 3 | 14 | 91 | A6 | 132 | 187 | A8 | 2 |
| 3 | 15 | - | C7 | - | 186 | E11 | 2 |
| 3 | 16 | 90 | B7 | 131 | 185 | E10 | 2 |
| 4 | 1 | 8 | E3 | 11 | 15 | F2 | 2 |
| 4 | 2 | 9 | - | 12 | 16 | F3 | 2 |
| 4 | 3 | 10 | E2 | 13 | 17 | G4 | 2 |
| 4 | 4 | - | E1 | 14 | 18 | G3 | 2 |
| 4 | 5 | 11 | F3 | 15 | 19 | F5 | 2 |
| 4 | 6 | 12 | F2 | 16 | 20 | G5 | 2 |
| 4 | 7 | - | - | - | - | - | - |
| 4 | 8 | - | - | - | - | - | - |
| 4 | 9 | - | - | - | - | - | - |
| 4 | 10 | - | - | - | - | - | - |
| 4 | 11 | - | - | - | - | - | - |
| 4 | 12 | - | F1 | 17 | 21 | H2 | 2 |
| 4 | 13 | 13 | G1 | - | 22 | H4 | 2 |
| 4 | 14 | - | - | 18 | 23 | H3 | 2 |
| 4 | 15 | - | - | - | - | H1 | 2 |
| 4 | 16 | - | - | - | 25 | H5 | 2 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 5 | 1 | - | L3 | - | 49 | R1 | 1 |
| 5 | 2 | - | - | 33 | 48 | N4 | 1 |
| 5 | 3 | - | - | - | 47 | N2 | 1 |
| 5(GCK1) | 4 | 23 | L2 | 32 | 46 | M3 | 1 |
| 5 | 5 | | L1 | 31 | 45 | P1 | 1 |
| 5(GCK0) | 6 | 22 | K3 | 30 | 44 | M2 | 1 |
| 5 | 7 | - | - | - | - | - | - |
| 5 | 8 | - | - | - | - | - | - |
| 5 | 9 | - | - | - | - | - | - |
| 5 | 10 | - | - | - | - | - | - |
| 5 | 11 | - | - | - | - | - | - |
| 5 | 12 | - | - | - | 43 | L3 | 1 |
| 5 | 13 | - | - | - | 41 | N1 | 1 |
| 5 | 14 | - | - | 28 | 40 | L4 | 1 |
| 5 | 15 | - | - | - | 39 | M1 | 1 |
| 5 | 16 | - | K1 | - | 38 | L5 | 1 |
| 6 | 1 | - | M1 | 34 | 50 | N3 | 1 |
| 6 (CDRST) | 2 | 24 | M2 | 35 | 51 | P2 | 1 |
| 6 | 3 | - | - | - | 54 | P4 | 1 |
| 6(GCK2) | 4 | 27 | N2 | 38 | 55 | P5 | 1 |
| 6 | 5 | - | - | - | 56 | R2 | 1 |
| 6 | 6 | - | - | - | 57 | T1 | 1 |
| 6 | 7 | - | - | - | - | - | - |
| 6 | 8 | - | - | - | - | - | - |
| 6 | 9 | - | - | - | - | - | - |
| 6 | 10 | - | - | - | - | - | - |
| 6 | 11 | - | - | - | - | - | - |
| 6(DGE) | 12 | 28 | P2 | 39 | 58 | T2 | 1 |
| 6 | 13 | - | M3 | 40 | 60 | N5 | 1 |
| 6 | 14 | 29 | N3 | 41 | 61 | R4 | 1 |
| 6 | 15 | - | P3 | 42 | 62 | M5 | 1 |
| 6 | 16 | 30 | M4 | 43 | 63 | R5 | 1 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 7 | 1 | - | - | - | 37 | K4 | 1 |
| 7 | 2 | - | - | - | 36 | L2 | 1 |
| 7 | 3 | - | - | - | 35 | K3 | 1 |
| 7 | 4 | - | - | - | 34 | L1 | 1 |
| 7 | 5 | 19 | J2 | 26 | 32 | K5 | 1 |
| 7 | 6 | 18 | J1 | 25 | 31 | K2 | 1 |
| 7 | 7 | - | - | - | - | - | - |
| 7 | 8 | - | - | - | - | - | - |
| 7 | 9 | - | - | - | - | - | - |
| 7 | 10 | - | - | - | - | - | - |
| 7 | 11 | 17 | H3 | 24 | 30 | J4 | 1 |
| 7 | 12 | 16 | H2 | 23 | 29 | K1 | 1 |
| 7 | 13 | 15 | H1 | 22 | 28 | J3 | 1 |
| 7 | 14 | 14 | G3 | 21 | 27 | J2 | 1 |
| 7 | 15 | - | G2 | 20 | - | J5 | 1 |
| 7 | 16 | - | - | 19 | - | J1 | 1 |
| 8 | 1 | - | N4 | 44 | 64 | R6 | 1 |
| 8 | 2 | - | - | 45 | 65 | N6 | 1 |
| 8 | 3 | - | - | 46 | 66 | R3 | 1 |
| 8 | 4 | - | - | - | 67 | M6 | 1 |
| 8 | 5 | - | - | 48 | 69 | T3 | 1 |
| 8 | 6 | 32 | - | 49 | 70 | P6 | 1 |
| 8 | 7 | - | - | - | - | - | - |
| 8 | 8 | - | - | - | - | - | - |
| 8 | 9 | - | - | - | - | - | - |
| 8 | 10 | - | - | - | - | - | - |
| 8 | 11 | 33 | M5 | 50 | 71 | T4 | 1 |
| 8 | 12 | 34 | N5 | 51 | 72 | P7 | 1 |
| 8 | 13 | 35 | P5 | 52 | 73 | T5 | 1 |
| 8 | 14 | 36 | M6 | - | 74 | N7 | 1 |
| 8 | 15 | 37 | N6 | - | 75 | R7 | 1 |
| 8 | 16 | - | - | - | 76 | M7 | 1 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 9 | 1 | 78 | C12 | 112 | 160 | B13 | 2 |
| 9 | 2 | 79 | B12 | 113 | 161 | B14 | 2 |
| 9 | 3 | - | - | - | 162 | C13 | 2 |
| 9 | 4 | 80 | A12 | 114 | 163 | A15 | 2 |
| 9 | 5 | | | | 164 | C12 | 2 |
| 9 | 6 | 81 | C11 | 115 | 165 | B12 | 2 |
| 9 | 7 | - | - | - | - | - | - |
| 9 | 8 | - | - | - | - | - | - |
| 9 | 9 | - | - | - | - | - | - |
| 9 | 10 | - | - | - | - | - | - |
| 9 | 11 | - | - | - | 166 | D13 | 2 |
| 9 | 12 | 82 | B11 | 116 | 167 | A14 | 2 |
| 9 | 13 | - | - | 117 | 168 | E13 | 2 |
| 9 | 14 | - | A11 | 118 | 169 | A13 | 2 |
| 9 | 15 | - | - | 119 | 170 | C11 | 2 |
| 9 | 16 | - | C10 | - | 171 | A12 | 2 |
| 10 | 1 | 77 | A13 | 111 | 159 | A16 | 2 |
| 10 | 2 | 76 | B13 | 110 | 158 | B15 | 2 |
| 10 | 3 | 74 | C13 | 107 | 155 | C14 | 2 |
| 10 | 4 | 73 | C14 | 106 | 154 | G11 | 2 |
| 10 | 5 | 72 | D12 | 105 | 153 | B16 | 2 |
| 10 | 6 | 71 | D13 | 104 | 152 | D15 | 2 |
| 10 | 7 | - | - | - | - | - | - |
| 10 | 8 | - | - | - | - | - | - |
| 10 | 9 | - | - | - | - | - | - |
| 10 | 10 | - | - | - | - | - | - |
| 10 | 11 | | | | 151 | E14 | 2 |
| 10 | 12 | 70 | D14 | 103 | 150 | C16 | 2 |
| 10 | 13 | - | - | - | 149 | F14 | 2 |
| 10 | 14 | - | E12 | 102 | 148 | F13 | 2 |
| 10 | 15 | - | - | - | 147 | E15 | 2 |
| 10 | 16 | - | E13 | 101 | 146 | G13 | 2 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 11 | 1 | - | B10 | - | - | B11 | 2 |
| 11 | 2 | - | | - | 173 | D11 | 2 |
| 11 | 3 | - | A10 | - | 174 | A11 | 2 |
| 11 | 4 | - | - | - | 175 | D10 | 2 |
| 11 | 5 | - | C9 | 120 | - | B10 | 2 |
| 11 | 6 | - | - | 121 | - | E12 | 2 |
| 11 | 7 | - | - | - | - | - | - |
| 11 | 8 | - | - | - | - | - | - |
| 11 | 9 | - | - | - | - | - | - |
| 11 | 10 | - | - | - | - | - | - |
| 11 | 11 | 85 | A8 | 124 | 178 | F12 | 2 |
| 11 | 12 | 86 | B8 | 125 | 179 | B9 | 2 |
| 11 | 13 | 87 | C8 | 126 | 180 | C9 | 2 |
| 11 | 14 | 89 | - | 128 | 182 | C10 | 2 |
| 11 | 15 | - | - | 129 | 183 | A9 | 2 |
| 11 | 16 | - | - | 130 | 184 | D9 | 2 |
| 12 | 1 | - | - | - | 145 | F15 | 2 |
| 12 | 2 | - | - | 100 | 144 | G14 | 2 |
| 12 | 3 | - | - | - | 143 | E16 | 2 |
| 12 | 4 | - | - | - | 142 | H12 | 2 |
| 12 | 5 | - | F12 | - | 140 | F16 | 2 |
| 12 | 6 | - | F13 | - | 139 | H16 | 2 |
| 12 | 7 | - | - | - | - | - | - |
| 12 | 8 | - | - | - | - | - | - |
| 12 | 9 | - | - | - | - | - | - |
| 12 | 10 | - | - | - | - | - | - |
| 12 | 11 | 68 | F14 | 98 | 138 | G15 | 2 |
| 12 | 12 | - | G12 | 97 | 137 | H13 | 2 |
| 12 | 13 | 67 | G13 | 96 | 136 | G16 | 2 |
| 12 | 14 | 66 | - | 95 | 135 | H14 | 2 |
| 12 | 15 | 65 | - | 94 | 134 | H15 | 2 |
| 12 | 16 | - | - | - | - | J12 | 2 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 13 | 1 | - | N13 | 75 | 107 | R15 | 1 |
| 13 | 2 | 53 | N14 | 76 | 108 | T16 | 1 |
| 13 | 3 | - | M12 | 77 | 109 | N14 | 1 |
| 13 | 4 | 54 | - | - | 110 | R16 | 1 |
| 13 | 5 | - | M13 | 78 | 111 | N15 | 1 |
| 13 | 6 | 55 | - | 79 | 112 | M15 | 1 |
| 13 | 7 | - | - | - | - | - | - |
| 13 | 8 | - | - | - | - | - | - |
| 13 | 9 | - | - | - | - | - | - |
| 13 | 10 | - | - | - | - | - | - |
| 13 | 11 | - | - | - | - | - | - |
| 13 | 12 | - | M14 | 80 | 113 | M13 | 1 |
| 13 | 13 | 56 | - | 81 | 114 | P16 | 1 |
| 13 | 14 | - | L12 | 82 | 115 | N16 | 1 |
| 13 | 15 | - | - | - | 116 | L14 | 1 |
| 13 | 16 | - | L13 | - | 117 | M14 | 1 |
| 14 | 1 | 52 | P14 | 74 | 106 | P15 | 1 |
| 14 | 2 | - | - | 71 | 103 | P14 | 1 |
| 14 | 3 | 50 | P12 | 70 | 102 | P13 | 1 |
| 14 | 4 | - | M11 | 69 | 101 | R13 | 1 |
| 14 | 5 | 49 | N11 | - | 100 | N13 | 1 |
| 14 | 6 | - | P11 | 68 | - | R14 | 1 |
| 14 | 7 | - | - | - | - | - | - |
| 14 | 8 | - | - | - | - | - | - |
| 14 | 9 | - | - | - | - | - | - |
| 14 | 10 | - | - | - | - | - | - |
| 14 | 11 | - | - | - | - | - | - |
| 14 | 12 | - | - | - | 99 | T15 | 1 |
| 14 | 13 | - | - | 66 | 97 | R12 | 1 |
| 14 | 14 | 46 | P10 | 64 | 95 | N11 | 1 |
| 14 | 15 | 44 | - | - | - | M11 | 1 |
| 14 | 16 | - | P9 | 61 | 91 | N10 | 1 |

## Pin Descriptions *(Continued)*

| Function Block | Macro-cell | VQ100 | CP132 | TQ144 | PQ208 | FT256 | I/O Bank |
|---|---|---|---|---|---|---|---|
| 15 | 1 | - | - | - | 118 | L15 | 1 |
| 15 | 2 | - | L14 | 83 | 119 | L13 | 1 |
| 15 | 3 | - | - | - | 120 | M12 | 1 |
| 15 | 4 | - | - | - | 121 | M16 | 1 |
| 15 | 5 | - | - | - | 122 | K14 | 1 |
| 15 | 6 | - | - | - | 123 | L16 | 1 |
| 15 | 7 | - | - | - | - | - | - |
| 15 | 8 | - | - | - | - | - | - |
| 15 | 9 | - | - | - | - | - | - |
| 15 | 10 | - | - | - | - | - | - |
| 15 | 11 | 58 | K13 | 85 | 125 | K15 | 1 |
| 15 | 12 | 59 | K14 | 86 | 126 | L12 | 1 |
| 15 | 13 | 60 | J12 | 87 | 127 | K16 | 1 |
| 15 | 14 | 61 | J13 | 88 | 128 | J14 | 1 |
| 15 | 15 | 63 | H13 | 91 | - | J15 | 1 |
| 15 | 16 | 64 | H12 | 92 | 131 | J13 | 1 |
| 16 | 1 | - | - | - | 90 | P10 | 1 |
| 16 | 2 | - | - | - | 89 | R10 | 1 |
| 16 | 3 | - | M8 | - | 88 | T10 | 1 |
| 16 | 4 | - | - | - | 87 | R9 | 1 |
| 16 | 5 | 43 | N8 | 60 | 86 | N9 | 1 |
| 16 | 6 | 42 | - | 59 | 85 | M8 | 1 |
| 16 | 7 | - | - | - | - | - | - |
| 16 | 8 | - | - | - | - | - | - |
| 16 | 9 | - | - | - | - | - | - |
| 16 | 10 | - | - | - | - | - | - |
| 16 | 11 | 41 | P8 | 58 | 84 | T8 | 1 |
| 16 | 12 | 40 | M7 | 57 | 83 | P8 | 1 |
| 16 | 13 | 39 | N7 | 56 | 82 | R8 | 1 |
| 16 | 14 | - | - | - | 80 | T7 | 1 |
| 16 | 15 | - | - | 54 | 78 | N8 | 1 |
| 16 | 16 | - | P6 | 53 | 77 | T6 | 1 |

**Notes:**

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.

## XC2C256 JTAG, Power/Ground, No Connect Pins and Total User I/O

| Pin Type | VQ100 | CP132 | TQ144 | PQ208 | FT256 |
|---|---|---|---|---|---|
| TCK | 48 | M10 | 67 | 98 | P12 |
| TDI | 45 | M9 | 63 | 94 | R11 |
| TDO | 83 | B9 | 122 | 176 | A10 |
| TMS | 47 | N10 | 65 | 96 | N12 |
| $V_{AUX}$ (JTAG supply voltage) | 5 | D3 | 8 | 11 | F4 |
| Power internal ($V_{CC}$) | 26, 57 | P1, K12, A2 | 1, 37, 84 | 1, 53, 124 | P3, K13, D12, D5 |
| Power Bank 1 I/O ($V_{CCIO1}$) | 20, 38, 51 | J3, P7, G14, P13 | 27, 55, 73, 93 | 33, 59, 79, 92, 105, 132 | J6, K6, L7, L8, J11, K11, L10, L9 |
| Power Bank 2 I/O ($V_{CCIO2}$) | 88, 98 | A14, C4, A7 | 109, 127, 141 | 26, 133, 157, 172, 181, 204 | F7, F8, G6, H6, F10, F9, H11 |
| Ground | 21, 25, 31, 62, 69, 75, 84, 100 | K2, N1, P4, N9, N12, J14, H14, E14, B14, A9, B3 | 29, 36, 47, 62, 72, 89, 90, 99, 108, 123, 144 | 13, 24, 42, 52, 68, 81, 93, 104, 129, 130, 141, 156, 177, 190, 207 | F11, F6, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, L11, L6 |
| No connects | - | - | - | - | A1, C2, E6, D1, E1, G2, F1, G1, M4, T9, P9, M9, M10, T11, T12, T13, P11, T14, J16, K12, D16, G12, C15, D14, D6, C6, E7, C5 |
| Total user I/O | 72 | 98 | 110 | 165 | 176 |

## Ordering Information

| Part Number | Pin/Ball Spacing | $\theta_{JA}$ (C/Watt) | $\theta_{JC}$ (C/Watt) | Package Type | Package Dimensions | I/O | Commercial (C) Industrial (I) |
|---|---|---|---|---|---|---|---|
| XC2C256-5VQ100 | 0.5mm | 43.1 | 10.9 | Very Thin Quad Flat Pack | 14mm x 14mm | 72 | C |
| XC2C256-6VQ100 | 0.5mm | 43.1 | 10.9 | Very Thin Quad Flat Pack | 14mm x 14mm | 72 | C |
| XC2C256-7VQ100 | 0.5mm | 43.1 | 10.9 | Very Thin Quad Flat Pack | 14mm x 14mm | 72 | C |
| XC2C256-5CP132 | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 8mm x 8mm | 98 | C |
| XC2C256-6CP132 | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 8mm x 8mm | 98 | C |
| XC2C256-7CP132 | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 8mm x 8mm | 98 | C |
| XC2C256-5TQ144 | 0.5mm | 37.2 | 7.2 | Thin Quad Flat Pack | 20mm x 20mm | 110 | C |
| XC2C256-6TQ144 | 0.5mm | 37.2 | 7.2 | Thin Quad Flat Pack | 20mm x 20mm | 110 | C |
| XC2C256-7TQ144 | 0.5mm | 37.2 | 15.0 | Thin Quad Flat Pack | 20mm x 20mm | 110 | C |
| XC2C256-5PQ208 | 0.5mm | 36.9 | 9.7 | Plastic Quad Flat Pack | 28mm x 28mm | 165 | C |
| XC2C256-6PQ208 | 0.5mm | 36.9 | 9.7 | Plastic Quad Flat Pack | 28mm x 28mm | 165 | C |
| XC2C256-7PQ208 | 0.5mm | 36.9 | 9.7 | Plastic Quad Flat Pack | 28mm x 28mm | 165 | C |
| XC2C256-5FT256 | 1.0mm | 34.6 | 6.1 | Fine Pitch Thin BGA | 17mm x 17mm | 176 | C |
| XC2C256-6FT256 | 1.0mm | 34.6 | 6.1 | Fine Pitch Thin BGA | 17mm x 17mm | 176 | C |
| XC2C256-7FT256 | 1.0mm | 34.6 | 6.1 | Fine Pitch Thin BGA | 17mm x 17mm | 176 | C |
| XC2C256-7VQ100 | 0.5mm | 43.1 | 10.9 | Very Thin Quad Flat Pack | 14mm x 14mm | 72 | I |
| XC2C256-7CP132 | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 8mm x 8mm | 98 | I |
| XC2C256-7TQ144 | 0.5mm | 37.2 | 7.2 | Thin Quad Flat Pack | 20mm x 20mm | 110 | I |
| XC2C256-7PQ208 | 0.5mm | 36.9 | 9.7 | Plastic Quad Flat Pack | 28mm x 28mm | 165 | I |
| XC2C256-7FT256 | 1.0mm | 34.6 | 6.1 | Fine Pitch Thin BGA | 17mm x 17mm | 176 | I |

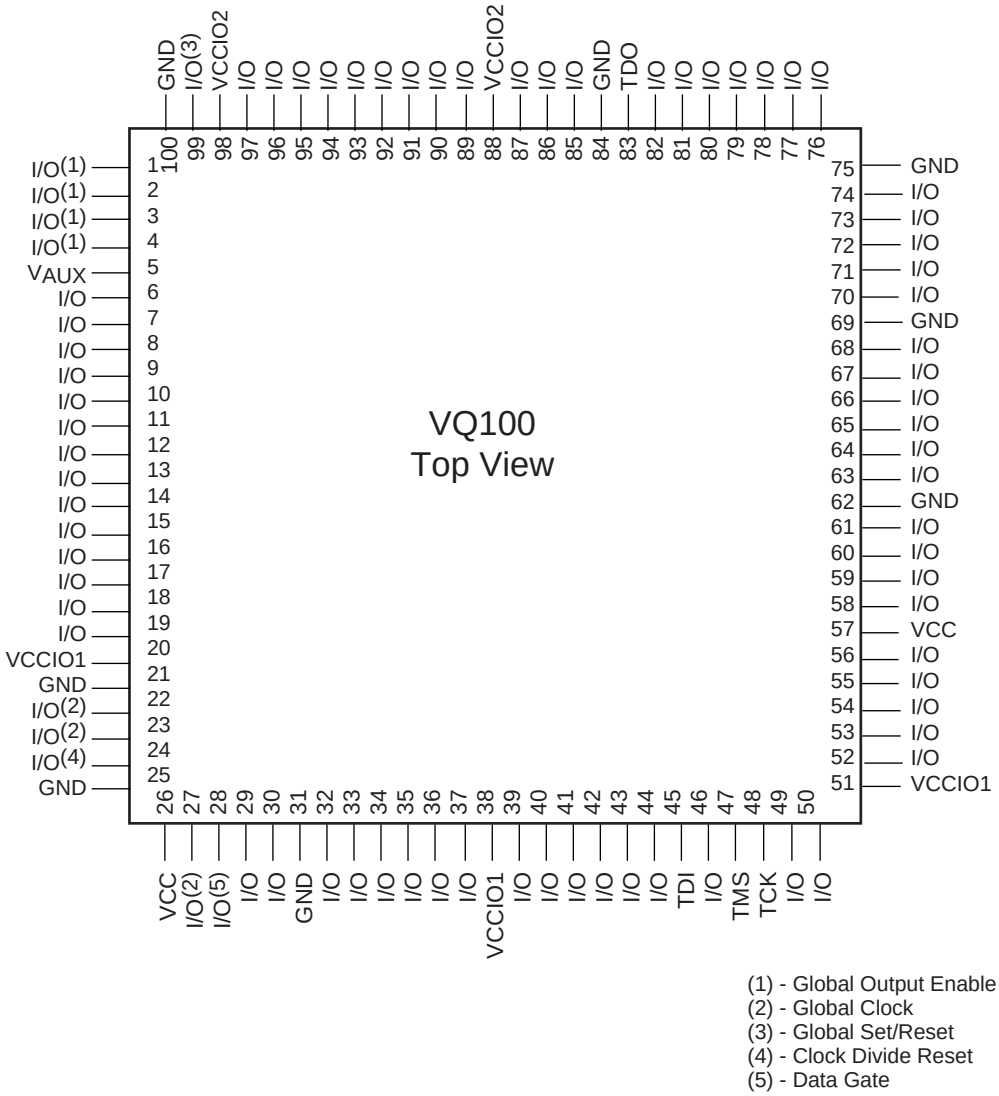
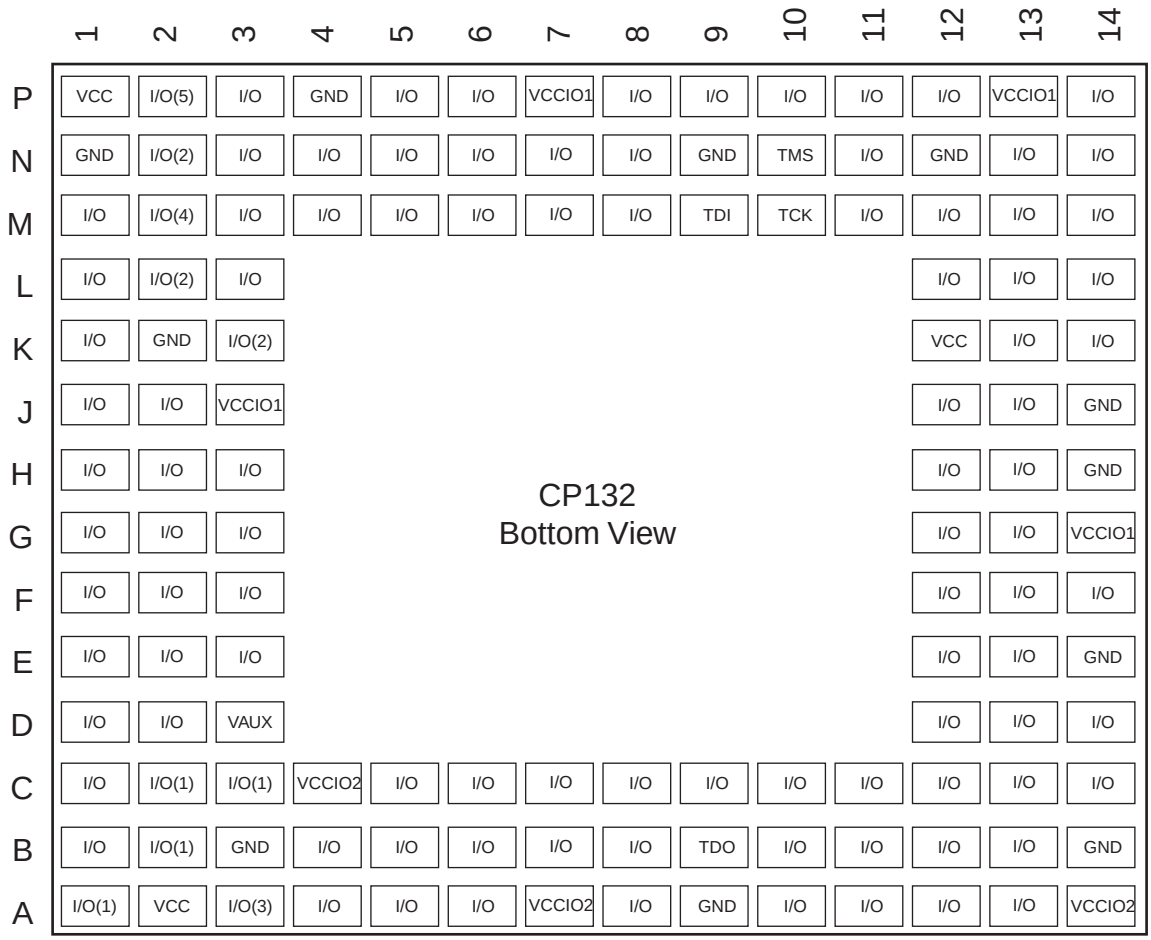
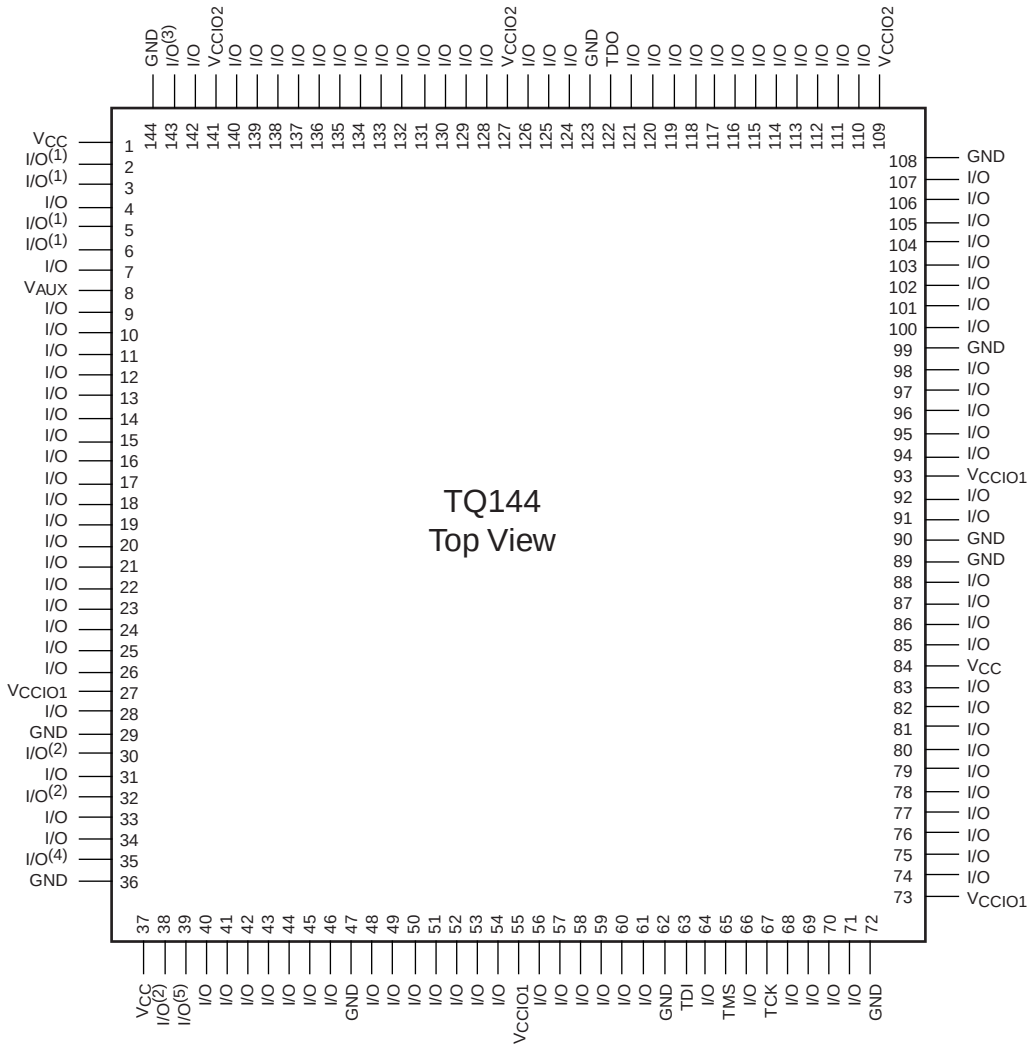



*Figure 2:* **VQ100 Very Thin Quad Flat Pack**




(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

*Figure 3:* **CP132 Chip Scale Package**




(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

*Figure 4:* **TQ144 Thin Quad Flat Pack**

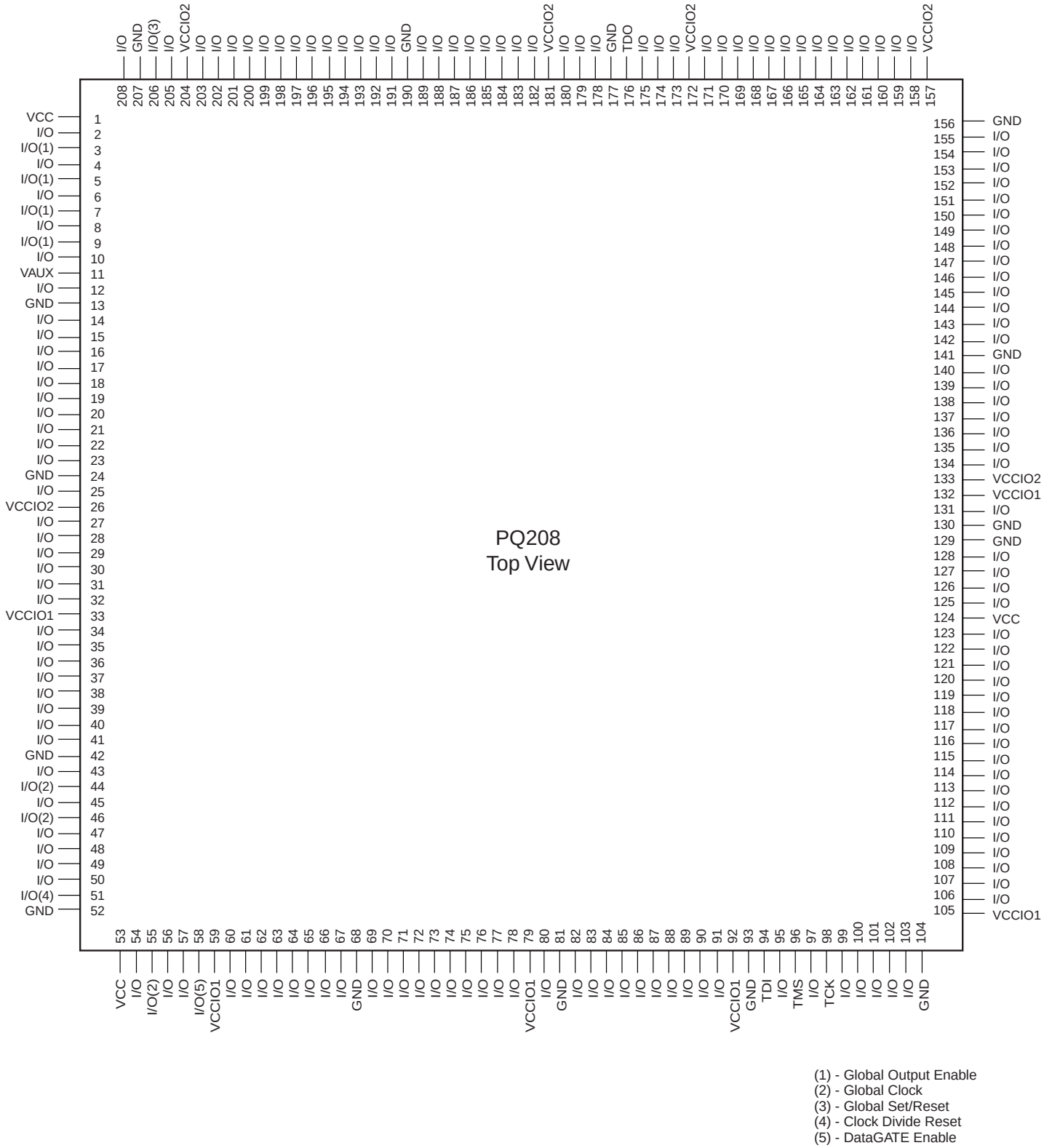
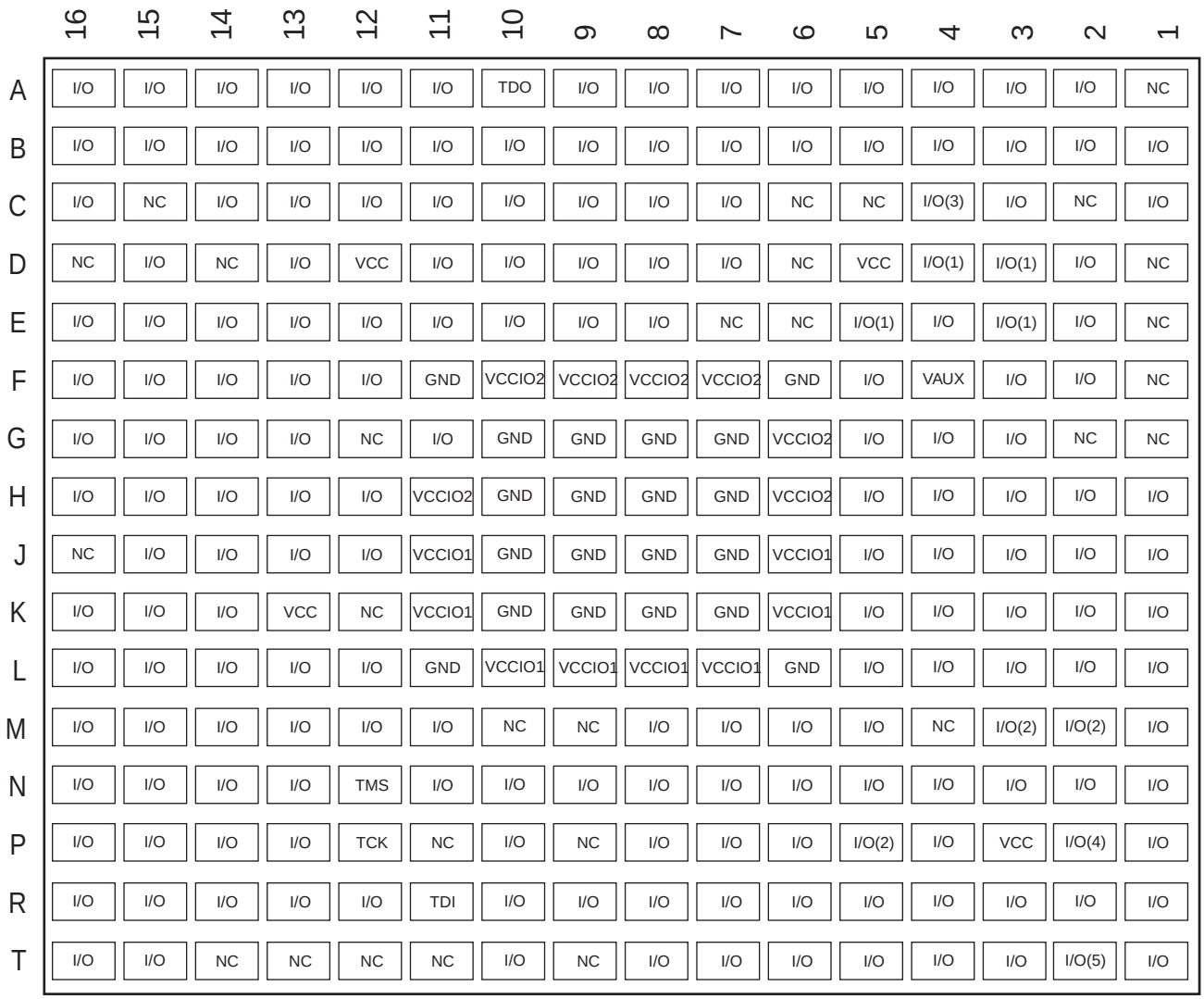



*Figure 5:* **PQ208 Quad Flat Package**



| | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | I/O | I/O | I/O | I/O | I/O | I/O | TDO | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | NC |
| B | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| C | I/O | NC | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | NC | NC | I/O(3) | I/O | NC | I/O |
| D | NC | I/O | NC | I/O | VCC | I/O | I/O | I/O | I/O | I/O | NC | VCC | I/O(1) | I/O(1) | I/O | NC |
| E | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | NC | NC | I/O(1) | I/O | I/O(1) | I/O | NC |
| F | I/O | I/O | I/O | I/O | I/O | GND | VCCIO2 | VCCIO2 | VCCIO2 | VCCIO2 | GND | I/O | VAUX | I/O | I/O | NC |
| G | I/O | I/O | I/O | I/O | NC | I/O | GND | GND | GND | GND | VCCIO2 | I/O | I/O | I/O | NC | NC |
| H | I/O | I/O | I/O | I/O | I/O | VCCIO2 | GND | GND | GND | GND | VCCIO2 | I/O | I/O | I/O | I/O | I/O |
| J | NC | I/O | I/O | I/O | I/O | VCCIO1 | GND | GND | GND | GND | VCCIO1 | I/O | I/O | I/O | I/O | I/O |
| K | I/O | I/O | I/O | VCC | NC | VCCIO1 | GND | GND | GND | GND | VCCIO1 | I/O | I/O | I/O | I/O | I/O |
| L | I/O | I/O | I/O | I/O | I/O | GND | VCCIO1 | VCCIO1 | VCCIO1 | VCCIO1 | GND | I/O | I/O | I/O | I/O | I/O |
| M | I/O | I/O | I/O | I/O | I/O | I/O | NC | NC | I/O | I/O | I/O | I/O | NC | I/O(2) | I/O(2) | I/O |
| N | I/O | I/O | I/O | I/O | TMS | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| P | I/O | I/O | I/O | I/O | TCK | NC | I/O | NC | I/O | I/O | I/O | I/O(2) | I/O | VCC | I/O(4) | I/O |
| R | I/O | I/O | I/O | I/O | I/O | TDI | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| T | I/O | I/O | NC | NC | NC | NC | I/O | NC | I/O | I/O | I/O | I/O | I/O | I/O | I/O(5) | I/O |

FT256 Bottom View

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

*Figure 6:* **FT256 Fine Pitch Thin BGA**

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 05/09/02 | 1.0 | Initial Xilinx release. |
| 05/13/02 | 1.1 | Updated AC Electrical Characteristics and added new parameters. |