Fermilab
Experiment Electronic Systems Group

DRAFT

Example Slave Interface for the CDF Front-end Crate (CDF_SLAVE)

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8/1/95
revised
3/28/96

1.0 Introduction

This note is intended to provide a very general example of a slave interface for the CDF Front-end Crate. The interface provides for A32/D32 transfers only. Both single word and block modes are supported. Address modifier codes 09 and 0B are supported.

This note assumes the reader is familiar with CDFNOTE 2388 and the VMEbus Specification.

2.0 Features

SLOT Address

The slot address is hardcoded into the Backplane on Pins GA0*-GA4* of the J1 VME64 Extensions Backplane. The five high order VMEbus address bits (VME_A31:VME_A27) will be compared to these slot address pins (GA4*:GA0*). A match will select the board.
(All boards should be designed to allow for this type of addressing.)

FPGA Slave Interface Design

An example CDF Front-end slave interface is implemented in a Xilinx 3164A part. The Xilinx schematics are included. This is a seed schematic which is being customized on a board by board basis. There is no reason why a designer could not choose another method of implementing this interface. The Xilinx design is being provided as an example.

Timing waveforms for a single word write and a block read are provided in an Appendix.

ETL Transcivers

The new TI ETL(Enhanced Transceiver Logic) transceivers, SN74ABTE16245, are being used in the design. These devices offer higher bandwidth, support live insertion, have low capacitance, are TTL compatible and offer high-drive outputs. They should lead to less noise on the backplane, which is our main reason for selecting them.

5 Row Connector

A 5 row connector designed for use by VME64Extensions' backplanes is now available. The five row connector is fully backward compatible with the current 3 row DIN connectors. All new board designs should allow for the use of the new 5 row connector and make all additional ground connections. On the PCB footprint, rows A, B and C remain in the same location. Rows z and d are located 100 mil to the left and right.

Memory Map (ALL MAPPING SHOULD FOLLOW CDFNOTE 2388)

YY00 0000 Diagnostic Register (32 bit Read/Write)

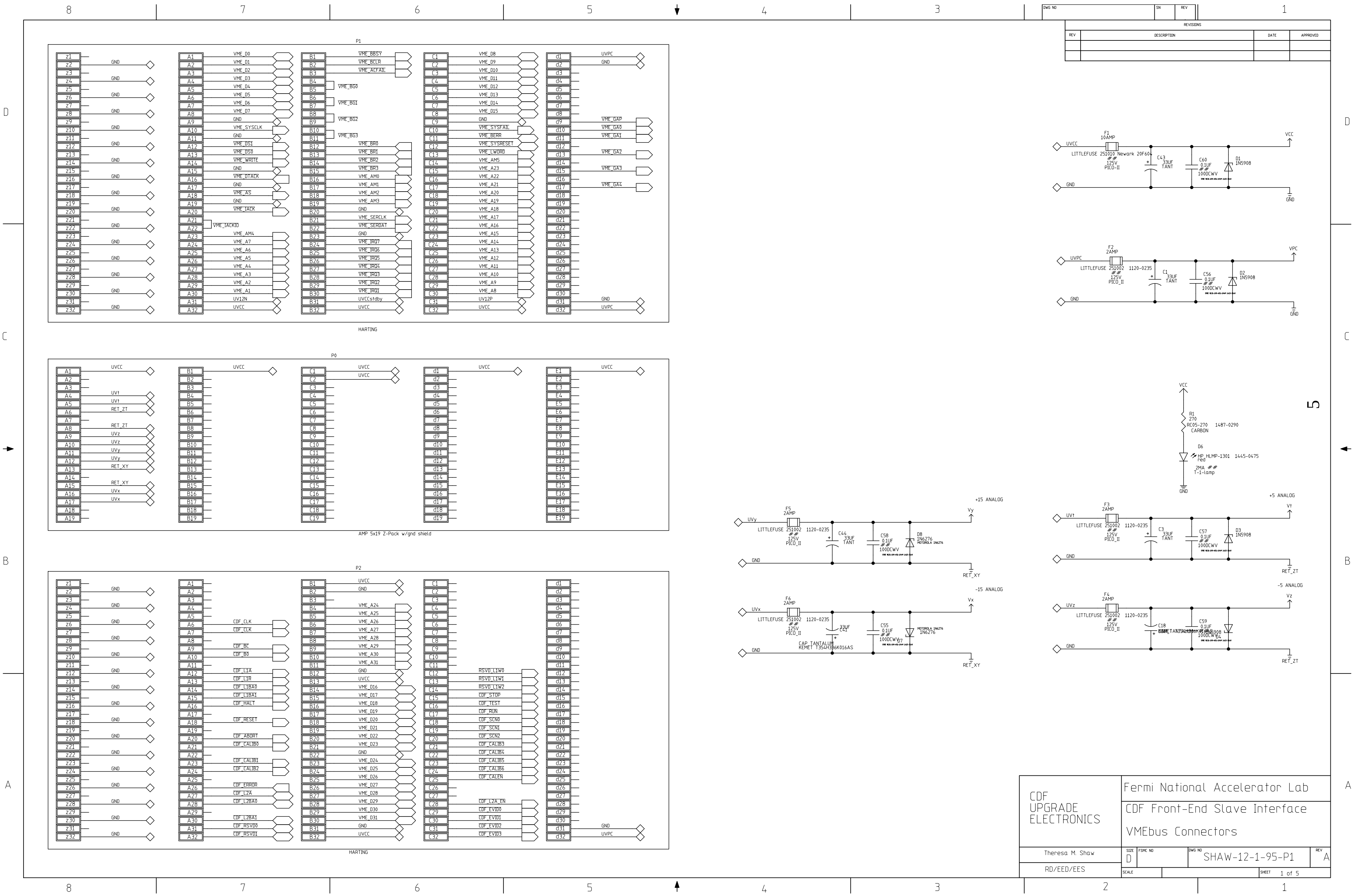
YY00 0004 Control (This register is **NOT** shown on schematic)

Bit	Function	
0	Software Reset	; =1 will issue software Reset
1-31	Undefined	

YY10 0020 - YY10 009C ID PROM (upper 8 bits)

YY is the VME slot address of the CDF_SLAVE.

APPENDIX A
Simple “CDF” VMEbus Slave Interface



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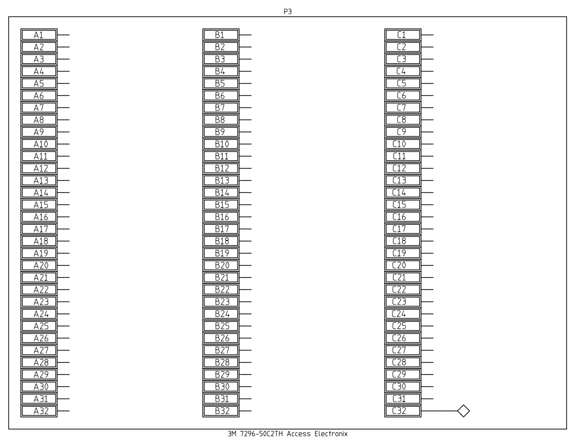

CDF UPGRADE ELECTRONICS

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CDF Front-End Slave Interface

VMEbus P3 Connectors

Theresa M. Shaw	SIZE D	FSMC NO	DWG NO SHAW-12-1-95-P2		REV A	
RD/EED/EES	SCALE			SHEET 2 of 5		

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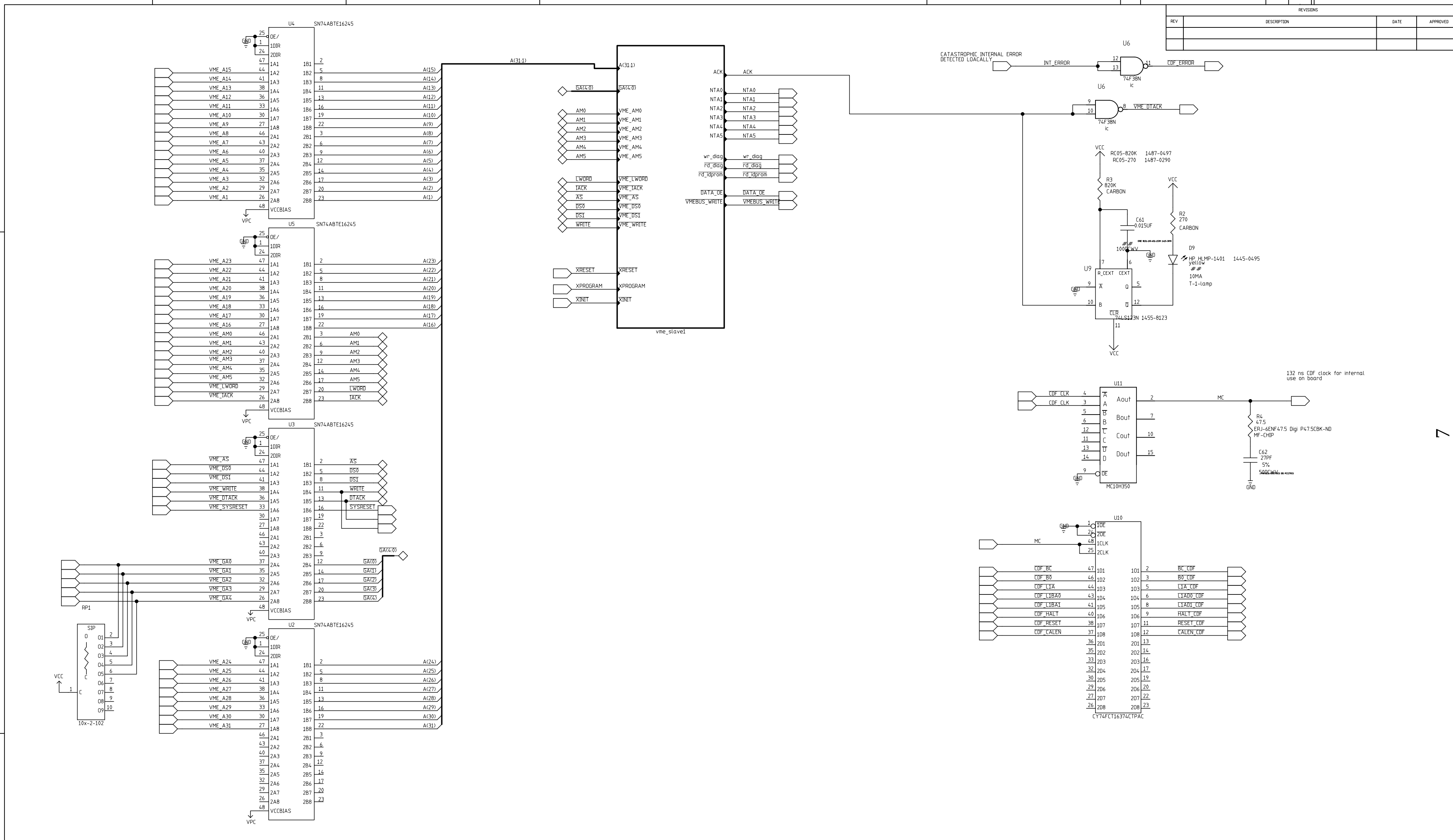
/tmp_mnt/home/cad_job2/job/ees-vme-seed/cae/cdf_slave.sbk(02;10) Thu Mar 28 14:34:41 1996



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CDF Front-End Slave Interface

VMEbus Slave Interface

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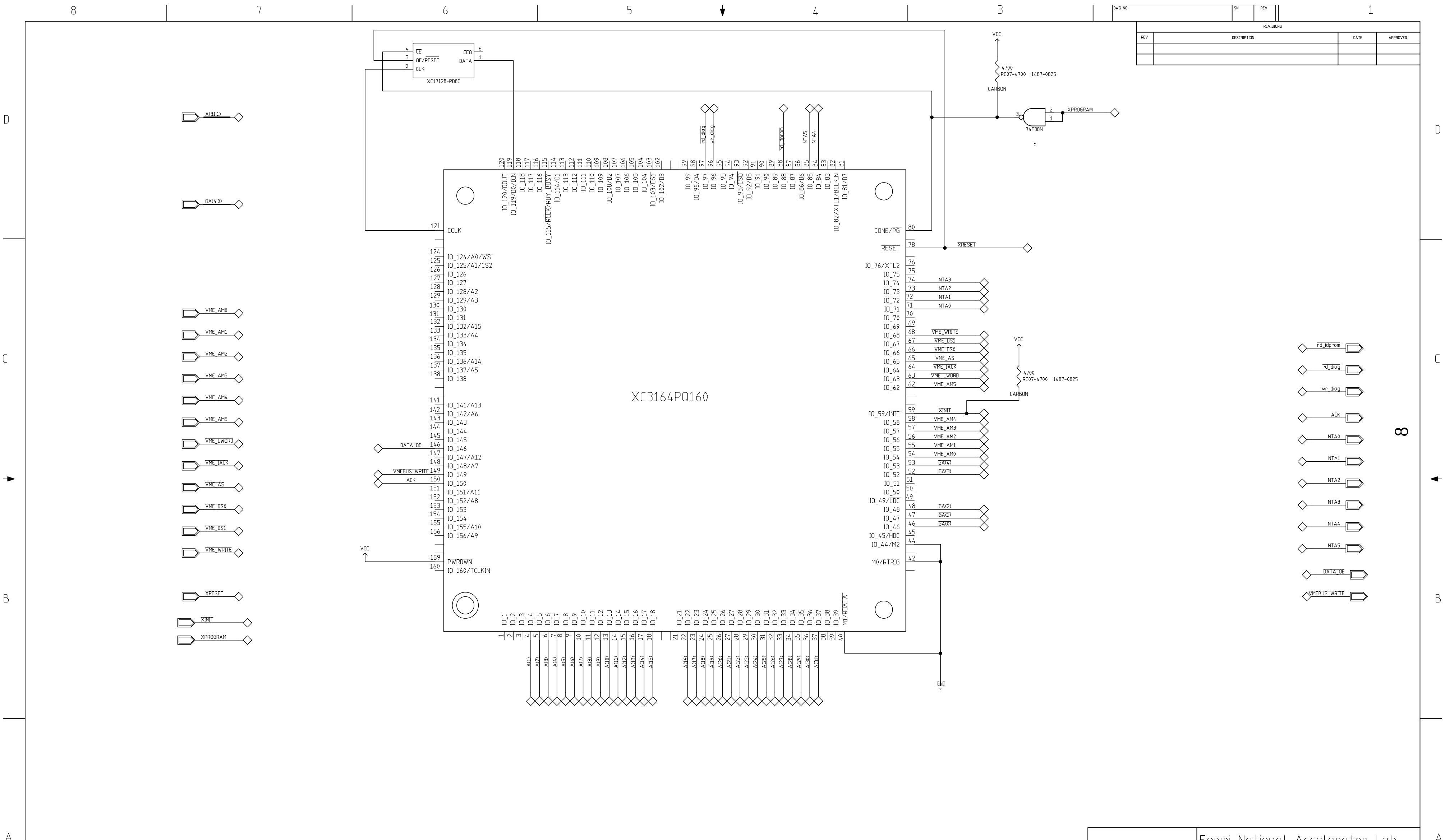
RD/EED/EES

SIZE D | DWG NO SHAW-12-01-95-P3 | REV A

SHEET 3 of 5



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CDF Front-End Slave Interface

XILINX Interface IC

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RD/EED/EES

SIZE D | DWG NO SHAW-12-01-95-P3-A | REV A

SHEET 1 of 1

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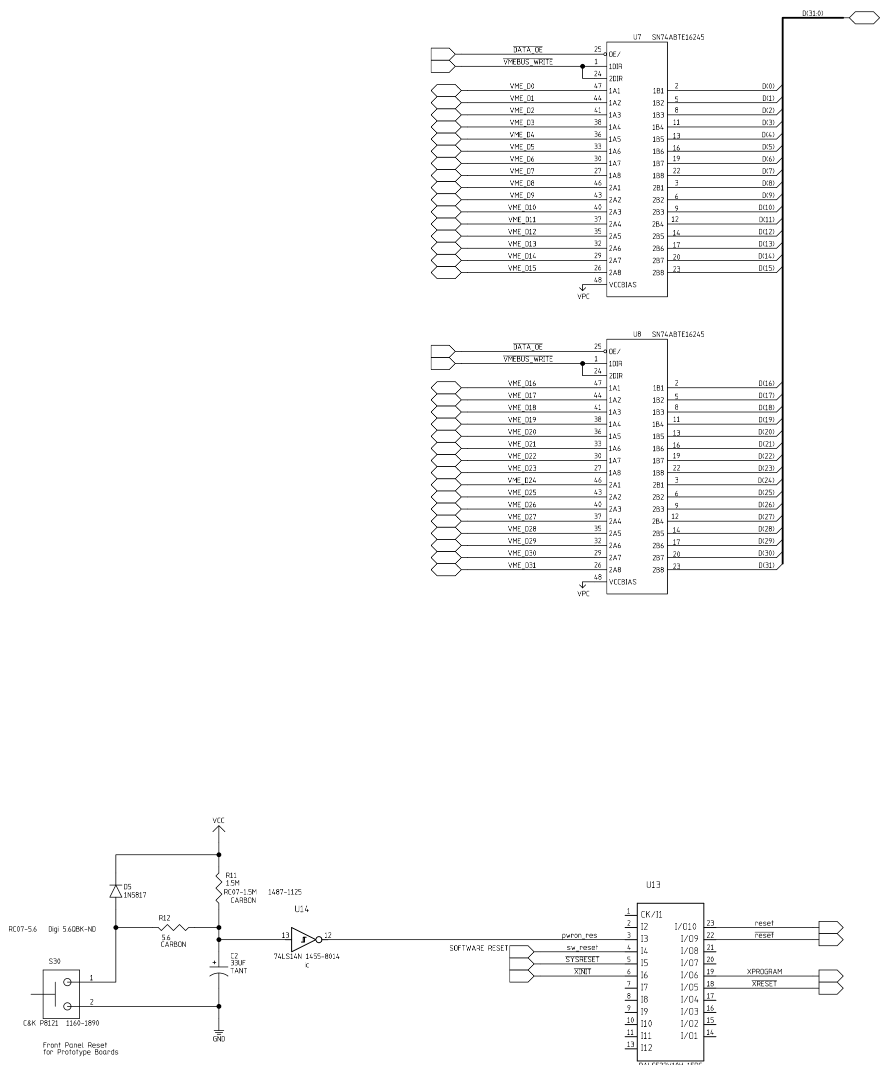
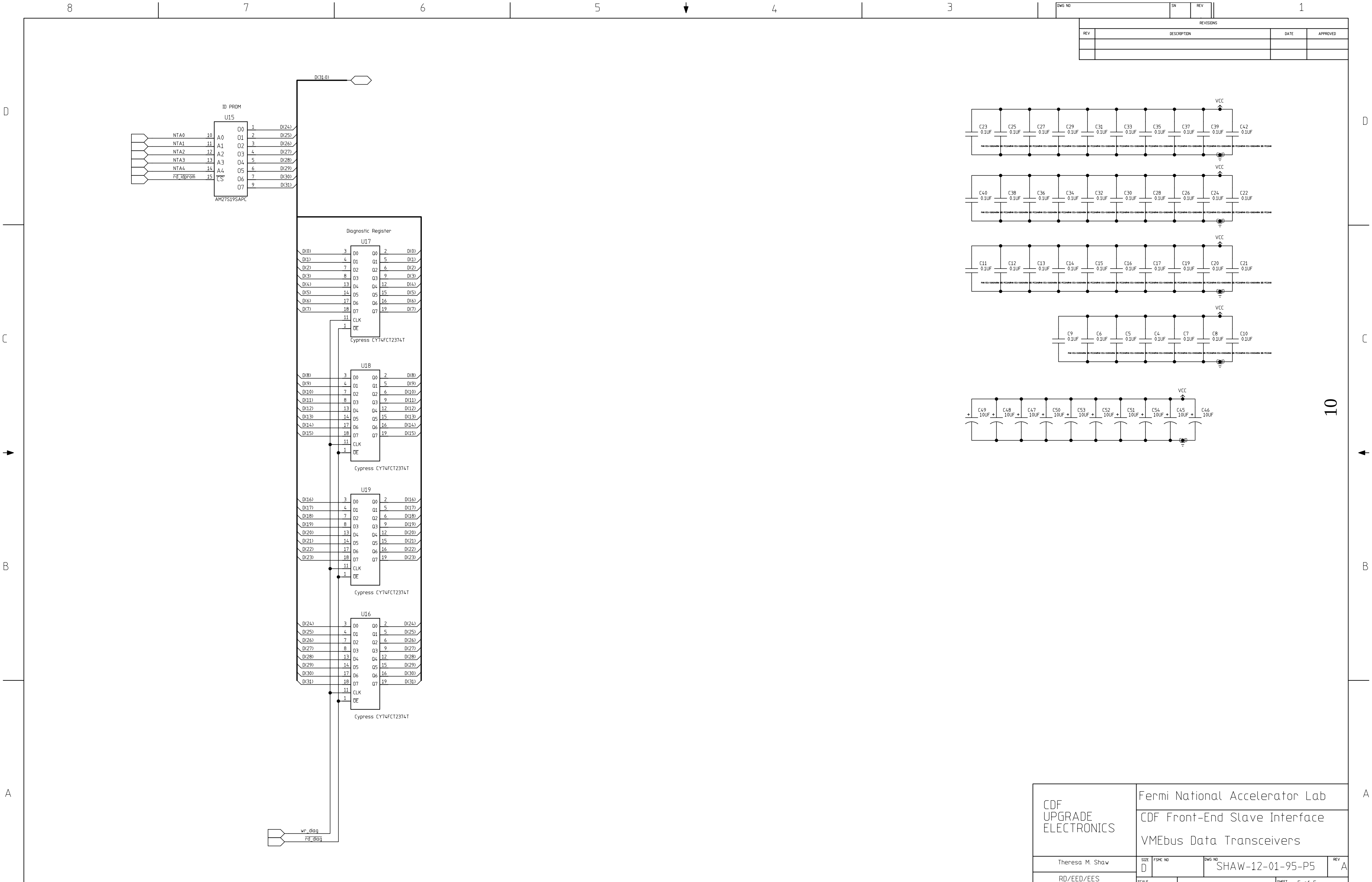


CDF UPGRADE ELECTRONICS	Fermi National Accelerator Lab
	CDF Front-End Slave Interface
	VMEbus Data Transceivers
Theresa M. Shaw	SIZE D — DWG NO SHAW-12-01-95-P4 — REV A
RD/EED/EES	SHEET 4 of 5

/tmp_mnt/home/cad_job2/job/ees-vme-seed/cae/cdf_slave.sbk(04;3) Thu Mar 28 14:34:55 1996



CDF UPGRADE ELECTRONICS

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CDF Front-End Slave Interface

VMEbus Data Transceivers

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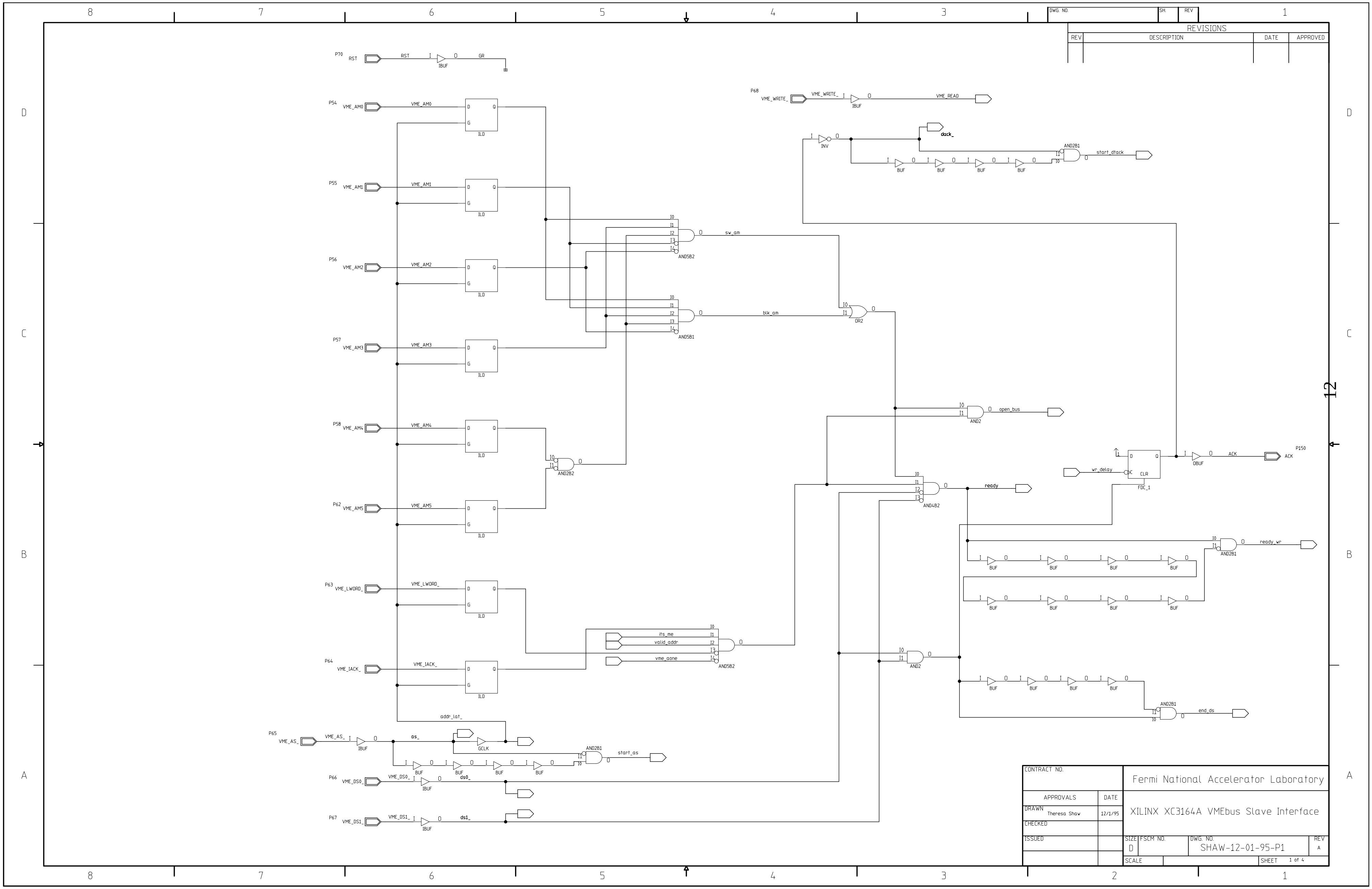
RD/EED/EES

SIZE D | DWG NO SHAW-12-01-95-P5 | REV A

SHEET 5 of 5

APPENDIX B
Xilinx FPGA Schematics for CDF VMEbus Slave



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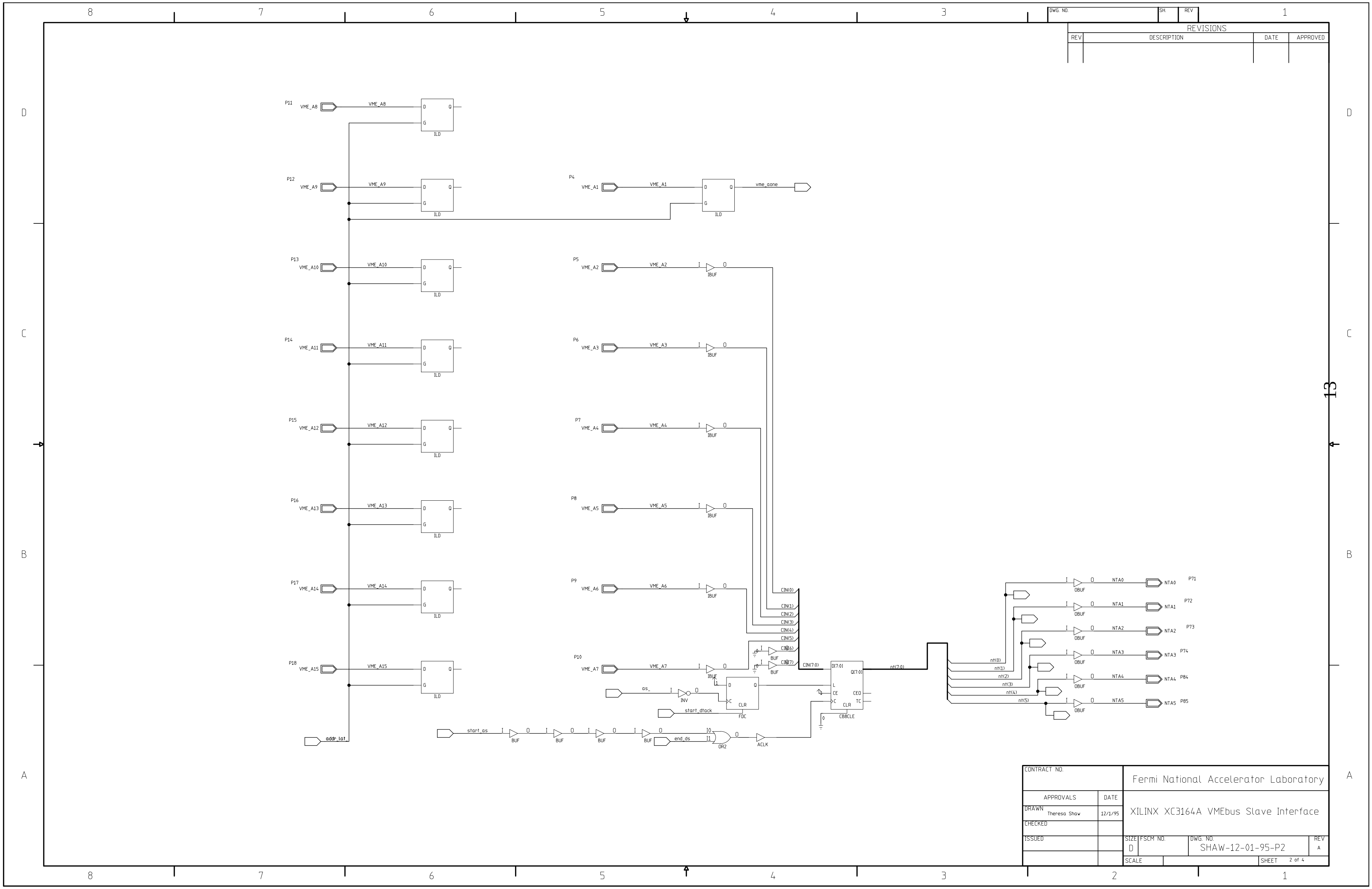

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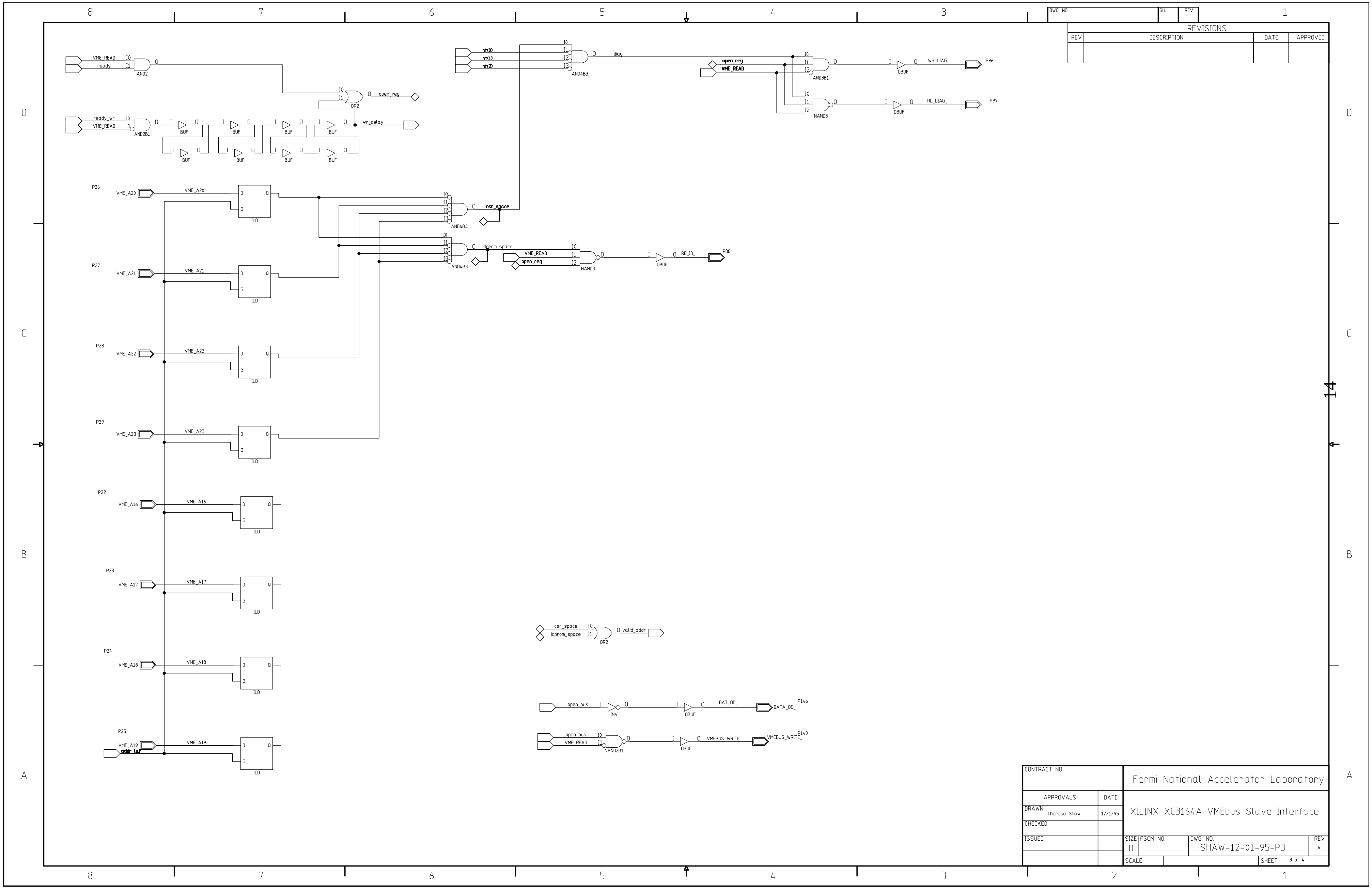

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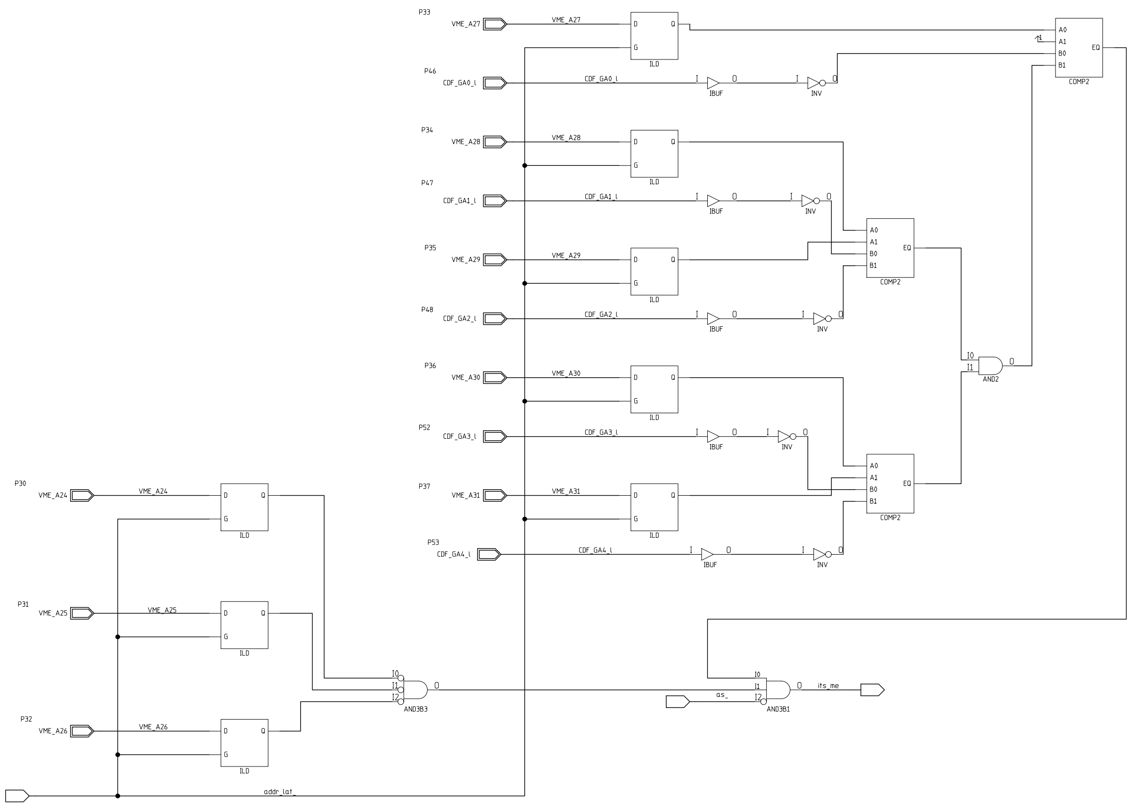

DWG. NO.	SH.	REV

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

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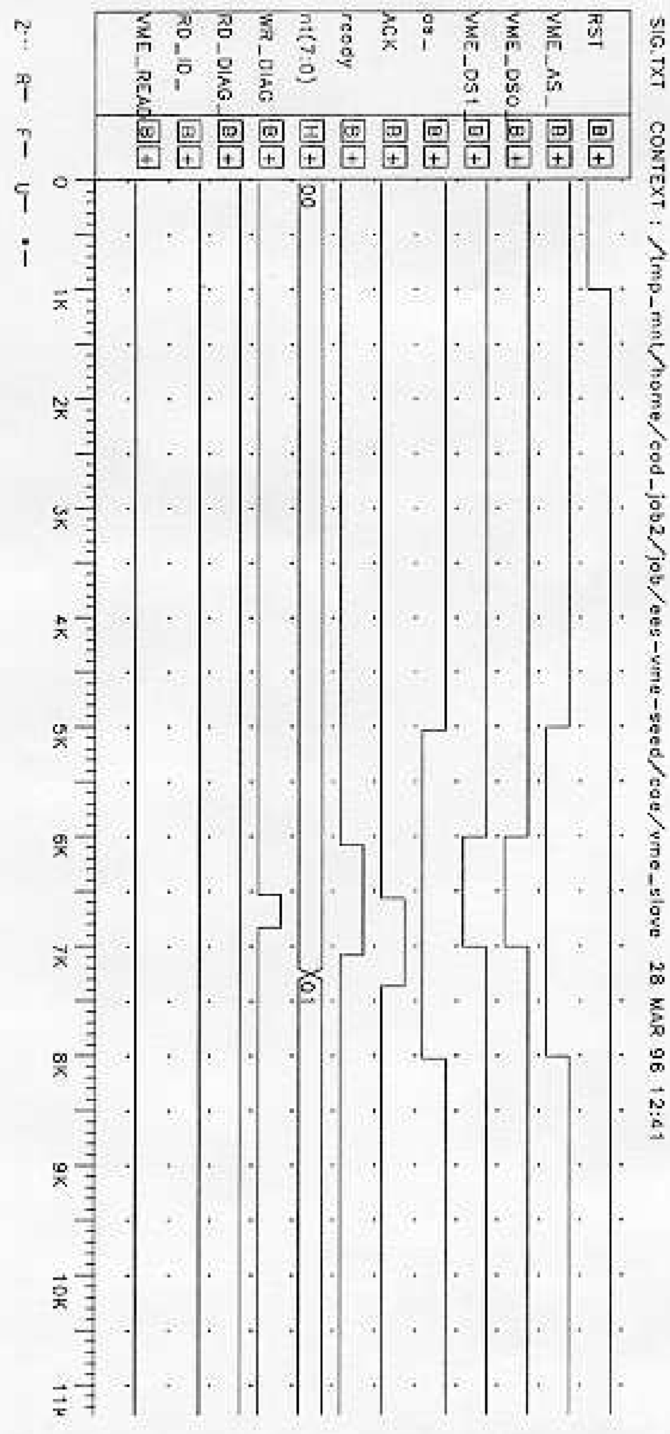
CONTRACT NO.		Fermi National Accelerator Laboratory
APPROVALS	DATE	XILINX XC3164A VMEbus Slave Interface
DRAWN Theresa Shaw	12/1/95	
CHECKED		
ISSUED		SIZE D · FSCM NO. · DWG. NO. SHAW-12-01-95-P4 · REV A
		SCALE · SHEET 4 of 4

APPENDIX C
Xilinx FPGA Sample Simulation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VME_AS_
VME_DS0_
VME_DS1_
ds_
ACK
ready
WR_DIAG
RD_DIAG_
RD_ID_
VME_READ
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01
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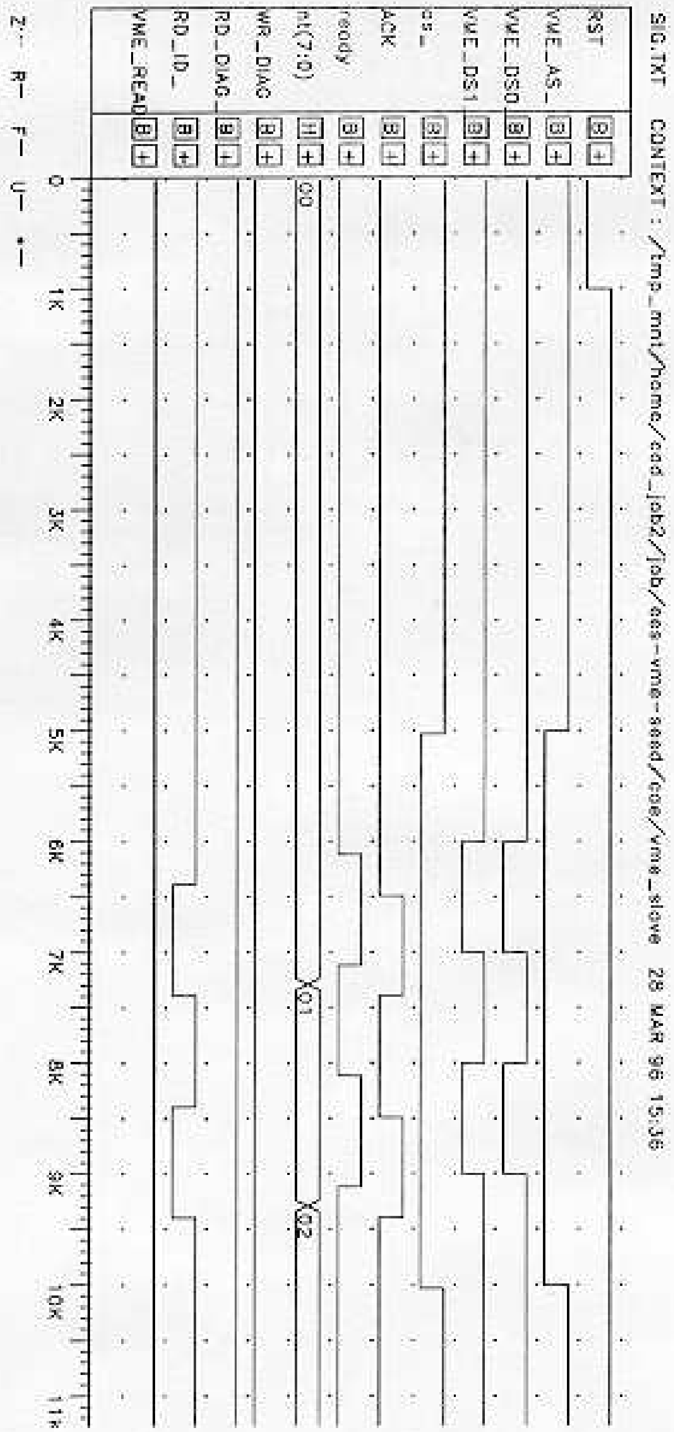
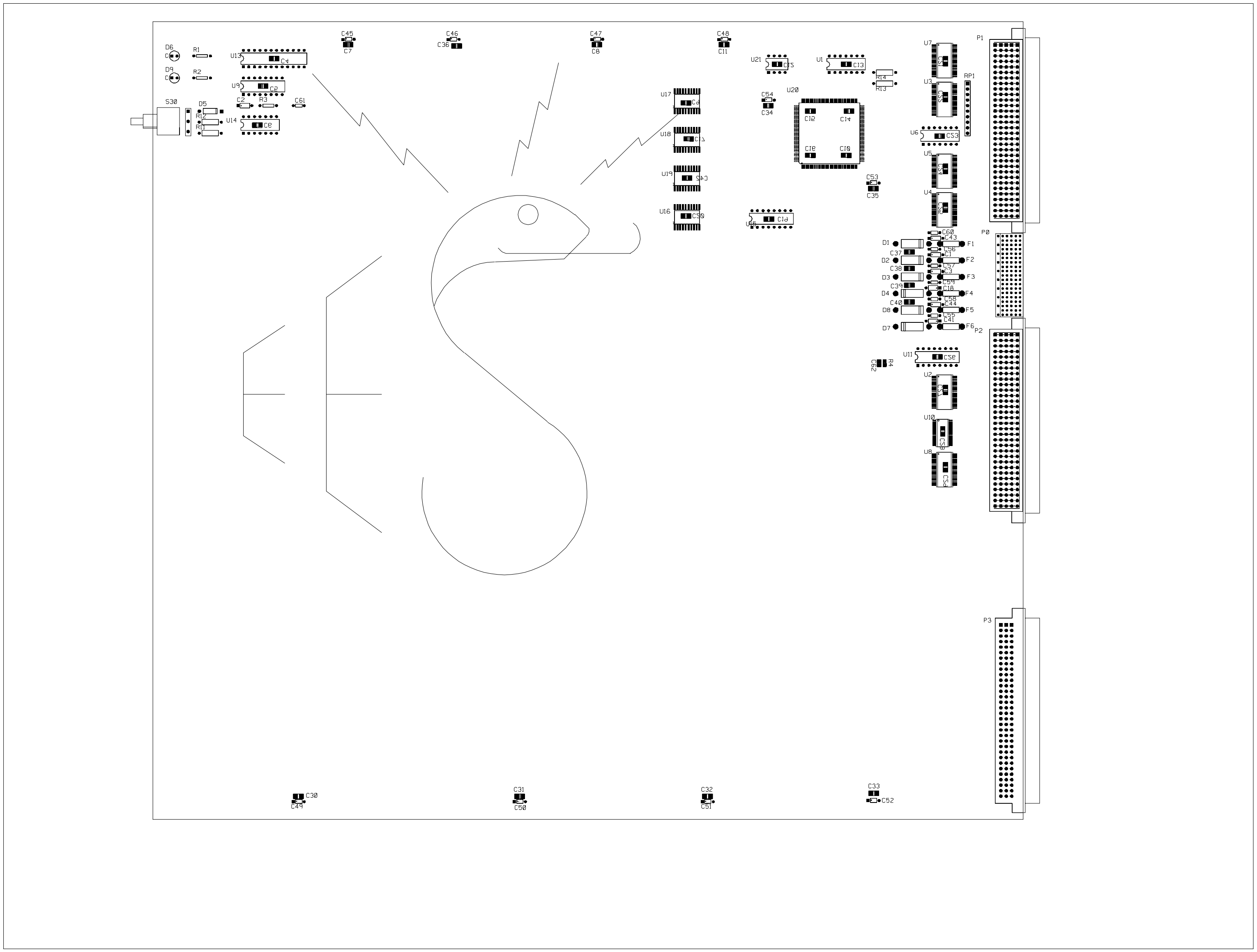
1K
2K
3K
4K
5K
6K
7K
8K
9K
10K



SIG.TXT CONTEXT : /tmp_mnt/home/esd_job2/job/ess-vme-seed/cse/vme_slave 28 MAR 96 15:36
RST
VME_AS_
VME_DS0
VME_DS1
cs_
ACK
ready
n(7:0)
WR_DIAG
RD_DIAG_
RD_ID_
VME_READ
00
01
02
0
1K
2K
3K
4K
5K
6K
7K
8K
9K
10K
Z- R- F- U- *-

APPENDIX D
Printed Circuit Layout



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