APPENDIX A

INTERFERENCE SUPPRESSION TECHNIQUES

INTRODUCTION

Many of the new radar systems planned for deployment in the 2700-2900 MHz band will operate in designated heavily used areas or in a collocated environment where many of the old radar systems will have relatively high transmitter spurious emission levels. Therefore, the new radar systems may be subjected to pulsed interference in performing their missions. The incorporation of interference suppression circuitry or software in the design of new radar systems will ensure that system performance requirements can be satisfied in the type of pulsed interference environment anticipated. Environmental signal characteristics for the 2700-2900 MHz band are discussed in Section 6.

Interference suppression techniques, often called Electronic Counter - Countermeasures (ECCM), are generally classified into three categories: antenna, transmitter and receiver. The receiver interference suppression techniques are further categorized into predetection, detection and post-detection. It suffices to say that, ECCM is vast electronic field in itself. In recent years there have been several comprehensive treatise on this area (Johnston, 1979) and (Maksimov, 1979).

The following is a cursory discussion on several receiver post-detection interference suppression techniques currently used in radionavigation and meteorological radars.

INTEGRATOR

Description

The process of summing the echo pulses from a target is called integration. Integrators are generally used in radars for two reasons:

1. To enhance weak desired tagets for PPI display.

2. To suppress asynchronous pulsed interference.

The principle of the radar video integrator is that radar signal returns from a point target consist of a series of pulses generated as the radar antenna beam scans past the target, all of which fall in the same range bin in successive periods (synchronous with the system). It is this series of synchronous pulses from a target which permits integration of target returns to enhance the weak signals. The integrator also suppresses asynchronous pulsed interference since the interfering pulses will not be separated in time by the radar period, and thus will not occur in the same range bin in successive periods (asynchronous with the system). Therefore, the asynchronous interference will not add-up, and can be suppressed.

Basically two types of integrators have been used in radionavigation radars. The most common type of integrator is the feedback integrator shown in Figure A-1. A binary integrator shown in Figure A-2 is used in the ASR-7 and AN/GPN-12 radars.

Feedback Integrator

The feedback integrator shown in Figure A-1 consists of an input limiter, an adder, and a feedback loop with an output limiter and a delay equal to the time between transmitter pulses (1/PRF). The overall gain, K, of the feedback loop is less than unity to prevent instability. The input limiter serves as a video clipping circuit to provide constant level input pulses to the feedback integrator, and is a necessary integrator circuitry element to suppress asynchronous pulsed interference. The input limiter limit level is usually adjustable, and controls the transfer properties of the feedback integrator.

The signal transfer properties of the feedback integrator to noise, desired signal, and asynchronous pulsed interference are discussed in detail in a report by Hinkle, Pratt and Levy (1979).

Figure A-3 shows a simulated normal channel radar unintegrated output for three interference sources (ASR-5, INR = 10 dB; ASR-8, INR = 15 dB; and AN/FPS= 90, INR = 20 dB), and a desired target signal-to-noise ratio of 15 dB. Figure A-4 shows for the same interference condition the radar output after feedback integration for an input limit level setting of 0.34 volts. The asynchronous interference has been suppressed by the feedback integrator.

Binary Integrator

The binary integrator shown in Figure A-2 consists of a threshold detector or comparator, binary counter (adder/subtractor circuit), a five bit shift register memory, and a digital-to-analog (D/A) converter. Each PRF period is divided into range bins. If a pulse of target return pulse train exceeds the

comparator threshold level, the enhancer stores a one level digital signal in the shift register memory for that range bin. If the successive pulses of the target return pulse train continue above the comparator threshold in the given range bin, the binary counter will add one level to the stored digital signal in the shift register memory in each PRF period until a maximum integrator level of 31 is reached. If in any PRF period the signal fails to exceed the comparator threshold, the binary counter subtracts one from the stored integrator state in a given range bin until a digital signal level of zero is reached. The subtraction provides the target return pulse train signal decay required after the antenna beam has passed the target, and also enables the suppression of asynchronous interfering signals. The voltage amplitude at the enhancer D/A converter output is determined by the binary counter level (0 to 31) for the particular range bin times .125 volts. Therefore, for a binary counter level of 31, the maximum enhancer output voltage would be 3.875 volts (31 x .125).

The FAA modified the ASR-7 binary integrator to improve the desired signal probability of detection, target azimuth shift, and angular resolution loss caused by the conventional integrator used in the ASR-7 radar. A detailed discussion of the transfer properties of the binary integrator are given by Hinkle, Pratt and Levy (1979).

Figure A-4 shows a simulated normal channel radar unintegrated output for three interference sources (ASR-5, INR = 10 dB; ASR-8, INR = 15 dB; and AN/FPS-90, INR = 20 dB), and a desired target signal-to-noise ratio of 15 dB. Figure A-5 shows for the same interference condition the radar output after binary integration. The asynchronous interference has been suppressed.

Trade-offs:

Target azimuth shift:	$.9^{o}$ for feedback integrator
	$.2^{o}$ for binary integrator
Angular Resolution:	1.2^{o} for feedback integrator
	0^{o} for binary integrator

Desired Signal Sensitivity:

Approximately 1 dB decrease when integrator is adjusted to suppress pulsed interference with the "Normal" video mode and with "MTI" in the 2 and 3 pulse canceller mode without feedback. However, in the "MTI" mode with feedback, the sensitivity loss can exceed 2 dB; adjusting the integrator to suppress interference may not be a practical solution in this case.

References

1. (Hinkle, Pratt and Levy, 1979)

2. (Skolik, 1962)

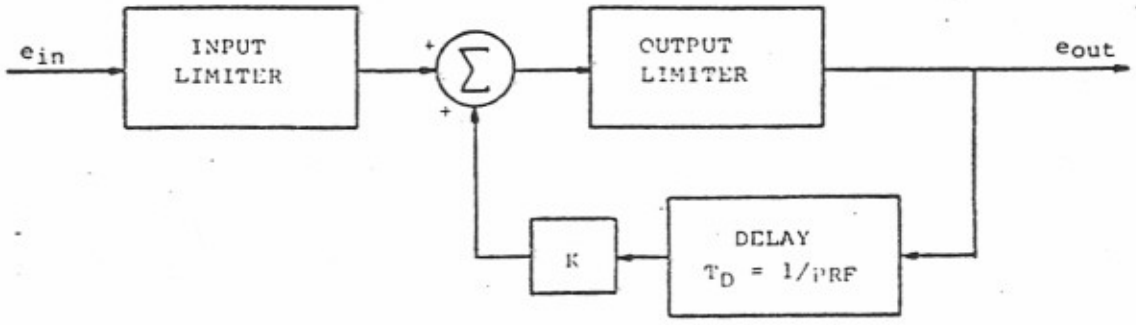

Figure A-1. Feedback Integrator Block Diagram

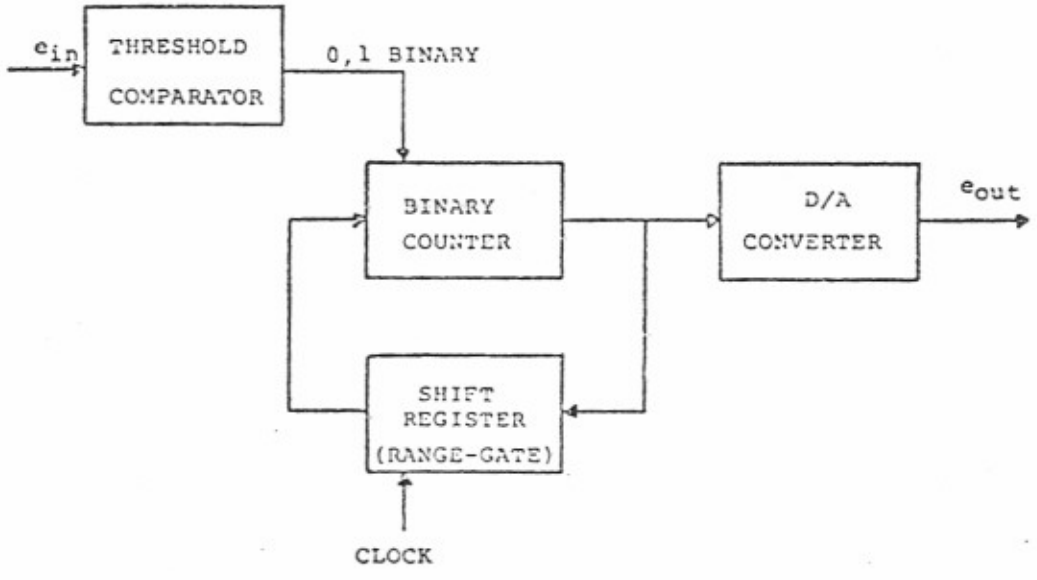

Figure A-2. ASR-7 (AN/GPN-12) Binary Integrator Block Diagram

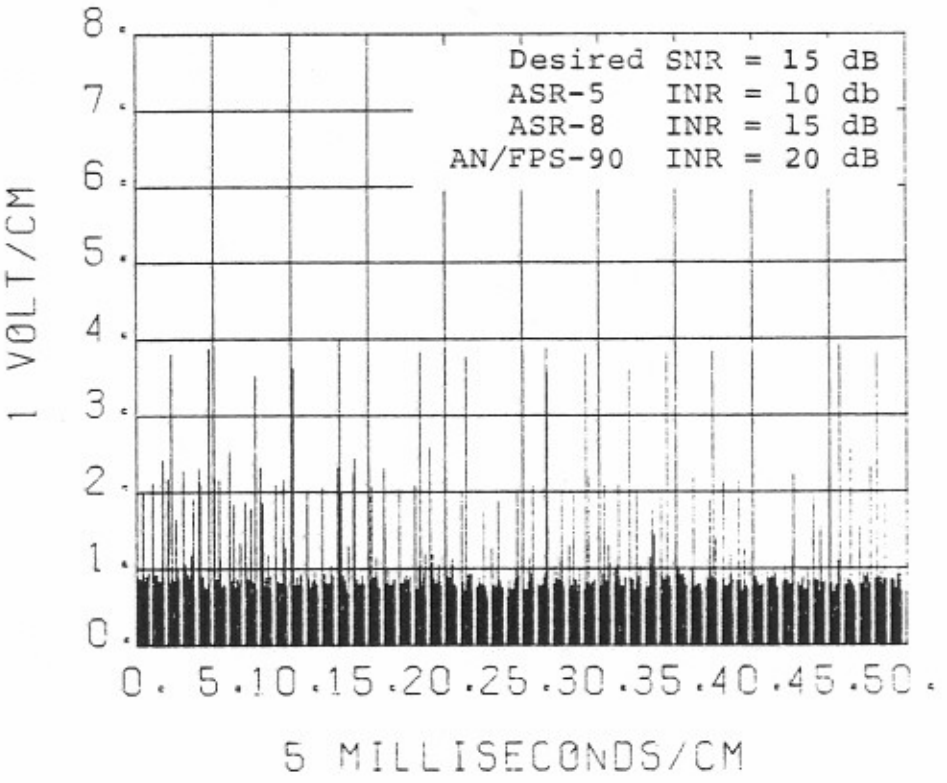

Figure A-3. Simulated Normal Channel Unintegrated Radar Output with Interference

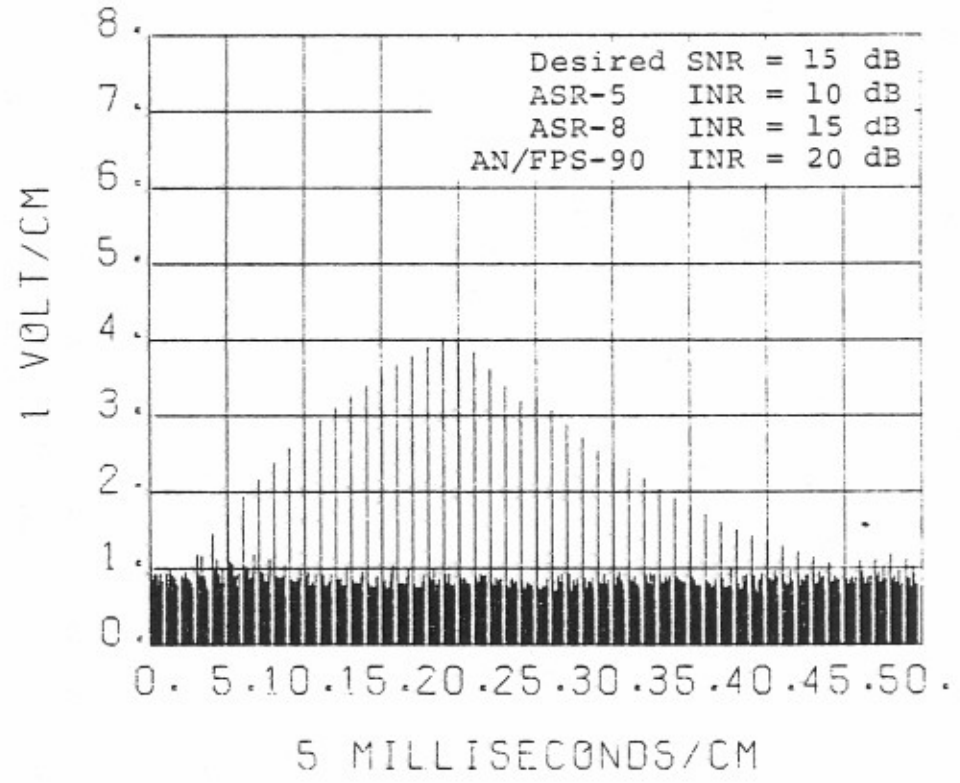

Figure A-4. Simulated Normal Channel Integrated Radar Output with Interference

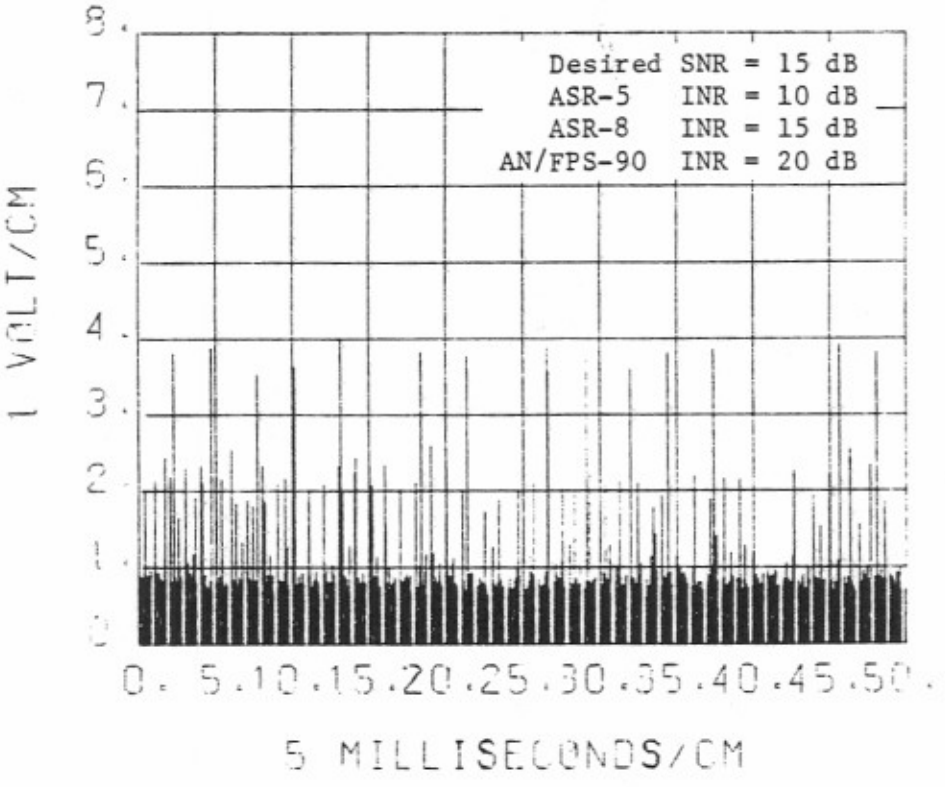

Figure A-5. Simulated Normal Channel Unintegrated Radar Output with Interference

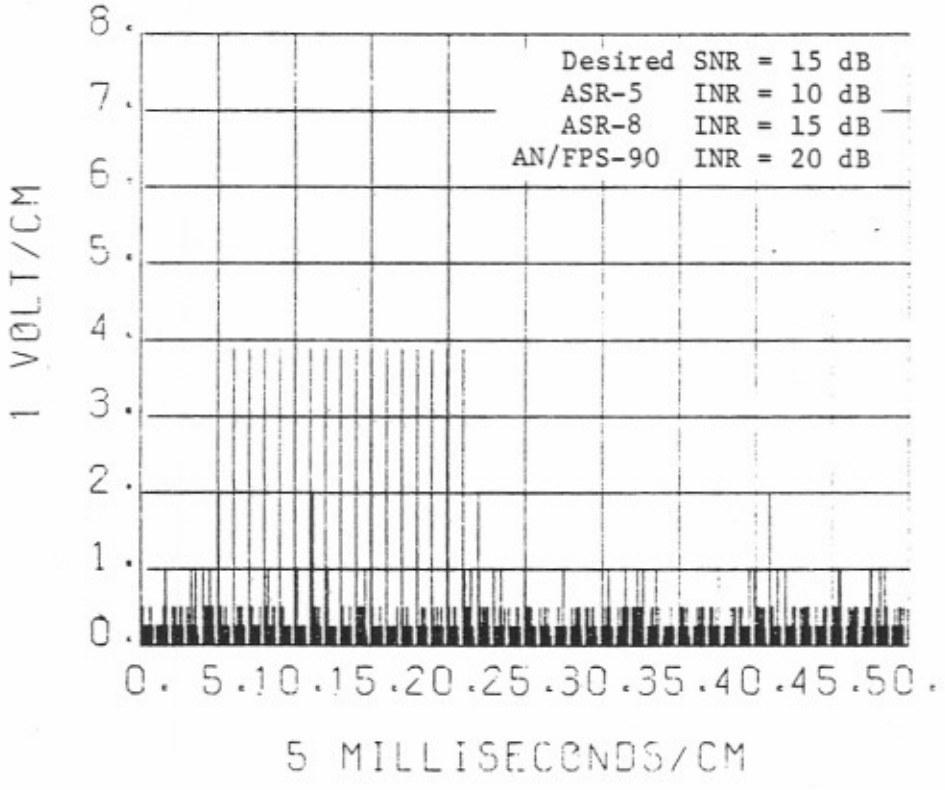

Figure A-6. Simulated Normal Channel Integrated Radar Output with Interference

DOUBLE-THRESHOLD DETECTION

Description

The double-threshold detector is a post detection signal processing technique used in radionavigation and search radars. The FAA double-threshold detection post-processing equipment is called a Common Digitizer (CD). A similar type of post-processing equipment (AN/FYQ-47) is also used by the DoD on search radars.

The function of the double-threshold detection circuit is to extract or identify targets from radar target pulse returns. However, the double-threshold method of detection also has an inherent capability to suppress false alarms caused by asynchronous pulsed interference. It also should be noted that the double-threshold detector is also refered to as a binary integrator, not to be confused with the binary integrator previously discussed. Figure A-7 shows a simplified block diagram of a double-threshold detector.

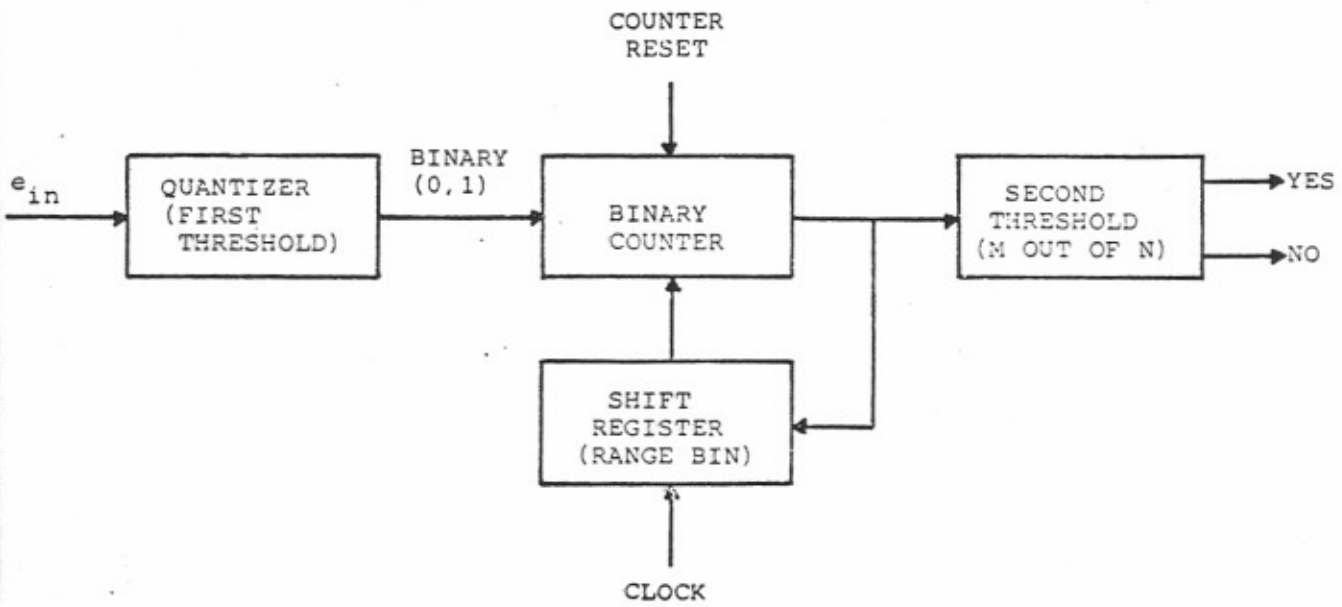

Figure A-7. Double-Threshold Detector Block Diagram

The "double-threshold" detector consists of establishing a bias level, T, the "first threshold", at the output of the radar, and then counting the number of pulses whose amplitude exceeds the bias level, T, in a "sliding window". The sliding window consists of N successive repetition periods in a given range bin. Where N, in accordance with usual practice, is assumed to be equal to the number of pulses omitted as the beam turns through an angle equal to the width between the one-way half-power antenna beam. If in any given range bin the number of pulses exceeding T in the sliding window is greater than or equal to a preassigned number M, the "second threshold", a target is declared to be present in that range bin. The values of the first threshold, T, and second threshold, M, are chosen to meet a particular probability of false alarm, P_{fa},

probability of detection, P_d. From this description, it is apparent why this targt detection technique is called both double-threshold detection and binary integration.

There are also more complex double threshold detection criteria than discussed above. For example, the FAA ARSR-3 has a fixed window size of 32 elements with separate leading and trailing edge target criteria. Also the FAA ARTS IIIA Radar Data Acquisition Subsystem (RDAS) has a variable window size with separate leading and trailing edge target criteria.

Intuitively, the double-threshold technique should be useful in reducing the effects of asynchronous pulsed interference. Target echos received as the beam scans past a target will occur in the same range bin. However, interfering pulses, occurring at random in the repetition period, will be unlikely to occur in any given range bin more than a few times in N repetition periods, unless the interfering pulse density is extremely high. Several studies have been made on the effects of asynchronous pulsed interference on double-threshold detection circuitry (Linder and Swerling, 1956) and (Hinkle, Pratt and Levy, 1979).

Trade-offs

The double threshold detector has a slightly poorer performance than the integrators which sum the target return pulses. The performance (P_d and P_{fa}) of the double threshold detector in suppression asynchronous pulse interference depends on both the first and second thresholds.

References

1. (Swerling, P., 1952)

2. (Linder, I.W. Jr, and Swerling, P., 1956)

3. (Di Franco and Rubin, 1968)

4. (Hinkle, Pratt and Levy, 1979)

PRF DISCRIMINATOR

Figure A-8 shows a simplified block diagram of a Pulse Repetition Frequency (PRF) discriminator. The PRF discriminator utilizes a threshold comparator, delay (shift register) and a coincidence circuit (AND gate) to suppress asynchronous interfering pulses that do not have the same PRF (interpulse period) as the desired signal. The discriminator usually operates at video, target pulses above the threshold are passed by the comparator; one pulse repetition period later, a second target pulse arrives at the input to the coincidence circuit just as the first leaves the shift register. In this scheme, all except the first pulse in the target return pulse train are processed. The threshold level of the comparator is generally set at a 6 to 8 dB threshold-to-noise ratio. More complex PRF discriminators can be designed to suppress multiples of the desired signal PRF.

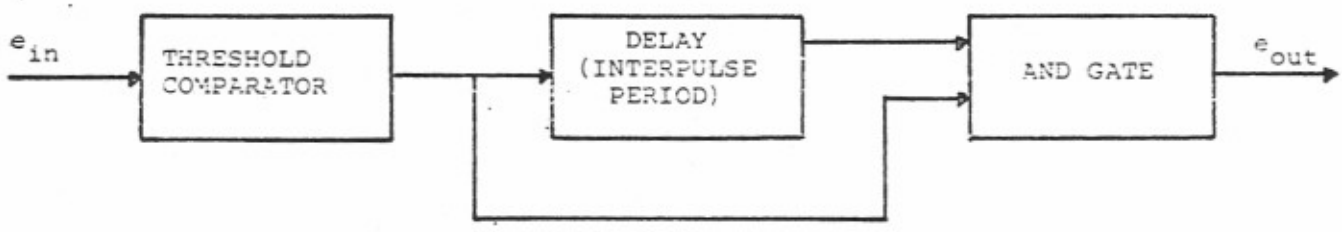

Figure A-8. PRF Discriminator Block Diagram

Trade-offs

The PRF Discriminator does not enhance the desired signal as the feedback and binary integrator circuits. Also there is a loss in desired signal sensitivity which is a function of the comparator threshold setting.

References

1. (Brown, 1973)
2. (Blythe, 1970)
3. (Skolink, 1970)

PULSE WIDTH DISCRIMINATOR

If the pulse width of the interference differs from that of the victim radar, it may be used to provide a means for discrimination. One method of implementing a pulse width discriminator is shown in Figure A-9. The input pulse is differentiated and split into two channels. In one channel the differentiated pulse is delayed a time corresponding to the width of the desired pulse τ, while in the other channel the differentiated pulse is inverted. If the input pulse were of width τ, the differentiated trailing edge inverted pulse would coincide in time with the leading edge pulse delayed in time τ. The coincidence circuit permits signals in the two channels to pass only if they are in exact time coincidence. If the input pulse were not of width τ, the two spikes would not be coincident in time and the pulse would be rejected.

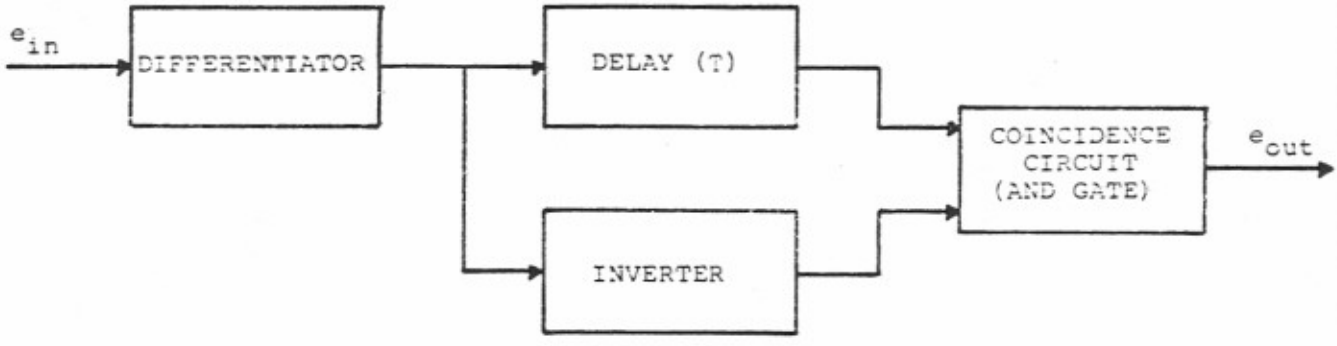

Figure A-9. Pulse Width Discriminator Block Diagram

Pulse width discriminators are generally not effective against off-tuned interference due to the inherent receiver IF output impulse response on the leading and trailing edge of an off-tuned pulsed signal. The leading and trailing edge impulse response of an off-tuned pulsed signal are typically similar to the desired signal because of the matched radar IF filter.

Trade-offs

The utilization of pulse-width discriminators generally results in reduced receiver sensitivity and probability of detection.

References

1. (Skolnik, 1962)

2. (Skolnik, 1970)

PULSE AMPLITUDE DISCRIMINATION

Description

Asynchronous pulsed interference can also be suppressed if the interfering signal levels are several dB above the receiver noise or clutter level. Pulse amplitude discrimination is used in the FAA MTD-II to suppress asynchronous pulsed interference. In the MTD-II, the signal level in the same range bin is added for several consecutive radar pulse periods. The magnitude is then stored and the average computed. Each range bin is then compared with four or five times the average. If any range bin exceeds this number, it is replaced by the average of the range bins. When there is interference in only one of the range bins and noise only in the other range bins, asynchronous pulsed interference with a peak INR greater than 12 to 14 dB (depending on the criteria of 4 or 5 times the average) will be eliminated from further processing in the radar.

Many different software algorithms can be developed to suppress asynchronous pulsed interferences based on pulse amplitude discrimination. The radar mission and type of radar signal processing must be taken into consideration in determining an appropriate pulse-amplitude discrimination algorithm.

Trade-offs

Desired signal trade-offs should be minimal with proper choice of algorithms. Pulse amplitude discriminators do not suppress weak interfering signals, and they do not work well if the presence of strong clutter.

References

1. (Cartledge and O'Donnell, 1976)

2. (McCrae and Ward, 1980)