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Capacitance Measurements of Double–Sided Silicon Microstrip Detectors

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Abstract

Direct measurements of the total capacitance with respect to ground of both the n- and p-sides of double– and single–metal silicon microstrip detectors over six frequency decades are described. Individual measurements of contributions to the total capacitance of a single strip are described. These include the detector's backplane capacitance and its coupling and interstrip capacitances. The combination of the constituent capacitances is shown to be consistent with the direct measurement and with a SPICE simulation. Additional n-side contributions due to the second-metal layer are also included in the direct measurement of total capacitance and in simulation. Measurements on detectors from a variety of vendors and with several geometries are compared with those of other workers. Detailed protocols for specific apparatus are given. A discussion of the isolation and grounding requirements for each class of measurement and a comparison of several meters is included.

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1 INTRODUCTION

This paper describes simulation and direct measurement of the total capacitance with respect to ground and several of its principle constituents for double–sided [1, 2] silicon microstrip detectors. The sum of the constituents is shown to be consistent with the direct measurement of the total capacitance and with a lumped element electrical model (SPICE [3] simulation). We compare these methods with those of other workers, including those based on noise measurements using calibrated front-end electronics bonded to detectors. The intent is to predict the overall signal–to–noise performance of a complete system, or "ladder," [1] of double–sided sensors and read-out electronics.

The techniques described in this paper permit comparison of various detector geometries from the standpoint of their capacitance as a predictor of noise performance. Capacitance measurements taken before and after irradiation allow specification of the final design that will maximize the useful performance lifetime of the device. It is important to emphasize, however, that these methods are no substitute for signal-to-noise measurements made on production ladders with the final data acquisition system. This will contain details such as the bandwidth, form factors, shaping and integration times of the read-out electronics, the capacitances distributed throughout the sensor (as opposed to modeling the detector *network* as a single, discrete capacitor connected to the input amplifier), proximity of read-out electronics to the sensor, as well as the effects neighboring sensors may induce, all of which may impact the signal–to–noise ratio.

SVX II [4], the upgrade of the silicon microstrip detector at the Fermilab Collider Detector Facility will incorporate double–sided technology to provide both $r - \phi$ and $r - z$ track reconstruction. One of the major branch points in the design of this detector is the choice between double–metal and glass z-print interconnect technology [5] to connect the $r - z$ read-out strips, which run transverse to the ladders, to hybrids at the ends. While ladder assembly is considerably simplified in the double–metal case, the second–metal layer contributes significantly to the total capacitance with respect to ground presented to the front-end amplifier, thereby lowering the signal–to–noise ratio. The effect of this additional capacitance on the signal–to–noise ratio and any changes it may undergo as a result of irradiation are factors driving this choice.

The signal–to–noise ratio is critical to realization of the full track reconstruction and resolution capabilities of SVX II. Noise voltages, V^i_{noise}, present at the input of the SVX III front-end amplifier, are reflected as equivalent charges, Q^i_{noise}, which compete with the (approximately fixed) charge collected from the ionizing track, Q_{signal}. The greater the capacitive load, C_{input}, presented to the input of the front-end amplifier, the lower the signal–to–noise ratio (S/N) is [6]:

$$S/N \quad = \quad \frac{Q_{\mathrm{signal}}}{\Sigma_i \; Q^i_{\mathrm{noise}}}$$

[1] Generally, in silicon vertex detectors, several silicon sensors are supported by rails and bonded to each other and to electronics at one or both ends. This basic functional unit is known as a ladder.

$$\approx \frac{Q_{\mathrm{signal}}}{C_{\mathrm{input}}\ \Sigma_i\ V^i_{\mathrm{noise}}}. \quad (1)$$

The various contributions to the S/N are uncorrelated, hence the summations are in quadrature.

The contributions to the capacitance presented to the front-end amplifier by the detector are summarized below. For both the p- and n-sides, these are:

- C_{coupling}: AC metal strip to DC implant strip (typically 10 pF/cm)

which capacitively divides the signal with:

- $C^{i-\mathrm{side}}_{\mathrm{backplane}}$ ($i = n$ or p): DC implant strip to ground plane (typically 0.35 pF/cm)
- $C^{\mathrm{DC}}_{\mathrm{interstrip}}$: DC implant to neighbor DC implant (typically 1 pF/cm/neighbor)
- $C^{\mathrm{AC}}_{\mathrm{interstrip}}$: AC metal to neighbor AC metal (typically 0.5 pF/cm/neighbor)

In addition to the four capacitances listed above, the second-metal layer introduces a network of capacitive couplings between read-out strips. These are shown in the lower half of Figure 1. These affect resolution and track reconstruction and may potentially impact the choice of a multiplexing scheme. The second-metal layer on the n-side contributes:

- C_{11}: 1$^{\mathrm{st}}$ metal AC strip to neighbor 1$^{\mathrm{st}}$ metal AC strip ($\approx$ 1/3 pF/cm/neighbor)
- C_{12}: 1$^{\mathrm{st}}$ and 2$^{\mathrm{nd}}$ metal overlap ($\approx$ 10 fF/overlap)
- C_{22}: 2$^{\mathrm{nd}}$ metal AC strip to neighbor 2$^{\mathrm{nd}}$ metal AC strip ($\approx$ 2/3 pF/cm/neighbor)

Less than 1 fF/overlap [7] is expected for the equivalent C_{12} with the glass z-print technology. The various capacitances are schematically represented in Figure 1.

2 Basic Detector Parameters

For prototyping purposes, detectors of eight different geometries were manufactured by the SINTEF/SI and Micron, Ltd. firms. (Two sensor sizes, one "long" and the other "short" were chosen to exploit the maximum area of the standard four-inch diameter silicon wafer.) The abbreviations used to identify each manufacturer and geometry are given in Table 1. The detector parameters pertinent to capacitance measurements and simulation for SINTEF/SI, Micron, Ltd., and Hamamatsu Photonics, K.K. detectors are given in Tables 2 and 3 for the p- and n-sides, respectively. The last column in Table 3 refers to the multiplexing factor. This indicates the number of first metal strips that are bonded to a second metal strip. This technique is used to reduce the number and density of the n-side read-out electronics in exchange for additional capacitance (lower signal–to–noise ratio) and increased possibility of "ghost" hits. (Since it is impossible to distinguish which of the implant strips was hit, the track reconstruction algorithm assumes that all strips were hit and then attempts to fit track segments to strips in several layers; the best fit strips are included. The other, spurious, tracks are referred to as ghosts). The Hamamatsu detectors use non-integral multiplexing, $m = 1.5$. This means that 2/3 of the implant strips are connected to two implants while the remaining 1/3 are connected to one implant. A ladder constructed of two detectors would have $m = 3$.

Table 1: A brief listing of detector types.

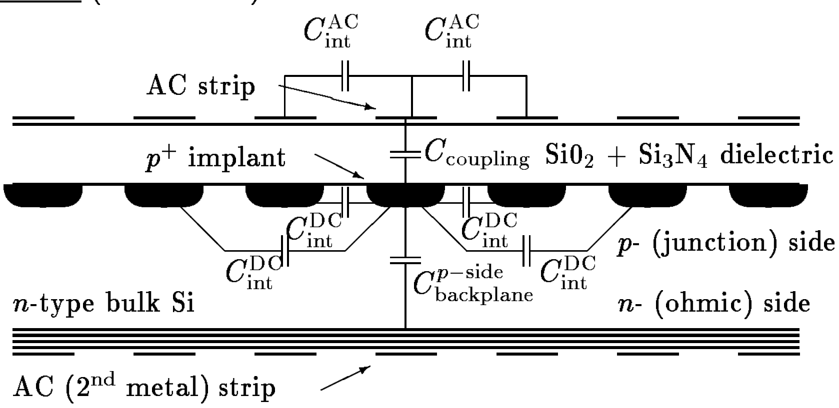
Designator	Description
SI	SINTEF/SI [a]
MI	Micron Semiconductor, Ltd. [b]
HA	Hamamatsu Photonics, K.K. [c]
A	"short" geometry; p-side intermediate strips [8]
B	"short" geometry
C	"long" geometry; n-side intermediate strips
D	"long" geometry
SM	n-side single–metal
DM	n-side double–metal

[a] SINTEF/SI
P.O. Box 124 Blindern
N-0314 Oslo, Norway.

[b] Micron Semiconductor, Limited
1 Royal Buildings, Marlborough Road
Churchill Industrial Estate, Lancing
Sussex BN15 8UN, England.

[c] Hamamatsu Photonics, K.K.
Solid State Division
1126-1 Ichino-cho
Hamamatsu-shi, 435 Japan.

cross section (not to scale):



top view, n-side, double-metal (not to scale):

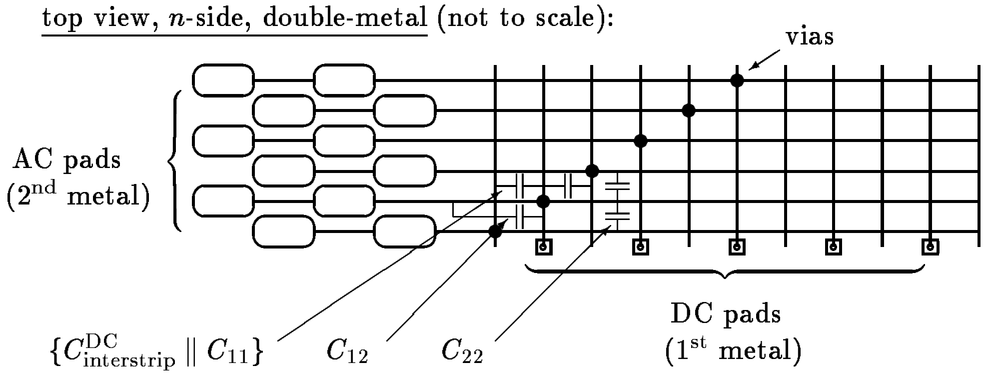


Figure 1: Capacitances of a double–sided, double–metal silicon microstrip detector. The upper half illustrates the p-side, in profile view, while the lower half displays the n-side seen from above. The dielectric is composed of $\mathrm{SiO_2}$ and $\mathrm{Si_3N_4}$ layers and is passivated with polyimide or an additional $\mathrm{SiO_2}$ layer not shown in the figure. $C_{\mathrm{interstrip}}^{\mathrm{DC}}$ is abbreviated $C_{\mathrm{int}}^{\mathrm{DC}}$. On the n-side, $C_{\mathrm{interstrip}}^{\mathrm{DC}}$ refers to the coupling between implant strips, C_{11} denotes coupling between strips of the first metal layer, C_{12} refers to coupling between overlapping regions of the first and second metal layers, and C_{22} refers to coupling between strips of the second metal layer.

Table 2: Nominal p-side detector parameters.

Detector Type	implant # strips	implant length (cm)	implant width (μm)	implant pitch (μm)	metal width (μm)	inter– mediate strips?
SINTEF/SI						
SI-A	768	4.1	10	25	7.5	yes
SI-B	384	4.1	10	50	7.5	no
SI-C	256	8.2	10	50	7.5	no
SI-D	256	8.2	10	50	7.5	no
DS641/640 [9]	1280	5.6	7	25	10	yes
Micron, Ltd.						
MI-A	768	4.1	11	25	10	yes
MI-B	384	4.1	11	50	10	no
MI-C	256	8.3	11	50	10	no
MI-D	256	8.3	11	50	10	no
Hamamatsu Photonics, K.K.						
HA-0	256	7.61	14	60	8	no
HA-1	384	5.88	14	62	8	no

Table 3: Nominal n-side detector parameters.

Detector Type	implant # strips	implant length (cm)	implant width (μm)	implant pitch (μm)	1st metal width (μm)	2nd metal length (cm)	2nd metal width (μm)	2nd metal pitch (μm)	p-stop width [a] (μm)	inter– mediate strips?	m
SINTEF/SI											
SI-A	384	2.0	12	103	7.5	4.1	7.5	50	60	no	1
SI-B	384	2.0	12	103	7.5	4.1	7.5	50	60	no	1
SI-C	1024	1.3	12	79	7.5	8.2	7.5	50	40	yes	2
SI-D	512	1.3	12	158	7.5	8.2	7.5	50	120	no	2
DS641/640	640	3.1	7	85	10	5.6	7	50	—	no	1
Micron, Ltd.											
MI-A	384	1.9	11	103	10	4.1	10	50	58	no	1
MI-B	384	1.9	11	103	10	4.1	10	50	58	no	1
MI-C	1024	1.2	11	80	10	8.3	10	50	40	yes	2
MI-D	512	1.2	11	160	10	8.3	10	50	115	no	2
Hamamatsu Photonics, K.K.											
HA-0	1024	1.53	18	74.5	12	7.64	8	59	45.5	no	2 [b]
HA-1	1152	2.37	16	66	10	7.64	8	60	39	no	1.5 [c]

[a] See References [10, 11].
[b] 1st metal strips are ganged in sets of two.
[c] 1st metal strips are ganged in sets of two, alternating with unganged strips.

3 Simulation

3.1 Goals

Detailed circuit models of silicon microstrip detectors were developed to aid in the interpretation of the capacitance measurements. The models were based on discrete electrical circuit components (capacitors and resistors). The SPICE electrical simulator was used to predict and verify the performance of the detector circuit models. SPICE employs the solution of the matrix equations describing the circuit voltages, currents and resistances (or conductances). (A field simulator using a boundary element solution method was not used.) The models were used to predict frequency response curves for the various detector geometries, then compared to the measurements obtained with LCR meters.

3.2 The SPICE Simulation

3.2.1 SPICE Model, Double-Sided Detector

The development of an accurate electrical network (SPICE) model of detector resistive, capacitive, and diode junction elements is an essential step (see Figures 2 and 3). The distributed nature of the coupling capacitor formed by the implant, dielectric (SiO_2 and Si_3N_4 layers) and aluminum layers (see Figure 4) mandates using a lumped model approach which involves connecting many small subcircuits in series. This approach was also used in the SPICE calculations performed in Reference [12]. Discrete, passive, components are used to represent each small section of the implant–readout strip combination (the lumped strip segment). Each lumped strip segment (see Figure 4) consists of a coupling capacitance ($C_{\rm coupling}$), DC interstrip capacitance ($C^{\rm DC}_{\rm interstrip}$), AC interstrip capacitance ($C^{\rm AC}_{\rm interstrip}$), implant strip resistance ($R_{\rm implant}$), readout strip resistance ($R_{\rm readout}$), and interstrip resistance ($R_{\rm interstrip}$).

An adequate number of lumps must be used such that the natural frequencies of the lumped elements do not occur in the frequency range of the simulation run. One lump per centimeter was determined to be adequate for these simulations. Around the lumped segments, additional components are added to represent the backplane capacitance ($C^i_{\rm backplane}$, where $i = n$ or p), bias resistance ($R_{\rm bias}$), and $p - n$ junction currents of the strips (D). Table 4 lists the various input parameters and their symbols as used in the model and this paper.

Three strips were included in the model of a detector with no intermediate strips [2] (see Figure 2), and five strips were used for the detector with intermediate strips (see Figure 3). For detectors which have intermediate strips and 2–times multiplexing, ten strips were included in the simulation. The model for detectors with double-metal readout also included

[2]Intermediate non-read-out strips are DC implant strips placed between read-out strips. Like the read-out strips, they have polysilicon bias resistors and collect charge left by ionizing tracks, however this charge is not coupled to an amplifier since there is no associated AC metal strip. Instead, depending on the geometry, a fraction of this charge is induced on each of the neighbor strips. See Reference [8].

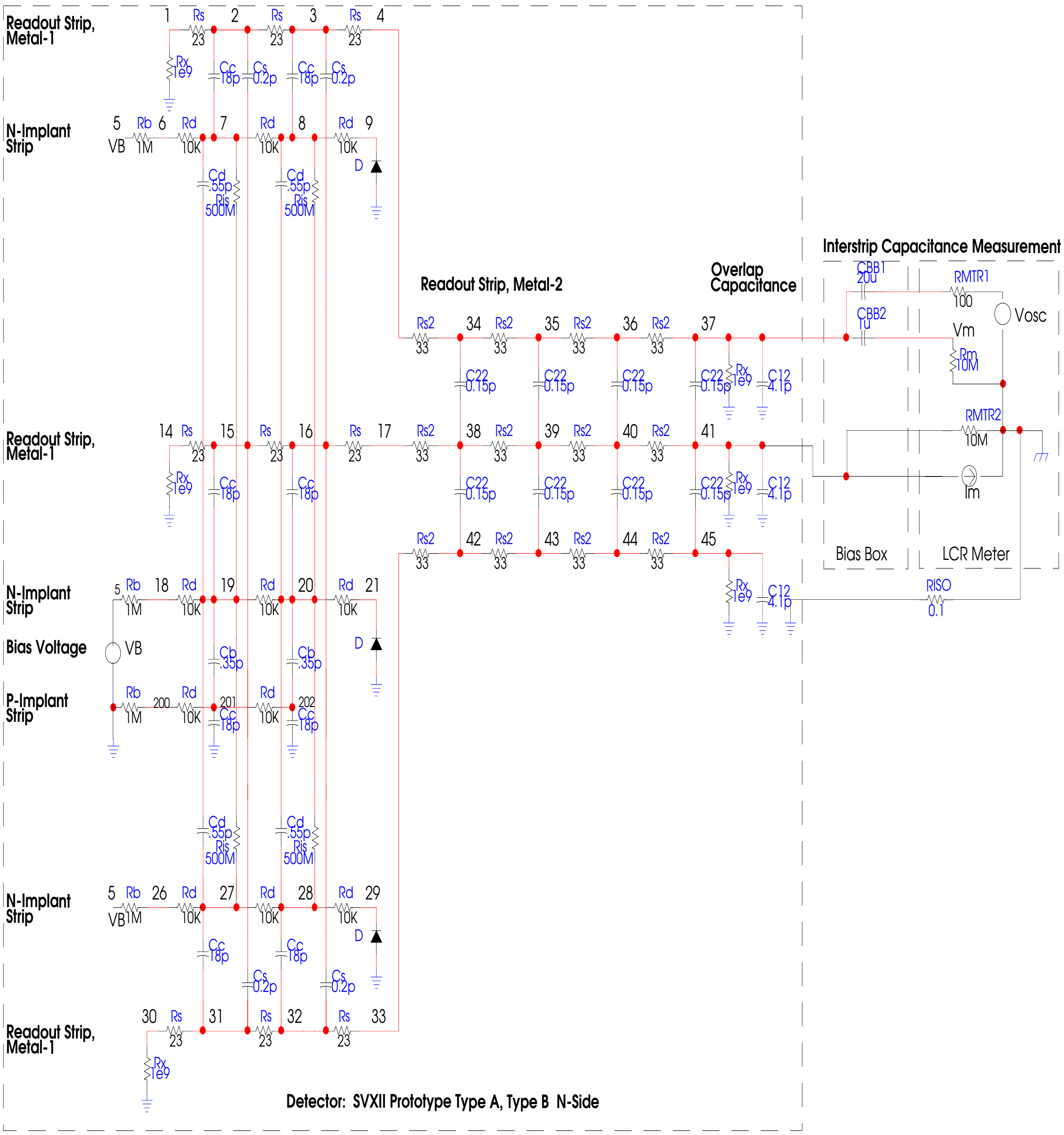


Figure 2: SPICE model of the n-side of the SINTEF/SI SVX II type A or type B prototype detector. The LCR meter is shown configured for an interstrip capacitance measurement. The "Bias Box" is the SPICE representation of the Bias Isolation Network described in Appendix A.2.1.

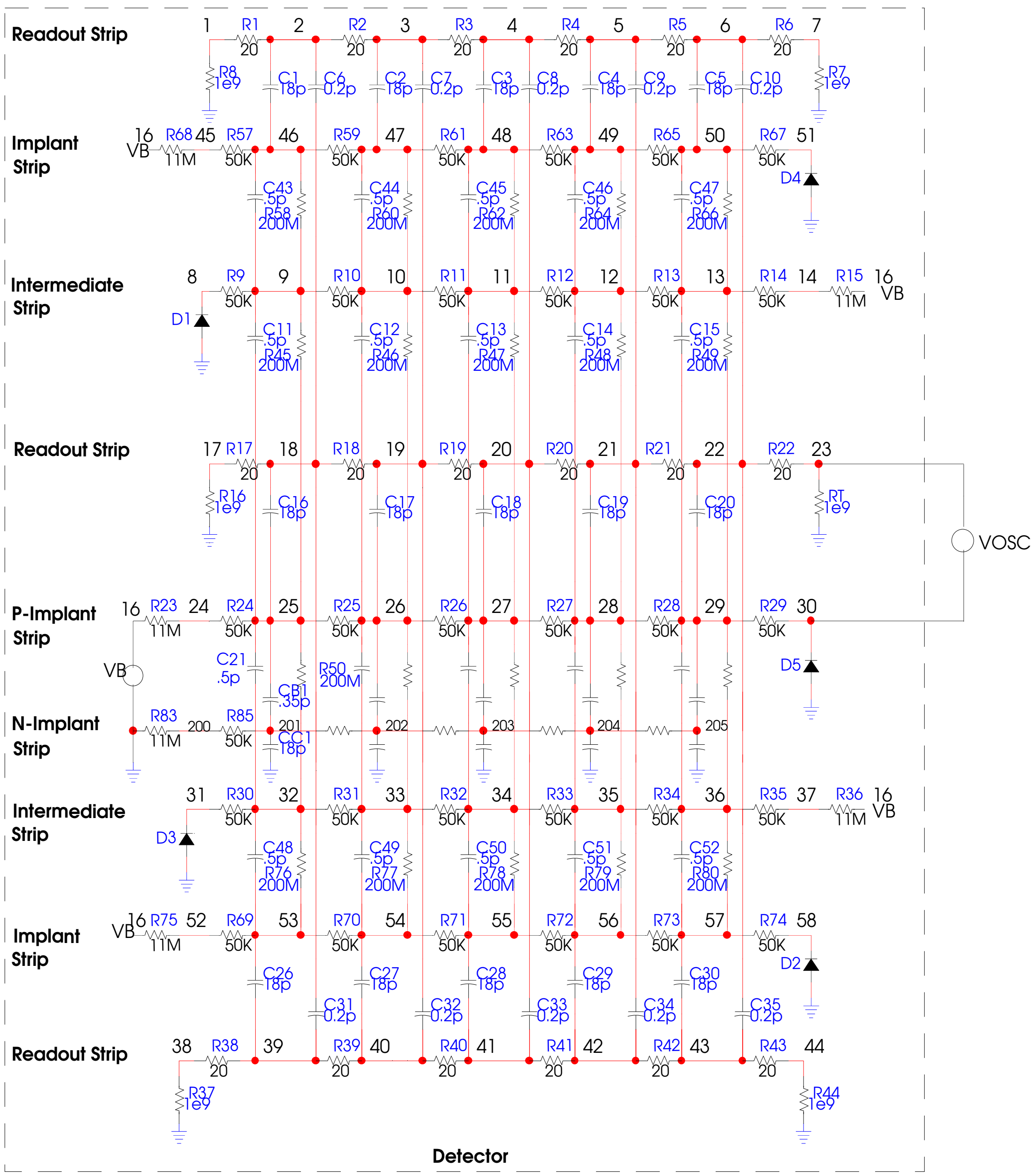


Figure 3: SPICE model of the p-side of the SINTEF/SI DS641/640 detector. Some component references and values have been deleted for clarity. The values for the first lump of the n-implant strip are shown; values for similar components in the subsequent lumps are the same.

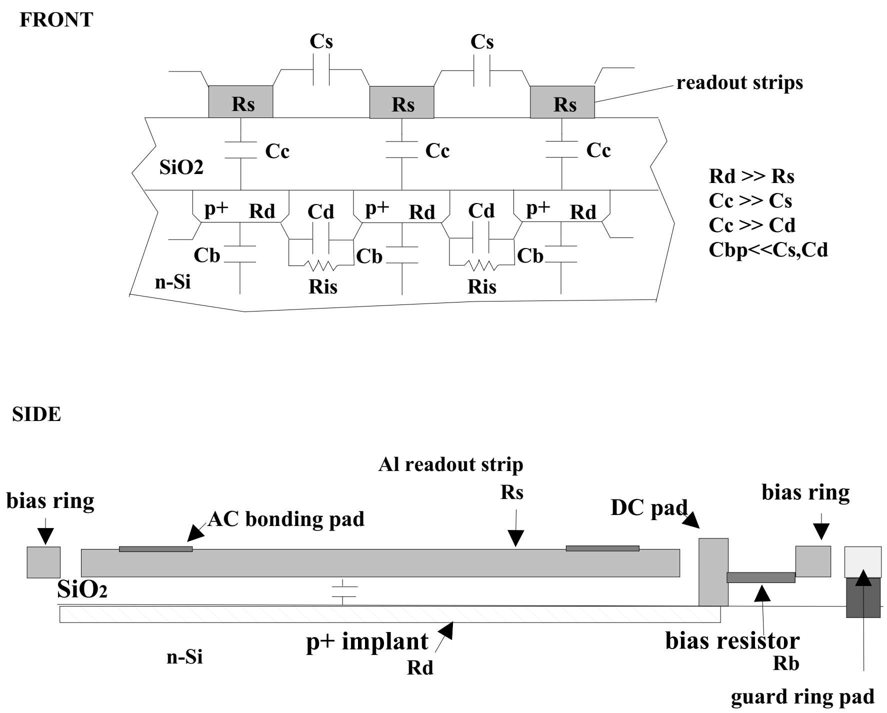


Figure 4: Detector cross sectional views used for the SPICE simulation.

separate lumped segments of one lump per centimeter of second metal interstrip capacitance (C_{22}), overlap capacitance (C_{12}), and second metal strip resistance ($R^{2^{\text{nd}}}_{\text{readout}}$). The interstrip capacitance terms were adjusted to include contributions from all the neighboring strips on a given detector. This adjustment factor is 0.1 pF/cm [13].

3.2.2 SPICE Model, Component Value Calculations

The calculation of SPICE model component values and tolerances used as input width and thickness specifications of the implant strips, readout strips, and insulator supplied by the detector manufacturers. From these, the component values input to the model may be calculated. Published measurements [13] and calculations [14] were also used wherever possible. A listing of typical values is given in Table 4. The following methods were used in the calculation of the individual component values:

Coupling Capacitance (C_{coupling}): The simple parallel plate capacitor model; $C_{\text{coupling}} = \epsilon/d$ yields the capacitance per unit area for a dielectric of permittivity ϵ and thickness d.

Interstrip Capacitance ($C^{\text{DC}}_{\text{interstrip}}$, $C^{\text{AC}}_{\text{interstrip}}$): For the p-side, Figure 4 of [13] gives an estimate for C_{total}. In the present model $C_{\text{total}} = (2 \times C^{\text{DC}}_{\text{interstrip}} + 2 \times C^{\text{AC}}_{\text{interstrip}}) + C_{\text{backplane}}$. The values obtained for adjacent strips have been scaled by 110 percent to account for the contributions of neighbors. First $C_{\text{backplane}}$ is calculated by scaling from the result given in [13], then $C^{\text{AC}}_{\text{interstrip}}$ and $C^{\text{DC}}_{\text{interstrip}}$ are estimated assuming that $C^{\text{DC}}_{\text{interstrip}} = 3\ C^{\text{AC}}_{\text{interstrip}}$. For the n-side the p-stops [3] are modeled. This is done using the observation that in most detector designs there is a gap between the n-strip and the p-stop which collects electrons attracted to the accumulation layer and increases the effective width of the n-strip [14]. Thus the width of the n-strip becomes $W_{\text{eff}} = \text{pitch} - W_{p-\text{stop}}$ [14]. With this correction then Figure 5 of [13] is used to obtain $C^{\text{DC}}_{\text{interstrip}}$ and $C^{\text{AC}}_{\text{interstrip}}$ as described above.

Backplane Capacitance ($C^{i}_{\text{backplane}}$, where $i = n$ or p): Equation (8) and Figure 8 of [13] are used to calculate the backplane capacitance.

Double-Metal Capacitances: The second layer of metal in a double-metal readout scheme adds several capacitive components, two of which are included in the SPICE model. Equation (1) of [14] is used to calculate the interstrip capacitance of the second layer metal strips (C_{22}). Equation (3) of [14] is used to find the capacitance due to the overlaps of the first and second layer metal readout strips (C_{12}). Capacitance due to the overlapping of the second metal readout strip with the p-stops or intermediate strips is not modeled.

Implant Strip Resistance (R_{implant}): Calculated from the manufacturer's specified sheet resistance.

Readout Strip Resistance (R_{readout}): Calculated from the width and thickness of the Al

[3] p-stops are "blocking" p-doped implant strips inserted between the n-strips. They defeat the accumulation layer that would otherwise increase with irradiation. This layer forms a conductive path between n-strips [10, 11].

Symbol SPICE[a]	Symbol text	Name	Typical Value	Unit
Cc	C_{coupling}	Coupling Capacitance	18	pF/cm
Cd	$C^{\text{DC}}_{\text{interstrip}}$	DC Interstrip Capacitance	0.55	pF/cm
Cs	$C^{\text{AC}}_{\text{interstrip}}$	AC Interstrip Capacitance	0.2	pF/cm
C11	C_{11}	Interstrip Capacitance-Metal-1	0.75	pF/cm
C22	C_{22}	Interstrip Capacitance-Metal-2	0.15	pF/cm
C12	C_{12}	Overlap Capacitance	8	fF/overlap
Cb	$C^{n-\text{side}}_{\text{backplane}}$	Backplane Capacitance	0.35	pF/cm
Cb	$C^{p-\text{side}}_{\text{backplane}}$	Backplane Capacitance	0.35	pF/cm
Rd	R_{implant}	Implant Strip Resistance	50	kΩ/cm
Rs	R_{readout}	Readout Strip Resistance	30	Ω/cm
Ris	$R_{\text{interstrip}}$	Interstrip Resistance	500	MΩ
Rb	R_{bias}	Bias Resistance	2	MΩ
D	D	$p-n$ Junction Current	1	nA/strip

[a] Figures 2 and 3 use a different notation than the text.

Table 4: SPICE model components. See Section 3.2.1 and Figures 2 and 3.

strip.

Bias Resistance (R_{bias}): Calculated from the manufacturer's specified sheet resistance.

Interstrip Resistance ($R_{\text{interstrip}}$): 500 megohms.

Currents (D): The diodes in Figures 2 and 3 represent the $p-n$ junctions between the bulk and the implant strips. A leakage current of approximately $1nA$ per strip is specified in the diode model in order to establish a realistic DC current through the strip.

3.2.3 SPICE Model, Capacitance Meter

Accurate representation of the measurement apparatus and fixturing setup (including the capacitance meter, bias isolation network, and cabling) was deemed necessary to represent properly effects external to the detector, such as grounding, isolation, and choice of probing points. The model of the LCR meter in Figure 2 is based on the "Auto Balance Bridge" technology common to the HP 4284A Precision LCR meter and HP 4192A Low Frequency Impedance Analyzer. These meters measure a complex impedance by injecting into the device under test a known AC voltage and phase signal over a range of frequencies, measuring the AC return current and phase, and calculating the impedance parameters (magnitude and phase of resistance, R, and reactance, X). The capacitance is extracted from the impedance measurement from the following relation: $Im(I) = 1/X = 2\,\pi\,f\,C$, yielding C *vs.* f. The SPICE simulation performs these same operations.

The modeling of the isolation between the power supply return and the meter's AC signal return is discussed in Appendix A.3.

3.3 Results

A complete summary of detector capacitance predictions by SPICE simulations for a sample population of vendors and geometries is shown in Table 9. The errors were estimated for each geometry by running 100 simulations in which each of the input parameters was subject to a uniform Monte Carlo variation over the tolerance range specified by the manufacturer, or $\pm$ 10% in cases where tolerances were not supplied. The SPICE model method for calculating detector capacitances gives results which are consistent with the measured capacitances to within 10 % for the n-side and to within 20 % for the p-side.

4 Measurements

The intent of this paper is to demonstrate two methods for measuring the total capacitance with respect to ground presented to the front-end amplifier chip by a single strip of a silicon microstrip detector, including effects of neighboring strips, and a SPICE model for each geometry measured and each of two measurement methods. In one method, the constituents are individually measured and then summed. The other yields the total capacitance with respect to ground in a single, direct, measurement. These two methods and the SPICE models are shown to be consistent in Section 4.5.3. A summary of the results obtained by the direct method is presented in Section 5.

Several capacitance measurements will be discussed. First, the bulk capacitance, from which depletion voltage, $V_{\rm depl}$, and the capacitance between a single implant strip and the opposite side of the detector (its backplane) $C^{i-\rm side}_{\rm backplane}$ ($i = n$ or p), may be derived, is described. Then the coupling capacitance, $C_{\rm coupling}$, and interstrip capacitance, $C_{\rm interstrip}$, are presented in Sections 4.5.1 (for the p-side) and 4.5.2. The direct and summed methods for measuring the total capacitance, $C_{\rm total}$, with respect to ground, are described in Section 4.5.3.

Where the n- and p-side measurement procedures differ, appropriate detail is given. The protocols used for the measurements reported here are listed in Appendix B. While these procedures are specific to the instrumentation used for each measurement, not every procedure need be repeated for each measurement.

4.1 Apparatus

Measurements may be taken manually or by computer control using programs written in Microsoft QuickBASIC^{TM} (with the appropriate IEEE 488 device drivers) and calls to the Hewlett–Packard 4192A or 4284A and Keithley 237 or with an object-oriented acquisition and analysis system such as National Instruments' LabVIEW^{TM} (with appropriate "Virtual Instrument" drivers). Manual acquisition allows the operator to observe stability of the measurement prior to recording the data. Details of the apparatus may be found in Appendix A.

4.2 Operating Voltage

Nominal operating voltages are given in Table 5. These reflect considerations of full depletion of the silicon and prompt charge collection addressed in Section 4.4.

Table 5: Typical operating voltages.

Manufacturer	Type	V_{oper} (V)
SINTEF/SI	DS641/640	50
SINTEF/SI	SVX II A,B,C,D	80
Micron, Ltd.	SVX II A,B,C,D	50
Hamamatsu Photonics, K.K.	SVX II	50

4.3 Typical Measurement Procedure

The general measurement procedure is as follows:

- Allow equipment to warm up for manufacturer's recommended time.
- Make DC bias connections through bias isolation network (Appendix A.2.1).
- Confirm isolation (Appendix A.3).
- Connect appropriate length extension, bias isolation network, and probe tips to LCR meter.
- Connect all grounds (LCR meter, power supply in OPERATE mode).
- Calibrate LCR meter (Appendix B.2).
- Mount detector in appropriate fixture (Appendix A.2.3).

- Land bias and guard ring probes on lower and upper sides of detector.
- Bring detector to full operating voltage (Section 4.2).
- Land LCR meter probe(s) as appropriate to the measurement.
- Record the data.

4.4 Bulk Capacitance, Depletion Voltage, and Backplane Capacitance

A procedure for measurement of the bulk capacitance of a complete silicon microstrip is described. From this, the depletion voltage (and therefrom the operating voltage) and the capacitance between a single strip and the opposite side of the the detector (the "backplane") may be measured.

4.4.1 Theory

Silicon microstrip detectors require a reverse-bias potential to create a region free of mobile carriers around the $p-n$ junction. (These carriers would otherwise be available to combine with charge liberated by the passage of an ionizing particle, making detection of the charge – and therefore the particle – impossible.) This region is called the depletion layer. The bias voltage must be sufficient to deplete fully the available volume within the bulk, thereby maximizing the amount of charge collected from the ionizing particle and providing rapid collection of that charge.

The rapid collection of charge from the microstrip detector is important because the next generation of high luminosity colliders requires much faster charge integration than is used at present. During Run II of the Fermilab Tevatron, the beam crossing time will be reduced from 396 to 132 ns [15]. This places a significant constraint on the integration time, which for the front–end electronics of SVX II will be approximately 100 ns. To assure prompt [4] collection of the charge, a bias voltage of 20 V or more above full depletion (defined below) will be used to operate SVX II detectors. This reduces the effects of drift and diffusion. The same conditions are used for the detectors tested here.

Additional constraints of high voltage breakdown, power consumption, heating, shot noise (which is proportional to the square root of the leakage current), and microdischarge noise [18] drive the operating voltage in the opposite direction. Further, radiation damage beyond that sufficient to invert the bulk silicon increases the depletion voltage [19, 20, 21]. It is therefore desirable to operate the device near the minimum bias voltage required for prompt signal collection.

[4] A SPICE simulation [16] of charge collection was run for SVX II prototype [17] detectors. In all configurations simulated, the collection time for the charge was under 60 ns.

Since the depletion voltage determines the operating voltage, a technique to measure the onset of full depletion is described. This technique is based on a model of the depletion layer as a parallel plate capacitor.

The bulk capacitance per unit area of the reverse-biased sensor is determined by the depth of the depletion layer, d:

$$C_{\mathrm{bulk}} = \frac{\epsilon_{\mathrm{Si}}}{d} \tag{2}$$

where ϵ_{Si} is the permittivity of the bulk silicon. The applied bias potential and the thickness of the depletion layer are related by [22]:

$$V_{\mathrm{bias}} = \frac{q\ d^2\ |N_{\mathrm{effective}}|}{2\epsilon_{\mathrm{Si}}} \tag{3}$$

where $N_{\mathrm{effective}}$ is the effective charge carrier density, the number of (negative) donors minus the number of (positive) acceptors, and q is the absolute value of the electron charge.

The depletion voltage, V_{depl}, is extracted from a plot of $\log\{C_{\mathrm{bulk}}\}$ *vs.* $\log\{V_{\mathrm{bias}}\}$. Below V_{depl} this curve falls proportionally to a power of the voltage, aV^n, as may be seen by inserting Equation 3 into Equation 2. The capacitance per unit area, C_{bulk}, is then given by:

$$C_{\mathrm{bulk}} = \begin{cases} \sqrt{\dfrac{q\ \epsilon_{\mathrm{Si}}|N_{\mathrm{effective}}|}{2\ V_{\mathrm{bias}}}} & \text{for } V_{\mathrm{bias}} \leq V_{\mathrm{depl}} \\ \\ \dfrac{\epsilon_{\mathrm{Si}}}{d_{\mathrm{depl}}} & \text{for } V_{\mathrm{bias}} > V_{\mathrm{depl}} \end{cases} \tag{4}$$

where d_{depl} is the full depletion depth of the device.

The point of inflection in a $\log\{C_{\mathrm{bulk}}\}$ *vs.* $\log\{V_{\mathrm{bias}}\}$ curve results from the transition from the upper line to the lower line in Equation 4 and thereby defines the depletion voltage, V_{depl}. To locate V_{depl}, first a line is drawn through the most steeply falling portion of the power-law region, as shown in Figure 5. A second, horizontal, line is drawn through the minimum of the approximately flat "toe" region as shown in the same figure. The intersection of the two lines defines the toe of the C_{bulk} *vs.* V_{bias} curve. The V coordinate of this point is the depletion voltage.

In the case of a planar electrode diode, above V_{depl} the curve is flat, owing to the uniform penetration of the electric field from the p-side electrode to the n-side electrode; the parallel plate capacitor model is a good approximation. In silicon microstrip detectors the onset of depletion is more gradual. This is due to periodic nonuniformities in the electric field around the n- and p-side implants. These regions of reduced electric field leave some of the silicon undepleted. Only by applying voltages beyond those sufficient to deplete a planar electrode diode of similar bulk geometry are these remaining regions depleted. Thus, the conventional intersection method provides an underestimate of depletion voltage when applied to silicon microstrip detectors. Full depletion is reached at voltages somewhat higher than those at which the $\log\{C_{\mathrm{bulk}}\}$ *vs.* $\log\{V_{\mathrm{bias}}\}$ curve begins to flatten. The size of this additional voltage is affected by the structure of the electrodes and depends on the width–to–pitch ratio of the strips [13].

Figure 6 shows the frequency dependence of the curve shape of an unirradiated detector. The three curves presented yield a consistent depletion voltage, since they share a common V coordinate for their inflection points. Radiation induced effects on frequency dependence of $C_{\rm bulk}$ measurements have been reported in [23].

The capacitance between a single strip, the depleted bulk silicon, and the strips on the opposite side is called the backplane capacitance. It is denoted $C^{i-\rm side}_{\rm backplane}$, where $i = n$ or p (see Figure 1). It may be approximated (edge effects are ignored) from $C_{\rm bulk}$ measured at full depletion voltage (or above) divided by the number of DC implant strips on the same side as the strip in question:

$$C^{i-\rm side}_{\rm backplane} \approx \frac{C_{\rm bulk}}{\#\text{ of strips on side } i} \qquad \text{for } V_{\rm bias} \geq V_{\rm depl}. \tag{5}$$

Typical backplane capacitances for unirradiated SINTEF/SI detectors are given in Table 6.

4.4.2 Procedure

The arrangement for the depletion voltage measurement is depicted in Figure 7. The probe station and its micro-positioners are not shown for simplicity. The power supply, LCR meter, and bias isolation network (Appendix A.2.1) are shown. Low parasitic capacitance probes (Appendix A.2.2) are used to probe the upper surface [5] while the bias and guard ring contacts on the lower surface are made through the probing chuck (Appendix A.2.3). The effect of the probes, fixtures, and cables that intervene between the detector and the device under test are compensated for by the calibration procedures described in Appendix B.2.

The lower surface of the detector has its bias and guard rings contacted using the underside probing fixture or conductive rubber. The bias and guard rings on the n- and p-sides of the detector are connected to their respective terminals on the power supply through the bias isolation network.

Capacitance is recorded as a function of bias voltage in steps of a few volts while the capacitance decreases to a minimum value. The bias voltage steps are chosen to provide good fits through the most steeply falling portion of the power law region and above the toe of the $C_{\rm bulk}$ *vs.* $V_{\rm bias}$ curve. These are set in software. Data taking is complete when the measured capacitance falls to a constant value or microdischarge noise makes further capacitance determination impossible.

The slope of the line through the most steeply falling portion of the power law region may be found by a χ^2 minimization offline or graphically. Similarly, the intersection of this line and the horizontal line through the region above the toe may be found algebraically or graphically.

[5] This is for convenience of making connections. The $V_{\rm depl}$ measurement is relatively insensitive to systematic errors in measured capacitance as described in Section 4.4.3.

Table 6: Backplane capacitance for unirradiated SINTEF/SI detectors.

Designator	Name	C_{bulk} (pF @ 100V)			$C^{p-\text{side}}_{\text{backplane}}$ (pF/cm @ 100V)			$C^{n-\text{side}}_{\text{backplane}}$ (pF/cm @ 100V)		
		1kHz	3kHz	10kHz	1kHz	3kHz	10kHz	1kHz	3kHz	10kHz
Single–Metal										
SI-A-SM	KB51-1	307	302	295	0.10	0.10	0.09	0.40	0.40	0.39
SI-B-SM	SVX2-B-6	312	299	302	0.20	0.19	0.19	0.41	0.39	0.41
SI-C-SM	SVX2-C-32	419	408	364	0.20	0.19	0.17	0.31	0.31	0.27
SI-D-SM	SVX2-D-4	382	379	361	0.18	0.18	0.17	0.58	0.57	0.55
Double–Metal										
SI-A-DM	KB54-1	283	279	273	0.09	0.09	0.09	0.37	0.36	0.36
SI-B-DM	KB54-2	312	299	302	0.20	0.19	0.19	0.41	0.39	0.39
SI-C-DM	LB54-1	365	349	315	0.17	0.17	0.15	0.27	0.26	0.24
SI-D-DM	LB54-2	388	363	340	0.18	0.17	0.16	0.58	0.55	0.51
DS641/640	S6-29	935	–	146	0.13	–	0.02	0.47	–	0.07

4.4.3 Estimate of Depletion Voltage Uncertainty

A listing of several sources of systematic errors in the V_{depl} measurement is given in Table 7.

Typical C_{bulk} *vs.* V_{bias} curves are shown in Figures 5 and 6. As the detector is depleted, the device capacitance drops from thousands to hundreds of pF. The uncertainties associated with the determination of the capacitance ($\sigma_{\text{HP 4284A}}$, $\sigma_{\text{LCR cable}}$, and $\sigma_{\text{LCR cal}}$) are relatively small. Further, they are all independent of bias voltage, since the LCR meter is isolated from the bias supply by the bias isolation network. Thus, any contribution to the $\log\{C_{\text{bulk}}\}$ *vs.* $\log\{V_{\text{bias}}\}$ plot will be a systematic vertical shift of the entire curve. Since V_{depl} is determined from the point of inflection in this curve, not from the absolute value of the capacitance, these effects contribute negligibly. The contribution is not zero due to the logarithmic capacitance scale which will affect the slope, and therefore the point of intersection with the horizontal region, in the event of an overall, additive, shift in capacitance.

The dominant error comes from the fitting, $\sigma_{\text{fit}} = \pm\, 1\ V$.

4.5 p-side Measurements

Measurements of coupling capacitance, interstrip capacitance, and total capacitance with respect to ground are presented. These results are shown to be consistent with simulation. (Interstrip capacitance measurements must be made with LCR meters with floating return connections; this requirement is discussed in Appendix A.3.)

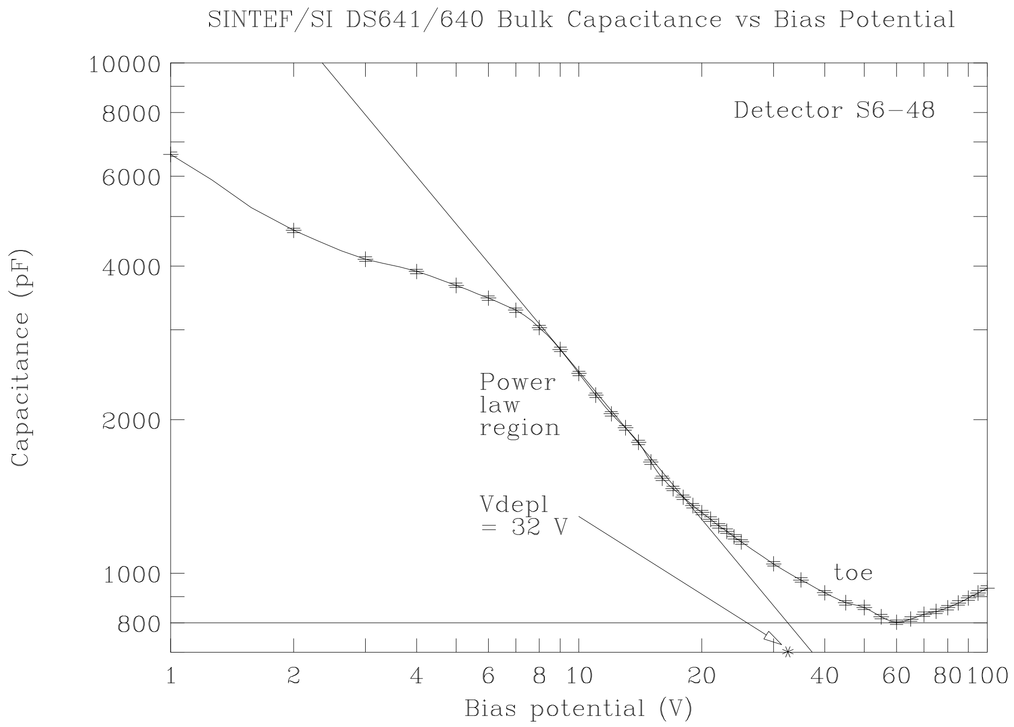


Figure 5: Example of a bulk capacitance versus bias potential measurement used to determine depletion voltage of a SINTEF/SI DS641/640 detector, S6-48. The measurement signal is 500 Hz at 1 V. V_{depl} is determined from the intersection of the line drawn through the power law region and a horizontal line drawn through the minimum above the toe. See Section 4.4 for a discussion of the details of the shape of the curve.

Table 7: V_{depl} uncertainty contributions.

Source	Magnitude
σ_V^{fit}	$\pm$ 1V
$\sigma_C^{\mathrm{cable\ loss}}$	$\pm\ 10^{-4}$ V
σ_V^{K237}	$\pm$ 0.033 V
$\sigma_C^{\mathrm{HP\ 4284A}}$	$\pm$ 0.3%
$\sigma_C^{\mathrm{HP\ 4192A}}$	$\pm$ 0.5%
$\sigma_C^{\mathrm{LCR\ cable}}$	$\pm$ 1 pF
$\sigma_C^{\mathrm{LCR\ cal}}$	$\pm$ 0.01 pF

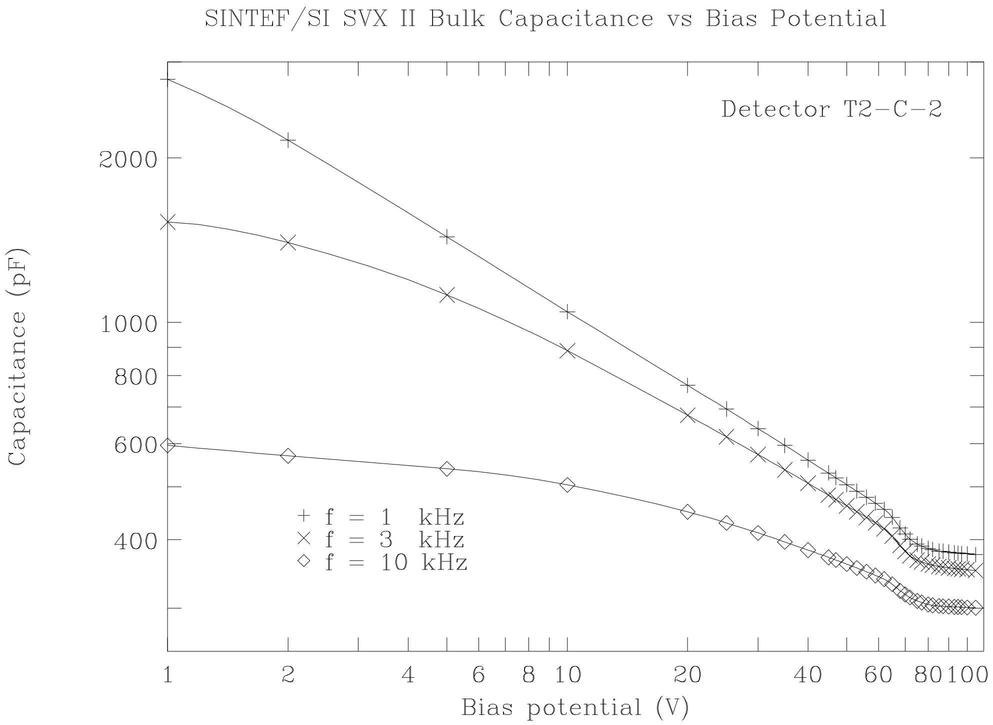


Figure 6: Example of a bulk capacitance versus bias potential measurement used to determine depletion voltage for a SINTEF/SI SVX II type C detector, T2-C-2. The frequency dependence of the capacitance has a negligible effect on the determination of the depletion voltage (prior to irradiation [23]). See Section 4.4 for a discussion of the details of the shape of the curve.

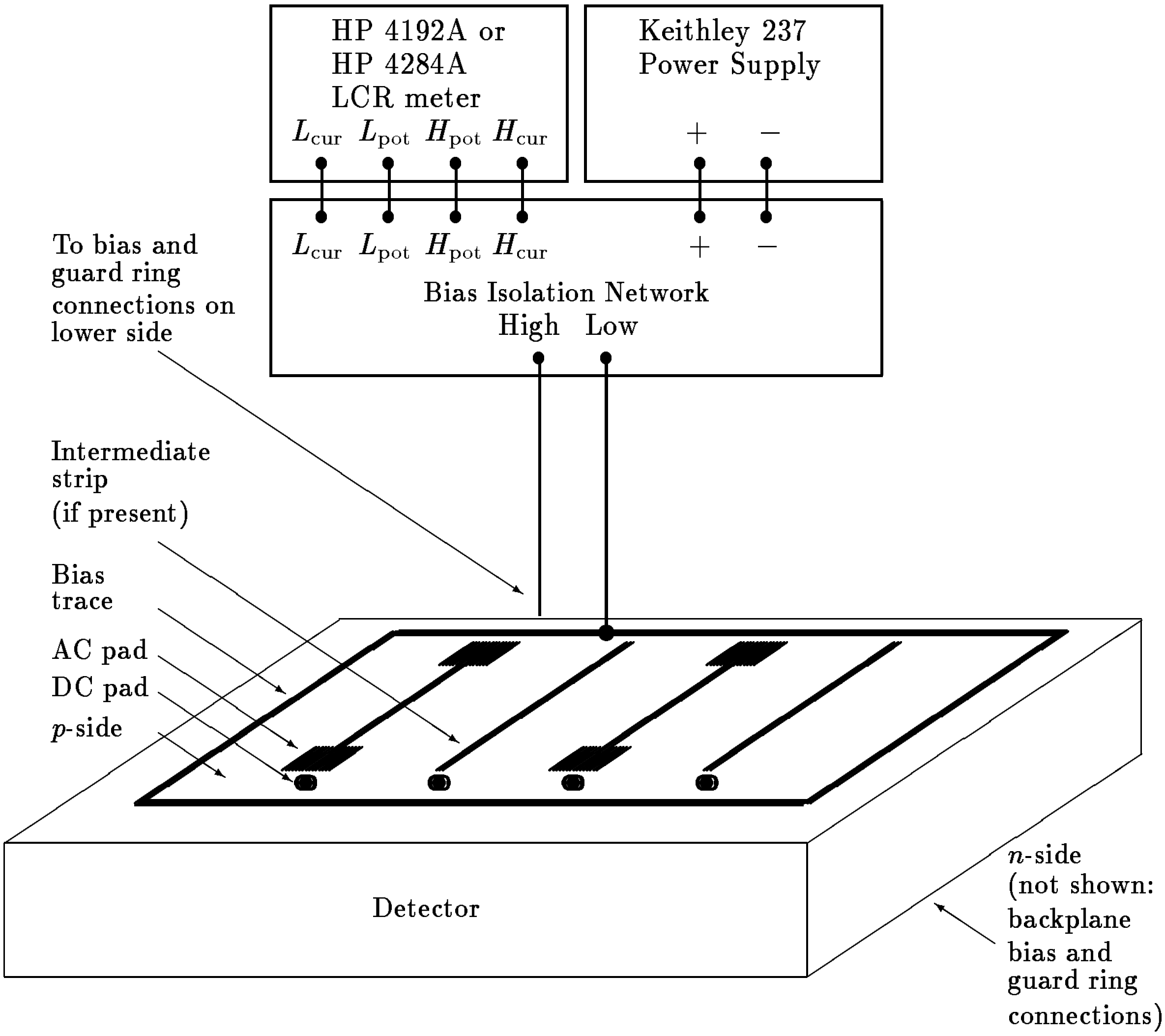


Figure 7: Depletion voltage measurement arrangement. The detector and probes remain in darkness during the measurement. The meter and power supply are computer–controlled via an IEEE488 bus. The meter's AC test signal and the (positive) bias potential are carried by the "High" terminal of the bias isolation network, while the return AC signal is delivered to the meter and the return bias potential to its "Low" potential terminal. The guard ring connections (not shown) are tied to the bias traces on their respective sides. (For the case of detectors with split traces for independent biasing of the even- and odd-numbered strips, two probes are required to contact these, and a third probe for the guard ring. All three probes are then tied to the appropriate terminal of the power supply. A similar arrangement is made for the opposite side. For simplicity, only one connection is shown in the figure.) The bias isolation network is illustrated in Figure 16. The meter and power supply are isolated according to a protocol described in Appendix A.3. See Section 4.4. This figure is based on a figure from Reference [24].

4.5.1 Coupling Capacitance

The capacitance between the AC metal read-out strip and the p^+ DC implant strip isolates the bias voltage and leakage currents from the front-end of the read-out chip. In terms of the overall total capacitance with respect to ground, the coupling capacitor couples the AC and DC components of the interstrip capacitance (Section 4.5.2) and allows both components to be measured by probing adjoining AC strips. This coupling is frequency dependent; therefore, it is important to understand the coupling capacitance in the context of the overall total capacitance measurement. As such, this capacitance is a factor in the total capacitance with respect to ground presented to the front-end amplifier and therefore affects the reflected equivalent noise charge of the chip. This capacitance also couples the charge in the DC implant strip to the read-out chip. Thus, the coupling capacitance impacts both the numerator and denominator of the signal–to–noise ratio.

The coupling capacitance is measured with much of the same equipment and many of the same procedures used for the depletion voltage measurement (Section 4.4). Using the double–sided detector probing chuck as illustrated schematically in Figure 8, the detector is biased and isolated. Two low parasitic capacitance probe tips are attached through the bias isolation network to the HP 4192A or 4284A meter. These probes are placed on the DC and AC pads of the strip under test. (In the case of the HP 4284A, the high potential probe – isolated by the capacitance in the bias isolation network – is landed on the DC pad to prevent shorting the detector bias through the LCR meter. The low potential probe, HP 4192A or HP 4284A signal ground, contacts the AC strip.)

The coupling capacitance (assuming a parallel equivalent measurement circuit, C_{parallel}, which the LCR meter uses to model the detector under test) [6] and the dissipation factor D [7] are recorded either automatically, using the IEEE488 bus and host computer, or manually. A logarithmic frequency sweep of between 6 and 48 points from 20 Hz to 1 MHz is made for each new detector type. A typical curve is shown in Figure 9. A flat region of the C_{coupling} *vs.* frequency plot is identified. Subsequent coupling capacitance measurements are made at a frequency well within the flat region. For the coupling capacitance measurements described in this paper, a frequency of 500 Hz was used.

An investigation of systematic uncertainties associated with measurements of coupling capacitance for the p-side of SINTEF/SI SVX II detectors is given in Section 4.7.2.

[6] The LCR meter also supports a series model (C_{series}). For the measurements discussed in this paper, the parallel model was used. The difference between the two models is negligible for the measurements described here. This is shown in Figure 15.

[7] The dissipation factor D ($= 1/Q$ where Q is the "quality factor") is a measure of the nonideality of the capacitor under test, i.e., its resistance. A perfect capacitor would have $D = 0$. D is an input to the determination of the basic accuracy of the LCR meter. The HP 4284A basic accuracy is guaranteed only for $|D| \leq 0.1$.

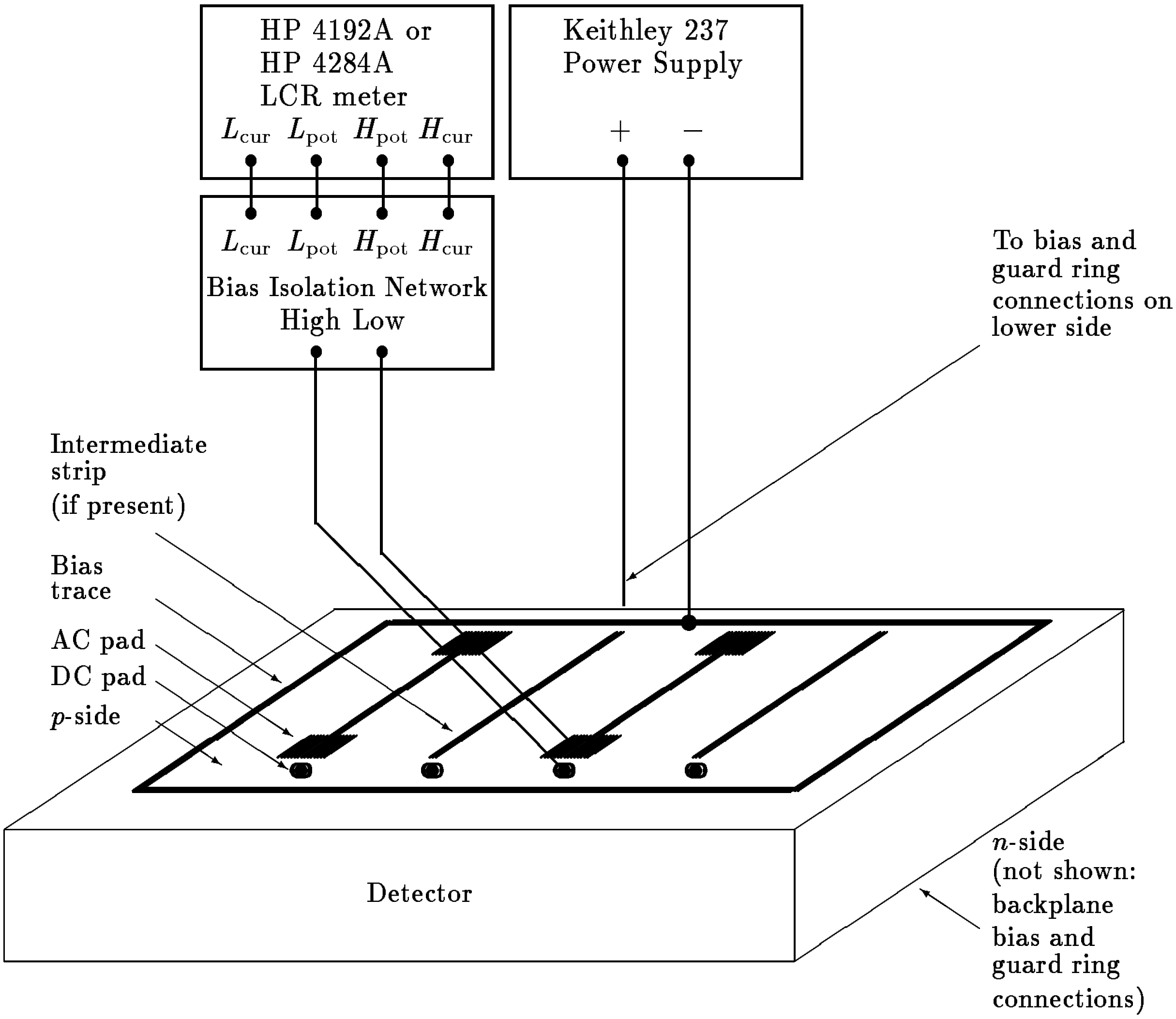


Figure 8: p-side coupling capacitance measurement arrangement. The guard ring connections (not shown) are tied to the bias traces on their respective sides. The bias isolation network is illustrated in Figure 16. The meter and power supply are isolated according to a protocol described in Appendix A.3. See Section 4.5.1. This figure is based on a figure from Reference [24].

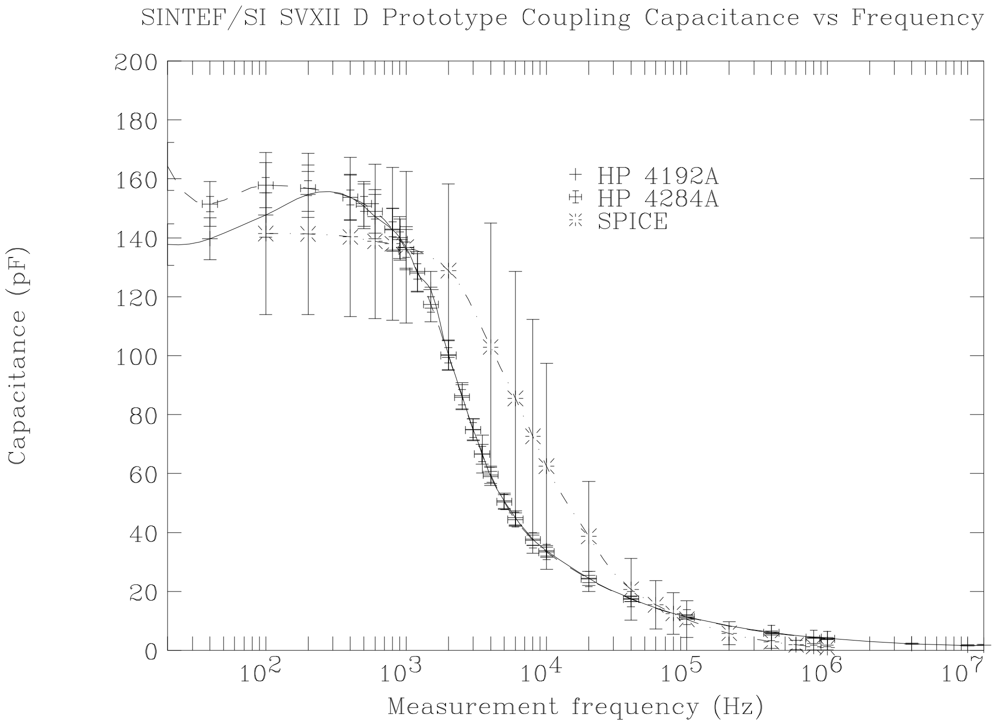


Figure 9: Coupling capacitance versus measurement frequency for the *p*-side of the SINTEF/SI SVX II prototype type D detector. Measurements using the HP 4192A Low Frequency Impedance Analyzer and the HP 4284A Precision LCR meter are shown. Results of a SPICE simulation are included.

4.5.2 Interstrip Capacitance

The interstrip capacitance is the dominant component of the total capacitance with respect to ground. The larger the ratio of interstrip to coupling capacitance, the more of the signal is coupled away to neighboring strips instead of to the front–end amplifier. This reduces the signal and thus lowers the signal–to–noise ratio as well. For these reasons, it is desirable to minimize the interstrip capacitance.

The measurement arrangement is shown in Figure 10. Neighboring strips are floated. We chose 1 MHz as the reference measurement frequency for the following reason: interstrip capacitance is composed of two components, $C^{\mathrm{AC}}_{\mathrm{interstrip}}$ and $C^{\mathrm{DC}}_{\mathrm{interstrip}}$, reflecting the capacitance between adjacent AC metal strips and the capacitance between adjacent implants, respectively. (See Figure 1.) These components are coupled by the coupling capacitor. At sufficiently high frequencies (above the toe in the graph shown in Figure 11), the coupling capacitors act as AC shorts (as may be seen by inspection of Figure 9), and a measurement of the $C^{\mathrm{AC}}_{\mathrm{interstrip}}$ component includes the $C^{\mathrm{DC}}_{\mathrm{interstrip}}$ component (and any cross couplings between the AC metal strip and its neighboring DC implant). The calibration procedure is described in Appendix B.2.

We have investigated the effect of probing next–to–nearest neighbor strips by leaving one floating strip between two probed strips, repeating with two floating strips in between, then three strips, and so on. We estimate on this basis that the sum of all neighboring strips raises the overall interstrip capacitance by approximately 10 percent over that provided by nearest neighbors alone.

Interstrip capacitance is sensitive to the ground reference of the measuring device. As discussed in Appendix A.3, a meter with fully floating inputs must be used to obtain meaningful results over a wide frequency range.

4.5.3 p-side Single AC Strip Capacitance With Respect to Ground

The direct measurement of the total capacitance presented to the front–end electronics is, of the measurements described in this paper, the most sensitive to the effects of ground loops, isolation, and probe contact quality. (See Appendices A.3 and B.5 for more on these topics.)

The probe placement and electrical connections are shown in Figure 12. Only a single probe is used, connected to the high potential terminals of the LCR meter. The LCR meter's L_{cur} and L_{pot} inputs are tied to the power supply terminals connected to the bias and guard rings on the underside of the sensor. The full operating potential is applied to the underside (n-side) of the sensor. The upper surface (p-side) is grounded.

With this connection scheme, the residual capacitance between the LCR meter's front panel and the device under test is approximately 0.5 pF more than for coupling and interstrip capacitance. Accordingly, a modified calibration protocol is called for. This protocol is

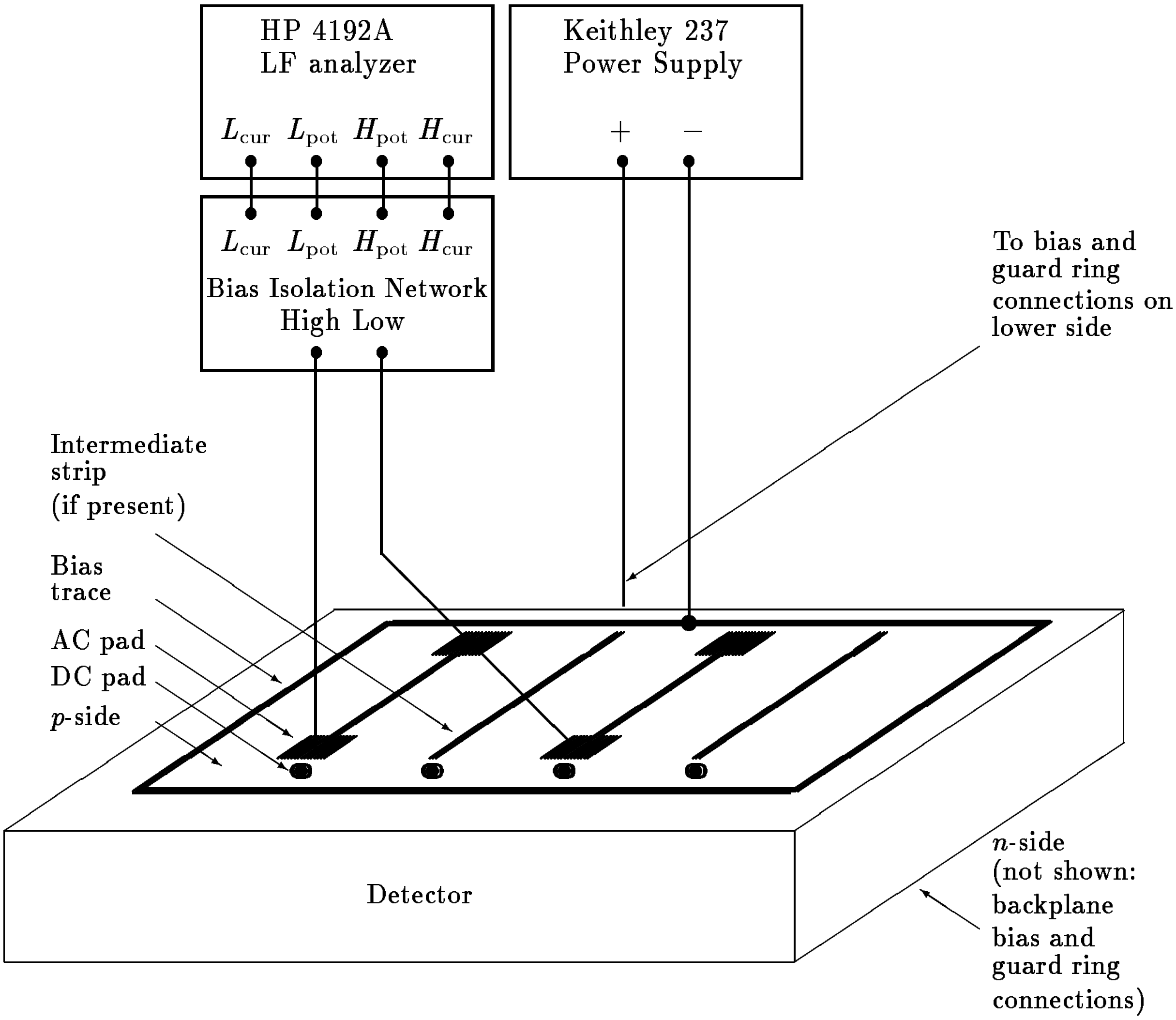


Figure 10: p-side AC interstrip capacitance measurement arrangement. For DC interstrip capacitance measurements, adjacent DC pads are probed. The guard ring connections (not shown) are tied to the bias traces on their respective sides. The bias isolation network is illustrated in Figure 16. The meter and power supply are isolated according to a protocol described in Appendix A.3. See Section 4.5.2.

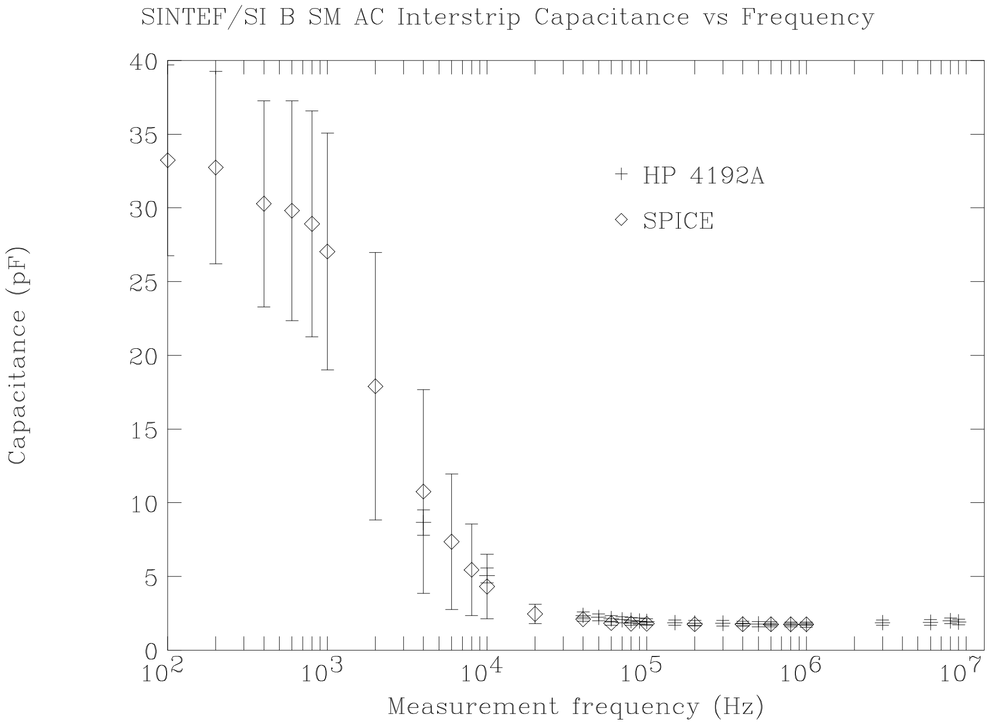


Figure 11: Interstrip capacitance versus measurement frequency for the p-side of a detector. The backplane contribution, $C^{p-\mathrm{side}}_{\mathrm{backplane}}$, is included in this measurement.

described in Appendix B.2.

The measured total capacitance with respect to ground is shown in Figures 13 and 14 for the HP 4192A and HP 4284A respectively. In each figure, two measurements and a simulation of a SINTEF/SI type B detector are presented: a direct measurement; a summed measurement, derived from interstrip capacitance measurements made with the same meter; and a SPICE simulation.

The summed measurements are derived from the interstrip capacitance measurements (Section 4.5.2) by multiplying the interstrip result by two, to include neighbors on both sides of the strips, and by 1.1, to account for non-nearest neighbor strips, for a total multiplicative factor of 2.2. The interstrip measurement already contains the backplane contribution to the total capacitance. The summed measurement derived from the HP 4284A meter is inconsistent with the other four curves at low frequencies. This effect is due to the loss of return AC signal when this meter is used for this measurement. This effect is discussed in Appendix A.3.

4.6 N-SIDE (DOUBLE–METAL) MEASUREMENTS

Measurements of the capacitance between DC implant strips ($C^{\rm DC}_{\rm interstrip}$), the interstrip capacitance between the first–metal AC strips (C_{11}), the overlap capacitance between the first–metal layer and the second–metal layer (C_{12}), and the interstrip capacitance between second–metal layer strips (C_{22}) on the n-side of a double–metal detector require use of a capacitance meter that supports fully isolated $L_{\rm cur}$, $L_{\rm pot}$, $H_{\rm cur}$, and $H_{\rm pot}$ inputs. Otherwise, the meter introduces an additional AC path for its return test signal to the power supply ground, which results in falsely low capacitance readings. This effect has been modeled in a SPICE simulation and is discussed in Appendix A.3. Accordingly, these measurements are beyond the scope of this paper. However, the net effect of these additional capacitances can be seen by comparing the total capacitance with respect to ground for the single–metal and double–metal cases. This is shown in Table 9.

4.6.1 COUPLING CAPACITANCE

On double–metal detectors, the AC and DC pads are located on adjacent edges of the sensor, instead of along one side. Thus the probe placement differs slightly from the p-side case. Otherwise, the n-side coupling capacitance measurement is performed in a manner identical to that used for the p-side (Section 4.5.1). Figure 15 indicates a typical n-side coupling capacitance measurement.

4.6.2 INTERSTRIP AND OVERLAP CAPACITANCE

Interstrip and overlap capacitance measurements require use of a capacitance meter that supports fully isolated inputs and are outside the scope of the present paper. A scheme to

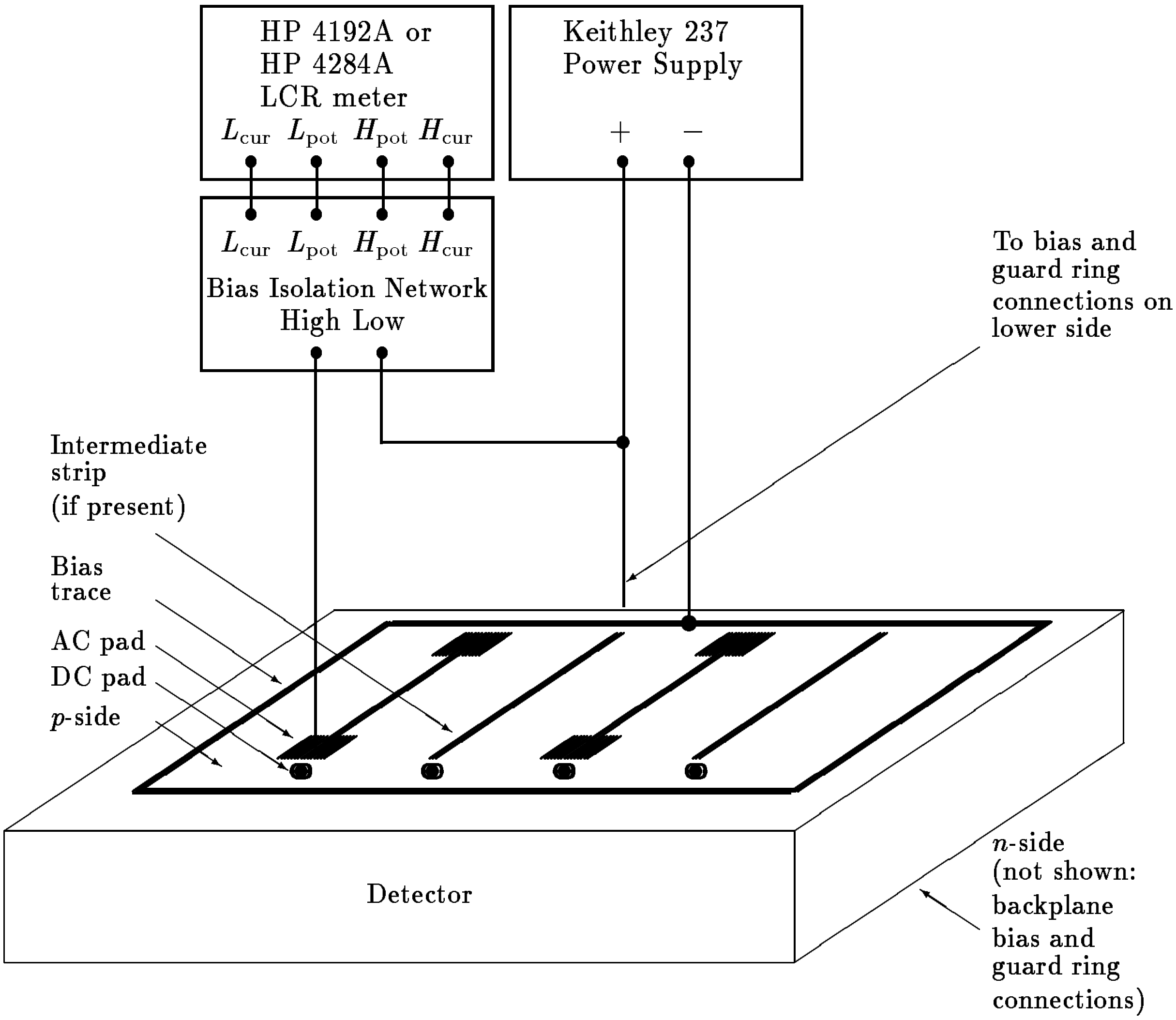


Figure 12: p-side total capacitance measurement arrangement. The guard ring connections (not shown) are tied to the bias traces on their respective sides. The bias isolation network is illustrated in Figure 16.

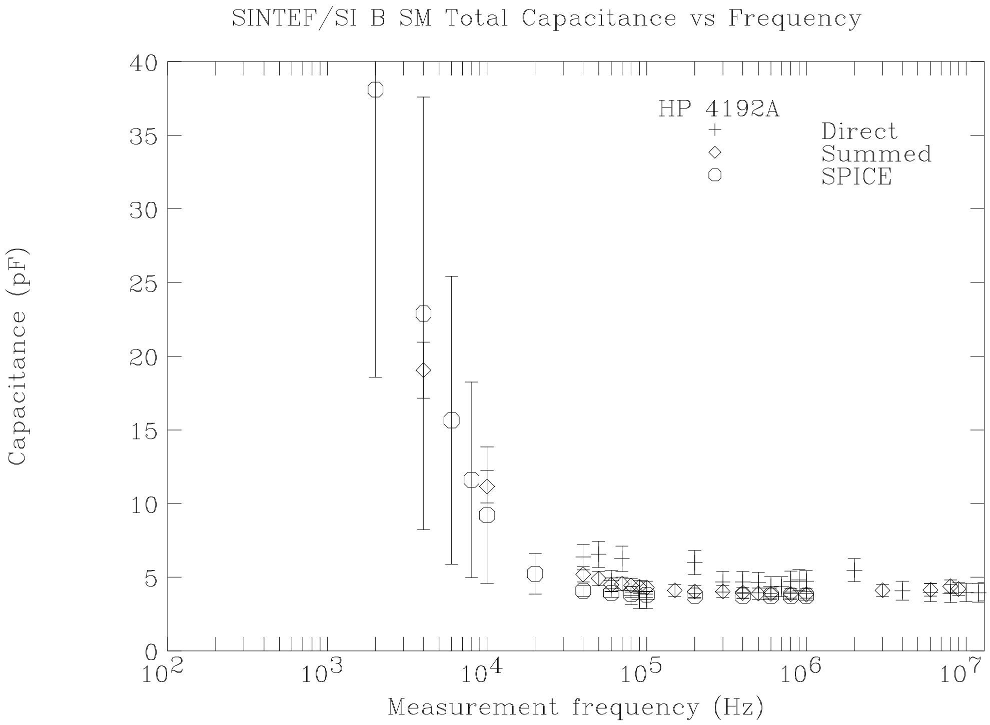


Figure 13: Total capacitance versus measurement frequency for the p-side of the SINTEF/SI SVX II prototype type B detector. See Section 4.5.3. Two curves are presented for the HP 4192A Low Frequency Impedance Analyzer; one represents a direct measurement and the other represents a summed measurement, derived from interstrip capacitance measurements (Section 4.5.2). The data presented have had the contributions due the cabling and probes intervening between the meter and detector subtracted. A SPICE simulation is also plotted. Note that in the summed case the HP 4192A (diamond symbol) and SPICE simulation (octagon) are consistent above 10^3 Hz. Compare with similar curves for the HP 4284A Precision LCR meter in Figure 14.

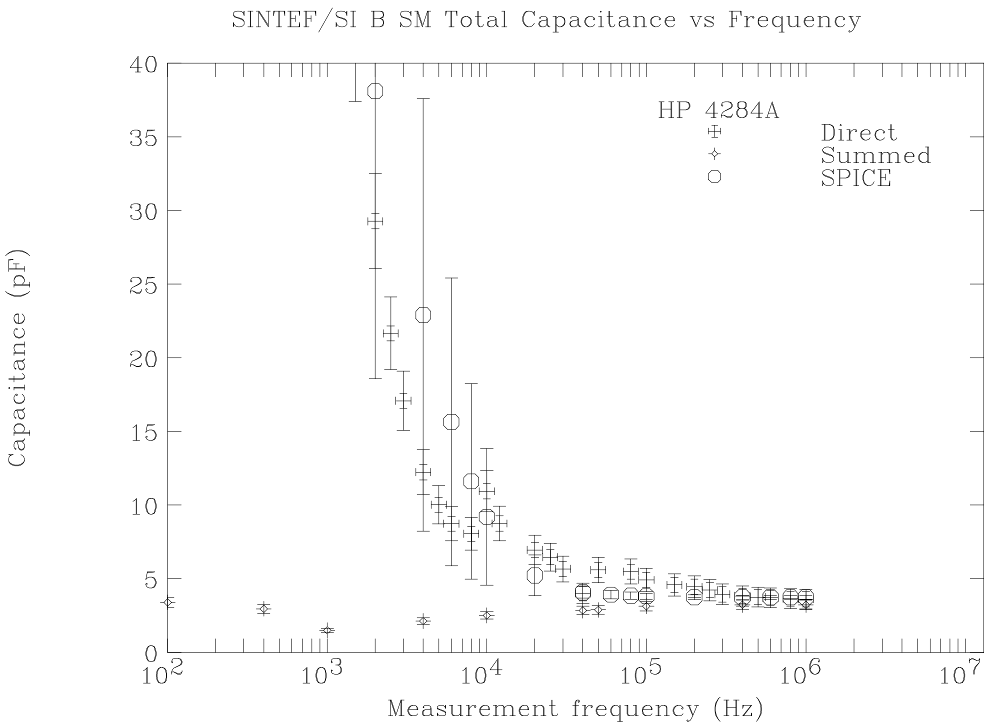


Figure 14: Total capacitance versus measurement frequency for the p-side of the SINTEF/SI SVX II prototype type B detector. See Section 4.5.3. Two curves are presented for the HP 4284A Precision LCR meter; one represents a direct measurement and the other represents a summed measurement, derived from interstrip capacitance measurements (Section 4.5.2). The data presented have had the contributions due the cabling and probes intervening between the meter and detector subtracted. A SPICE simulation is also plotted. Note that in the summed case the HP 4284A ("fancy diamond" symbol) and SPICE simulation (octagon) approach consistency only above 10^5 Hz. This effect is discussed in Appendix A.3. Compare with similar curves for the HP 4192A Low Frequency Impedance Analyzer in Figure 13.

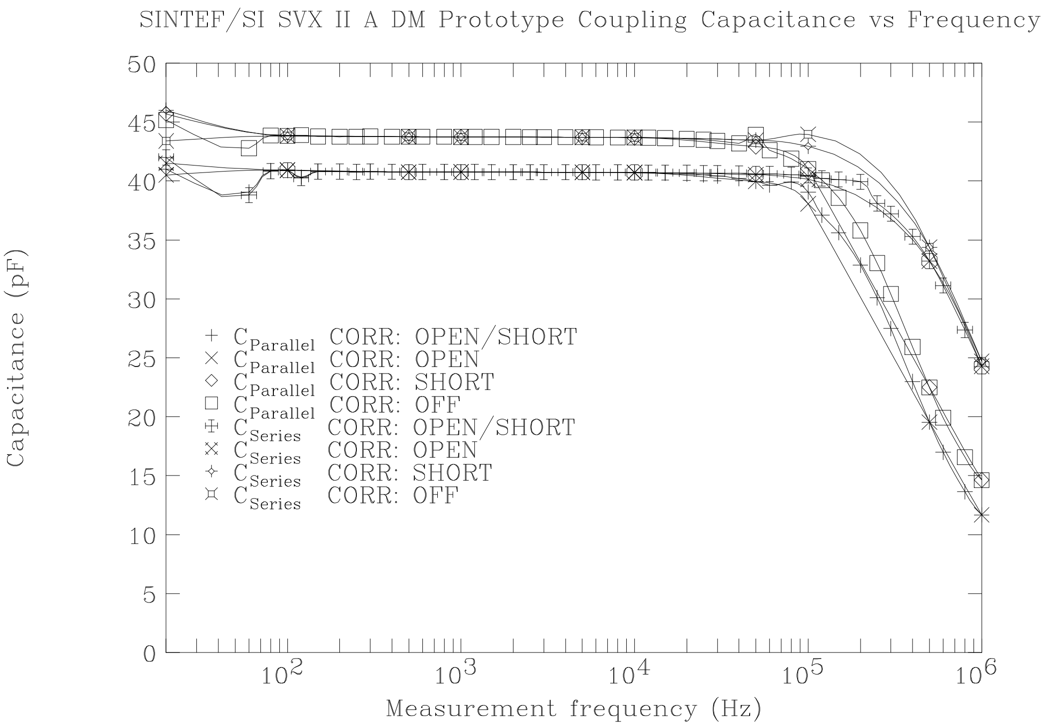


Figure 15: Coupling capacitance versus measurement frequency for the n-side of the SINTEF/SI SVX II prototype type A detector. No errors are shown. The various measurement options of the HP 4284A LCR meter are shown. These include the modeling of parasitic capacitances as being in *parallel* or in *series* with the device under test, and the use of several calibration modes (CORR:), including no calibration (OFF), OPEN, SHORT or both (OPEN/SHORT). The two families of curves are separated by 3 pF in the flat region. This is the amount applied by the OPEN calibration of the HP 4284A Precision LCR Meter to correct for the residual capacitance of the 2 meter extension (HP 16048D), bias isolation network, fixturing, and probe tips. Similar corrections apply for other measurements. The calibration procedure is discussed in Appendix B.2.

make such measurements is described in Section 7.

4.6.3 n-side Single AC strip Capacitance With Respect to Ground

The total capacitance with respect to ground on the n-side is measured in the same manner as on the p-side, detailed in Section 4.5.3.

4.7 Estimate of Capacitance Uncertainty

4.7.1 Systematic Errors

The coupling, interstrip, and direct total capacitance measurements share many of the same sources of systematic error. The overall error assigned to the direct and interstrip measurements is 10 percent. The coupling capacitance, which is an order of magnitude larger, is assigned a five percent systematic uncertainty. The direct method of measuring total capacitance is preferred to the summed method where a straightforward quadrature sum of the component errors would exceed that of the direct measurement. Sources considered in making this estimate are listed in Table 8 and discussed below.

Table 8: Measured capacitance uncertainty contributions.

Source	Magnitude
$\sigma_C^{\text{fixturing}}$	$\pm$ 0.5 pF
$\sigma_C^{\text{cable loss}}$	$\pm\ 10^{-4}$ V
$\sigma_C^{\text{HP 4284A}}$	$\pm$ 0.3%
$\sigma_C^{\text{HP 4192A}}$	$\pm$ 0.5%
$\sigma_C^{\text{LCR cable}}$	$\pm$ 1 pF
$\sigma_C^{\text{LCR cal}}$	$\pm$ 0.01 pF

The principle difference between this and Table 7, where the contributions to depletion voltage uncertainty are listed, is in the contribution of the intervening cabling and fixturing, $\sigma_C^{\text{fixturing}} = \pm\ 0.5\ p\text{F}$. This is the dominant term. Unlike the case of depletion voltage (Section 4.4.3), where absolute errors in measured capacitance do not affect determination of the point of inflection of the C *vs.* V curve, here the capacitance intervening between the meter and the device under test must be compensated. As mentioned previously, this additional capacitance is on the order of 2.5 to 3.0 pF before OPEN/SHORT correction (HP 4284A) or pedestal subtraction (HP 4192A). After this correction, the meter routinely reads less than $\pm$ 0.1 pF (often less than $\pm$ 0.001 pF) when the probes are raised. Thus, the quoted uncertainty represents a conservative estimate.

A systematic effect seen in measurements of the p-side coupling capacitance of SINTEF/SI SVX II prototype detectors is discussed separately in Section 4.7.2.

4.7.2 Nonuniformities in p-side Coupling Capacitance for SINTEF/SI SVX II Prototypes

The p-side coupling capacitance versus frequency for a typical detector is shown in Figure 9. The coupling capacitance for 24 unirradiated SINTEF/SI SVX II prototype detectors taken at a measurement frequency of 500 Hz is shown in Figures 12a and 12b of [25]. Each data point represents an average over five strips distributed uniformly over the surface of the detector. The error bars are determined from the standard deviation of the average. Many of these p-side measurements exhibit substantial nonuniformities across the surface of the detector as reflected in the large standard deviations; as great as ten times those of similar n-side (*ibid.*, Figures 11a and 11b) measurements (see Section 4.6.1) of both single–metal and double–metal detectors.

These large standard deviations are not explainable in terms of processing variations affecting strip width, strip thickness, implant width, implant depth, dielectric thickness, etc., both according to the manufacturer [26] and normal variations input to a SPICE simulation (see Section 3). Several possible causes were investigated.

Two tests were performed. One test was designed to investigate the possible effect of low interstrip resistance or low bulk resistivity as a possible sink of the LCR meter signal (with attendant, falsely low capacitance readings as described in Appendix A.3). No results consistent with low resistance were observed. The second test was designed to investigate possible charge up of the polyimide passivation layer. This test was determined to be affected by the relative humidity of the ambient air and was inconclusive. The large variations in coupling capacitance on the p-side of the SINTEF/SI SVX II prototype detectors remain under investigation.

5 Summary of Total Capacitance Measurements

Direct measurements of total capacitance for the n- and p-sides with respect to the detector backplane are presented in Table 9. Two summed measurements are included for comparison. Three vendors, one with eight distinct geometries, are represented. Of these, the Micron, Ltd. and SINTEF/SI type D double–metal and the Hamamatsu Layer 0 double–metal designs approximate the SVX II baseline design.

We have performed a comparison of the total capacitance obtained by direct measurement and by summing the interstrip and backplane contributions. We find that the direct and summed measurements are in agreement, as shown in Figures 13 and 14 (and for one Micron, Ltd. and one SINTEF/SI detector in Table 9).

These measurements are in agreement with direct and summed probe-station based measurements made on similar detectors by other workers [27] and with noise based measurements using calibrated SVXH3 amplifier chips [28, 29]. In several cases the same detector was measured at different institutions.

Except for the case of Hamamatsu detectors, a SPICE simulation (Section 3) is given for comparison in Table 9. The simulation and direct measurements are consistent [8] within 1 σ in 63% of the cases reported. 88% of the simulations and measurements are consistent within 2 σ. We note that the larger discrepancies appear to be associated with longer strip lengths for the p-side.

Based on a measurement of the SINTEF/SI type D detector, which resembles the Layer 0 baseline design for SVX II, we predict a total ladder (2 sensor) n-side capacitance of $20. \pm 1.4$ pF presented to the front-end of the SVX III chip. Similarly based on the Micron, Ltd. type D detector, our prediction is $19. \pm 1.3$ pF. The difference between the Micron, Ltd. process and the SINTEF/SI process is smaller than our systematic error.

The Hamamatsu Photonics, K.K. detector measured 19 ± 1.9 pF with a resulting Layer 0 ladder capacitance of $38. \pm 2.7$ pF. This is almost a factor of two larger than the Micron, Ltd. and SINTEF/SI case. If this is confirmed, this would predict a shorter performance lifetime for this design. Other workers [27] have measured two similar prototypes with consistent results.

It should be noted that unlike the type D's, the Hamamatsu Photonics, K.K. design employs "ganged" metal-1 strips. This doubles their contribution to the total capacitance while increasing the efficiency of charge collection for oblique tracks. This design also doubles the number of Metal 1/Metal 2 overlaps, further increasing the total capacitance. However, a subsequent Hamamatsu Photonics, K.K. design does not employ a ganged geometry and is expected to have lower capacitance [30].

6 Conclusion

Direct measurements of the total capacitance presented to front–end amplifier chips by a variety of double–sided silicon microstrip detectors have been given. The constituents of the total capacitance for the p-side, the bulk and interstrip capacitance, have been measured separately and demonstrated to sum to the total capacitance over a wide frequency range. SPICE simulations based on first principles for corresponding quantities agree to within 20% with these measurements over a wide frequency range.

Direct measurements of the total capacitance with respect to ground for the n-side have been presented. These reflect the additional contributions of the interstrip capacitance of the second–metal layer and the overlap of the first and second–metal layers. These agree with SPICE simulations of the n-side to within 10% over a wide frequency range. Separate measurements of these additional n-side contributions are beyond the scope of this paper; such measurements require use of a capacitance meter that supports isolation of its input

[8] We define σ for purposes of comparing measurement (M) and simulation (S) as $\sigma = \sqrt{\sigma_M^2 + \sigma_S^2}$.

Table 9: Summary of direct measured ($C_{\rm total}^{\rm meas}$), summed measured ($C_{\rm total}^{\Sigma}$), and simulated ($C_{\rm total}^{\rm sim}$) capacitances for several detectors and geometries. The basic detector geometries are described in Table 1.

Designator	Name	strip length (cm)	$C_{\rm total}^{\rm meas}$ (pF @ 1 MHz)	$C_{\rm total}^{\Sigma}$ (pF @ 1 MHz)	$C_{\rm total}^{\rm sim}$ (pF @ 1 MHz)
		n-side, Single–Metal			
SI-A-SM	KB51-1	2.0	2.8 ± 0.28	–	2.0 ± 0.13
MI-A-SM	1119-4B	1.9	2.0 ± 0.20	–	2.4 ± 0.17
SI-C-SM	SVX2-C-32	1.3	2.0 ± 0.20	–	2.7 ± 0.29
SI-D-SM	SVX2-D-4	1.3	2.2 ± 0.22	–	1.6 ± 0.80
		n-side, Double–Metal			
SI-A-DM	KB54-1	$2.0 + 4.1^{a}$	8.3 ± 0.83	–	6.2 ± 0.85
SI-C-DM	LB54-1	$(2^{b} \times 1.3) + 8.2^{a}$	7.2 ± 0.72	–	7.3 ± 0.60
SI-D-DM	LB53-2	$(2^{b} \times 1.3) + 8.2^{a}$	$10. \pm 1.0$	–	9.7 ± 1.1
MI-D-DM	1115-24B	$(2^{b} \times 1.2) + 8.3^{a}$	9.6 ± 0.96	–	$13. \pm 1.4$
HA-0-DM	SDX32287-6-0th-A	$(2^{b} \times 2^{c} \times 1.56) + 7.64^{a}$	$19. \pm 1.9$	–	–
		p-side			
SI-A-DM	KB54-1	4.1	3.7 ± 0.37	–	3.6 ± 0.20
SI-A-SM	KB51-1	4.1	3.7 ± 0.37	–	3.6 ± 0.20
MI-A-SM	1119-4B	4.1	3.7 ± 0.37	3.6 ± 0.36	3.7 ± 0.42
SI-B-SM	SVX2-B-4	4.1	3.6 ± 0.36	3.8 ± 0.38	3.7 ± 0.16
SI-B-SM	SVX2-B-5	4.1	3.4 ± 0.34	–	3.7 ± 0.16
SI-C-DM	LB54-1	8.2	5.5 ± 0.55	–	7.5 ± 0.30
SI-D-DM	LB53-2	8.2	6.1 ± 0.60	–	7.5 ± 0.30
SI-D-SM	SVX2-D-32	8.2	5.9 ± 0.59	–	7.5 ± 0.30
MI-D-DM	1115-24B	8.3	5.5 ± 0.55	–	7.8 ± 0.35
HA-0-DM	SDX32287-6-0th-A	7.61	6.5 ± 0.65	–	–

[a] 2nd metal; [b] multiplexing; [c] ganging.
Note: Measurements averaged over 5 or more strips; systematic errors only.

terminals from the meter system ground. Interstrip capacitance measurements and SPICE simulations of both the isolated and non-isolated cases have been presented to demonstrate this requirement.

Direct total capacitance measurements using non-isolated meters have been validated by comparison with isolated meters and with SPICE simulations. A conservative assignment of systematic error at ten percent for the measurements presented in this paper has been made.

Detailed summaries of the steps required for each measurement have been given, including a listing of sources of systematic error. A list of grounding and isolation requirements has been included.

The total capacitance measurements presented are consistent with measurements by other workers. The measurements presented in this paper forecast an acceptable pre-irradiation capacitive load on the front-end amplifier of $20. \pm 1.4$ pF, averaging the Micron, Ltd. and SINTEF/SI type D cases together. We predict an acceptable pre-irradiation signal–to–noise ratio for data taking in the regime of the 132 ns crossing time of the Fermilab Tevatron Run II.

7 Outlook

Measurements of the total capacitance with respect to ground on the n- and p-sides of SVX II prototype sensors irradiated beyond 1 MRad are ongoing. These will indicate whether the p- and n-side capacitances will remain at a level acceptable for physics data taking over a useful portion of Run II. Such measurements will allow a prediction of the amount of delivered integrated luminosity at which layers of SVX II must be replaced. The SVX III deadtimeless data acquisition system is in the prototyping stage as is SVX II ladder prototyping. These key elements will allow for signal–to–noise ratio measurements on the final detector system to be performed under conditions matched to actual detector operation. This will be the ultimate test of the noise performance of SVX II at turn-on.

Use of a capacitance meter with fully isolated inputs (such as the HP 4192A) will further the investigation of the individual contributions to the total capacitance with respect to ground on the n-side of a silicon microstrip detector: $C^{\mathrm{DC}}_{\mathrm{interstrip}}$, C_{11}, C_{12}, and C_{22} can be directly measured in a manner electrically similar to the p-side interstrip case, detailed in Section 4.5.2. There is a mechanical difference, however. The vias connecting the first– and second–metal layers must be broken to decouple these capacitances. This is an irreversible and therefore destructive act. These procedures have been described in References [27] and [31].

These measurements will allow the effect of varying levels of irradiation to be investigated and the performance of SVX II in Run II to be predicted.

8 ACKNOWLEDGEMENTS

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APPENDICES

A INSTRUMENTATION

Measurements of double–sided detectors require several pieces of apparatus, some highly specialized. These are discussed below.

A.1 COMMERCIALLY AVAILABLE EQUIPMENT

The following pieces of commercially available equipment are representative of technology we have found useful in making the measurements reported here. Measurements of similar quality may be made with equipment from other suppliers and with other models.

- Alessi REL4100A analytical probe station with MH and MD series micro-positioners.
- Hewlett–Packard 4192A Low Frequency Impedance Analyzer with IEEE 488.2 interface and:
  - HP 16047A: test fixture
  - HP 16048A: 1 m extension cable

  The Hewlett–Packard 4284A Precision LCR meter with IEEE 488.2 interface and:
  - Firmware Option 006: 2 or 4 m extension
  - HP 16048D: 2 m extension cable

  may be substituted [9] for the above.
- Keithley 237 Source/Measure unit with IEEE 488 interface and separable chassis and line grounds. (The HP 4142B DC Source/Monitor may be substituted.)
- Apple Macintosh IIci host computer with IEEE 488 interface card.
- National Instruments LabVIEW™ software, version 3.1 or higher.
- Microsoft QuickBASIC™ software.
- Terra Universal Laminar Flow hood (must be made light–tight).

[9] This unit is not recommended for interstrip or overlap capacitance measurements. See Appendix A.3 for a comparison of the HP 4192A and HP 4284A and other meters in the context of these measurements.

The basic accuracy of a meter is a measure of its ability to reproduce a measurement of a known standard, usually secured in a specified test fixture mounted on its front panel. For probe station measurements, where the device under test is several meters removed from the measuring device, in a nonstandard fixture, the basic accuracy is degraded by the parasitic impedance of the intervening probes, cabling, fixturing, and any phase errors induced by the extension cables due to their additional propagation time.

For measured $|D| < 0.1$, the basic accuracy of the HP 4284A LCR meter is $\pm$ 0.3% in the $C_{\mathrm{parallel}} - D$ measurement mode [32]. This includes the degradation of performance due to Option 006 and 2 m extension cable HP 16048D. Under similar conditions, using the 1 m extension cable HP 16048A, the basic accuracy of the HP 4192A Low Frequency Impedance Analyzer is $\pm$ 0.5% [33].

A.2 Custom Made Equipment

A.2.1 Bias Isolation Network

The Hewlett–Packard HP 4284A precision LCR meter is rated for up to $\pm$ 42 volts across its input terminals. (The HP 4192A Low Frequency Impedance Analyzer has a similar limit.) Some silicon microstrip detectors may require bias potentials far in excess of this to deplete [10] so a means must be found to isolate the external bias supply from the LCR meter during measurement.

In the case of a bulk capacitance measurement, the bias isolation network supplies the bias potential to the probes which, in turn, deliver bias voltage to the detector. In the case of all other measurements described in this paper, the network serves to protect the LCR meter from high voltages which are supplied independently to the sensor. The network allows the LCR meters AC test signal to reach the high potential probe and AC return signal to be picked up from the low potential probe while isolating the LCR meter from the DC bias potential.

This is accomplished by circuitry based on that described in [35], using coupling capacitors and limiting diodes to isolate the LCR meter's high potential terminals from the device under test. The circuit has been modified to provide additional bias supply filtering (C_3) and to capacitively isolate (C_4) the low potential terminals as shown in Figure 16. This allows the capacitance between two terminals, both at high voltage (e.g. $C^{\mathrm{DC}}_{\mathrm{interstrip}}$, the inter-implant strip capacitances) to be measured. Isolating the low potential terminals violates the HP 4284A design specifications and is not recommended by the manufacturer. The accuracy penalty of this modification as a function of frequency has been documented in Figure 17. Switch S_1 permits the experimenter to bypass the additional isolation capacitor.

[10] See [21] and references therein for details.

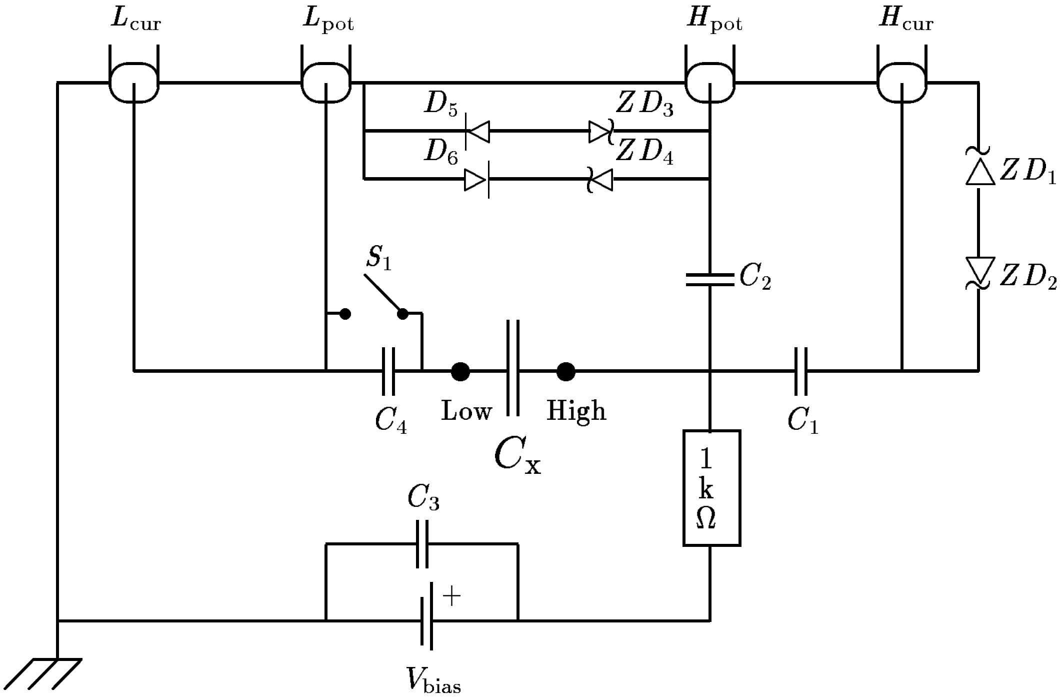

Figure 16: External DC voltage bias protection circuit (the "Bias Isolation Network" shown between the LCR meter and the detector probes in Figure 7.) It is constructed with an aluminum enclosure which forms the indicated ground plane. $L_{\rm cur}$, $L_{\rm pot}$, $H_{\rm pot}$ and $H_{\rm cur}$ are the low and high current and potential inputs to the HP 4284A precision LCR meter and HP 4192A Low Frequency Impedance Analyzer. C_x is the capacitance under test. $V_{\rm bias} \leq 200\ V$. Switch S_1 serves to bypass capacitor C_4. For the measurements described in this paper, S_1 remained closed.

The circuit is shown in the configuration used for $C_{\rm bulk}$ *vs.* V measurements, when the detector is biased through the probe tips of the LCR meter. For localized measurements, for example coupling capacitance, the detector is biased separately, and the power supply, filter capacitor and current limiter ($V_{\rm bias}$, C_3 and the 1 kΩ resistor) are omitted. The power supply return and LCR meter return are isolated according to Appendix A.3.

This circuit is based on Figure 5-62 of [35]. The component values are listed in Table 10.

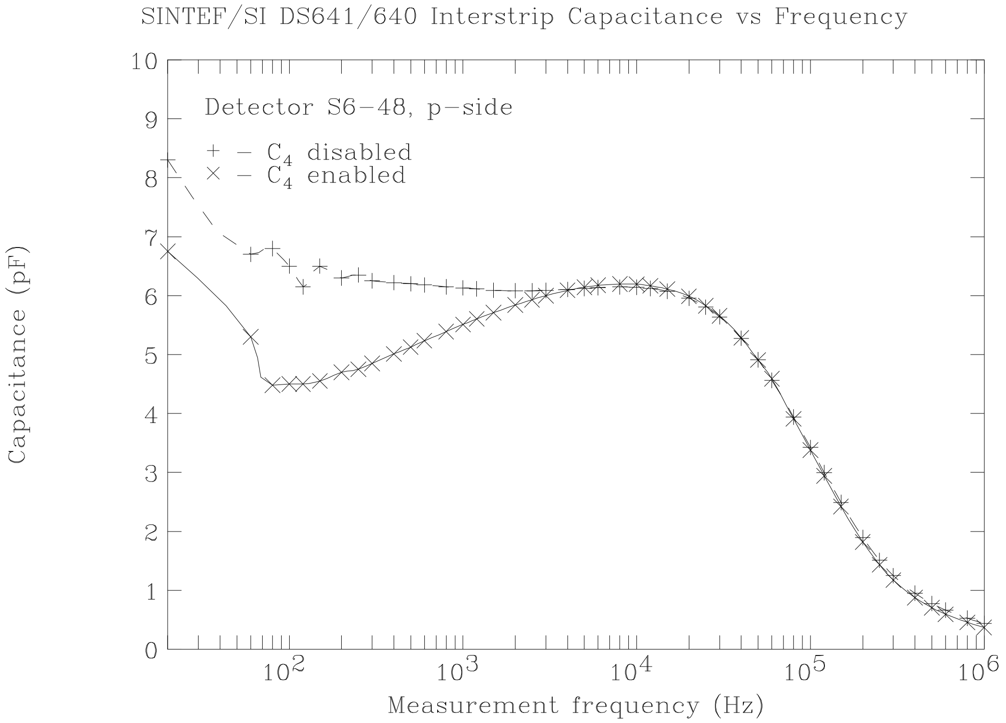

Figure 17: Effect of isolating the low level inputs ($L_{\rm cur}$, $L_{\rm pot}$) in the HP 4284A LCR meter in an interstrip capacitance measurement using capacitor C_4 shown in Figure 16. In the upper trace, switch S_1 is closed, bypassing capacitor C_4. In the lower trace, it is open. This isolation violates the manufacturer's requirement that one terminal of the device under test be held at LCR meter system ground.

Table 10: Bias isolation network components. See Figure 16 for a schematic diagram.

Part	Description	value	unit	tolerance	rating
C_1	Metalized polypropylene capacitor	20	μF	20%	200 V
C_2	Metalized polypropylene capacitor	1	μF	20%	200 V
C_3	Metalized polypropylene capacitor	20	μF	20%	200 V
C_4	Metalized polypropylene capacitor	30	μF	20%	200 V
$ZD_{1,2}$	Zener diode	47	V	5%	1 W
$ZD_{3,4}$	Zener diode	3.3	V	5%	1 W
$D_{5,6}$	Power diode	200	V	—	1 A
S_1	Single pole single throw switch	—	—	—	250 V

A.2.2 Low Parasitic Capacitance Probe Tips

Low parasitic capacitance probes were used in the measurements reported here. As shown in Figure 18, these are made from a 3.25 or 5.5 inch length of 0.078 inch diameter stainless steel rod with an inch of shrink wrap tubing attached at one end. Another piece of tubing is slipped over the first, and the base of an Alessi PTT-06/4 tungsten probe tip is inserted into the space between the two layers. The second layer of tubing is heated, securing the probe tip to the rod mechanically and leaving it electrically isolated. A 0.15 inch length of 0.015 inch diameter nickel wire is welded transverse to the probe tip where it exits the layers of shrink tubing. The central connecter of a one foot length of RG174U cable, terminated in a LEMO connector, is soldered to the nickel and strain relieved with a third layer of shrink wrap around the entire package.

A.2.3 Vacuum Chuck for Lower Side Probing

A device for probing the underside of a fully depleted detector while leaving the upper surface available for probing has been described in [34]. The design goals for this device include independent control of V_{bias} and V_{guard} on the lower surface, suitability for clean room use, unobstructed access to the upper surface (including use of low-profile probe cards), protection of the lower surface, micro-positionable probing under operator supervision via microscope, and secure, reproducible positioning of the detector.

It is possible to use a conductive silicone rubber sheet [11] instead of a chuck. This offers rapid, low cost, and safe contact to the bias and guard ring contacts on the lower side. If the detector has DC pads, they will also contact this sheet, so any isolation afforded by the bias resistors may be lost. We have found the underside probing method best reproduces the operating conditions of an actual ladder of silicon microstrip detectors.

[11] For example, Chomerics Sheet Stock 40-30-1015-1350 from Grace Electronic Materials, Chomerics, 77 Dragon Court, Woburn, MA 01888 USA.

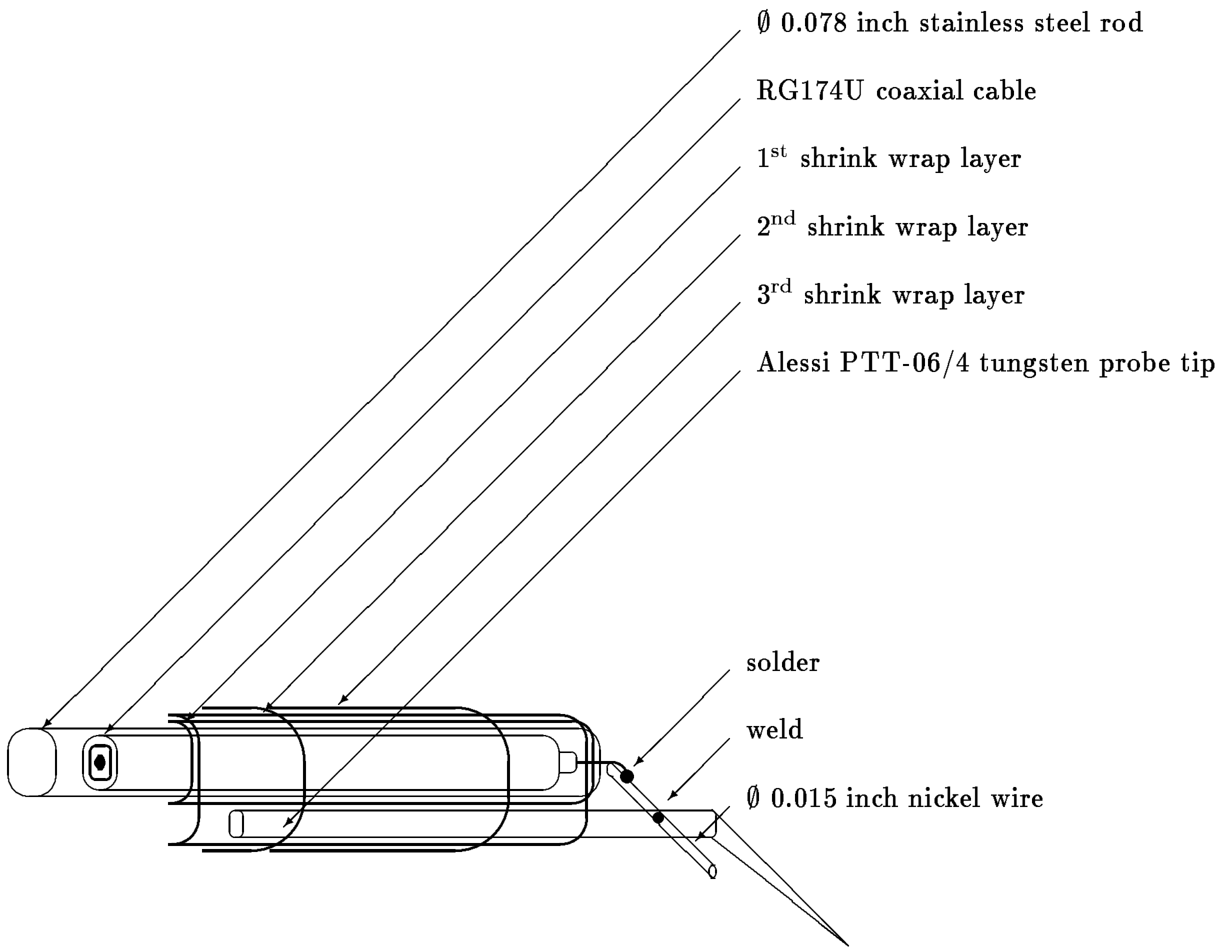

Figure 18: Low Parasitic Capacitance Probe Tip.

A.2.4 Bias Distribution Network

A shielded distribution panel for the Keithley 237 Source/Measure Unit output and return was constructed. Input is by two bayonet or three bayonet triaxial connector or BNC, all isolated from the chassis. It uses two fields of output connectors, one for high voltage and one for return. Each field has 3 LEMO connectors, three BNC connectors, three unshielded 0.040 inch connectors, and three banana connectors. The 0.040 inch connectors match those on the probe station and the micro-positioners. The BNC and LEMO connectors are isolated and may have their shields terminated by one of several means to eliminate ground loops. In addition to providing convenient distribution of power, the panel converts bias and return from a single coaxial cable to separate shielded coaxial cables (with power supply return on the central conductor of one and power supply output on the central connector of the other), allowing maximal shielding and minimal contact resistance.

A.3 Isolation and Grounding

Over the course of designing and debugging the measurements described in this paper, several instabilities (fluctuations in measured capacitance, over a wide range, including negative capacitances) were traced to ground loops. These will be briefly mentioned here to give the flavor of what the reader might investigate in his or her own system.

We have used the SPICE simulation to demonstrate that leakage of the LCR meter's test signal to sinks other than the LCR meter's return (e.g. the bias supply return) will result in falsely low capacitance values in the configuration we describe (C_{parallel}, the LCR meter's calculated capacitance assuming parasitic capacitances are in parallel with the device under test). The effect was modeled by introducing a specific resistance, R_{iso}, into the SPICE simulation (Section 3) to study the effects of grounding and isolation in the system, as shown in Figure 2. This effect depends on the measurement frequency, the type of measurement, and to some extent the detector under test. Below 1 kHz the effect is most severe; near 1 MHz in many cases it is negligible.

The isolation parameter, R_{iso}, is intended to model the isolation between the power supply and LCR meter. (It represents the net sum of ground loops described below.) Comparison of interstrip capacitance measurements made with isolated returns L_{cur} and L_{pot} (e.g. HP 4192A) and with L_{cur} and L_{pot} referenced to the meter's system ground (e.g. HP 4284A) indicate an approximate value of $R_{\mathrm{iso}} = 8\ \mathrm{k}\Omega$ for the ground referenced case. (Compare the $R_{\mathrm{iso}} = 8\ \mathrm{k}\Omega$ trace in the simulated interstrip capacitance measurement of Figure 19 with the measured HP 4284A interstrip capacitance trace in Figure 20. Then compare the $R_{\mathrm{iso}} = 800\ \mathrm{M}\Omega$ and HP 4192A traces in the two figures.) Similar comparisons of coupling capacitance and total capacitance measurements (Sections 4.5.1 and 4.5.3) and simulations indicate that these measurements are insensitive to differences between grounded and isolated returns.

For this reason it is desirable to eliminate all paths between the power supply (Keithley 237) return and the LCR meter (HP 4192A or HP 4284A) return. We have observed the

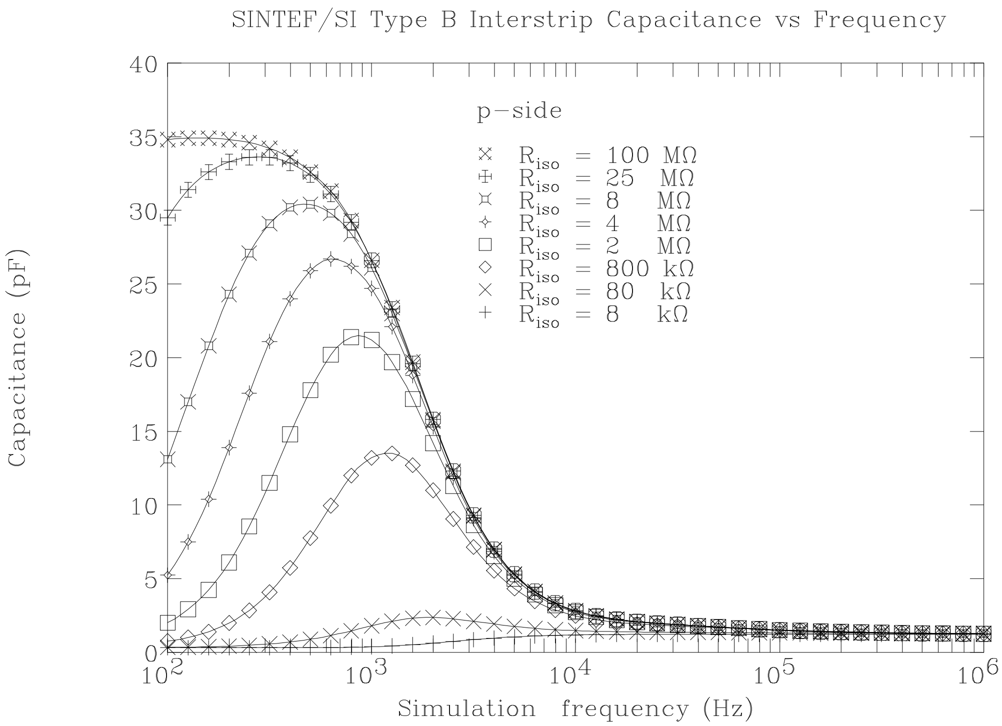

Figure 19: SPICE simulation of LCR meter and power supply isolation for a SINTEF/SI SVX II prototype type B detector. The interstrip capacitance for the p-side is shown. The value of the isolation parameter, $R_{\rm iso}$, between the LCR meter return and the power supply return was varied between 8 kΩ and 100 MΩ. Based on a comparison of this figure with Figure 20 the isolation between the HP 4284A returns ($L_{\rm pot}$ and $L_{\rm cur}$) and the power supply returns is approximately 8 kΩ while the isolation between the HP 4192A returns and the power supply return is in excess of 100 MΩ. See Appendix A.3.

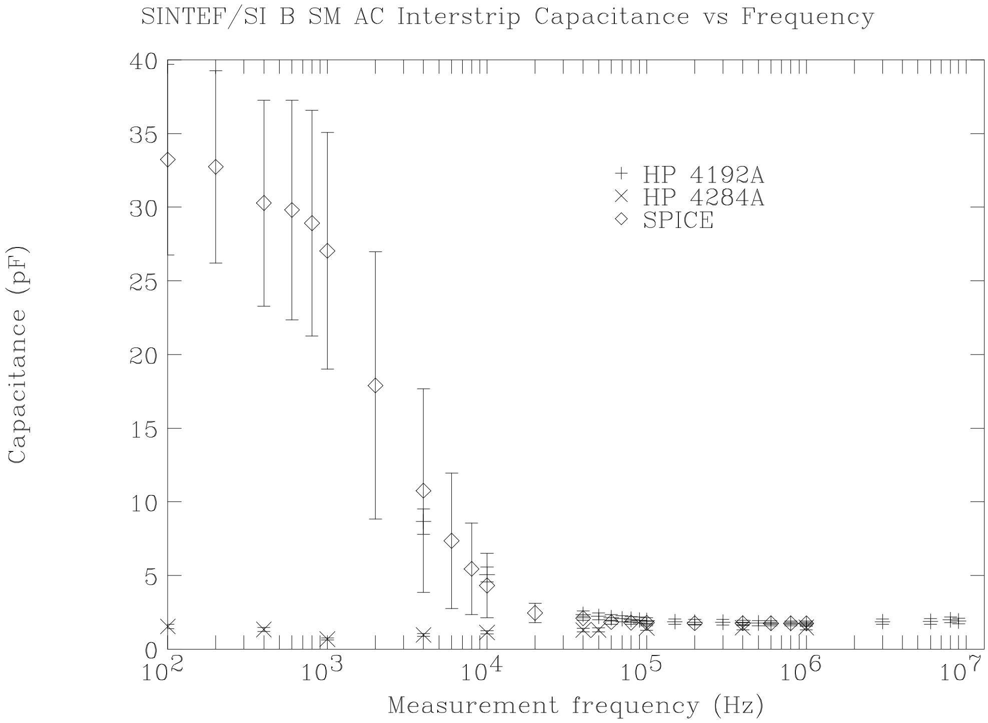

Figure 20: Interstrip capacitance versus measurement frequency for the p-side of the SINTEF/SI SVX II prototype type B detector. The backplane contribution, $C_{\text{backplane}}^{p-\text{side}}$, is included in this measurement. Note that the HP 4192A Low Frequency Impedance Analyzer and SPICE simulations are consistent above 10^3 Hz while the HP 4284A Precision LCR meter approaches agreement at 1 MHz. This effect is discussed in Section A.3.

following pathways between the meter and power supply returns:

- The third wire (ground) contact on the Keithley 237 and HP 4192A or HP 4284A AC power cords.
- The IEEE488 bus (a custom cable without pin 12 — earth ground — may be prepared).
- The earth ground and system ground shorting bar on the Keithley 237 rear panel.
- Shielding on coaxial cables between the probe chuck, bias isolation network, and bias distribution network.
- The low potential and low current inputs and system ground of the HP 4284A.

This last ground loop may be eliminated by substituting another measuring device for the HP 4284A which supports fully isolated (or floating) inputs, such as the HP 4192A Low Frequency Impedance Analyzer (5 Hz – 13 MHz) or the Keithley 590 Capacitance meter (100 kHz and/or 1 MHz options) [27]. [12]

For the measurements described in this paper, comparison between the HP 4284A and HP 4192A indicate good agreement for bulk, coupling and total capacitance with respect to ground at a wide range of frequencies. For reasons that are understood, the measurements of the HP 4284A are generally poor and lack stability with respect to the HP 4192A (and SPICE simulations) for interstrip and overlap capacitance (C_{12}) though there is generally substantial agreement at 1 MHz. (The HP 4192A and HP 4284A measurements and the SPICE simulation are compared for an interstrip capacitance measurement in Figure 20.) This is to be expected as the HP 4284A lacks the abovementioned floating inputs; it was designed for the measurement of discrete electrical components instead of measurements of semiconductor devices.

The resistivity of the bulk silicon and any trapped surface charges determine the ultimate isolation between the power supply and LCR meter returns once all other paths have been eliminated.

B Protocols

B.1 General Preparation for Capacitance Measurements

The following list indicates preparation of the necessary probe station and associated equipment for capacitance measurements:

1. Adapt the probe station for microscope viewing over a large area:

[12] Each of the meters described above will generally have a unique IEEE 488.2 bus command set necessitating the use of appropriate data acquisition software.

- Remove the microscope from $x - y$ stage on probe station.
- Swing the Olympus stereo microscope over the vacuum chuck.

2. HP 4192A Low Frequency Impedance Analyzer:
   - Turn the power on.
   - Allow unit to warm up for 60 minutes or more.
   - Select **LOCAL** mode (for manual measurement taking).
   - Select INTernal **TRIGGER** (for manual measurement taking).
   - Select C mode for **DISPLAY A**.
   - Select D mode for **DISPLAY B**.
   - Select parallel **CIRCUIT MODE**.
   - Check that 1 m extension switch is on.
   - Attach 1 m extension (HP 16048A); connect L_{cur}, L_{pot}, H_{pot}, H_{cur}, and chassis ground to bias isolation network.
   - Select 1 V p-p **OSC LEVEL** signal level.
   - Select the measurement **SPOT** FREQuency (Appendix B.3).
3. HP 4284A precision LCR meter:
   - Turn the power on.
   - Allow unit to warm up for 60 minutes or more.
   - Select **LOCAL MODE** (for manual measurement taking).
   - Select $C_{\text{parallel}} - D$ mode.
   - Check that 2 m extension software option is enabled.
   - Attach 2 m extension (HP 16048D); connect L_{cur}, L_{pot}, H_{pot}, H_{cur}, and chassis ground to bias isolation network.
   - Select 1 V p-p (or higher) signal level.
   - Select the measurement frequency (Appendix B.3).
4. Keithley 237 source/measure unit:
   - Turn power on.
   - Allow unit to warm up for 60 minutes or more.
   - Select **LOCAL MODE** (for manual measurement taking).
   - Select **SOURCE V, MEASURE** I.
   - Set V = 0.0 volts.
   - Set **OPERATE** off.
   - Attach the triaxial cable from the Keithley 237 to the bias distribution network inside the laminar flow hood.

B.2 Capacitance Meter Calibration

The principle function of calibration of the HP 4192A Low Frequency Impedance Analyzer and HP 4284A Precision LCR Meter is to null the effect of any contributions to the measured capacitance due to the extension cable, bias isolation network, and probes that intervene between the meter and the device under test. (Their calibration protocols are described in Appendices B.2.1 and B.2.2, respectively.)

The calibration nulls typically 2.3 pF (in the case of the HP 4192A) and 3 pF (for the HP 4284A) for interstrip and coupling capacitance measurements. The difference arises due to the 1 and 2 meter extensions used with the respective instruments. The effect of calibration for several measurement modes of the HP 4284A is shown in Figure 15.

Typically two calibration measurements are made, one with the low and high potential probe tips in contact, and the other with them separated (the OPEN and SHORT correction method). The sides of the tips are contacted, rather than the tips. After contact is made, one tip is slid back and forth along the other, several times, using the micro-positioner. This will remove excess material and improve contact quality. In the case of a measurement of total capacitance with respect to ground, only one probe (connected to H_{cur} and H_{pot}) is used. In this case the residual capacitance between the LCR meter and the device under test is somewhat lower than for the interstrip and coupling capacitance measurements.

Accordingly, for total capacitance measurements, the calibration protocol is modified. The low potential probe is replaced by one of the built-in probes of the underside probing chuck (with detector removed). The high potential probe is moved into contact with the chuck's probe tip for SHORT measurements and moved away (by approximately 1 mm) for OPEN measurements. The sides of the two probe tips are contacted. It is recommended to slide one tip along the other several times using the micro-positioner. [13] The Keithley 237 Source/Measure Unit (the power supply) is set to 0 V in OPERATE mode to assure that the grounding is identical to that during normal operation.

B.2.1 HP 4192A Calibration

The HP 4192A has an OPEN/SHORT calibration for a single ("spot") frequency. As such, this feature is not useful for frequency sweeps since the contribution from probes and fixturing is in general frequency dependent. Accordingly, we employ the following calibration procedure wherein a standard 4.7 pF mica capacitor is used to establish a reference standard:

1. Turn off OPEN/SHORT correction.
2. Select $C_{\mathrm{parallel}} - D$ mode.
3. Measure 4.7 pF capacitor over the range 5 Hz – 13 MHz on HP 16047A fixture to obtain the standard reference.

[13] Alternatively, a small, clean, brass plate may be prepared and vacuum attached to the probe chuck as one would a sensor (it has similar dimensions). The chuck's probes are then landed on the lower surface of the brass in the usual way. The SHORT data are taken by landing the high potential probe on the top of the brass plate. The OPEN data are taken by raising the probe tip until contact with the plate is broken.

4. Measure 4.7 pF capacitor over the range 5 Hz – 13 MHz on probe station.
5. Subtract (3) from (4) to form pedestal table.
6. Measure capacitance versus frequency of the device under test.
7. Subtract pedestal from measurement made above.

B.2.2 HP 4284A Calibration

The HP 4284A Precision LCR meter has a feature to compensate for sources of constant parasitic capacitance. The following is a variation of the standard procedure, modified in accord with the particulars of fixturing and probing double–sided detectors. As in the standard procedure, the OPEN correction accounts for stray admittance, and the SHORT correction compensates for residual impedance of the test fixture. [14] These corrections are used together for high precision measurements.

Option 006 for the HP 4284A is a firmware correction for the phase shift error caused by using 2 m and 4 m leads. It is recommended that the shortest possible extension be used and that the appropriate length correction be applied.

Performing the OPEN/SHORT calibration of HP 4284A:

1. Attach all high voltage, ground and other leads to the probe station chuck and underside probe chuck. [15]
2. Place brass shorting plate on underside probe chuck (or conductive rubber) as one would mount a detector. The bare brass faces down. Apply vacuum.
3. Land probes in the usual manner if using underside probe chuck. (Use a single probe attached to the high potential terminal of the bias isolation network for total capacitance measurements.)
4. Verify less than 1 Ω contact resistance between LEMOs 1 & 2 as labeled on the chuck to confirm underside probe contact.
5. Mount low parasitic capacitance probes in micro-positioners.
6. Attach probes to bias isolation network using LEMO connectors.
7. Land capacitance probes in small uncovered area on top of shorting plate.
8. Verify less than 1 Ω total contact resistance through both probes to confirm topside probe contact.
9. Close switch S_1 on front of bias isolation network.
10. Set 0 V bias voltage on Keithley 237 (current should be $\approx$ 0 A).
11. Select **OPERATE** on Keithley 237.

[14] See Table 6-2 on page 6-16 of [32]. A further LOAD correction feature is not used.

[15] These are sources of parasitic capacitance. Having them present and connected allows them to be compensated by the OPEN/SHORT procedure.

12. Perform HP 4284A SHORT procedure:
    - Press **MEAS SETUP**.
    - Press **CORRECTION**.
    - Confirm selection of **CABLE : 2M** (change if necessary).
    - Select **SHORT: ON**.
    - Press **MEAS SHORT** (test takes several minutes).
13. Perform HP 4284A OPEN procedure:
    - Raise low parasitic capacitance probe tips by $\approx$ 0.5 mm.
    - Press **MEAS SETUP** (if not already selected).
    - Press **CORRECTION** (if not already selected).
    - Select **OPEN : ON**.
    - Press **MEAS OPEN** (test takes several minutes).
14. Press **DISPLAY FORMAT** to return to measurement mode.
15. Lower probes on underside probing chuck.
16. Close vacuum path to chuck and remove shorting plate.

B.3 Measurement Frequency Selection

The measurement frequency may be set by the data-taking software or manually:

Select HP 4192A measurement frequency (5 Hz – 13 MHz):

1. Press **Spot Freq** button.
2. Use the numeric keypad to enter the measurement frequency.
3. Press the **Hz, kHz** or **MHz** button, as appropriate.

Select the HP 4284A measurement frequency (20 Hz – 1 MHz):

1. Press **DISPLAY FORMAT**.
2. Move cursor until **FREQ :** is highlighted.
3. Use up and down arrow keys to select desired frequency, or use keypad, followed by the **Hz, kHz** or **MHz** softkey, as appropriate, to enter frequency.

B.4 Identification of Adjacent Interleaved Strips

The determination of accurate interstrip capacitance measurements requires contact to the DC pads of adjoining strips. The bias connections for the odd- and eve-numbered strips of the SINTEF/SI DS641/640 and SVX II prototype [17] detectors are interleaved, with polysilicon bias resistors feeding alternate strips from opposite ends. Accordingly, the DC pads for adjacent strips lie on opposite sides of the detector. Beyond a single point feature located every 16 pads the strips of the DS641/640 are not marked or numbered. (SINTEF/SI SVX II prototype detectors have every sixteenth strip numbered on the p-sides and on the n-sides for the double–metal geometry.) It is therefore desirable to have a means to reliably identify a pair of neighboring strips and to mark them appropriately. This procedure is described below.

Determination and marking of location of (unlabeled) adjacent strips:

1. Mount double–sided vacuum chuck on probe station's $x - y$ stage.
2. Mount detector on double–sided vacuum chuck.
3. Choose a reference strip, one of the pair you will measure.
4. Approximately center the midpoint of the reference strip on $x - y$ stage.
5. Square $x - y$ stage and detector:
   - Locate the end of a reference strip on the detector.
   - Lower a probe tip to within a few mils of this strip.
     (Do *not* contact the surface.)
   - Move the stage in the direction (x or y; turning a single control) most parallel to strip.
   - Rotate the chuck on the stage until the strip is approximately parallel on one axis of the $x - y$ stage. Repeat as necessary.
   - A: Continue the parallel motion while observing the probe tip through the microscope, moving from the center of the reference strip to one end.
   - B: Count the number, N, of strips that cross the reference probe position as you move toward the opposite end of the reference strip.
   - C: Rotate stage back toward the reference strip until half ($N/2$) of the strips have been crossed.
   - D: Reverse direction toward opposite side and repeat (B) and (C).
   - F: Iterate (A) - (D) until the deviation along reference strip is less than pitch/4 over the entire length of the strip.
   - The reference probe tip now serves as a marker of both ends of the reference strip, and the detector is squared on the $x - y$ stage.
6. Using a second micro-positioner and probe tip make a *small* mark below (or above) the reference strip on the bias ring. Do not cut the ring.
7. Move the detector parallel to the reference strip until you reach the opposite edge of the detector. Use the reference probe to visually "track" the reference strip during the traversal.
8. Using the second micro-positioner and probe tip make a second *small* mark above (or below) the reference strip on the bias ring.

   Mark the opposite end of the very same strip as in (3).

9. Move the stage parallel to the reference strip back to the opposite side and confirm that you have marked both ends of the *same* strip.

B.5 Probe Tip Preparation

The capacitance measurements described in this paper are sensitive to the contact quality between the probe and the pad(s) on the detector under test. Instabilities (fluctuating, occasionally negative readings) in interstrip, coupling, and total capacitance were sometimes traced to this cause. Probing of features of dimension 25 μm and below is facilitated by having sharp, stiff and clean tips — qualities degraded with use. The tip tends to collect loose material from the surface of the detector, necessitating sharpening or replacement. We generally choose sharpening since it takes less time, particularly in the case of tips integrated into other devices, for example the underside probing chuck and low parasitic capacitance probes.

The following procedure produces a tip with better than factory specifications. This procedure removes material from the probe tip; no more than twenty-five cleanings should be performed before replacement. The schematic diagram for the etching device is shown in Figure 21.

Procedure for cleaning and sharpening of probe tips using electrochemical etching:

- Line the bottom of the 10 ml Pyrex beaker with a layer of NaOH pellets.
- Fill the beaker to 3/4 capacity with distilled water.
- Dissolve the NaOH pellets with ultrasonic cleaner.
- Place the beaker into etching machine.
- Insert the loop electrode into banana plug and into beaker.
- Insert the probe tip into 0.078 inch diameter probe arm as necessary.
- Insert the probe tip several mm below the surface of the NaOH.
- Fix the probe arm with etcher clamp.
- Ground the probe tip to the etcher chassis as necessary. (Use LEMO connector for low parasitic capacitance probes.)
- Select "DC" and "low" switch positions on front panel.
- Apply DC current to the probe tip for several seconds. Observe bubbling in region of probe tip to gauge the rate. Each application accomplishes substantial sharpening.
- Remove probe. First rinse in distilled H_2O, then in ethyl alcohol for rapid drying.
- Inspect the tip under microscope when dry. If necessary, repeat etching until satisfactory sharpness is achieved.
- Remove and rinse loop electrode.
- Cover beaker with glass top to prevent evaporation.

One beaker will suffice for hundreds of etchings. The formation of a dark residue on the bottom of the beaker does not seem to affect etching time or quality.

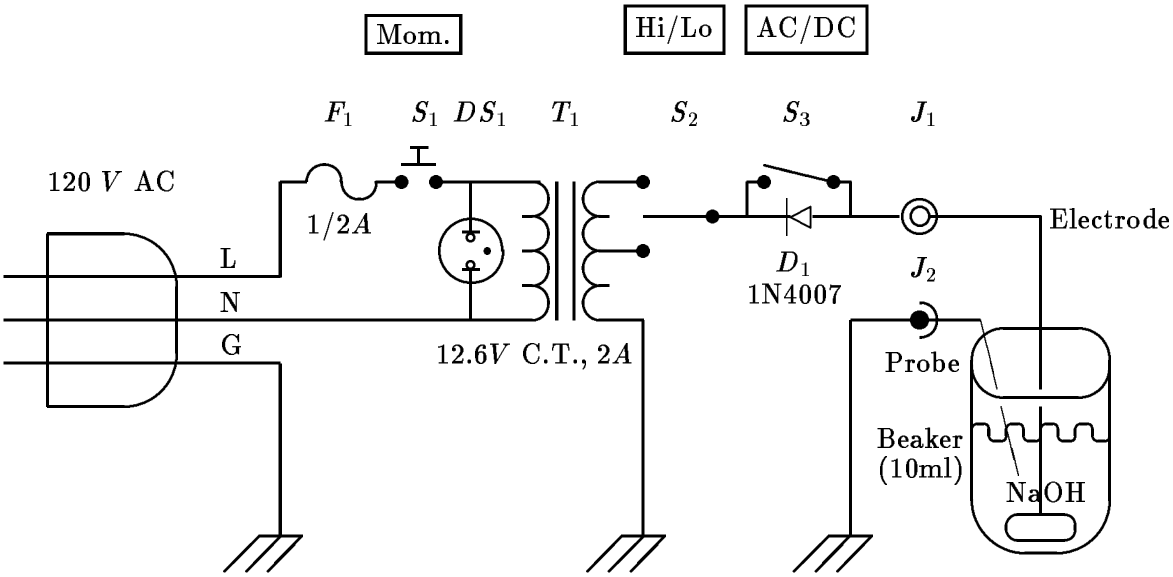

Figure 21: Probe tip etching power supply.

Table 11: Probe tip etcher components. See Figure 21 for a schematic diagram.

Part	Description	value	unit	rating
D_1	1N4007 Power Diode	1k	PIV	1 A
DS_1	Neon bulb (and $\approx$ 0.5M Ω resistor)	125	V	—
F_1	Fuse	0.5	A	250 V
J_1	Subminiature banana connector	250	V	—
J_2	LEMO connector	250	V	—
S_1	Momentary contact switch	—	—	250 V
S_2	Single pole double throw switch	—	—	250 V
S_3	Single pole single throw switch	—	—	250 V
T_1	Center tap transformer	12.6	V	2 A