R. Hughes
XFT Mini-Review
DAQ Upgrade Meeting
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XFTII Overview

<u>XFTII Group:</u>

Fermilab:	Finder/Linker/Backplane/Cabling
	Jim Freeman
	Scott Holm
	Terri Shaw
	Tom Wesson
	Intae Yu
Johns Hopkins:	TDC Mezzananine Board
	Zhong Feng
	David Gerdes
	Joao Guimaraes da Costa
	Amy Rosenberg
Ohio State:	Finder/Linker/simulation
	John Hoftiezer
	Richard Hughes
	Mark Johnson
	Phillip Koehn
	Brian Winer
Rochester:	Simulation
	Greg Veramendi

Track Processor Specifications:

- High efficiency for tracks with $P_T \geq 1.5GeV/c$

  Eff $\geq$ 96%

- Must have good momentum resolution

  $\Delta P_T/P_T^2 \;\leq\; 2.0$ (%/GeV/c)

  Allows sharp threshold for high-Pt physics

- Must find tracks in time for the Level 1 decision

  Level 1 processing time $5.5\mu sec$

  Tracks needed about halfway through

- Must have low fake rate, since fakes tend to grow with luminosity

- Must have ϕ_0 resolution adequate for Silicon Vertex Trigger

  $\phi_0 \leq 8m$Radians

- Must operate well for chamber wire efficiency $\geq$ 92%

- Must operate well for luminoisities up to $10^{33}cm^{-2}sec^{-1}$.

	Specification	Simulation
Track finding efficiency	$\geq$ 96%	97%
Momentum resolution ($P_t \geq 3.0$)	$\leq 2.0\%/GeV/c$	$0.8 - 0.9\%/GeV/c$
ϕ_0 resolution	$\leq$ 8mR	$3.0 - 7.0$mR
μ Trigger rate (@10 GeV/c)	$\leq 50Hz$	$30Hz$
Fake Fraction (@10 GeV/c)	$\leq$ 50%	$1 - 2\%$

Table 1: Comparison of XFT specifications vs results obtained from simulation.

Global Algorithm Description:

- Takes hit data from Tracker TDC
- Hit data is binned.
  For 115 nsec max drift:
  - Prompt bin 0-43 nsec window
  - Delayed bin 44-121 nsec window
  - Logic to reject long Prompt hits in the Delayed window.
- Finder:
  - Operates on hit data
  - Identifies track segments ($P_T \geq 1.5$) in all 4 axial superlayers
  - Outputs pixel position of track segment
  - 12 pixels/cell in Layers 1,2
  - 6 pixels/cell, 2 slopes/pixel in Layers 3,4
- Linker:
  - Operates on Finder output
  - Identifies tracks with $P_T \geq 1.5\ GeV/c^2$ (one per 1.25°)
  - Outputs track P_T and ϕ
- Track results are sent to XTRP for extrapolation:
  - 7 bits Pt (including sign bit)
  - 3 bits mini-phi
  - 3 bits code (short track, isolation, reserved)

Finder Algorithm Description:

- Each Finder covers 4 adjacent COT cells.
- Total of 68 COT wires needed on input:
  the 4*12 wires for each of the 4 cells
  plus 2*10 neighbor wires.
- Finder stores patterns for only one cell. Remaining 3 cells are multiplexed.
- Store *all* patterns of wires needed to find every segment from tracks with $P_T \geq 1.5\ GeV/c$.
- Allow up to 3 misses (programmable)
- $\sim$ 100% segment finding efficiency
- Each Finder reports pixel position of all segments found (with $P_T \geq 1.5\ GeV/c$).
  48 bits output per Finder per 132 nsec.

The expected efficiency for track finding depends on the expected wire efficiency.

Example:
For wire efficiency of 99.0%,

- Allowing 1 miss in the Finder patterns
- Segment finding efficiency = 99.4%
- Track finding efficiency = 97.6%

Example:
For wire efficiency of 92.0%,

- Allowing 3 misses in the Finder patterns
- Segment finding efficiency = 98.8%
- Track finding efficiency = 95.3%

(assuming no holes in finder patterns, linker roads)

Linker Algorithm Description:

- Works off of Finder segment info
- 288 total Linkers, each covering 1.25 degrees
- Road is defined as the pixel/slope locations on all 4 axial layers for tracks with $P_t \geq 1.5\ GeV/c^2$
- Total number of roads needed/Linker is $\sim$ 2900
- Total input pixels/Linker from 4 COT axial layers is 212
- Output for each Linker is the best (highest) P_T track in that ϕ slice.
- If no track passing through all 4 layers is found, best track in layers 1,2,3 is reported.

Number of Masks/SL:

Layer	Number of Masks
1	170
2	230
3	282
4	339

Number of Roads

Pixels 1,2	Pixels 3,4	Number of Roads
6	6	1290
12	6*(2 slopes)	2419
6*(2 slopes)	12	2937
12	12	4853

XFTII Simulation:

- Functional XFT simulation is implemented using VAX-Fortran

  FINDER masks stored in a database

  LINKER roads stored in a database

- Remaining parts of algorithm are written to match how we implement them in the chip.

- Using 2 simulation methods for COT:

  - Standalone simulation used for COT.

    Geometry is implemented

    Distribution with 40nsec mean, 20nsec width used for pulse-width.

  - Full CDFSIM used for COT.

    "Standard" Run II geometry database.

    Use standard CDF code for pulse-width modelling, etc.

Events used for Standalone simulation studies:

- For all studies described below, used Run 1A data sample of Level 1 muon triggers (no CFT bias). Used offline reconstructed tracks from this sample, not hit data. (Did not try to map CTC hits onto COT geometry).
- Overlayed on top of this hit data from minimum bias events from Monte Carlo.
- For Luminosity of 2E32, use mean number of interactions/crossing of 2
- For Luminosity of 1E33, use mean number of interactions/crossing of 10
- Varied COT wire efficiency from 0.99 to 0.92 (varied number of allowed misses accordingly).

Performance:

- Momentum resolution
- Muon trigger rate vs P_T
- Fake track rate vs P_T

These are studied vs imbedded minimum bias events.

Muon Trigger Rates

- Only done using Standalone COT simulation (so far).
- Use 10 μb cross section for CMP confirmed CMU.
- Increase expected rate for Run II by factor of 1.3 for increased coverage.

XFT track finding efficiency for muon triggers associated with a real offline track:

- With $P_T^{offline} \geq 1.5\ GeV/c$,
  efficiency = $(96.5 \pm 0.7)\%$

Standalone XFTII simulation results

No "or"ing Mask set
2 time bins
64 bin roads

Min Bias	Hit Eff.	Mu Rate	% fakes(Mu) $P_T \geq 5$	%fakes(all) $P_T \geq 5$	P_T Res (%GeV/c)	Phi Res (mRad)	Eff
2	99%	27.4	1.2%	1.3%	0.78	2.28	96.1%
2	92%	23.1	0.0%	3.2%	1.03	3.11	95.9%
10	99%	137.2	1.3%	2.0%	0.92	2.74	96.7%
10	92%	151.7	3.8%	34.3%	1.23	4.16	96.5%

Standalone XFTII simulation results (continued)

- 64 P_T Bin road set:
  - each P_T bin equally spaced in curvature.

- 48 P_T Bin road set:
  - 16 Lower P_T bins are twice as wide (in curvature) as the 32 Higher P_T bins.
  - The boundary is at $\sim 3\ GeV/c$.

bins	all Pt	0-3 GeV	3-5 GeV	$\geq$ 5 GeV
all tracks:				
48	1.03 (.01)	1.04 (.01)	.80 (.04)	.92 (.14)
64	0.87 (.01)	0.87 (.01)	.80 (.04)	.92 (.14)
Mu tracks:				
48	0.89 (.03)	0.93 (.04)	.70 (.05)	1.07 (.38)
64	0.78 (.02)	0.78 (.03)	.70 (.05)	1.06 (.38)

Detailed Presentations To Follow:

- Hardware Overview - Terri Shaw
- TDC Mezzanine Board - Dave Gerdes
- Finder Chip Status - Scott Holm
- Linker Chip Status - Brian Winer