THE INTERPLAY OF SURFACE MOUNT SOLDER JOINT QUALITY AND RELIABILITY OF LOW VOLUME SMAS

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Abstuact

Spacecraft electronics including those used at the Jet Propulsion Laboratory (JPL), denrand production of highly reliable assemblies. JPL has recently completed an extensive study, funded by NASA's code Q, of the interplay between nanufacturing defects and reliability of ball grid array @GA) and srn face mount electronic components.

More than 400 hundred test vehicles were assembled using ceramic and plastic BGAs, LCCs, J-leads, and gull wing components. These were subjected to thermal cycle testing and solder joint defects were logged prior to testing and solder damage propagation over time was documented. These findings offer valuable information to designers and quality assurance personnel alike on package robustness as well as in better understanding the defects that can actually lead to failure.

Objectives

NASA Headquarters, code Q, has established an Electronic Packaging and Assembly Program to address the common needs of NASA programs. Oneof these programs funded during 1993 -1995 focused on the use of SMT for high reliability, Ultra Low Volume (ULV) spacecraft electronics as used in the NASA community. The other funded during 1994-1996 concentrated on evaluation of quality and reliability of Ball Grid Arrays.

Aspects of SMT technology were carried out by four RTOPs (Research & Technology Objectives & Plans) at NASA's Jet Propulsion Laboratory. These RTOP's are interdependent and were conducted concurrently. Each RTOP concentrated its efforts on a particular aspect of the design, modeling, manufacturing, test, and deployment (aging) cycle. The primary objectives of the RTOPs were as follows:

- Identify the critical parameters of SM'f manufacture. Determine the methods and tools required to integrate QA procedures into the design and manufacturing processes so that the critical parameters can be bounded and controlled.
- Develop a thorough understanding of the creep-fatigue mechanism underlying solder joint failures of surface mount electronic packaging systems. Develop generic, broadly applicable design guidelines, analysis methodologies, and data requirements.
- Develop an assembly level qualification test methodology for surface mount technology and apply this methodology to electronic packaging systems through the use of experimental design techniques and phased experimentation.
- Disseminate NASA Guidelines for SMT, developed from the knowledge gained from the JPL RTOPs, as well as the efforts of other NASA centers, industry knowledge centers, and industry partners.

References 1-9 document some of activities performed in the SMf RTOP areas. In conjunction with the RTOPs, a survey and a series of Phase 1 and Phase 2 cooperative test program involving all RTOPs were performed. Results of the survey and Phase 1 and Phase 2 test programs with emphasis on the Qual it y Assurance efforts are presented.

The objectives of the Ball Grid Array project are to demonstrate the robustness, quality and reliability of BGA technology, and to assist in tbe development of the rapidly growing industrial infrastructure for this technology. BGAs are electronic packages used for higher I/O (Input/Output) counts that also provide improved electrical and thermal performance and better manufacturing and ease of handling compare to the conventional Surface Mount (SMT) leaded parts.

Tomeet requirements of NASA community, including JP1., for highl y reliable assemblies in an Ultra-Low Volume (UL V) environment, an integrated system approach was used. The focus included identification of BGAs' critical manufacturing parameters, evaluation and development of inspect ion techniques, and determination of tlie effects of manufacturing defects on solder joint reliability. The Quality Assurance (QA) procedures developed will be then integrated into design and manufacturing so that critical parameters can be bounded and controlled.

JPL solicited industrial, academic and other related consortia to work together to leverage their resources and expertise into a synergistic cooperative effort. All participants furnished in-kind contributions. The wide industrial use of BGA technology will afford NASA as well as consortium industries inexpensive access to this technology and support miniaturization thrusts for their next generation applications.

The consortium objectives are to complete characterization of BGAs in the following areas:

- Processing/assembling Printed Wiring Beads (PWBs) using BGAs. Variables include PWB's material types and surface finishes, and use of ceramic and plastic packages with different balls populations and I/Os.
- Inspection and Quality Assurance (QA) methods for ascertaining the process controls, acceptance methodologies, and final quality of BGA assemblies. Characterization of package properties such as coplanarity, inspection for solder joint quality, damage progress recording during environmental exposure, and defect/reliability correlations as well as estimations of life of solder joints.
- investigating the reliability of BGAs' assemblies in several different environments (thermal and dynamic).

A large number of variables inside the design, manufacturing anrf test of the test vehicles (TVs) were statistically toggled using a Design of Experiment

(DoE) technique to determine the influence and criticality of these variables. References 10-12 document some of the activities on the BGA Program.

SMT- Conventional Components

SMT Survey

NASA centers involved with SMT were surveyed in 1993 (Reference 1). One section of the survey addresses QA issues for SMT hardware. The objectives of the SMT QA survey were to identify the critical parameters of the SMT manufacture and to determine the methods and tools presently used by industry to identify and control them. It was concluded that the leading causes of SMT rejects were solderability and solder paste deposition problems. Some operations did not have corrective action feedback loops to change a design or process even when data indicated a problem.

Phase 1 Test Program

The Phase 1 test involved the use of a single ceramic component, 0.050 inch pitch) soldered to an epoxy-fiberglass FR-4 board (Reference 4). LCCs, J. lead cerquads, and gull wing cerquads were the SMT components. The JPL SMT Training Facility assembled 20 and the Electronics Manufacturing Productivity Facility (EMPF) in Indianapolis, Indiana assembled 205 test boards.

Thermomechanical cycle testing (-55°C to 100"C, 45 minutes dwells and duration of 246 minutes) on Phase 1 assemblies having LCCs, began in August, 1993. All LCC assemblies have failed (open circuit). Two-parameter Weibull equations were used to characterize failure distribution (Figure 1). Phase 1 testing of the J-leads was initiated in January, 1994, and now (October 1996) has reached more than 3,000 cycles with no failure, Testing of the gull wing cerquads started in July, 1994, and they have now accumulated more than 3,000 cycles with numerous failures with the first failure at 1,720 cycles.

All Phase 1 assemblies were inspected prior to thermal cycling, and have been, or will be, periodically inspected as they are cycled to electrical (solder joint) failure. Conflation between manufacturing defects, dimensional characteristics, inspection observations and life of the solder joint have been analyzed for the failed LCCs and is presented (Figure 2). The figure shows an approach that tracks damage growth of individual solder joints and graphs damage accumulation for solder joints with specific manufacturing defect categories. Solder joints with a higher defect category showed earlier signs of damage growth as well as accounting for higher failed joint percentages.

Since JPL and organizations surveyed are using visual inspection for acceptance/rejection of solder joints, we also used this technique. To selectively validate observations we utilized other more powerful visual aids including SEM and cross-sectional microscopic evaluation. Crack initiation and propagation over time were documented using visual inspection and/or SEM (Reference 7).

Two methods were developed for ease of inspection data visualization and trends identification. In the first method (Reference 8 and 9), inspection data were displayed in an innovative graph representation that allows instant visualization of damage progress levels and correlation to pin locations. In the second method, the damage that progressed over time was plotted for a group of leads that had the same category of manufacturing defect. These methods could be adapted for use with other type of data, and other graphical display methods for ease of data visualization and trend recognition,

Phase 2 Test Program

Phase 2 used several different types of packages similar to phase 1 as well as capacitors and resistors on a polyimide board. The overall purpose of the Phase 2 testing was to perform statistically significant testing of surface mount assemblies to better understand the failure modes and inherent fatigue life of the solder interconnect, and to continue development of tailored qualification methods. Critical SMT manufacture parameters were controlled to determine their effects and to further develop QA methodologies. Design of Experiment (DOE) test methodology was utilized to meet these objectives. The DOE was a hybrid of full factorial and partial factorial approaches. The majority of environmental testing will consist of flight-like thermal cycling, i.e., thermal cycling within a vacuum environment.

Extensive planning and coordination were required to implement the DOE requirements in a manufacturing environment. A total of 33 test boards with over 3,000 components that included about 600 LCCs, J-leads, and fine pitch gull wings were assembled at Lockheed-Martin, Sunnyvale, California. One test vehicle was assembled at the JPL SMT Training Facility Center for electrical and thermal characterization and validation.

For ease of manufacturing flow, the boards were divided into six groups, each differing by at least one variable. Variables included tinning for J-leads and LCCs, reflow profile for the board assembly, and lead height for the fine pitch gull wings. Also, prior to assembly, J-leads and LCC packages were tinned manually by dipping in a molten solder pot. There were no solder defects when the LCCs were tinned (4 times -- once for each side); however, occasional ceramic lid debonding did recur.

After solder paste application and package placement, thirty boards were mass reflowed using standard and three using a modified reflow profile. Modification of the profile was made by rapid cooling of the assembly just after solder solidification to produce a representative of a hand soldering condition.

Assemblies were visually inspected at JPL for solder joint manufacturing defect and one or more defect codes were assigned. For ease of visualization and trend identification, inspection data was graphed in three-dimensional plots and conversion to rare defect type occurrences were identified for package types and assembly locations (Figure 3-4). In addition, gull wings of four test vehicles were reworked as a part of the DOE test plan even though they did not have defects, Two gull wings were reworked by removing and replacing the solder while the refraining six had the ten corner solder joints reworked, These assemblies are being subjected to thermal cycling exposure per DOE requirements to determine the effects of these variable on reliability.

Solderability of gull wing lead remnants were evaluated for comparison to gull wing manufacturing defect. The dip-and-look qualitative test method was used at the vendor site and a quantitative Multicore Universal Solderability Tester (MUST) that measures wetting force was used at JPL. The vendor tested about twenty and JPL tested approximately 500 strips of leads. Leads were held in place by a plastic strip in bundles of 41 and 64 leads representing a side of 164 and 256 gull wing packages, respectively. Results of visual inspection, dip-and-look, and MUST print-out data were compared for 164 and 256 gull win packages. Based on the dip-and-look test results, all of the 164 and most of the 256 gull wing leads failed solderability testing. Results of solder joint assembly inspection contradict the dip-and-look test results for the 164 gull wing leads whereas they agree with results of the of 256 leads.

SMT Test Results

Phase - LCC Solder Joint Manufacturing Defects

Table 1 lists summary defects observed for LCC assemblies during the manufacturing inspections prior to thermal cycling. This Table also includes defect codes used for Phase 1 testing that include other packages, e.g. cork 29 for gull wing, as well as those generally used for crack propagation mapping (codes 13 to 20).

Table 1. Defect Codes and Types for identification of Solder Joint Quality

Defect Code/Type		68 LCC	28 LCC	20 LCC	Defect Code/Type		68 LCC	28 LCC	20 LCC
1	NO MFG DEFECT	138	107	32	21	SOLDER BRIDGE	0	6	0
2	SOLDER BALLS	23	33	0	22	GRAINY SOLDER	1429	1866	90
3	DEWETTING	0	0	0	23	LUMPY SOLDER	9	66	4
4	NON-WETTING	0	2	0	24	STRETCH MARKS	10	131	3
5	INCLUSION	0	5	0	25	BOARD CONTAMINATION	623	364	20
6	VOID	3	0	0	26	INSUFFICIENT TINNING	0	2	0
7	ICICLES	7	2	0	27	LEAD SOLDERED TO BODY	0	0	0
8	INSUFFICIENT SOLDER	401	64	46	28	LEAD TOO HIGH	0	0	0
9	EXCESS SOLDER	0	3	11	29	TOE DOWN	0	0	0
10	NO FILLET	0	0	0	30	LEAD DEFORMED	0	0	0
11	LEAD OVERHANG	0	1	0	31	DAMAGED JOINT	0	0	0
12	CONTAMINATION (ON SOLDER)	477	30	0	32	CONTAMINATION (IN SOLDER)	0	0	0
13	LIGHT STRESS	0	0	0	33	HEEL NO FILLET	0	0	0
14	MODERATE STRESS	0	0	0	34	OPEN	0	0	0
15	HEAVY STRESS	0	0	0	35	LUMP SOLDER ON LEAD	0	0	0
16	POSSIBLE CRACK	0	1	0	36	CYCLING PEEL OFF	0	0	0
17	CRACK @ 25% FEATURE LENGTH		0	0	99	NO CYCLE STRESS DEFECT	0	0	0
18	CRACK @ 50%	0	0	0					
19	CRACK @ 75%	0	0	0					
20	CRACK @ 100%	0	0	0					
Total assemblies*		**24**	**73**	**8**					
Total Joints		1632	2844	160					

* Note: Some of the assemblies fabricated were not inspected and thermally cycled

As the l'able shows, no dewetting or non-wetting was observed. Defects such as icicles, solder bridging, inclusion, void, and light stress defects were extremely rare. The next most commonly occurring significant manufacturing deft'cLs were associated with the improper control of solder paste amount, including observations of excess and lumpy solder joints. Solder joints with excess solder were few while the number of joints with insufficient solder were very high. Solder and board contamination commonly occurred. Grainy solder (defect 22) was the single most frequently observed defect with a percentage of more than the total percentages of solders with other defect types.

Phase 1- Cycles to Failure and Weibull Distribution

Figure 1 shows cycles to failure for 68-, 28-, and 20-pin LCC assemblies. Failures were detected by Anatech® and verified by visual inspection. The failure distribution percentiles were approximated using a median plotting position, Fi= (i-0.3)/((n+ 0.4). As expected, there was a large spread in cycles to failure because of variance in solder joint volume, quality and location. The first failure for the 68-pin LCCs was detected at 53 cycles while the last sample failed after 139 wifb 93 average cycles, 28-pin LCCs failed at much higher cycles in the range of 352 to 908 with 660 average cycles, The 20-pin cycles to failure were in the same range as for those of 28-pins and failed within 57310863 averaging 674 cycles,

If only f Distance from Neutral Points (DNPs) are considered, the 20-pin LCCs should have failed at higher cycles. Cycles to failure is directly proportional to DNP. However, cycles to failure also inversel y depends on the effective solder fillet height. Solder fillet height for 20- and 28-pin LCCs was .021 and .033 inches respectively, which is lower for a 20-pin resulting in higher shear strain for the same CTE mismatch displacement. The difference in part size could have been off-set by the difference in the fillet height.

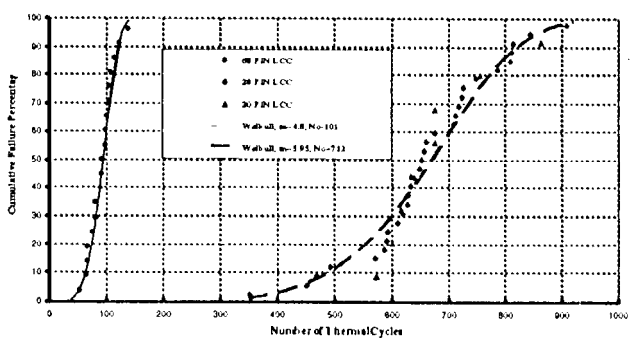


Figure 1. Cumulative Failure Distribution Plots for LCC Assemblies

Often, t wo-parameter Weibul I distribut ions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to fit 68- and 28- pin LCCs' cycles to failure data, The Weibull graphs are plotted in Figure 1 as solid and dash lines for 68- and 28-pins, respectively. For 68-pin LCCs, the scale and shape parameters were 101 cycles and 4.8, respectively. These were 712 cycles and 5.95 for the 28-pin LCCs. Both data sets showed excellent linear correlation in log-log plots with a coefficient of correlation of at least 0.97.

-Manufacturing Defects and Reliability Correlation

The effects of manufacturing defects on solder joint reliability were determined using visual inspection data of I, CC? assemblies. Crack propagation was mapped over time for solder joints with a manufacturi ng defect categories including grainy and insufficient solder joints. Analysis of damage growth enables one to quantitatively define the criticality of each defect category, and based on the results, provide general or specific guidelines for the rejection of manufacturing defects.

Figures 2 show an approach that tracks damage growth of individual solder joints and graphs damage accu mulation for solder joints with specific manufacturing defect categories. Qualitati ve visual damage progress for 20-pin I.CC, were shown. Plots are for those solder joints showing no signs of defect and those with insufficient solder defects. It is clear from these and similar plots for 68-pin I.CCs (Reference 7 and 8), that the solder joints with a nigher defect category showed earlier signs of damage growth as well as accounting for higher failed joint percentages. Similar plots were generated for other 1.CCs.

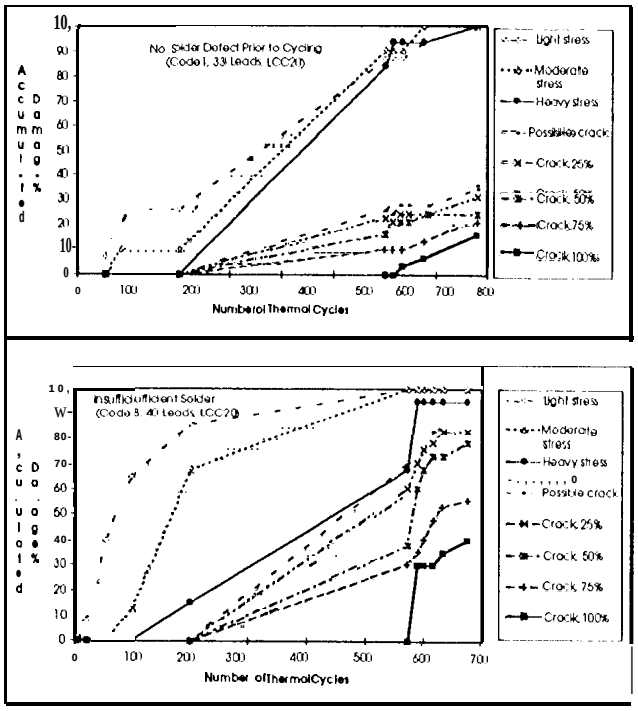


Figure 2. Accumulation of Damages for 68-Pin I.CC Solder Joints With and Without Manufacturing Defects

Phase 2- Solder Joint Manufacturing Defects

Assemblies were visually inspected at 1O-5OX magnification for solder joint quality at JPI, and one or more defect codes were assigned to a joint (defect codes of I'able 1). The total number of defects for the three main categories, i.e., gull wing, J-leads, and I.CCs included:

- 73,211 inspection points for gull wing leads with 16,118 leads showing no signs of defects and the rest showing defects
- 17,243 inspection points for I.CC terminations with 7,991 showing no signs of defects and the rest showing defects
- 13,843 inspection points for J-leads with 4,271 showing no signs of defects and the rest showing defects

It should be noted that the total of inspection points were generally much higher than the total number of solder joint leads/terminations inspected, since often a lead has more than one inspection point (defect type). To visualize data, these were presented in three dimensional plots (Figures 3-4). To generate the z axis percentages, the total number for a defect type was divided by the total number of the inspection points for that package. For example, for 256 gull wings, the total number of lead overhangs were 449. This number was divided by 24,481, the total number of inspection points for this assembly to obtain the defect percentage. Some of the general observations are as follows:

- Leaded packages showed a higher number of defects than I.CC type packages. Fine pitch gull wings showed a higher number of defects than J-leads. The higher values for gull wings were partially attributed to the leads not being straight to start with
- Lead deformed defect for gull wings, lead overhang for J-1eads, and grainy solder for I.CCs were the major contributors to defects
- The defect distribution and number for 164 and 256 gull wing packages were independent of location
- Gull wings with 164 leads showed about a six times higher number of leads with excess solder than the 256 lead gull wings. This is in agreement with solderability test results performed on these leads (1'able 2)
- The 28 J-leads that were located in the center of the printed wiring board snowed much higher number of grainy solder defects than those J-leads at corner areas. This is possibly due to temperature non-uniformity with temperatures reaching higher values at the center during the reflow process

Similar to the Phase 1 Quality Assurance approach, the Phase 2 assemblies will be periodically inspected as they are cycled to electrical (solder joint) failure. Correlations between manufacturing defects, dimensional characteristics, inspection observation.s and the life of the solder joint in different cycling environments (atmosphere and vacuum) and cycling temperature ranges will be analyzed and will be presented in a future paper.

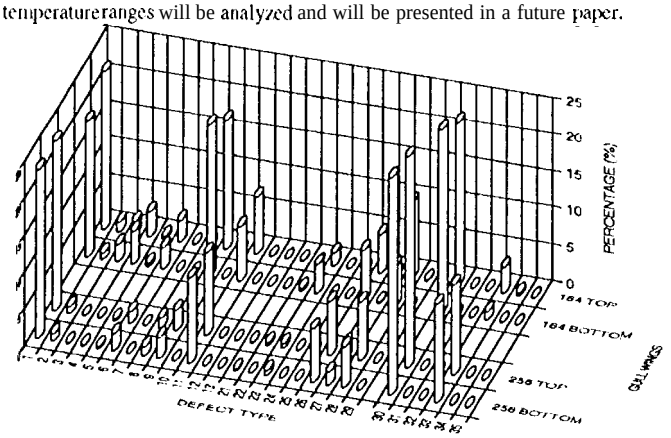


Figure 3. Manufacturing Defects for Fine Pitch Gull Wing

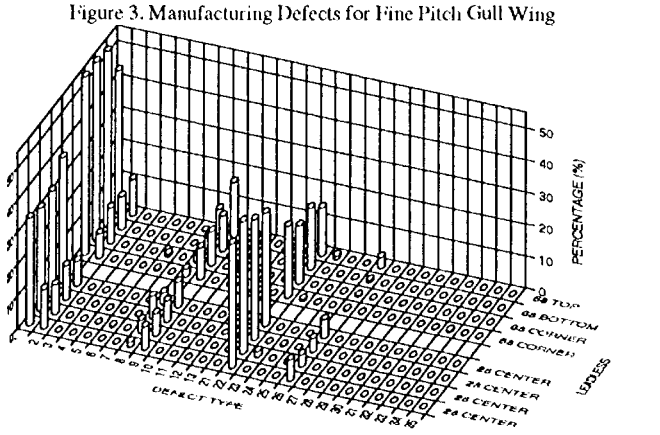


Figure 4. Manufacturing Defects for I.CCs

Ball Grid Array (BGA)

Introduction

The production of surface mount assemblies (SMAs) now surpasses assemblies using through hole technology (THT). In surface mount technology (SMT), components are mounted and terminated directly onto the printed wiring board (PWB) surface. One of the most important component parameters is the lead pitch, which is continuously decreasing to meet the need for higher 1/0 count

The use of fine and ultra fine pitch (FP and UFP) components with less than 0.020 inch pitch is growing, often resulting in more than 200 leads for a single device. Typically, these components have gull wing leads, FP and UFP components, in addition to being extremely delicate and easily damaged during handling, are also difficult to process and are prone to misalignment, anrf rework with the associated reliability implications.

One important emerging technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral array packages (PAP), is BGA. Unlike PAPs, BGAs have balls, covering the entire area, or a large portion of the area, on the bottom of the package.

BGAs offer several distinct advantages over F}' and UFP SMCs having gull wing leads, including:

- BGAs are capable of high pin counts, generally > 200.
- Larger lead pitches, which significantly reduces the manufacturing complexities for high 1/0 parts.
- Higher packaging densities are achievable since the lead envelope for the gull wing leads is not applicable in the case of AAPs; hence, it is possible to mount more packages pcr board.
- Faster circuitry speed than gull wing SMCS because the terminations are much shorter.
- Better heat dissipation than gull wing leaded SMCs.

The BGAs are also robust in processing. This stems from their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing

BGAs, however, are not compatible with multiple solder processing methods and individual solder joints cannot be inspected and reworked using conventional methods. In ultra low volume SMT assembly applications, e.g., NASA's, the ability to inspect the solder joints visually has been standard and is a key factor providing confidence in the solder joint reliability.

Objectives

The objectives of consortium efforts arc to demonstrate the robustness, quality and reliability of AAP technology for space and military applications and to further infrastructure development for this technology

The organizations that have been an integral part of tbc consortium activities are as follows (see Figure 5):

- **Military** sectors- Hughes Missile Systems Company (HMSC) designed Printed Wiring Board (PWB), Boeing Defense and Space Group is performing environmental testing for military applications, and Loral (Lockheed-Martin), Canada, to assemble and test validate the reliability of an additional 200 test vehicles assembled in a military manufacturing facility.

- **Commercial facilities**- Amkor/Anam Electronics, Inc. provided more than 700 plastic packages, Altron Inc. fabricated 300 PWBs, FR-4 and polyimide materials, Celestica, Canada, assembled 200 test vehicles, Electronics Manufacturing Productivity Facility (EMPF) is performing environmental testing, American Micro Devices (AMD) provided resistive die, IBM provided ceramic packages at a minimum charge, Nicolet assisted in X-ray, and View Engineering measured coplanarity and warpage of packages using their 3-D laser scanning equipment.

- **Infrastructure**- Interconnection Technology Research Institute (ITRI) established by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) has provided a vehicle for collaboration among the various sectors of electronic interconnection indu.skies.

- **Academia**- Rochester Institute of Technology (RIT) assembled 35 test vehicles. More than 20 industrial advisors including people from JPL helping to redirect the RIT metal manufacturing laboratory into a Computer Integrated Electronics Manufacturing (CIEM) facility to better meet the current national dentand for electronics manufacturing engineers.

The consortium objectives are to complete characterization of BGAs in the following areas:

- Processing/assembling Printed Wiring Boards (PWBs) using BGAs. Variables include PWB's material types and srrt-face finishes, ceramic and plastic packages with different balls populations and 1/0s.

- Inspect ion and Quality Assurance (QA) methods for ascertaining the process controls, acceptance methodologies, and final quality of BGA assemblies. Characterization of package properties such as coplanarity, indirection for solder joint quality, damage progress recording during environmental exposure, and defect/reliability correlations as well as estimations of the life of solder joints.

- Investigating the reliability of BGAs' assemblies in several different environments (thermal and dynamic).

A large number of variables in.side the design, manufacturing and test of the test vehicles (TVs) were statistically toggled using a Design of Experiment (DoE) technique to determine the influence and criticality of these variables. Each test vehicle has four BGA packages that are in the "300" and "600" I/Os categories. Two sites were used for assembling of TVs:

- Celestica, IBM/Canada, a commercial contract facility with extensive experience, and,
- RIT, a university with no experience in assembling BGAs.

University laboratories are participating in assembling of advanced electronic parts for use in NASA's missions.

After process optimization and assembling of 20 trial TVs, a total of 200 additional TVs were assembled (about 170 by Celestica and 30 by RIT) and were. subjected to various types of inspections including X-ray and scanning electron microscopy prior to environmental exposure. Figure 6 snows photographs of the two test vehicle assemblies, where, unassembled packages are placed on the top of assemb le ones. There two types of TVs::

- Type 1, ceramic and plastic BOA packages with nearly "300" 1/0s, and,
- Type 2, ceramic and plastic BGA packages with nearly "600" 1/0s. Also, a 256 leaded and a 256 plastic BGA packages for direct manufacturing robustness and reliability comparison.

Package configurations include: full array population, peripheral configuration, and depopulated type.

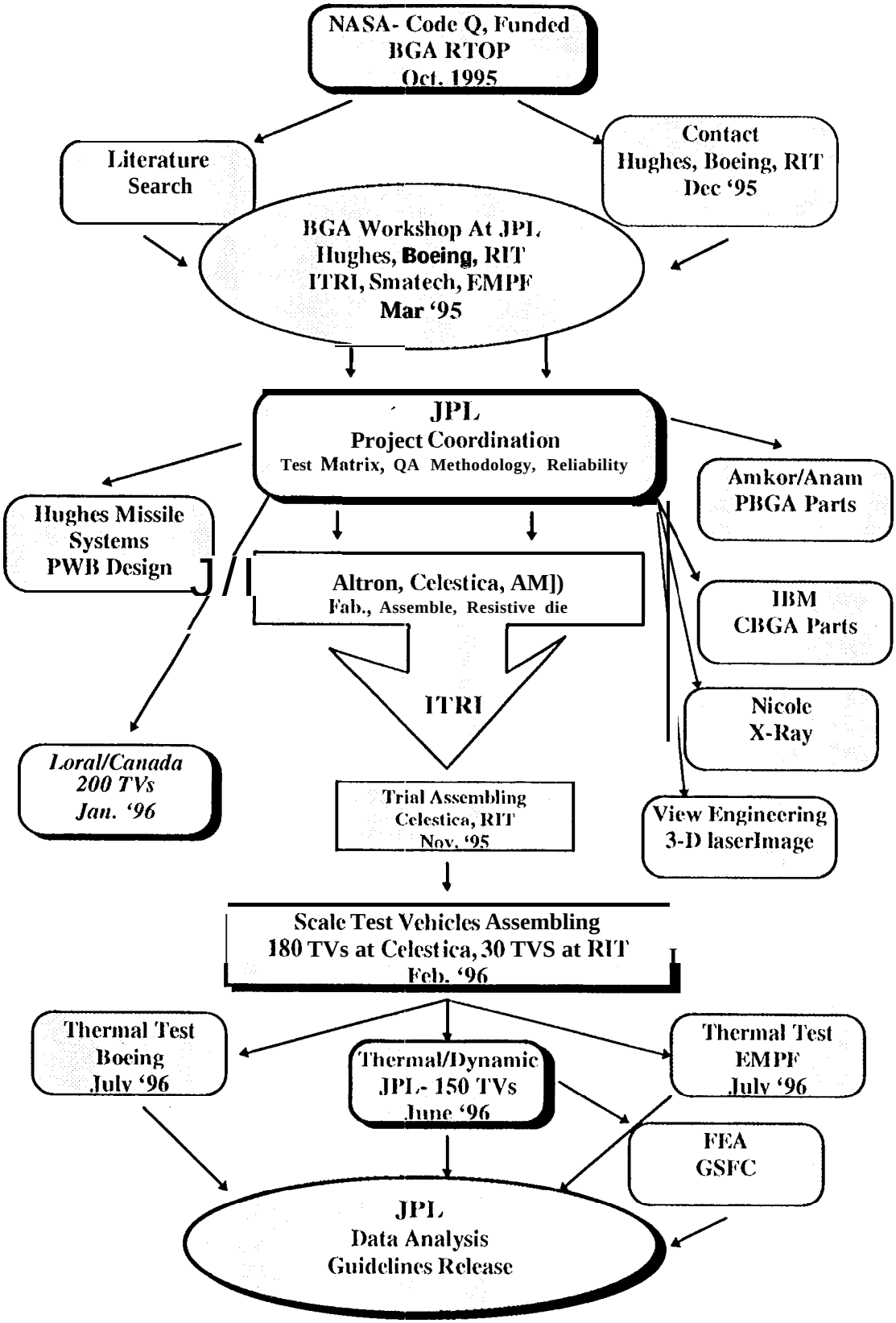
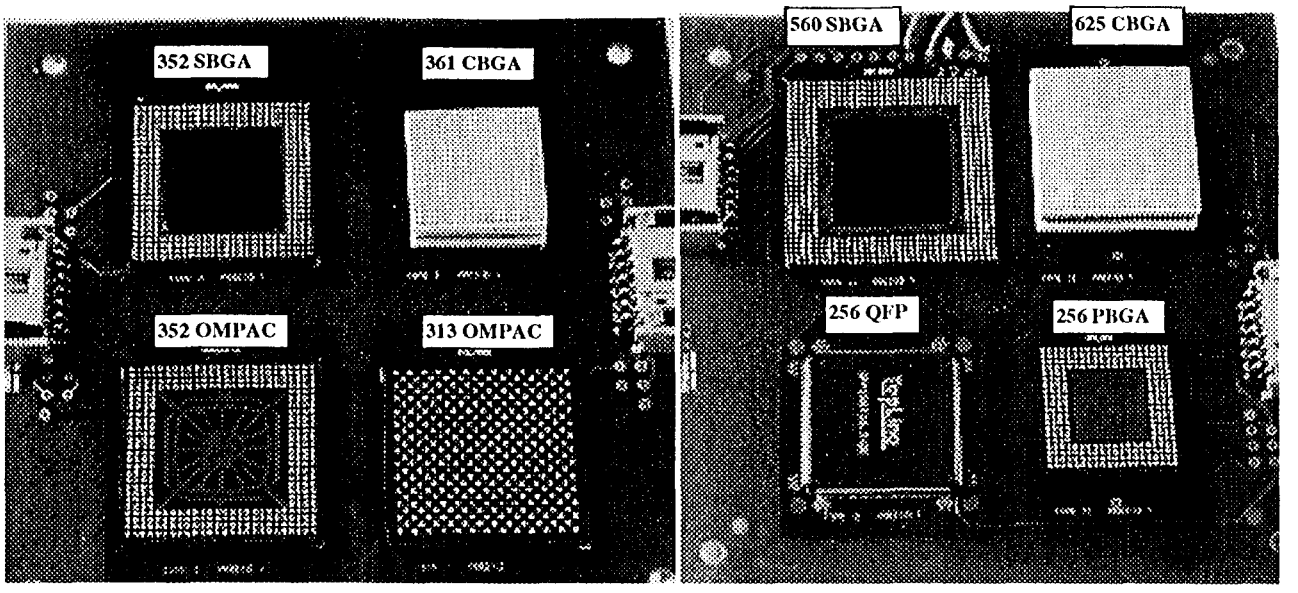


Figure 5. BGA Program Flow



a) Type 1 BGA Configurations and I/Os

b) Type 2 BGA Configurations and 1/0s

Figure 6. Test Vehicles with Unassembled Parts on the Assembled Ones

Currentl y, an additional of 200 test vehicles are being assembled in a military manufacturing environment at Loral/Canada, a recent participant in the project. Majority of the Loral's TVs will be tested by Loral and only about 30 TVs will be tested at J}']. to generate a baseline allowing to compare the reliability results gathered from four sites. I oral invest igates: non woven aramid PWB materials, thermal aging exposure effects prior to thermal cycling on reliability, and reliability of TVs to be manually assembled.

The TVs are being thermally cycled at three sites, in three environmental conditions, and are being monitored continuously through daisy chains to electrical failure of all daisy chains. Ninety (90) TVs are being thermally cycled at JPL and the remaining (60) TVs will be subjected to cycling, power cycling, and dynamic exposures. Boeing is cycling 19 and EMPF 33 TVS. JPL's cycle is between -30 "C and 100 "C with about 10 minutes dwells. Boeing and EMPF thermal cycles are much harsher than the JPL's and are between -55 °C and 125 °C. Dwell and ramping rates are different for the twos ites.

Extensive monitoring are being performed to understand and record cycling damages progress. Five TVs from Boeing and EMPF will be removed and sent to JPL for inspection characterization. Boeing and EMPF are performing visual inspections at specified intervals. Boeing also performing limited SEM evaluation. At JPL, there are a sets of TVs al located for thorough inspection, few individual y cut specimens for scanning electron microscopy (SEM) evaluation. "Inspection" TVs and cut specimens are being removed periodically for visual inspection, SEM evaluation, and cross-sectioning for crack propagation mapping.

Data gathered will be analyzed and categorized using the Weibull distribution, and the Coffin-Manson relationships for the cycles to failure distribution and failure projection, Manufacturing defects and occurrence frequencies for different surface finishes and package types and configurations will be correlated, Finite element modeling techniques to be developed at the Goddard Space Flight Center (GSFC) wil I be used to con elate theory and the experimental results.

Ceramic and Plastic Package Dimensional Properties

Package dimensional characteristics as well as PWB's are among the key variable that affect solder joint reliability. Dimensional characteristics of all packages were measured using View Engineering 3-D laser scanning system. Output of n easurements include solder ball diameter, package warpage, and coplanarity y stored in ASCII files for analysis. Packages were also inspected visually and by SEM and results documented.

SEM Inspection

Amkor/Anam the largest manufacturer of plastic packages provided all plastic packages including the most recently developed SuperBGA packages. Packages cover from OMPAC to SBGA that has improved thermal characteristics over conventional PBGAs.

The ball size is 303 1 mils. The solder ball collapses dnri ng reflow to an oval geometry of about 1 g mils in height (Figure 7). In SPBGA fbc IC dic is directly attached 10 an oversize copper plate providing a better heat dissipation efficiency. The copper plate also act as a stiffener and ground plane of the package. It is also expected to scc an improvement in solder joint performance compare (o PBGA because the chip is mounted on tbe sar ne side of the solder balls as opposed to PBGAs.

- Die size of 13.5 mil was selected to be used for the 352 OMPAC, 352 SPBGA, and the 313 OMPAC. Die size of 10.8 mil was selected for the 256 PBGA.

Resistive die size of 15.2S mil were for the 560 SPBGA which wi II also be subjected to power cycling, These dices were contributed by American Micro Device (AMI)).

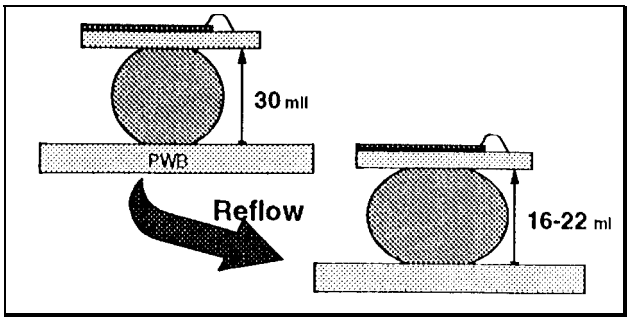


Figure 7. Plastic packages collapse during reflow

1 BM provided ceramic packages and Amkor/Anam all plastic packages. The balls in the CBGAs are populated in full array. The substrate in CBGA is a multi-layer alumina ceramic that provides a better thermal and electrical performance than PBGAs. Ceramic solder balls have 0.035 inch diameter and are made of high melting temperature 90Pb/10Sn. These balls are attached to ceramic substrate with eutectic solder (63 Sn/37Pb) material. At reflow, substrate eutectic material and PWB eutectic paste reflow and provide the electro-mechanical interconnects.

Figures 8 shows SEM photos of ceramic packages with 625 1/0s that solder balls are straight whereas Figure 9 a package with tilted solder balls.

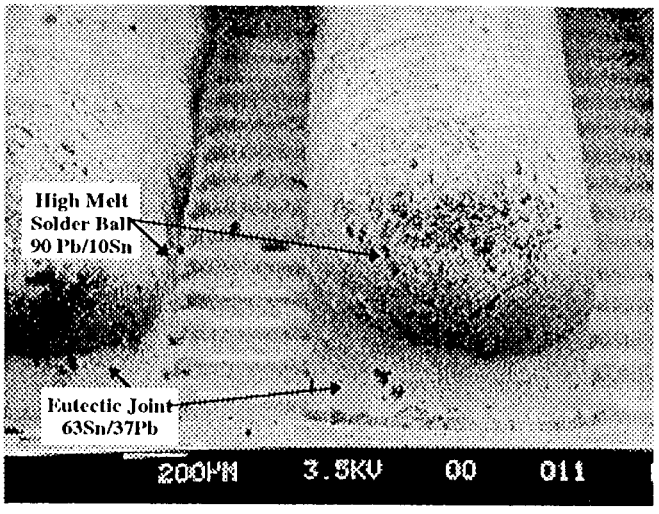


Figure 8 Solder Balls With no Tilting in a 625 CBGA

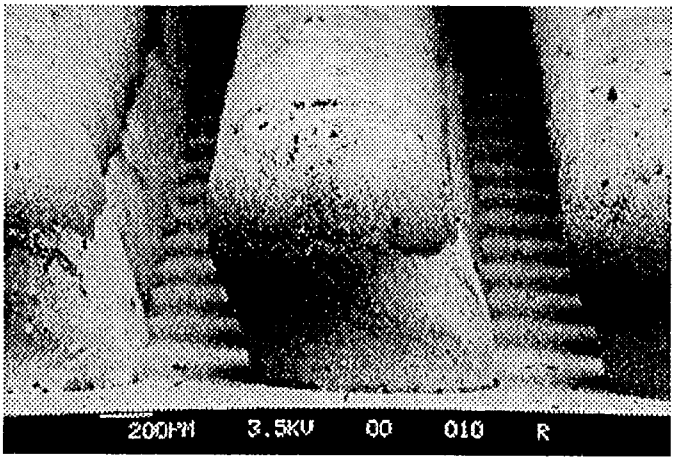


Figure 9 Tilted Solder Balls in a 625 CBGA

Dimensional Characteristics Measured by a 3-D Laser System

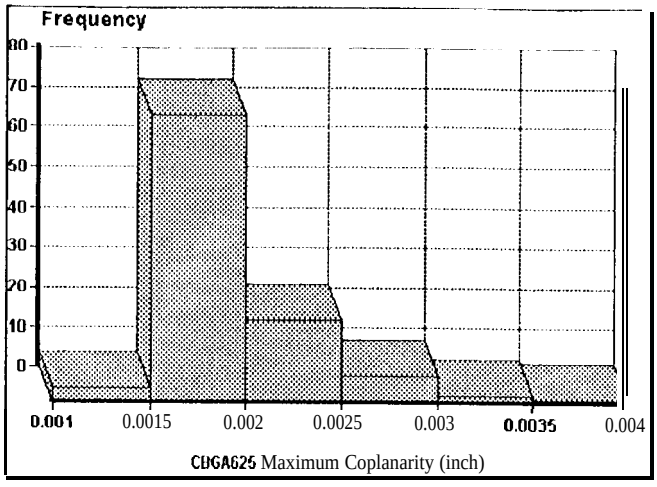
Package coplanarity is defined as the distance between the highest solder ball (lead for QFP) and the lowest solder ball. Coplanarity can contribute to the yield of surface mount manufacturing as well as log-term solder joint integrity. For leaded parts such as QFP, the nonplanarity in excess of 0.0003 inches is not allowed.

There is a direct correlation between coplanarity and package substrate, package size, package thickness. For ceramic packages, solder bail diameter tolerance and coplanarity is much more critical that those of plastic packages, Solder balls in plastic packages collapse during reflow eliminating gaps due to copalanarit y. J} :DEC specifi cat ion for coplanarity y requirement is 0.006 inch which is double the value of QFP package, In this paper, only the results of package properties for 625 CBGA and 560 Super BGA will be given, These data are being used to determine the influence of these parameters on the solder joint cycles 10 failure,

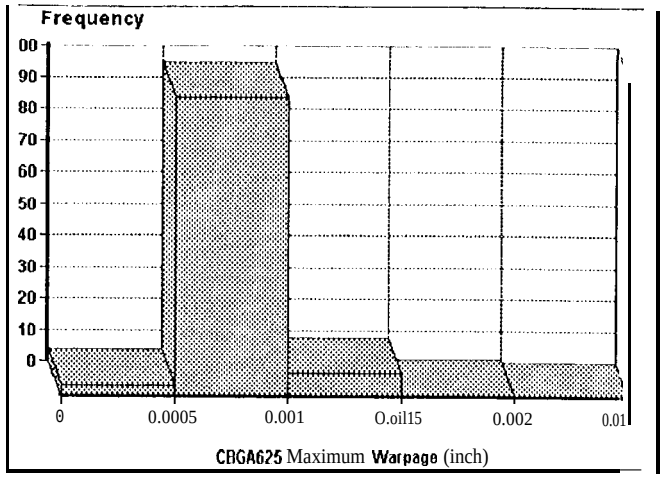
Figure 10 shows histogram plots of coplanarity y and warpage distributions for 108 ceramics with 625 1/0s and coplanarity distribution for a package (ID#98) with the maximum coplanarity of 0.0042 inch. Results from these and similar plots are:

- Balls' coplanarities are 0.0015 to 0.002 inches for 104 parts; ().003 to 0.0042 inches for 4 parts.
- Maximum solder balls' diameters are 0.0315 to 0.0334 inches; minimums 0.028 to 0.029 inches. Diameters were measured only for 36 parts.
- Maximum warpages are 0005 to 0.0029 inches.

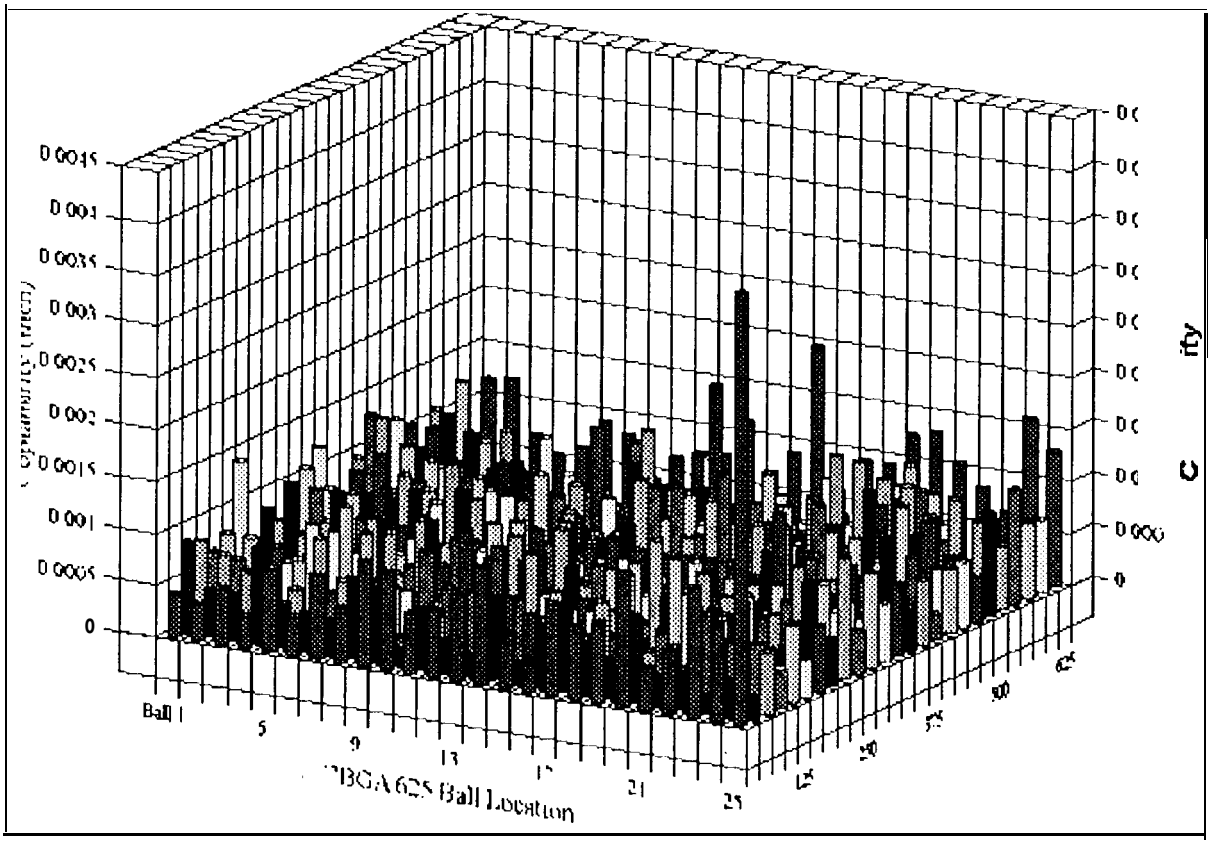
Coplanarity distribution plot for #98 reveals that solder ball are generally uniform in heights with few at two extreme levels that are randomly distributed.



a) Maximum Coplanarity Distribution for CBGA 625

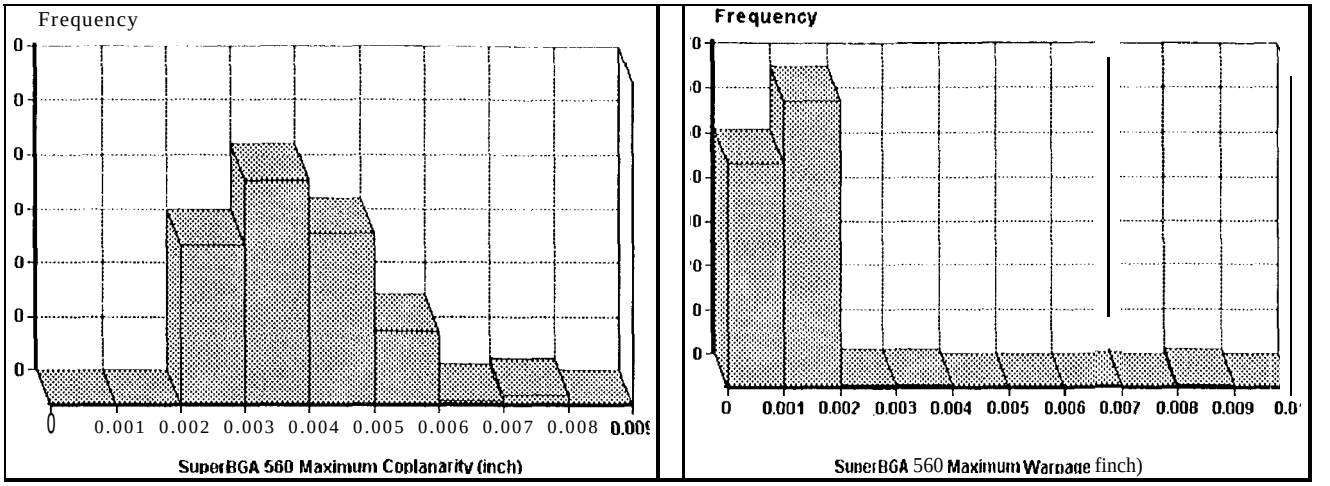


b) Maximum Warpage Distribution for CBGA 625



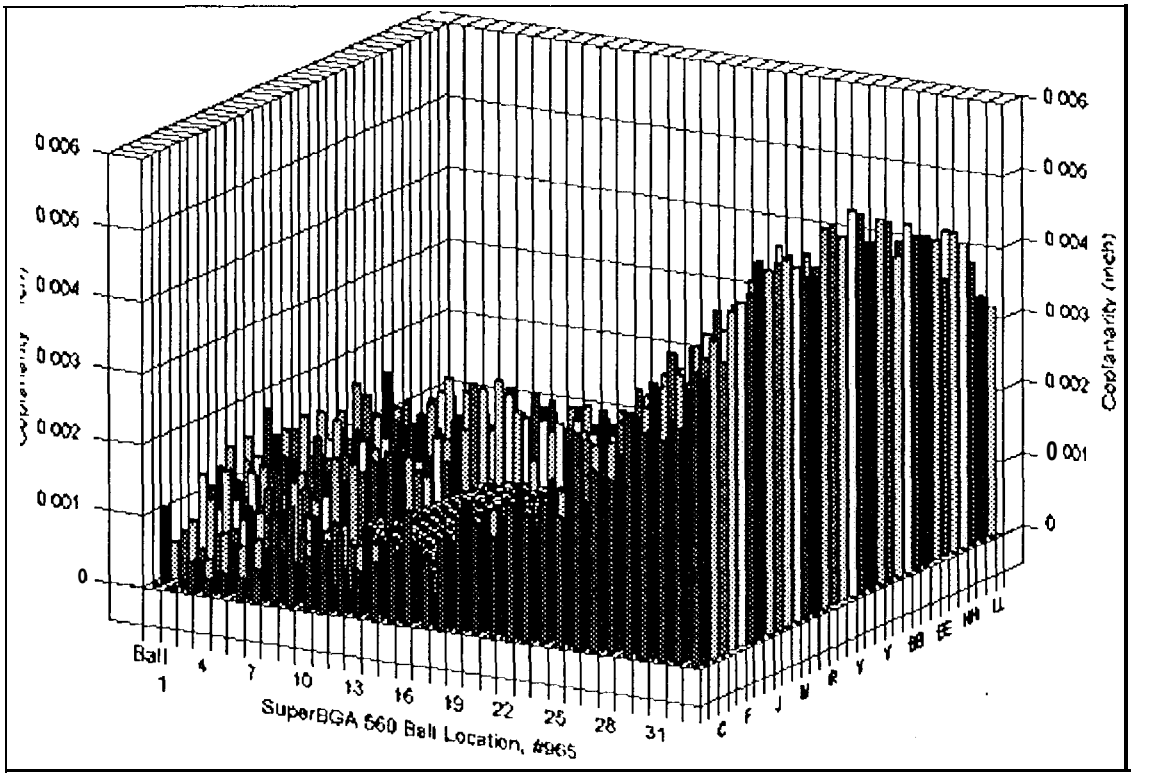
c) Coplanarity Distribution for a CBGA 625 Package

Figure 10. Package Dimensional Characteristics of Ceramic BGA with 625 I/Os



a) Maximum Coplanarity Distribution for SuperBGA 560

b) Maximum Warpage Distribution for Super BGA 560



c) Coplanarity Distribution for a SuperBGA 560 Package

Figure 11. Package Dimensional Characteristics of SuperBGA with 560 I/Os

Figure 11 shows histogram plots of coplanarity and warpage for 120 Amkor/Anam 560 SuperBGAs and coplanarity distribution for a part (#965) with the maximum coplanarity of 0.0054 inch. Results of these and similar plots are as follows:

- Balls' coplanarities are 0.002 to 0.004 inches for 72 parts; 0.004 to .006 for 45 parts; and 0.006 to 0.00766 for 4 parts.
- Maximum solder balls' diameters are 0.0275 to 0.0290 inches; minimums 0.0213 to 0.0263 inches,
- Maximum warpages were 0.00165-0.0096 for 110 packages, 0.01012 - 0.021 inches for 8 packages, and 0.034 inches for one package.

Coplanarity distribution plot for #965 reveals nonuniformity; one region showing higher heights than the other. Such nonuniformity could cause package lifting during reflow; thus, increasing susceptibility to 'manufacturing defect formation.

It is stated that IBM ceramic packages use high melting solder balls with 0.035 inch diameter. lhe 3-D laser imaged solder ball diameters for both CBGA 361 and 625 1/0 packages were lower than 0.035 inch. IBM's recent measurement (Jul y 1996) of solder ball diameters (50 out of 300,003) as part of their incoming inspection were within the ball diameter specification,

One possibility is that even though the View Engineering system is accurate for measuring coplanarity and other dimensional parameters, it is not accurate for solder ball diameter measurement. Solder ball diameter is calculated from a mathematical curve that is fitted to the shape of the balls. The results therefore depends on how well the curve is representative of the actual shape of the ball.

Another possibility could be due to the tilt and skewness of solder balls attachment to the substrate observed (Figure 8). The tilt could cause distortion in image detected by laser scanning and results in different values that those reported by IBM. A measurement of solder ball diameter using the SEM photo resulted .0355 inch that agrees with the IBM specification values.

Discussion

Ultra-low volume surface mount assemblies considered for space applications do not permit the proof of process potential as do commercial or military production quantities. Ibis fact mandates that Quality Assurance involvement be proactive and be included throughout the process of val id at ion and proof of process build, and as well as problem detection by inspection, The QA engineer should bc responsible for ensuring that manufacturing coat rols are in place and that crit i cat steps are considered and understood for inspect ion.

In this cooperative investigation, the QA role being proactive and concurrent resulted in better understanding of some of the critical parameters in solder joi nt reliability y as well as more confidence in the methodology of visual inspection. In conflating visual inspection results to those of SEM and microsectioni ng, it has been demonstrated that once trained, QA personnel would indeed be able to detect conventional SMT solder joints with potential reliability problems.

At J}']., the conventional paw/fail qualification criterion relies on visual inspection at 10x to 50x magnifications. For leaded parts, once cracking is observed, it was demonstrated that more than an one order of magnitude of additional cycles are required before the failure, whereas this is not the case for leadless assemblies. Crack initiation and propagation in the heel fillet of gull wing leads, which are considered to be key factors in solder joint failure mechanisms, are being closely monitored. Onc solder joint showed signs of heel fillet cracking al 50 cycles, but did not continue propagating significantly up to 1,000 thermal cycles. For leadless, however, cracks usually initiate inside the joint, at fbc corner underneath the part, and propagate outward. For a 68-pin LCC assembly, cracks were not observed until 47 cycles, Complete cracking and failure occurred after 71 cycles,

M icr ostr uctur al changes observed during environmental exposure for conventional SMT solder joints could also bc used to determine aging history and estimate refraining life of solder joints. These include observation of phenomena such as solder ball spreading, and minor to major surface roughening due 10 solder grain growth, The solder joint feature ch anges also depend on the initial properties of solder including solder composit ion, solidification rate, and interface joint metallurgy.

Similar characterization are being performed on the evaluation of periphery joints in BGA assemblies. Damage progress and indicators for the BGAs are being defined.

Infor mation obtained fr om crack propagation and microstructural changes is being incorporated into prediction guidelines for design and reliability and twining materials for inspection and manufacturing personnel. Similar pr ocedures are being

Anotbcr aspect of this investigation is to better understand the interplay of manufacturing defects and reliabil it y, and to provide QA personnel with the necessary toos to increase their effectiveness in detection of solder joints with potential reliability problems. To establish such criteria, visual criteria such as signs of heavy stress or crack initiation possibly in com bination with ther mal aging including signs of grainy due to grain growth and ball spreading need to be investigated, The approaches including crack propagation mapping over time for solder joints defects were aimed at identif ying a quantitative dcf i nit ion about the criticality of each defect category. Qualitative indicators could be used to reject solder joints that do not meet cycle requirements for a rni.mien thermal environment.

It was hoped that the interpretation of results of solder damage progress would provide the required quantitative visual indicator. Plots for cycles tc, failure for LCCs, because of missing inspection data intervals and combining solder joints ir respective of lead location, could be used oal y to come to conclusion that those defect categories investigated result in early failure and possibly cause reduction of the Weibull shape parameter (increase in coefficient of variation). Elimination of the cause of such defects will decrease failure spread and therefore provide higher confidence in predicating reliability for a significantly lower rate of failure.

Currentl y inspection results for 28-pin LCC with nearl y 1,000 solder joints are being analyzed to determine if a more definite trend can be established. Results will be analyzed similarly to those presented here as well as considering corner and center joints separatel y. Si milar techniques will also be used for leaded parts of SMT Phase 1 and Phase 2 test programs as well as those fur BGAs.

In the BGA study, for example, solder balls' planarities were significantly higher for PBGA than those of ceramic packages, Ibis might cause minor differences on solder joint reliability since planarity control is significantly less critical for PBGA than that of CBGA. PBGA solder balls collapse during reflow process accommodating some planarit y d ifference among fbc solder balls. This is not the case for CBGA that high melt solder balls are used to control the stand off and they are not remelted during manufacturing reflow.

in the BGA progra n, the effects of these and many other variables are being investigated. Similar to those of conventional package, variables and inspection results will be correlated to reliability to identify indicators that could be used to discern the solder joints with poor performance. Based on the results, QA will provide general or specific guidelines for the acceptance/r ejection of solder joints for a mission thermal environment.

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