Test procedures and results for the ELEFANT ASIC

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Contents

- Hardware
- Software: IGOR
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The test board

- Locally regulated supply voltages.
  6-bit DACs for reference voltages.

- Two differential drivers for the eight FADC-inputs. Direct connection from pulse generator to TDC input.

- Rise time restoration (1 ns) and adjustable delay for system clock and sample clock.

- All digital inputs are preset using switches. The setting is overruled by a connected pattern generator pod.

Software

We use a package called IGOR.
Its main features are

- Publishing quality data presentation
- Good data analysis capabilities:
  Curve fitting, histogramming, FFT and much more.
- Programmable in a bare-bones, no-frills version of C. But C-programs can be linked.
- Supports the DAQ and GPIB-cards of National Instruments
- Low cost: $500

Test environment

- PowerMac and IGOR for automated tests.
- GPIB accessible devices:

Pattern generation:	HP16500C system
Logic analysis:	HP16522
Pulse generation:	LeCroy 9210 system
Precision DC-voltages:	HP universal source
Power supplies:	AmRel PPS-2322

- Parameters under remote control:

  frequency, V_{DD}

The ELEFANT ASIC

There are eight channels on a chip; each with its own FADC and TDC.

Eight circular "latency" buffer (192 buckets) are continuously written to. Data (1 byte) are FADC data, unless a TDC reports a hit and submits its information.

On a "Level 1" accept the oldest 32 buckets of each channel are transferred into one of four buffers.

Each channel and each buffer can be read out individually

A small SRAM holds additional information, including an event identifier and a "hit map" to guide a sparse-readout controller.

Testing: Overview

- Performance evaluation

  SRAM

  FADC

  TDC

  Trigger logic

  Auxiliary SRAM

Fixed error in prototype: SRAM

- At 50 MHz

  start test_mode (data = counter values)

  fill latency buffer

  stop test_mode

  transfer data to output buffer

  $\Longrightarrow$ data are correct

- Don't stop test_mode $\longrightarrow$ data are corrupted.

  But no problem at 25 MHz.

- This problem has been solved.
  Data transfer during acquisition now works at all frequencies.

Fixed error in prototype: FADC

- Problem:

  Only 15% of the analog receiver/amplifiers were working. A redesign was (mostly) successful.

- Each FADC has its own resistive ladder. The top and bottom reference voltage are supplied from a common bus.

  Result: The FADC's work fine, but the bus was too resistive, resulting in contracting FADC ranges.

  This problem has been solved.

Fixed error in prototype: TDC

There is a set of 64 voltage-controlled (by V_{ctrl}) delay elements. Each delays the sample clock by a fixed amount.

Total chain delay = one sample clock period

The signal arrival time is measured by comparing its *rising* edge to the output of the delay elements.

Problem: The chain delay was adjusted using the *falling* edge of the sample clock. $\longrightarrow$ too great a chain delay. The 64-count TDC became a 63-count TDC with one double code (62) and one missing code (0).

This problem has been solved.

Tested chip summary

The preproduction run arrived in two distinct shipments.

1) EPP-001 TO EPP-050 were partially tested.

   All were tested for power consumption and V_{ctrl}.
   Some had their analog sections characterized before shipping to SLAC and Canada.

2) EPP-051 to EPP-134 were extensively tested.

   All had their ADCs characterized.
   Half of them received a battery of digital tests.

Performance evaluation: FADC & TDC

Summary from 84 chips, including more than 650 channels.

- FADC at lowest gain setting, $\times 5.25$.
  All quantities are input voltage referred.

FADC	mean	rms
offset	41 mV	1.7 mV
slope	224 counts/V	2.5 counts/V
bin width	4.3 mV	1.4 mV

- TDC at 64 MHz

TDC	mean	rms
offset	24.0 ns	0.17 ns
slope	1.0158 ns	0.00076 ns
bin width	0.98 ns	0.10 ns

Two new problems

- FADC offset:
  Capacitive clock feed through coming from comparators is too much to handle for analog receiver.

- FADC code errors:
  At sys_clock $>$ 60 MHz we find 1 LSB, 2 LSB and 4 LSB code errors increasingly likely.

- Both problems have been addressed for next submission.

Directory of plots following this slide

These plots are on the web site. Consult the link http://design.lbl.gov/~levi/elefant/FDR.

- (1) Analog receiver pulse linearity.

- (2a) Typical FADC-performance, (64 MHz).
  (2b) Typical TDC-performance.

- (3a) FADC offset histogram.
  (3b) FADC slope histogram.
  (3c) FADC INL histogram.
  (3d) FADC rms error histogram

- (4a) TDC offset histogram.
  (4b) TDC slope histogram.
  (4c) TDC INL histogram.
  (4d) TDC rms error histogram

- (5) FADC/TDC DNL histograms
  (6) TDC performance at var. frequencies.
  (7) FADC, offset & code error problem.

Irradiation test

Two chips have been irradiated using a ^{60}Co-source.

Dose: 20 krad in 17 hours

Conditions:
One chip under power, with clock (60 MHz) in test_mode, SRAM_enable and chip_select high.
One chip not connected to anything.

Result:
No discernible change compared to pre-exposure operation.
Tested: Power consumption, V_{ctrl}, FADC & TDC parameters. Digital tests.

Miscellaneous

- Power consumption:
  Supply current is 82 mA with an rms spread of 2.6 mA at nominal operating conditions.

- PLL-voltages:
  The control voltage of the delay-locked loop is 3.23 V with an rms spread of 0.05 V at 60 MHz.

- Supply voltage range:
  $V_{DD} < 4.6\,V \longrightarrow$ top most FADC-comparator fails if $V_{top} = 4.0\,V$
  $V_{DD} > 5.2\,V \longrightarrow$ data from memory are corrupted.
  $\Longrightarrow$ valid range: [4.7V, 5.1V]

Failed-chip summary for chip number 51 to 134.

chip	FADC	TDC	buffer	trigger	hit map
57	all	all	all	OK	n/a
63	0	OK	OK	OK	OK
66	2	OK	2	OK	OK
77	OK	1	OK	1	1
78	1	OK	OK	OK	OK
96	OK	OK	OK	OK	all
103	OK	OK	OK	OK	1
105	OK	6	OK	OK	OK
110	3	OK	all(3)	OK	OK
119	0	0	all(0)	OK	OK
131	5	5	all(5)	OK	OK
132	OK	1	OK	1	1
134	all	all	all	OK	n/a

First entry: number of affected chip. In subsequent columns OKmeans passed the test; a number indicates the channel that failed; in the 'buffer' column an entry $n(m)$ indicates that channel m in buffer n failed. Failure of the trigger or hit map test may be due to either tdc or fadc failure (in this table). n/a means not applicable

Test plan

Requirements for test procedure:

- Comprehensive functionality test, to address all sections of the circuitry.
- Decisive characterization of the ADC performances, ie offset, slope, INL, DNL.
- Push button operation for easy use by minimally trained personnel.
- Flexibility to modify, add or drop tests without having to change the software.

Flow chart—digital tests

Read to-do list and work through it.

Each time do:

- Read command file
- Create Pattern generator program and test vector list for the simulator.
- Load pattern generator, run program, read logic analyser.
- Run simulator (behavioral model)
- Compare data
- If {OK} continue;
  else {
  Save data; continue; }

Command file (excerpt)

```
test_mode 1 tag 21 buf_wr 0 repeat 768 ;
test_mode 0 L1_accept ;
L1_accept 0 ; ; ;
repeat 200 ;


cs 1 ch_sel 0 ds 1 repeat 4 ;
ds 0 di 1 buf_rd 0 repeat 4 ;
ch_sel 0 repeat 124 ;
ch_sel 1 repeat 128 ;
ch_sel 2 repeat 128 ;
ch_sel 3 repeat 128 ;
ch_sel 4 repeat 128 ;
ch_sel 5 repeat 128 ;
ch_sel 6 repeat 128 ;
ch_sel 7 repeat 128 ;
buf_rd 1 ch_sel 0 repeat 128 ;
```

Flow chart—Analog tests

Load specific pattern generator program

Use preset parameters for offset, stepsize and no. of points.

Run test, gather data.

Analysis: Find endpoints, do least-square fit, compute offset, slope, DNL, INL for each FADC and each TDC channel.

Compare to preset limits.
Alert user in case of failure.

Run control

Three panels allow user control of the test stand:

- **Run panel**
  Tells user when to insert/remove chips.
  Waits for user OK to resume testing.

- **Parameter & results panel**
  Run control parameters for analog tests (step size, no. of points, V_{DD}, etc.)
  Acceptance limits for offset, slope, DNL, INL. Result display for those quantities.
  PASS/FAIL test overview

- **Utility panel**
  Unscheduled activities,
  (power on/off, etc.)

Sequence of tests

Each test is designed to address as many issues as possible or reasonable to minimize test time.

Digital test run time: 5min. Analog: 3min.

1) **All buffer test:**
   In test_mode, verify all 4 buffers.
   Tests: Memory, sys_clock counter, ‘synch’ and L1_accept.
   The 4 L1_accepts are timed to make all memory bits toggle.
   Power consumption is logged and compared to limit.

2) Readout same buffer 4 times.
   Use simultaneous data transfer and readout during first read.

3) **SRAM2** in test_mode.
Tests: hit map, buffer-and-tag word, and 'sys_clock' counter.
Choose L1_accept and 'tag' to toggle all affected bits.
Verify mode_sparse operation.

4) **Trigger** test in normal mode
Verify mode_trig operation

5) **δ-bit computation**
Send ramped pulses to analog receivers and record FADC data.
Compare δ-bit with expectation.
Verify threshold bits.

6) Quick characterization of FADC and TDC
Using 128 data points, look for bad channels.
Determine offset and slope (and INL).
Verify gain setting.

7) Full characterization of FADC and TDC performance (optional)
Using a 1000 data points, measure DNL and INL.

Conclusion

- We have a flexible and productive testing environment, good for automatic screening and and detailed investigation.

- Recognized flaws in the prototype ELEFANT design have been corrected.

- We are well prepared to thoroughly test a large number of chips in a reasonable amount of time.

- Yield:
  Note: δ-bit generation and gain setting have not yet been rigorously checked on a large number of chips.

  Based on test 1, 3, 4 and 7, we have:
  13 rejects out of 84 chips.
  $\Longrightarrow$ rejects = 15%