TDC Full Crate Test

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- Goal is to test TDCs in environment of full crate of cards
  - Tests at Michigan limited to a few cards/crate
- Use TRACER calibration pulse to run TDC internal calibration system
  - TDC CALIB signal bussed on J2 backplane to TDCs
  - CALIB signal routed through multiplexer to JMC96 TDC chip inputs
- Manpower:
  - Frank C., Kevin P., Jim P., Sergei B., Peter W., Aurore S. Sergei L., Simona R.
  - All working very part-time
  - Recently: Bill Orejudos (LBL)
    - See Next Talk!
- Progress
  - Crate - 7/98
  - 18 TDCs - 9/98
  - “Final” Power Supply - 10/98
  - RPS - 11/98
  - Software - 11/98
  - First plots - 12/98
- Today:
  - Backplane Scope Pictures (PJW)
  - TDC Data analysis (Bill O.)
- Deadline for TDC sign-off:
  - Mid-March

TDC Full Crate Configuration

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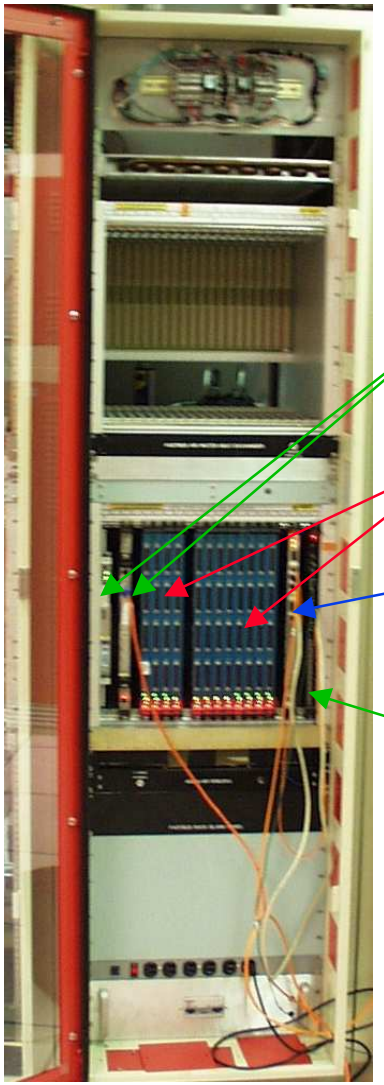
- Up to 19 Rev C TDC Boards (So far up to 16 boards)
- MVME 167 and MVME 2301
- TESTCLK to provide 132ns clock
- 1 TRACER
- TRACER TDC Calibration pulsing software (Frank):
  - Control start time and width, 100 pulses with each start time then change start time.
  - Issue L1A automatically
  - L2A written to each TDC register (TRACER Calib doesn't issue L2A)



Test Plans

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For each of the first five:

- Measure slopes and T0s from CALIB pulsing. Slope should be 1 to few parts in 10^5
- Look at RMS from pulsing at a specific pulse delay (pulse jitter).

1. Compare performance when pulsing a single TDC in crate with same TDC (same slot) when pulsing many (16-18) TDCs in crate.
   - Try this with several different TDCs.
   - Try this with TRACER at end of crate and in middle of crate to see if our clock problems affect the calibration (see clock problems).
   - In progress, See Bill's talk
2. Performance as a function of PS voltage: 4.9, 5.0, 5.2V (w/16-18 TDCs)
3. Time/temp stability (w/16-18 TDCs):
   - Performance as a function of time after turning on crate (eg every 10 minutes for 1 hour).
   - Turn crate off and on and repeat.

Tests for TDC Full Crate Test (cont)

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4. Long term running stability (w/16-18 TDCs). Calibrate every hour for a day
   - Stability of slopes and T0s
   - Number of readout errors etc
5. Stability of TRACER calibration signal. Stability of absolute time of pulsing at a given TDC. Are any variations coherent or incoherent between TDCs?
   - In progress
6. Effect of TDC operation on power supply voltage: while pulsing and reading out all TDCs look at power supply voltage on scope. Compare to quiescent state.
   - See below
7. Measure readout speed with MVME2301
8. Connect to VRB and test full readout.
   - Test TRACER SPY mode operation - Done (Jim and Sergei B.)
   - Measure link error rate - Done (Jim and Sergei B.)
   - Readout timing

CDF Clock Measurements in TDC Crate

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- Look at CDF Clock on TDC and DIRAC board with different number of cards in crate
- Clock receiver card plugged into back of P2 in slots 17 (red) and 20 (purple). Uses Motorola receiver.
- TDC in 17 (yellow)
- DIRAC in 18 (green) Uses AT&T receiver.
- ADMEM in 16
- TRACER in 19
- TESTCLK in 21

CDF Clock Measurements
(cont)

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- Clock receiver card plugged into back of P2 in slots 17 (red) and 20 (purple)
- TDC in 17 (yellow)
- DIRAC in 18 (green)
- TDCs in 2-15,17
- ADMEM in 16
- TRACER in 19
- TESTCLK in 21
- Puzzle: TDC clock signals get ring but DIRAC and clock receiver don't

CDF Clock Measurements
(cont)

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First Plots from Kevin (Dec 98)

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Fits for four sample channels (Channel n vs Channel 0):

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It will print correctly to a PostScript printer.
File Name : linsamp.eps
Title : linsamp.eps
Creator : HIGZ Version 1.23/09
CreationDate : 98/12/11 10.03

Fitted Slope vs Channel Number:

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Title : linvchan.eps
Creator : HIGZ Version 1.23/09
CreationDate : 98/12/11 10.00

Effects of TDC Activity on +5v Power Supply

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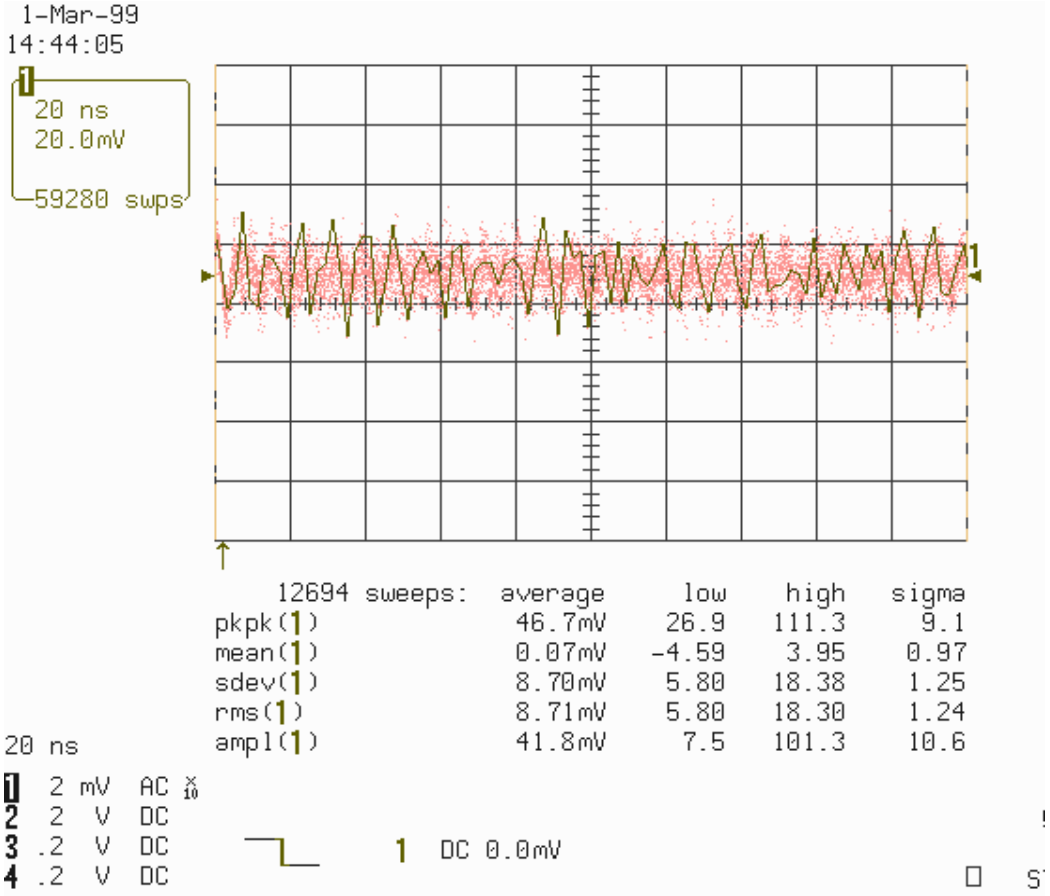
- Scope probe on +5v power pin on J2 Backplane pin
- Standard crate config:
  - Slot 1 - MVME 167
  - Slot 3 - MVME 2301
  - Slot 5 -18, 20 TDCs
  - Slot 19 TRACER
  - Slot 21 Testclk
- Compare Quiescent state with states with activity

Quiescent State



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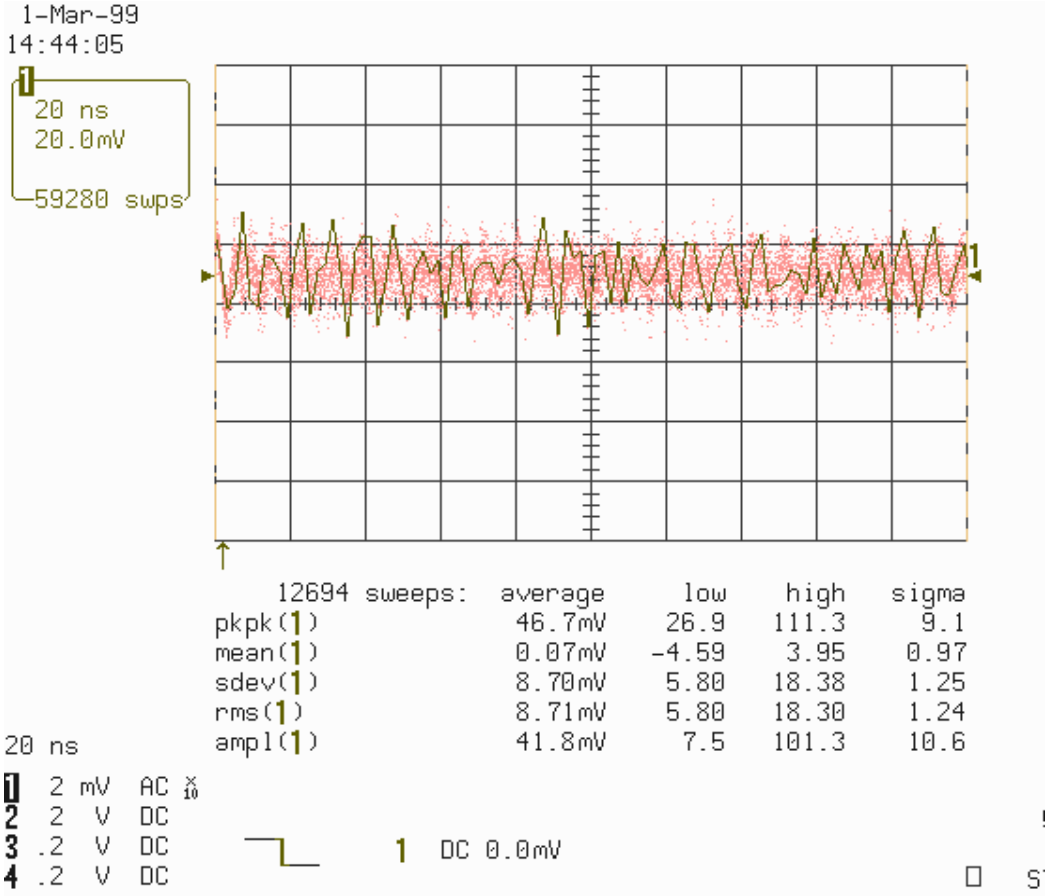
- Quiescent State
  - V_{rms} = 9mV
  - V_{P-P} = 50 mV

Quiescent State



Power Supply While Pulsing 15 TDCs

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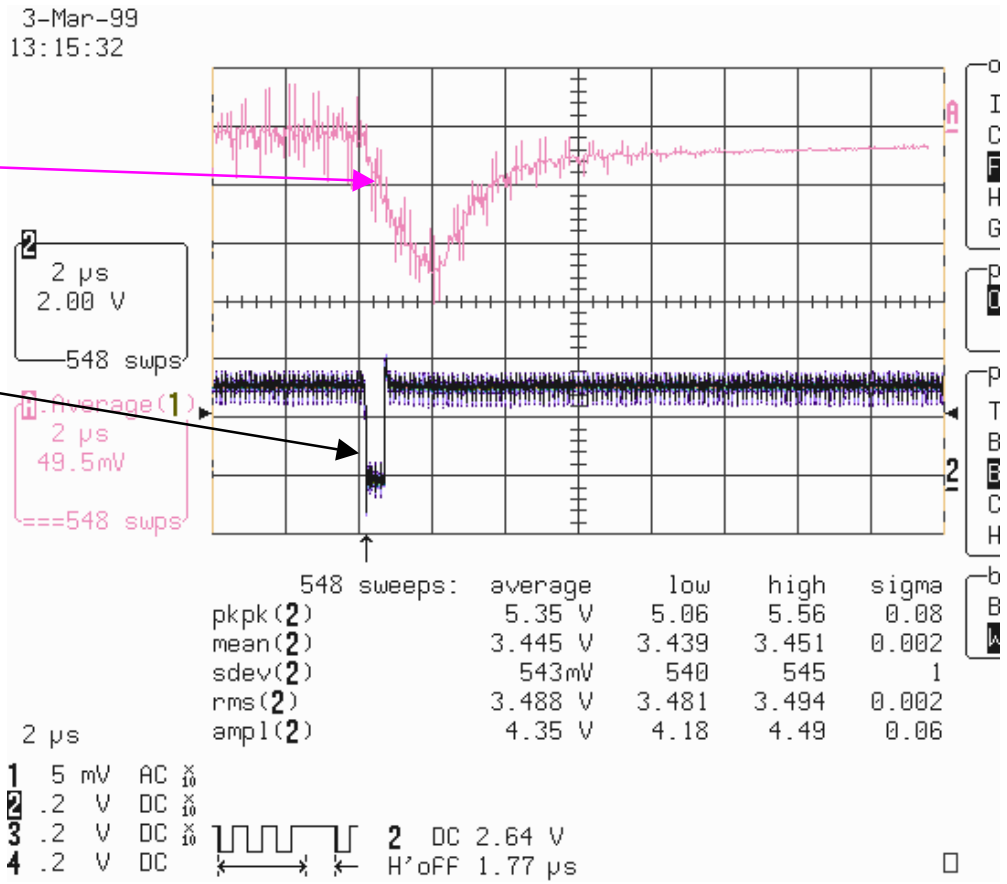
- Run CALIB code pulsing and reading out 15 TDCs
- See 125mV drop in supply around time of L1A
- 2 microsec time constant, 25 microsec tail
- Trigger Scope on L1A signal
- Corresponds to period when TDC chips are transferring data into L2 buffers
- Cannot see an effect during DSP operation
  - However DSPs not starting simultaneously
  - Need to try with TESTCLK generating L2A



Power Supply While Pulsing 1 TDC

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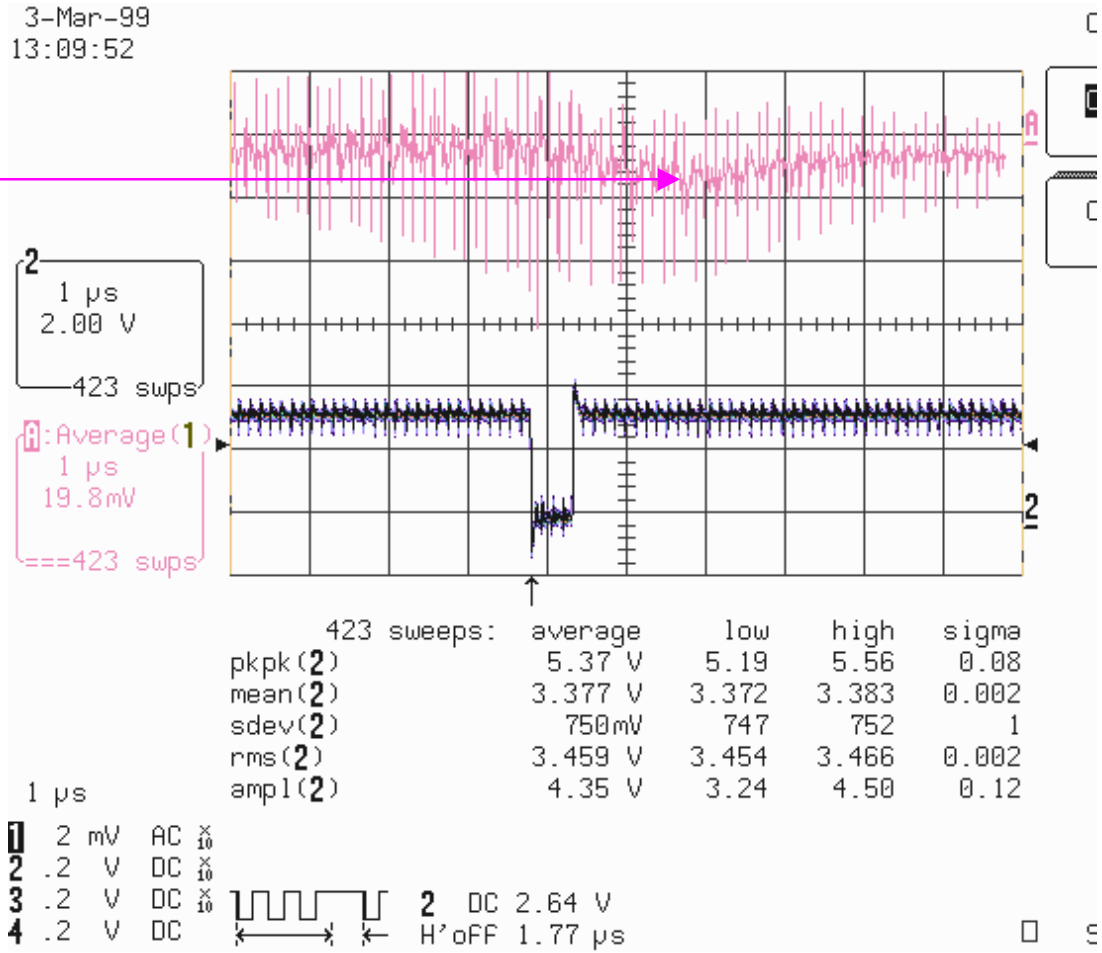
- Run CALIB code pulsing and reading out 1 TDCs (15 in crate)
- 5-10mV sag in +5V power
- Trigger Scope on L1A signal
- Naively, think that should only depend on number of boards receiving L1A not number pulsed
  - May be misunderstanding of what the code is doing
  - Want to try with readout code but no CALIB pulsing



Power Supply with 1 TDC in Crate

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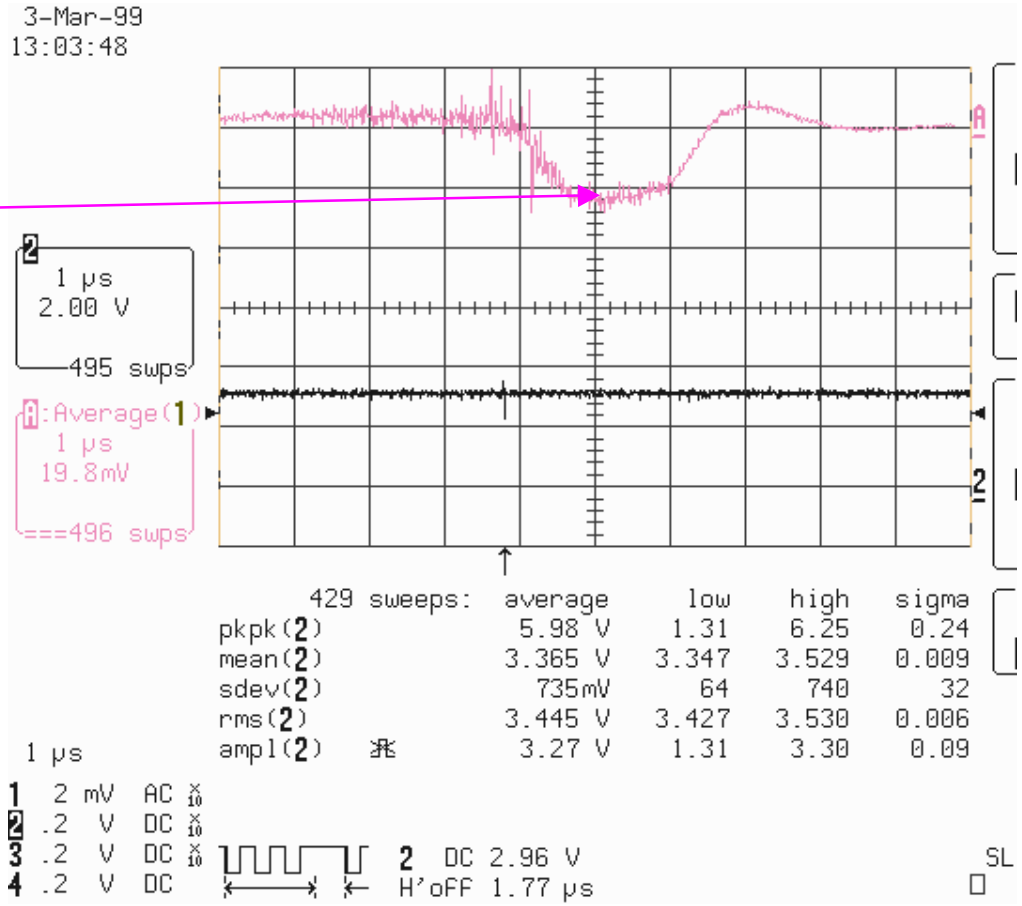
- Run CALIB code pulsing and reading out 1 TDCs (1 in crate)
- Trigger Scope on L1A signal
- 20mV sag in +5V power
- Don't understand why this is bigger than with 15 TDCs in crate

Other signals to look at:

- CALIB pulse shape and timing
- TDC done signal after L2A - DSP readout time