Development of a Pixel Readout Chip for BTeV

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Abstract

A description is given of the R&D program underway at Fermilab to develop a pixel readout ASIC appropriate for use at the Tevatron collider. Results are presented from tests performed on the first prototype pixel readout chip designed at Fermilab, and a new readout architecture is described.

1 Introduction

At Fermilab, the BTeV experiment(1) has been proposed for the new C-Zero interaction region of the Tevatron collider. The most ambitious aspect of this proposal is the plan to use a detached vertex trigger as the lowest level trigger for the experiment. This trigger will be based on information from a 93 plane silicon pixel vertex detector which will be placed inside a dipole magnet centered on the interaction point. The experiment is being designed for a luminosity of $2 \times 10^{32} cm^{-2} sec^{-1}$ (which corresponds to an average of two interactions per colliding beam crossing, given 132 ns between crossings). Simulations have shown that a pixel chip of active area 8mm$\times$7.2mm placed 6mm from the beam (the innermost chip in the current BTeV design) will be hit by one or more tracks in approximately one bunch crossing (BCO) out of four(2). The number of pixel cells hit by a single track depends on the pixel size and the track angle with respect to the pixel sensor. Given a pixel size of $50\mu \times 400\mu$, the simulations indicate that an average of five pixels will be hit in the innermost readout chip in those crossings in which one or more tracks hit the chip. Therefore, this pixel chip has to sustain an average readout rate of 1.25 pixels per BCO. To account for statistical fluctuations and allow for effects not included in the simulations, the chip must be capable of even higher data transfer rates, and must be able to buffer hit information which can not be immediately read out.

An effort has begun at Fermilab to develop a pixel detector readout ASIC appropriate for use by the BTeV experiment. This chip must be radiation hard so that it can be used close to the beamline. It should be optimized for the 132 ns time between crossings planned for future Tevatron operations, and it must be capable of the very fast readout described above. We have begun an R&D program which calls for a series of prototype pixel readout chips, each with specific engineering goals. We expect the final design to be realized using the radiation hard Honeywell 0.5μ CMOS SOI process. In this paper, we report the results of measurements made on our first test chip (FPIX0), the primary purpose of which was to establish an analog front end optimized for 132 ns between crossings. We also describe the design of our second test chip (FPIX1), which is the first implementation of a readout architecture which we believe can be extended to meet the requirements of the BTeV experiment. While this development effort is being driven by the specific needs of BTeV, we hope the final readout chip will be appropriate for use by any Tevatron collider experiment.

2 FPIX0

2.1 FPIX0 Design

The FPIX0 is a column based pixel readout chip with $50\mu \times 400\mu$ pixel cells arranged in an array of 64 rows by 12 columns. It was fabricated in the fall of 1997 using the HP 0.8μ CMOS process. The cell geometry was chosen to be compatible with test pixel sensors designed by the ATLAS collaboration(3). This first prototype pixel-detector readout chip was designed with three goals: 1) Establish a front end design appropriate for use at the Tevatron collider; 2) Verify that the analog and digital sections of the chip can be isolated from one another; 3) Verify that coupling through the sensor is not a problem (metal 3 is used as a shield between the sensor and the readout chip).

FPIX0 consists of an array of pixel unit cells together with relatively simple digital logic that provides a zero-suppressed readout of the chip. Each unit cell includes an amplifier with test input, a discriminator with programmable kill, a peak detector, and readout logic. The amplifier consists of two folded cascode stages, AC coupled to one another. The first stage is a charge amplifier that uses a current controlled feedback circuit(4). The feedback current controls the return to baseline time and compensates for sensor leakage current. The second stage provides additional gain and is DC coupled to the discriminator. The discriminator is a classic two stage comparator. When the discriminator fires, a set-reset flip-flop is set, and a fast-OR signal is asserted. Upon receipt of a token, the cell places its address on a global output bus, and connects the output of its peak detection circuit to a global analog output line. An

Fig. 1. Photograph of an FPIX0 bonded to one corner of an ATLAS test pixel sensor

externally controlled token-advance signal is used to release the token to the next hit pixel cell. This signal also causes the cell that releases the readout token to reset itself.

Two of the twelve columns contain amplifiers with lower first stage feedback capacitance (10 fF instead of 20 fF). These cells have higher gain than the standard cells, and correspondingly smaller dynamic range.

2.2 Mounting on Sensor

Four FPIX0 chips have been indium bump bonded (by Boeing North America, Inc.) to ATLAS test sensors manufactured by Seiko and CiS. Each sensor consists of an array of 160 rows by 18 columns of pixel cells. The FPIX0 chips have been bonded to one corner of the sensor array, as shown in Figure 1. Eleven of the twelve columns in FPIX0 are bonded to sensor pixels and one column is left unbonded. This allows us to compare the performance of bonded and unbonded cells in the same readout chip. Amplifier and discriminator outputs from one row of pixel unit cells are routed directly to pads on two sides of the FPIX0. The outputs from four of these cells are accessible in the bonded assembly (the rest are obscured by the sensor). These include three cells bonded to sensor pixels and one unbonded cell.

All of the measurements reported here were made on a single FPIX0 bonded to an ATLAS test sensor manufactured by Seiko. For all of these measurements,

Fig. 2. Terbium x-ray spectrum recorded by a single FPIX0 channel

the sensor bias voltage was set to -75 V, which is well beyond the full depletion voltage of approximately -45 V.

2.3 Scale calibration

Fluorescence x-rays from a number of metal foils were used to provide an absolute calibration of the FPIX0. Figure 2 shows the pulse height spectrum collected using one of the direct amplifier outputs while the sensor was being illuminated with Terbium x-rays. The Kα_1 peak (44.5 keV) is easily identified at 407 mV. Since it is known that a 44.5 keV x-ray creates 12300 mobile e-hole pairs in fully depleted silicon, the scale for this channel is 30.2 input electrons per mV peak output signal. We have verified the linearity of the FPIX0 amplifier response to small input signals using a variety of characteristic x-rays.

The x-ray spectra obtained using the three direct amplifier output signals also allow us to interpret the response to an injected test signal in terms of electrons input to the amplifier, or equivalently, to determine the value of the charge injection capacitor. This, in turn, allows us to interpret discriminator threshold scans of all of the pixel cells in the array in absolute terms (assuming only that $C_{injection}$ is the same for all cells). It also allows us to interpret the dynamic range of the amplifier in terms of the equivalent input in electrons. For FPIX0 cells with $C_f = 20$ fF, the dynamic range is approximately 52000 electrons at the input.

2.4 Amplifier Noise and Discriminator Threshold Dispersion

A discriminator threshold scan was performed for each pixel cell by holding the discriminator threshold constant, and scanning the injected test pulse voltage through the threshold. The fraction of the time that the discriminator fired was recorded for each value of the injected pulse. The resulting curves were fit to the integral of a Gaussian noise distribution, yielding an rms noise and discriminator threshold (50%-point). The rms of the discriminator threshold distribution was calculated directly from these 50%-points.

Figure 3 shows noise distributions inferred from these measurements for three columns of pixel cells. The top histogram corresponds to a column of bonded pixel cells with the higher gain version of the amplifier. The middle histogram is for a standard gain bonded column. The bottom histogram shows the noise of an unbonded column of standard gain pixel unit cells. Two conclusions can be drawn. First, there is a trade-off between the larger dynamic range associated with the standard front end, and the lower noise and reduced discriminator threshold dispersion of the higher gain front end. Second, the bonded cells are only slightly noisier than identical unbonded cells. If all of this noise difference is attributed to the difference in input capacitance, then a SPICE simulation indicates that the total input capacitance of the sensor pixel and bump bond is approximately 180 fF.

2.5 Pickup and Cross Talk

No pickup of the digital activity associated with readout has been detected. With the metal 3 shield grounded, there is no significant coupling through the detector. The capacitance between the metal 3 shield and a sensor pixel has been inferred to be approximately 1.8 aF/μ^2. This capacitance was inferred by disconnecting the shield from its ground, injecting a pulse on the shield, and measuring the output voltage from a single pixel unit cell.

We have measured the pixel-to-pixel cross talk both in the short direction of the pixel cells, and in the long direction. When a pulse is injected into an FPIX0 front end which is bonded to a sensor pixel, the neighboring cell in the long direction registers a signal $\sim 2\%$ as large as the cell which received the charge injection. When an unbonded cell is selected, the cross talk to the neighbor in the long direction is $\sim 1\%$. This indicates that the cross talk through the sensor is $\sim 1\%$. We believe that the balance of the cross talk occurs through the charge injection network itself. In our next prototype pixel readout chip (FPIX1), we have modified the layout of the charge injection network to reduce the cross talk.

Fig. 3. Amplifier noise inferred from discriminator threshold scans (rms variations in discriminator thresholds are also given).

3 Test Beam Plans

Simulations done by the BTeV collaboration(5) indicate that a significant improvement in point resolution over binary readout can be obtained by a very coarse digitization of the analog information. Figure 4 shows the calculated resolution obtainable with 50 μ wide pixel cells as a function of track angle, assuming binary readout, and two and four bit analog readout. The resolution expected with a four bit ADC is only slightly better than the resolution expected with a two bit ADC. Based on this result, we have decided to include a two bit flash ADC in the FPIX1 unit cell. FPIX0 chips bonded to ATLAS sensors will be used in beam tests during the 1999 Fermilab fixed target run to verify these simulations, and to perform general studies of the use of pulse height information to improve spatial resolution.

4 Pre-FPIX1

In order to gain experience with the HP 0.5μ process in which FPIX1 will be fabricated, we submitted a small scale design in early 1998 called Pre-FPIX1. This circuit contained 9 columns of pixel unit cells, each with 20 identical cells. Each column contained a different version of the front end tested in FPIX0. In three of the columns, a single stage amplifier was AC coupled to a discriminator. Three more contained a two-stage amplifier as in FPIX0, but AC coupled to a discriminator. The remaining three contained a two-stage amplifier, DC coupled to a discriminator. For each front end type, there was one column with C_f = 5 fF, one with C_f = 10 fF, and one with C_f = 20 fF. Noise and threshold dispersion measurements were made using the discriminator scan method described above. The results are shown in Table 1. As can be seen in the table, the lower gain of the single stage designs resulted in significantly larger discriminator threshold dispersion. AC coupling to the discriminator (which would be required for a single stage design) did not yield a significant advantage over DC coupling for the two-stage designs. Based on these results, we decided that the FPIX1 pixel unit cell should contain a two-stage amplifier, DC coupled to a discriminator (the same configuration as FPIX0).

5 FPIX1

The FPIX1 readout chip, which was submitted for fabrication on October 28, 1998, is the first implementation of a new readout architecture designed for use at the Fermilab collider. Each pixel hit is associated with a six-bit time

Fig. 4. Expected spatial resolution as a function of track angle for 50 μ wide pixel cells. The different curves are for binary readout, and for analog readout with a two and four bit ADC.

Table 1
Pre-FPIX1 amplifier noise and discriminator threshold rms measurements

number of amp stages	C_f (fF)	disc. coupling	amp noise (e^-)	disc. threshold rms (e^-)
1	5	AC	37	720
1	10	AC	43	1132
1	20	AC	52	2286
2	5	AC	32	135
2	10	AC	41	229
2	20	AC	47	387
2	5	DC	32	167
2	10	DC	38	214
2	20	DC	48	304

stamp (the beam crossing number) and the hit information is stored in the pixel unit cell until being read out or reset. Two readout modes are provided: an externally triggered mode, in which external logic requests the readout of hits associated with a specific time stamp, and a continuous readout mode, in which the chip itself generates a trigger for *every* beam crossing. The time stamp is not held in the hit pixel cell, but rather in a register located at the End of the Column (EOC) of pixels. All pixels in a given column which are hit in the same 132 ns beam crossing are associated with the same End of Column (EOC) timestamp register. In FPIX1, each column has four EOC timestamp registers, each associated with command generating logic in an "EOC command set." This indirect addressing principle is similar to that proposed by Wright, *et al.*(6).

A schematic diagram of the FPIX1 layout is given in Figure 5. FPIX1 is composed of three mutually dependent building blocks: the pixel unit cell, the end of column logic, and the chip control logic. The active area is designed to match an ATLAS pixel sensor of the type described above, and consists of an array of 160 rows by 18 columns of pixel cells, each $50\mu \times 400\mu$. All "normal" chip I/O is through a double row of pads (shown along the bottom in Figure 5). The opposite side of the chip is used to provide direct access to amplifier and discriminator outputs from one row of pixel cells. In addition, one column of pixels is designed to be read out under external control.

Fig. 5. FPIX1 Floor Plan

5.1 Pixel Unit Cell

A block diagram of the pixel unit cell is given in Figure 6. The front end is very similar to the FPIX0 front end described above. An 8 fF feedback capacitor is used in the first stage of the amplifier. This will result in a dynamic range of approximately 32000 e^-. The discriminator threshold dispersion should be significantly reduced with respect to FPIX0.

The flash ADC consists of three comparators (identical to the comparator used in the discriminator) directly connected to set-reset flip-flops. The four thresholds are input to the chip as DC levels, and are common to all pixel cells. During readout, tri-state buffers connect the outputs of the ADC flip-flops to the chip control logic, where they are encoded into two bits. The digital section of the pixel unit cell consists of a command interpreter, and a bus controller. The command interpreter has four inputs, corresponding to the four EOC

Fig. 6. The FPIX1 Pixel Unit Cell

sets. Four commands are used: “idle,” “reset,” “output,” and “look for data.” Commands are presented by the EOC logic simultaneously to all pixel cell command interpreters in a column. If one of the EOC sets is asserting the “look for data” command, and a discriminator fires, the command interpreter in that cell associates itself with the EOC set that is issuing the “look for data” command. Simultaneously, it alerts the EOC logic to the presence of a hit via the wire-OR’ed “Hit Fast-OR (HFastOR)” signal. After this association to a particular EOC set has been made, the command interpreter in the hit pixel cell ignores commands from all other EOC sets. The pixel hit information is stored in the unit cell until the associated EOC set issues an “output” or “reset” command.

When the associated EOC set issues the “output” command, the command interpreter issues a bus request and asserts the wire-OR’ed “Readout Fast-OR (RFastOR)” signal. This operation is executed independent of the readout clock. The balance of the readout proceeds synchronous with the readout clock. The EOC logic provides a column token on the bottom of the column. The token quickly passes empty pixel unit cells, and stops when it reaches a cell that is requesting the column bus. At the next rising readout clock edge, the hit pixel cell with the column token loads its data onto the column bus and drives it to the EOC logic for one readout clock cycle. In parallel, the column token is transmitted to the next hit pixel. This allows the readout of one pixel cell per readout clock cycle. As a hit pixel is read out, it resets itself and withdraws its assertion of the RFastOR signal. RFastOR returns to its inactive state just after data from the last hit pixel in the column is placed

Fig. 7. FPIX1 End of Column Logic

on the readout bus.

At any given time, only one EOC set is permitted to broadcast the “look for data” command. This ensures that hit pixel cells are associated with only one EOC set. Pixel cells that have not been hit continue to monitor all four EOC sets, waiting for a hit to occur in coincidence with a “look for data” command. If a pixel is hit and no EOC set is issuing the “look for data” command, the hit is ignored.

The “throttle” input allows the data acquisition system to command the FPIX1 to disregard new hit data (creating dead time, but no data bias) when the hit rate exceeds the readout bandwidth, threatening loss of data. While “throttle” is asserted, the pixel cell command interpreters are disabled and no new data is latched in the chip.

5.2 End of Column Logic

Figure 7 shows a block diagram of the EOC logic. It consists of a priority encoder, a token and bus controller, and four EOC command sets. The EOC sets themselves consist of a timestamp register, a state machine that generates the commands, and two comparators.

The priority encoder selects one idle EOC set to issue the “look for data” command. When there is a hit somewhere in the column, the HFastOR signal is asserted by the hit pixel. The state machine inside the assigned EOC set responds by storing the Current Beam Crossing number (CBCO) in its EOC timestamp register. This latched number is then referred to as the Stored Beam Crossing number (SBCO). The state machine changes its command from "look for data" to "idle" at the next rising edge of the BCO clock. The priority encoder assigns the next available EOC set to issue the "look for data" command to the column at the next rising edge of the BCO clock. This ensures that all pixels in a given column that are hit in one beam crossing are associated with a single EOC set. Since the EOC logic has four EOC sets, pixel cells in the column can be hit without loss of data in four different crossings before any data is read out.

A hit EOC set waits for matches with its stored timestamp. If the match is between SBCO and the Requested BCO (RBCO, see section 5.3), the EOC set broadcasts the "output" command. If the match is between SBCO and the Current BCO (CBCO), it broadcasts the "reset" command. The comparison between SBCO and CBCO can be programmed to allow a user-defined reset delay (by ignoring some of the bits in the comparison). This feature is designed primarily for the externally triggered readout mode.

The token and bus controller manages access to the chip-wide EOC data bus as well as its associated column bus. Conflicts between the various EOC token and bus controllers are arbitrated by an EOC token. As soon as an EOC set issues the "output" command, the token controller releases the column token to the column, and waits for the EOC token. When the EOC token is received, the bus controller connects the column bus to the chip-wide data bus. The early release of the column token, before the EOC token is received, allows pixel data to be asserted on the chip-wide bus as soon as the EOC token arrives at a column containing hit data. When the RFastOR signal returns to the inactive state, indicating that the transfer of data from the last hit pixel in the column has begun, the token and bus controller releases the EOC token. This allows the EOC token to reach the next hit column in time to insure that control of the chip readout bus is transferred and readout proceeds without an empty readout clock cycle.

5.3 Chip Control Logic

The chip control logic (Figure 8) consists of chip programming logic, counters which hold the current and requested beam crossing numbers, a readout controller, and multiplexers. The Current Beam Crossing number (CBCO) increments synchronously with the externally supplied Beam Crossing Clock, and is delivered to the EOC logic. Depending on which readout mode is being used (external trigger or continuous), either the internally generated or the

Fig. 8. FPIX1 chip control logic

externally supplied Requested Beam Crossing number (RBCO) is delivered to the EOC logic to initiate readout. The RBCO counter used in the continuous readout mode is incremented by the readout clock, and is forced to lag two counts behind the CBCO, in order to allow time for hit data to settle in the pixel unit cells. After the readout of an event, the RBCO quickly increments (at the readout clock frequency) until another event with hit data is reached, or the RBCO reaches two counts behind the CBCO.

Other functions of the chip control logic include external bus arbitration (using another token) and control of the configuration of the chip. The chip configuration is programmed using a serial bit stream to set features such as the pixel cell kill pattern (used to disable noisy pixels) and pulse injection select.

5.4 FPIX1: Final Remarks

The FPIX1 uses a low voltage differential swing convention to provide maximum common noise immunity for all clocks and outputs. The pixel address and two bit ADC information are read out in one readout clock cycle onto a parallel bus. Simulations indicate that FPIX1 will be able to read out an average of ~ 3 pixel hits per 132 ns crossing time. This is fast enough to meet the nominal BTeV requirement of an average readout rate of 1.25 pixel hits per 132 ns, but does not provide a comfortable margin over the specification. A straightforward redesign of the column token logic using multiple tokens should increase the readout rate to ~ 10 pixel hits per crossing. If clusters of four pixels are read out instead of individual pixels, the readout rate could be as high as 40 pixels per crossing.

6 Summary

This paper has described the R&D effort underway at Fermilab to develop a pixel readout chip for use by BTeV at the Fermilab Tevatron collider. A front end design with all of the desired properties has been established. Beam tests planned for the 1999 Fermilab fixed target run should allow a decision to be made on how best to process pixel pulse height information to achieve optimal spatial resolution. Finally, we have just submitted a prototype chip which is the first implementation of a new readout architecture designed to facilitate the use of pixel information in the earliest stages of on-line event selection.

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