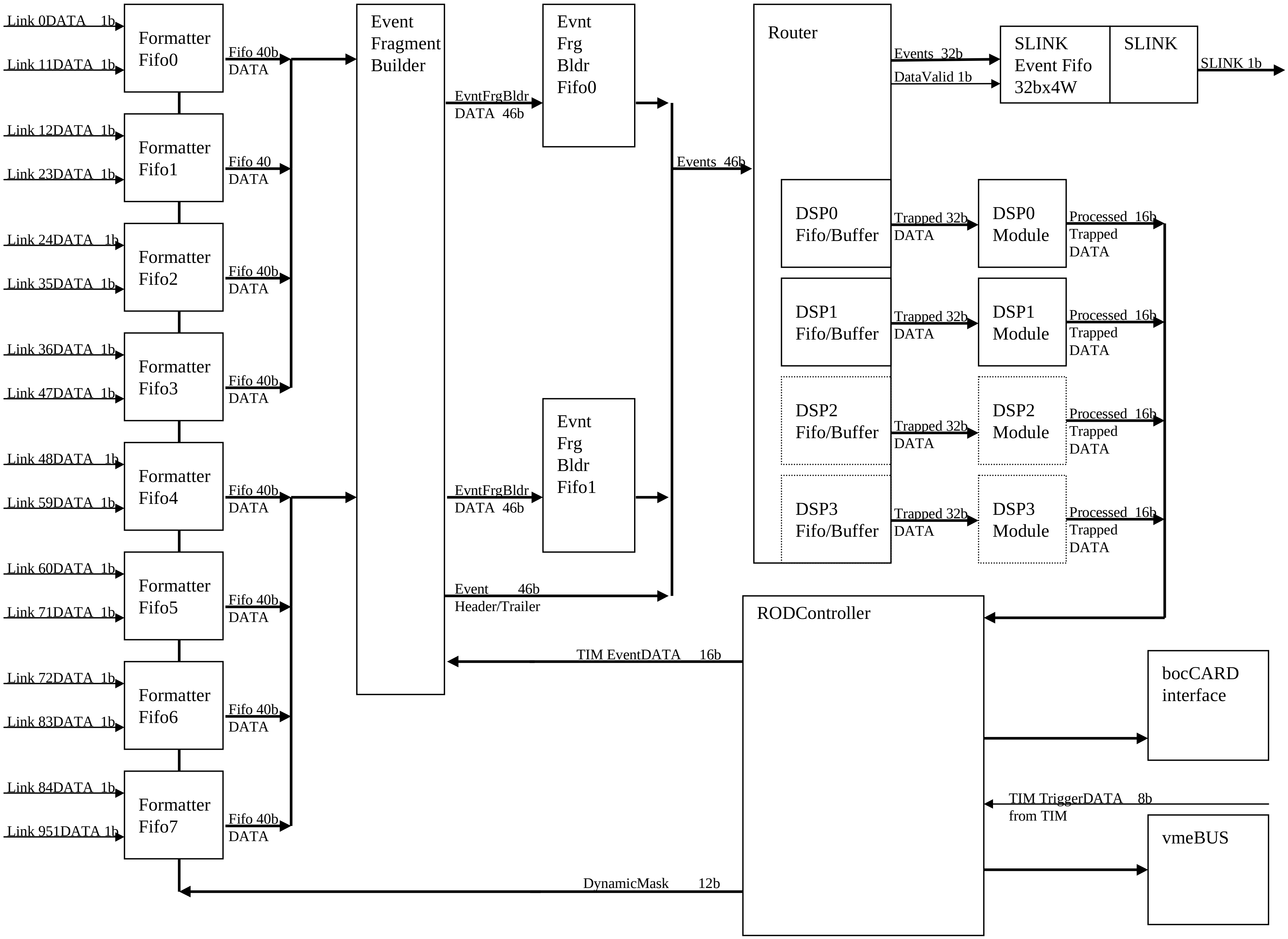
FPGA ROD
Implementation Model #2

Atlas - Wisconsin Group

Khang Dao, Damon Fasching, Richard Jared, John Joseph, Mark Nagel, Linda Stromburg and Lukas Tomasek

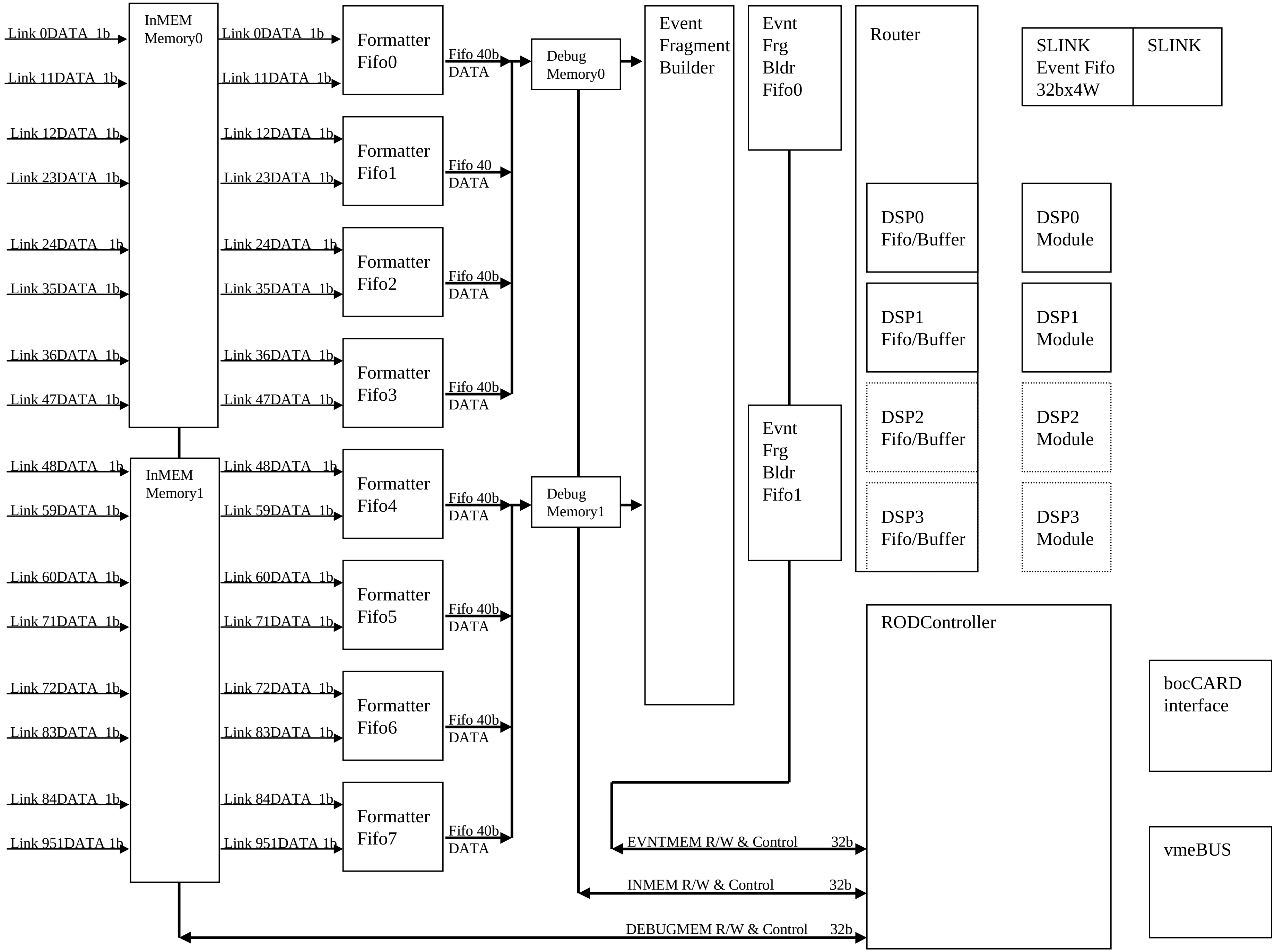
December 17, 1999

Model #2 96Link ROD Event DataPath



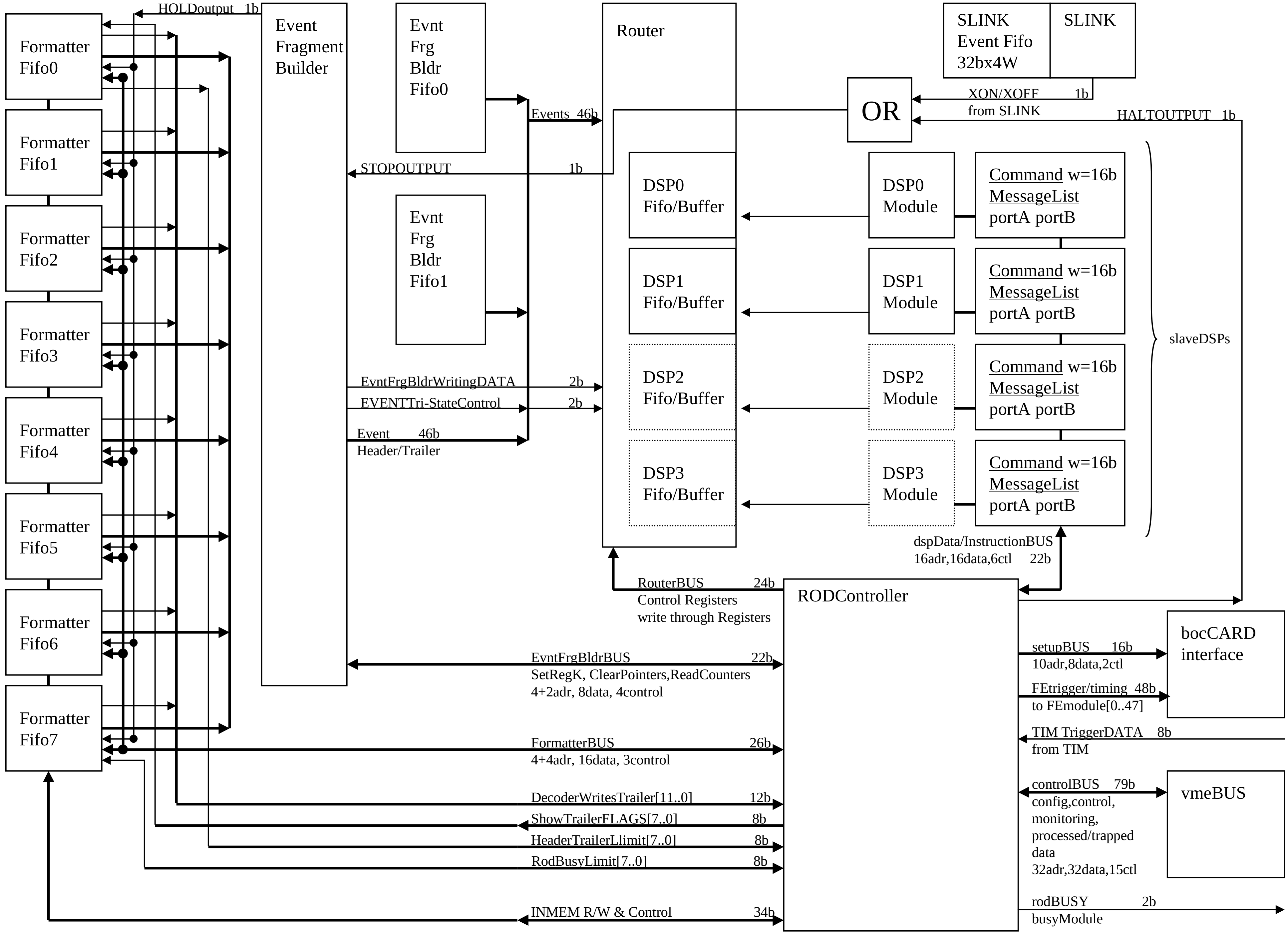
NOTE: Some signals have been omitted for clarity

Model #2 96Link ROD DebugPath



NOTE: Some signals have been omitted for clarity

Model #2 96Link ROD ControlPath



NOTE: Some signals have been omitted for clarity

FPGA ROD
Implementation Model #2
Formatter/Fifo

Atlas - Wisconsin Group

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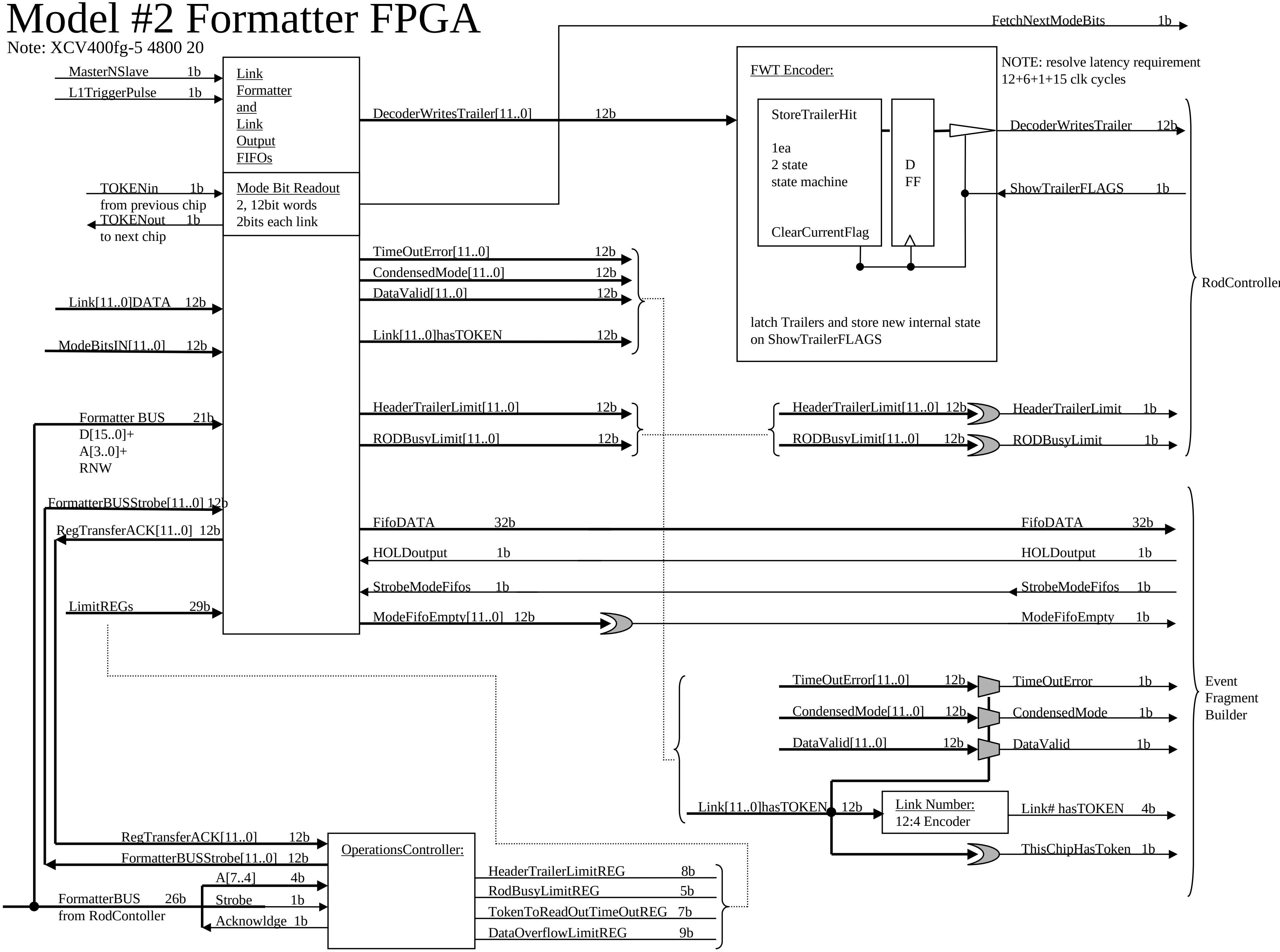
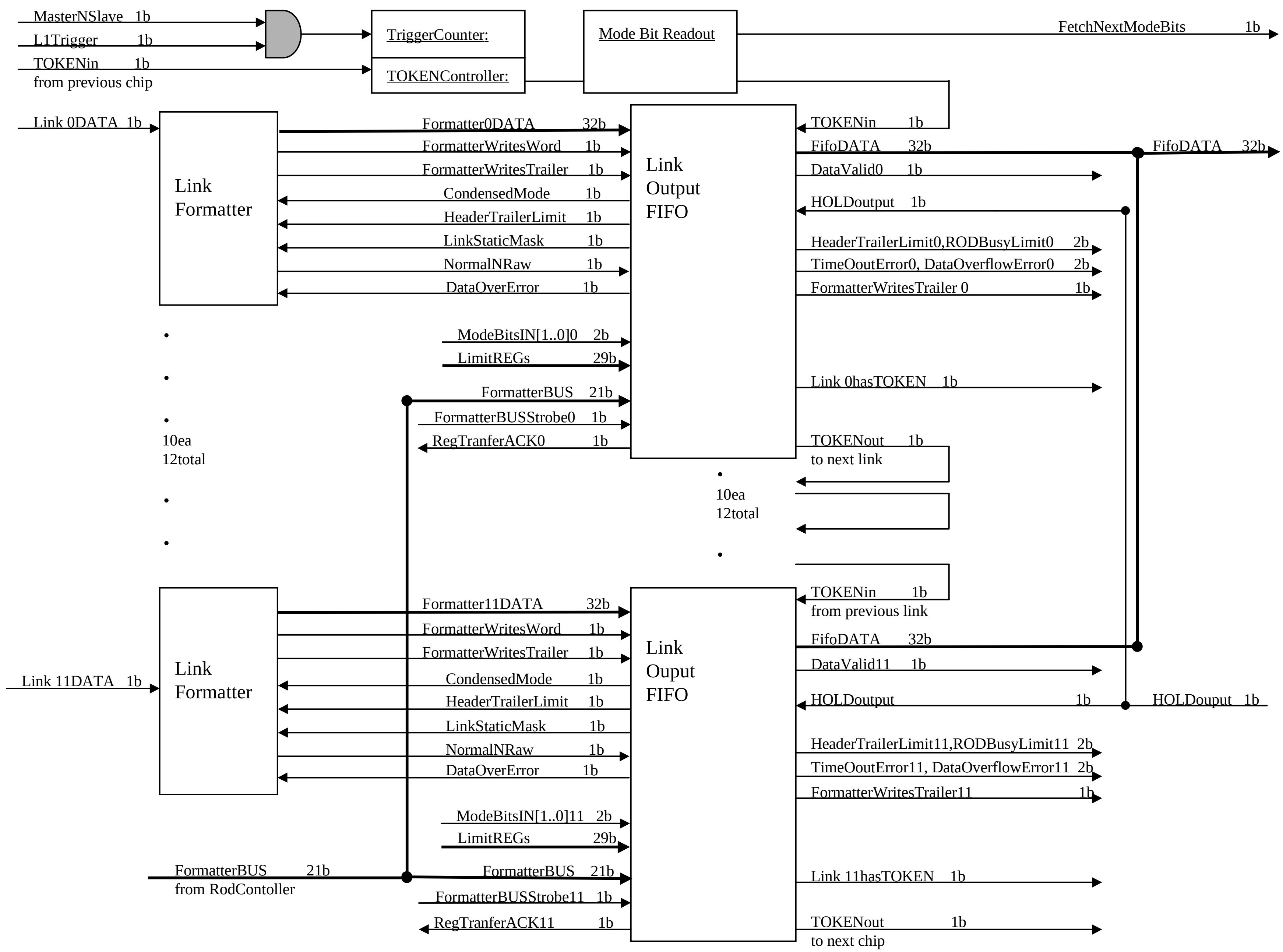
Model #2 Formatter FPGA

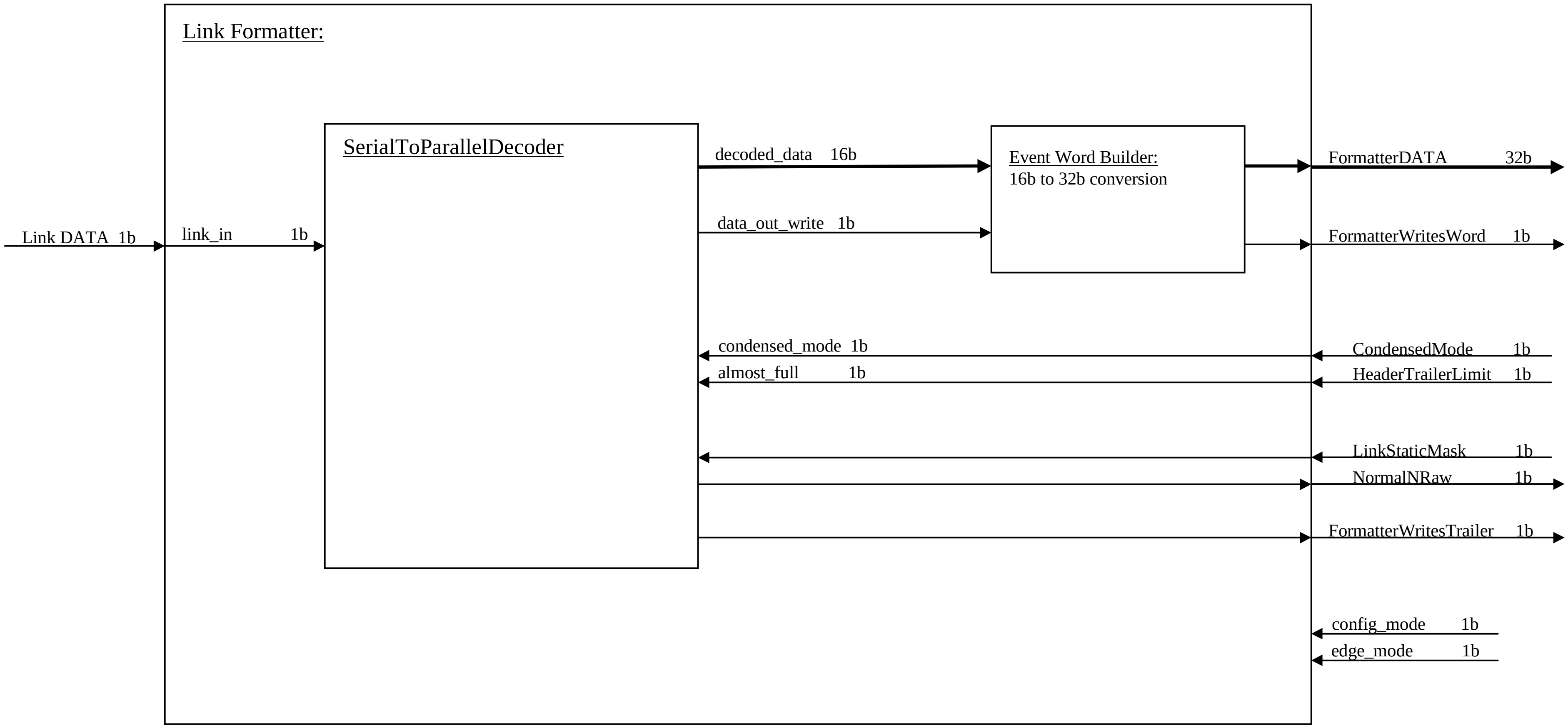
Note: XCV400fg-5 4800 20



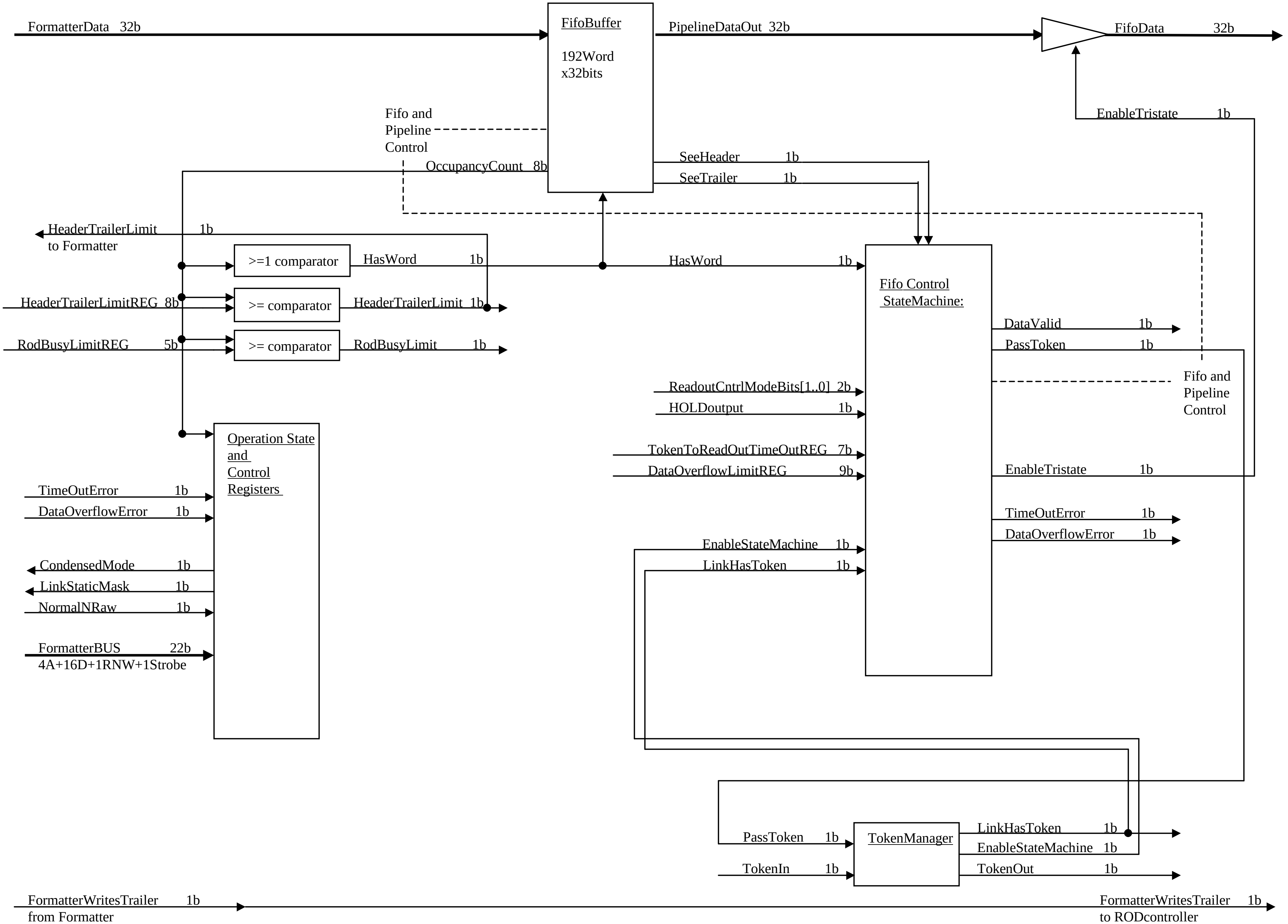
Model #2 Formatter FPGA: Link Formatter and Link Output FIFO



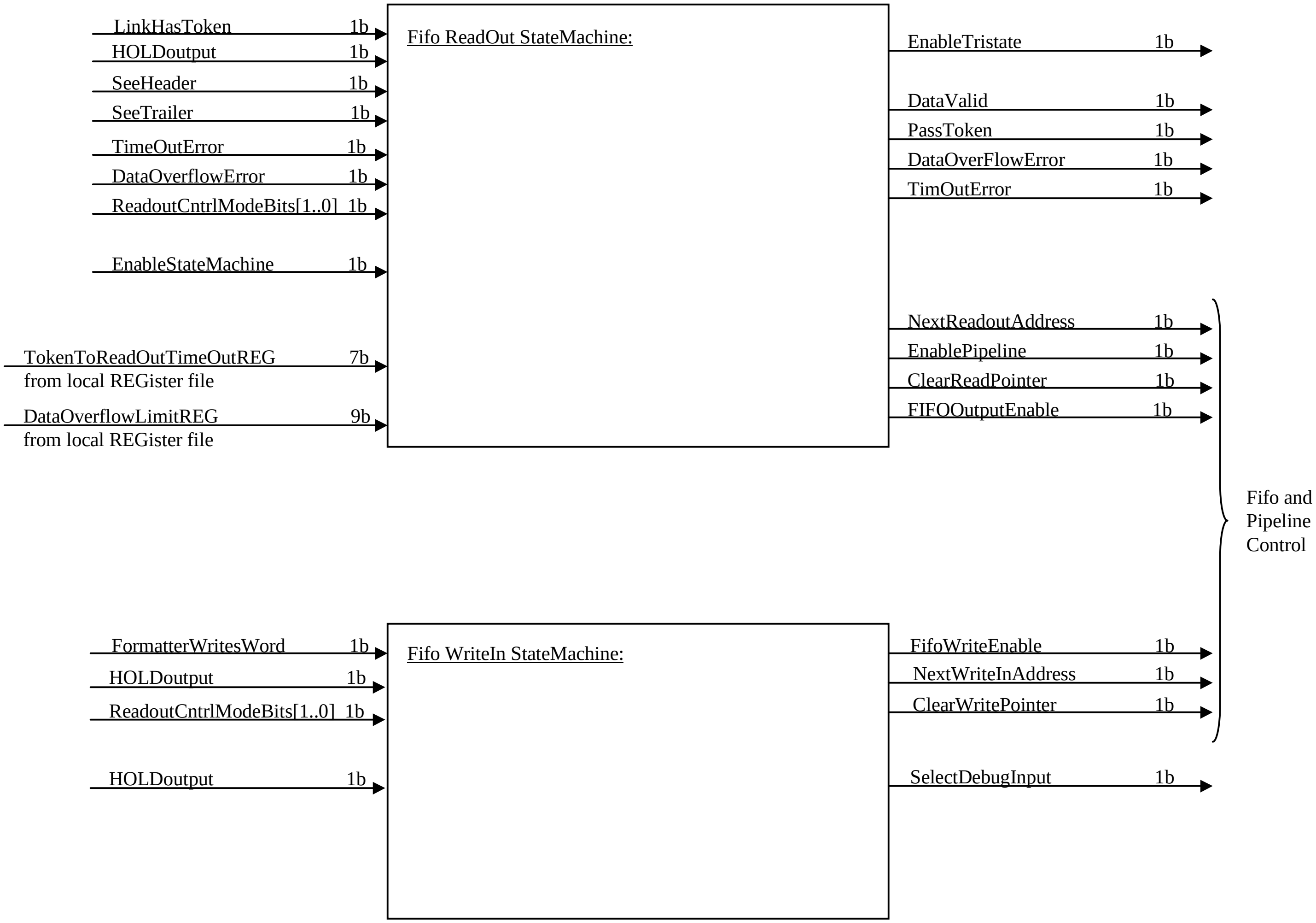
Model #2 Formatter FPGA: Link Formatter



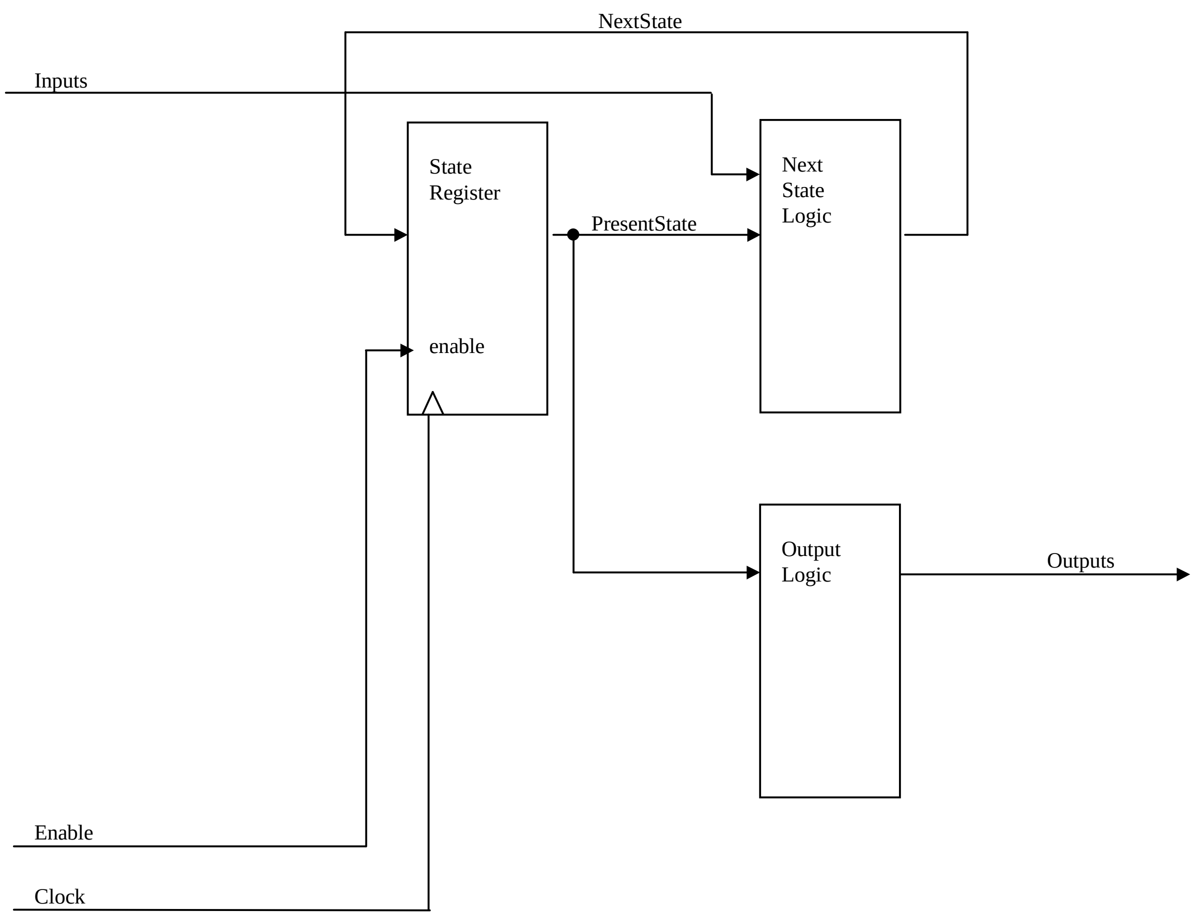
Model #2 Formatter FPGA: Link Output FIFO



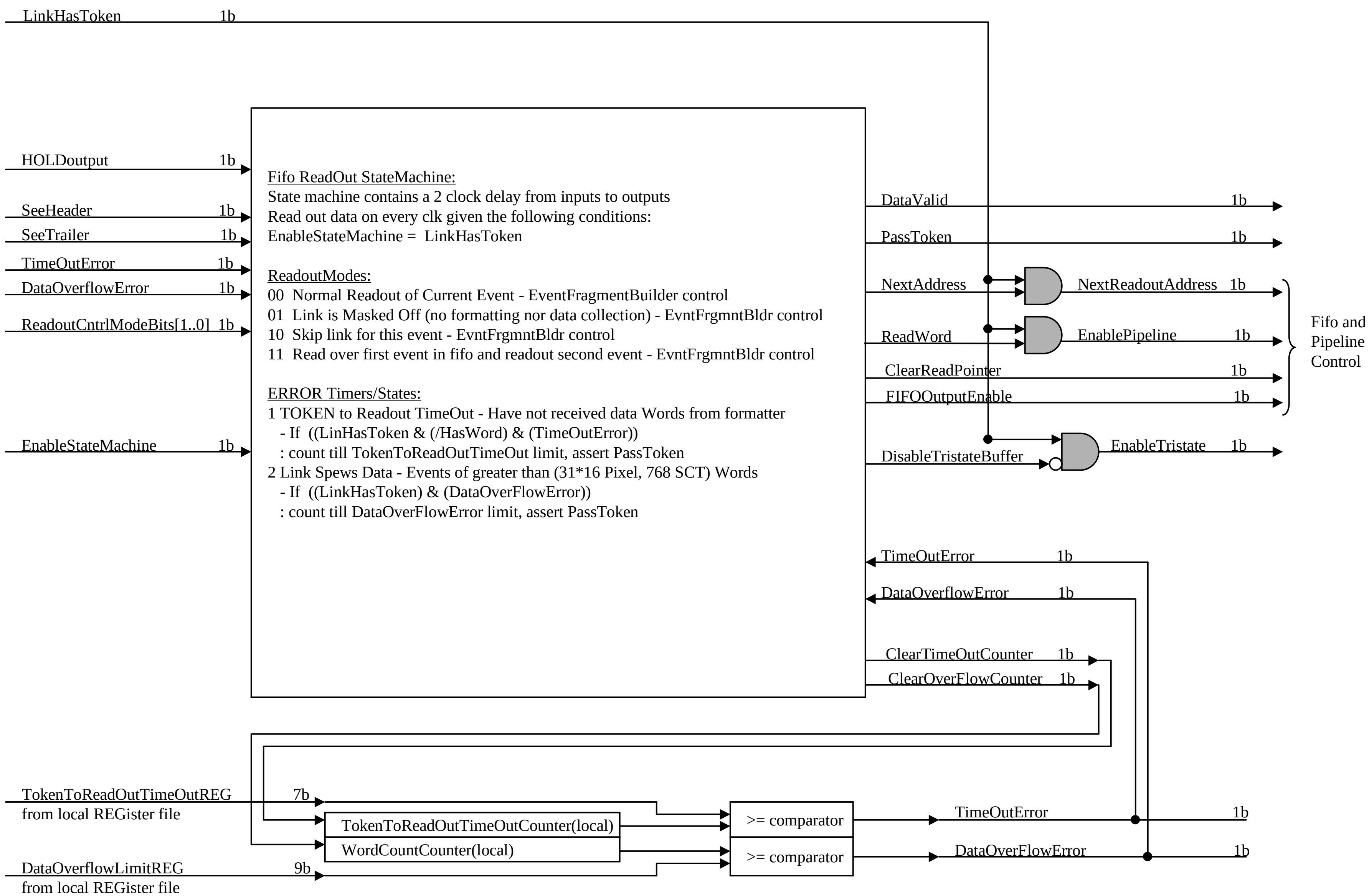
Model #2 Formatter FPGA: FIFO Control StateMachine and Signals



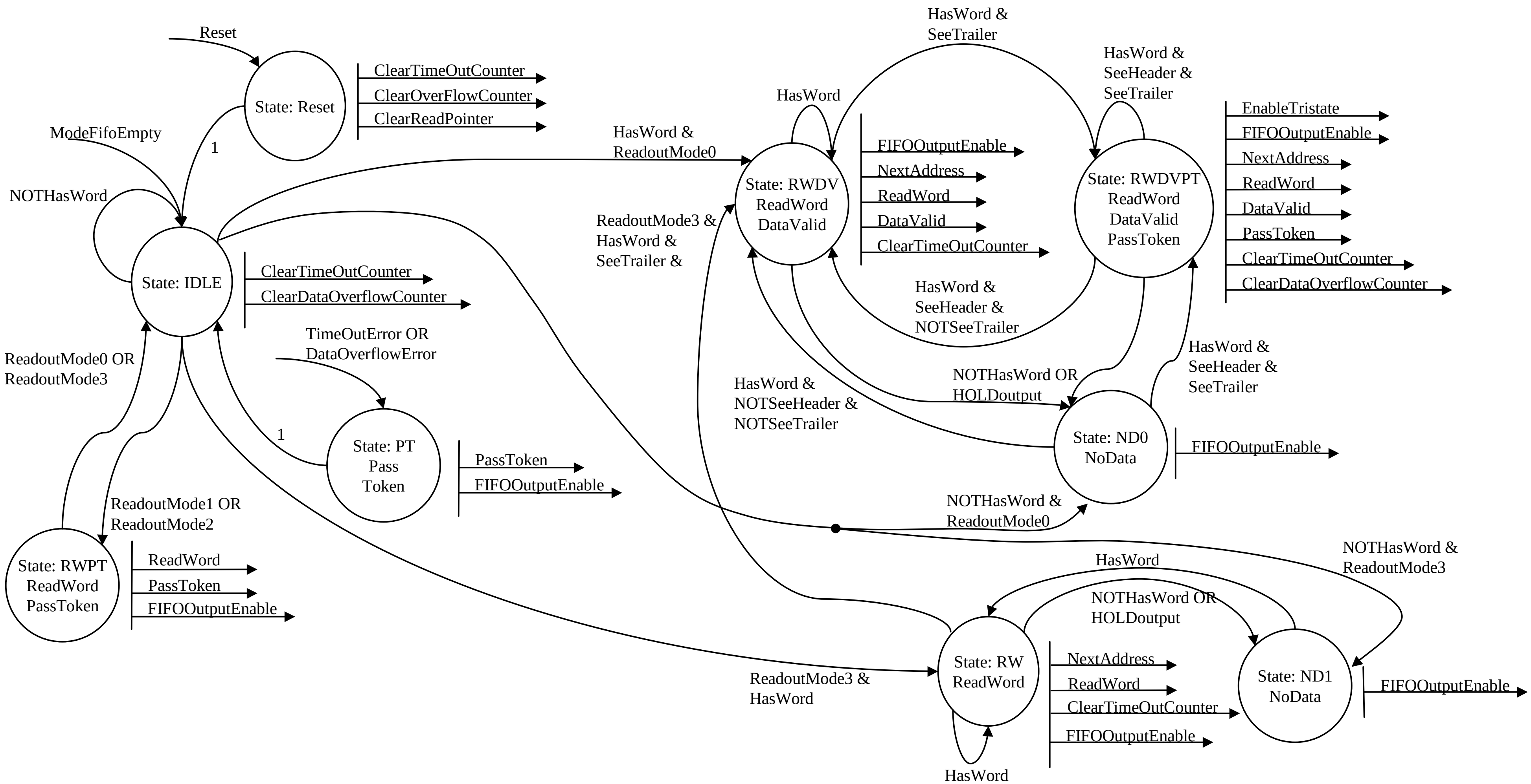
Model #2 Formatter FPGA: FIFO StateMachine Structure



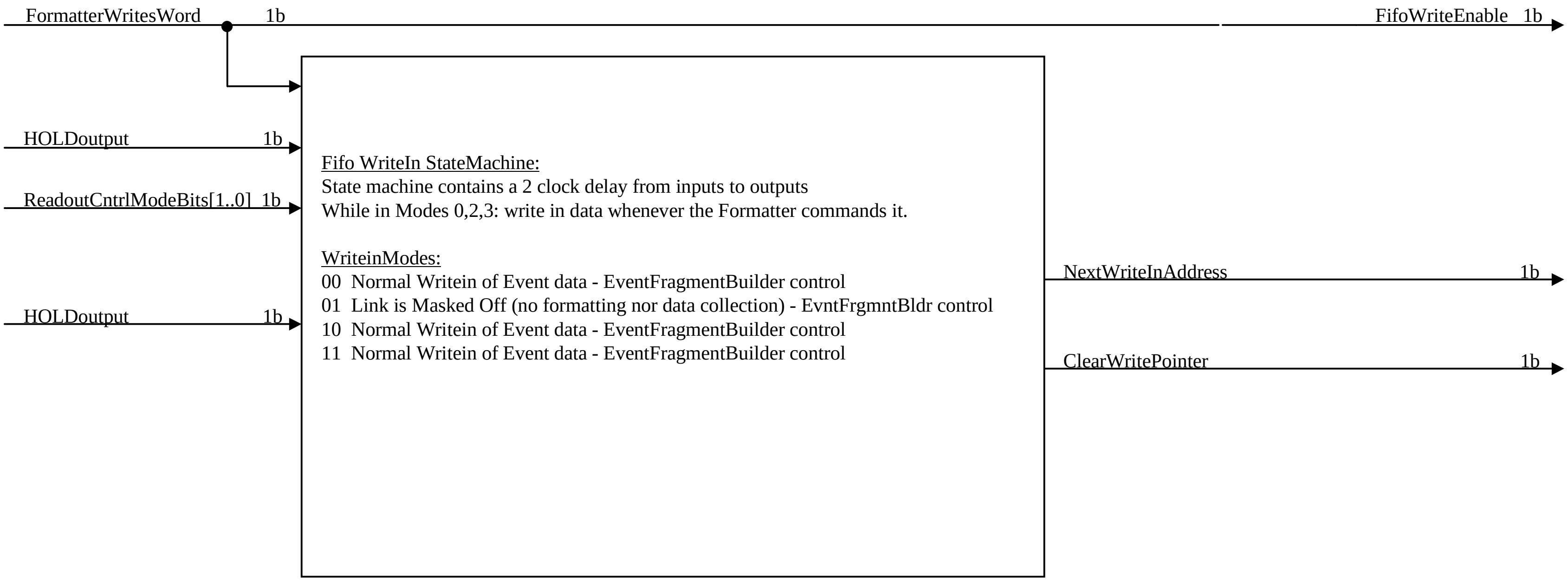
Model #2 Formatter FPGA: FIFO ReadOut StateMachine and Signals



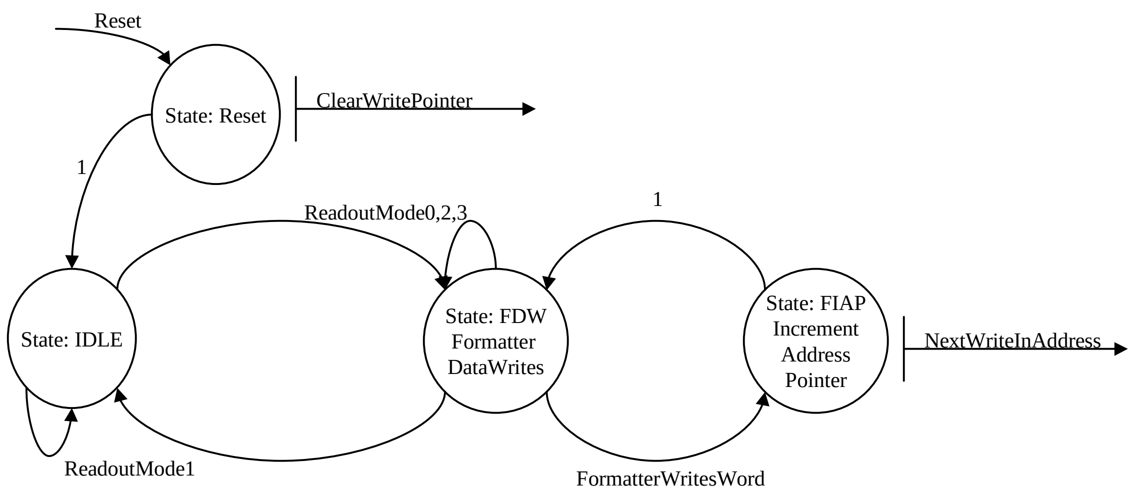
Model #2 Formatter FPGA: FIFO ReadOut StateMachine State Diagram



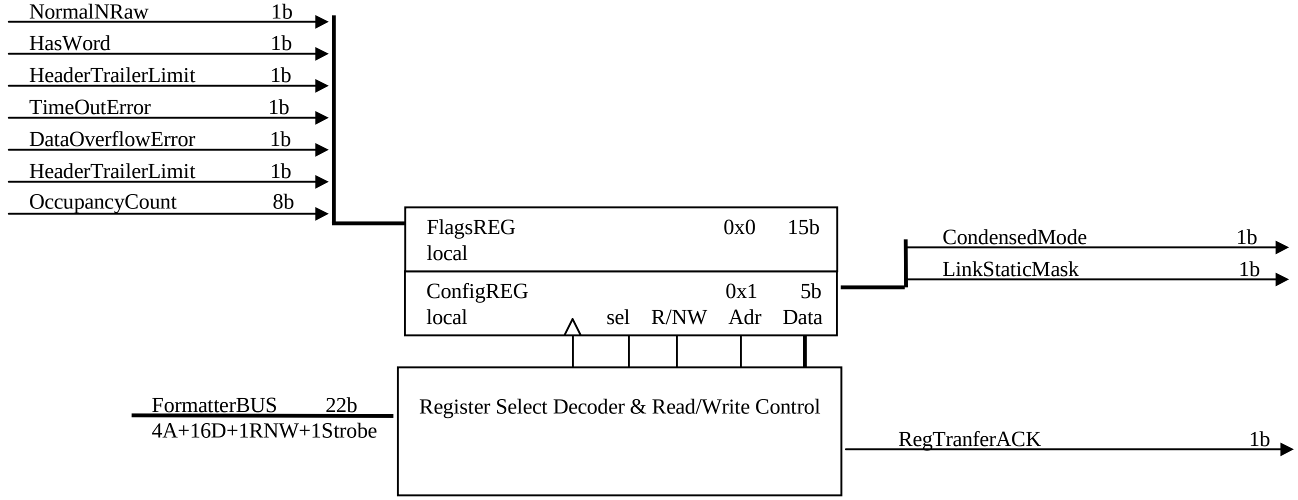
Model #2 Formatter FPGA: FIFO WriteIn StateMachine and Signals



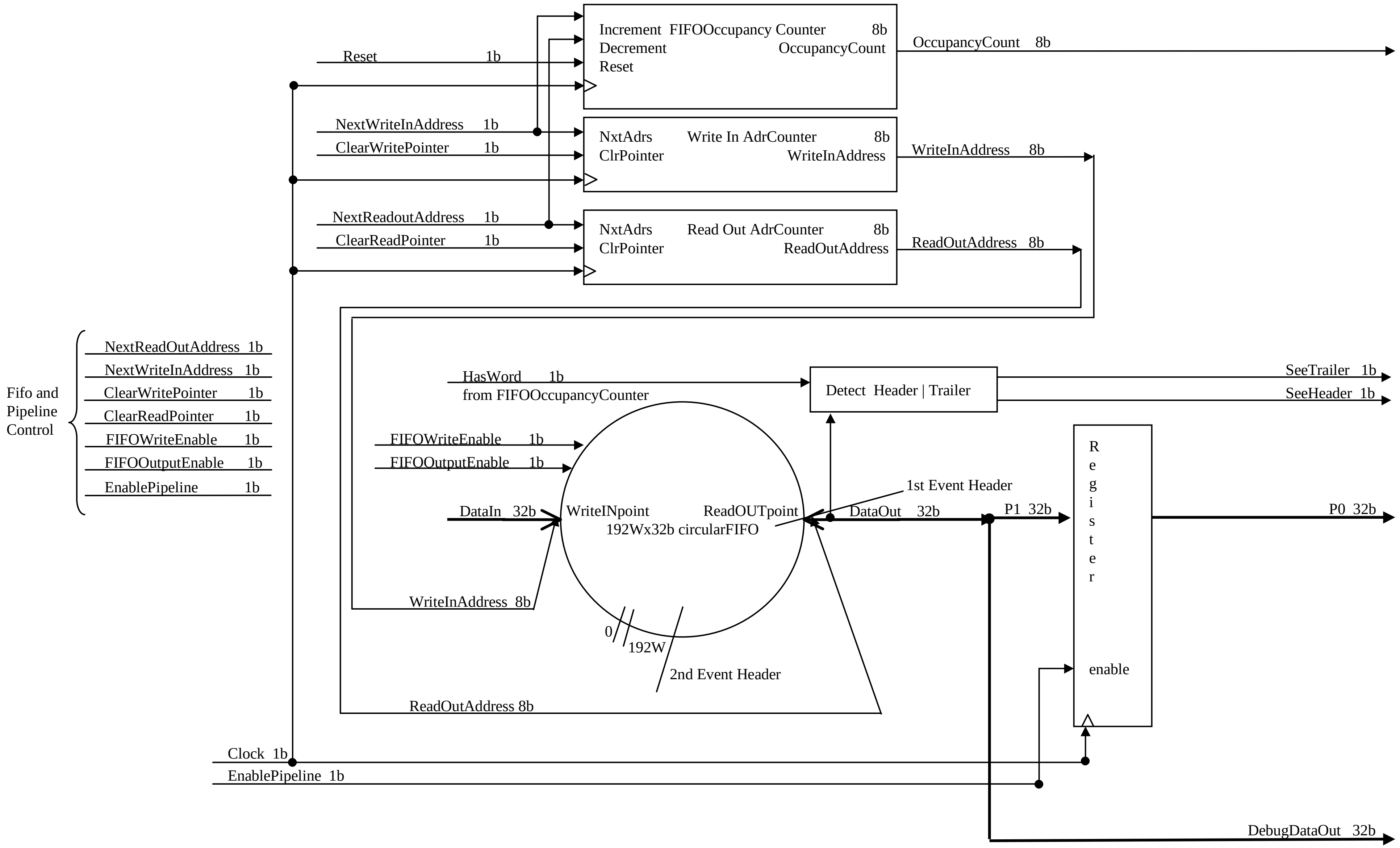
Model #2 Formatter FPGA: FIFO WriteIn StateMachine State Diagram



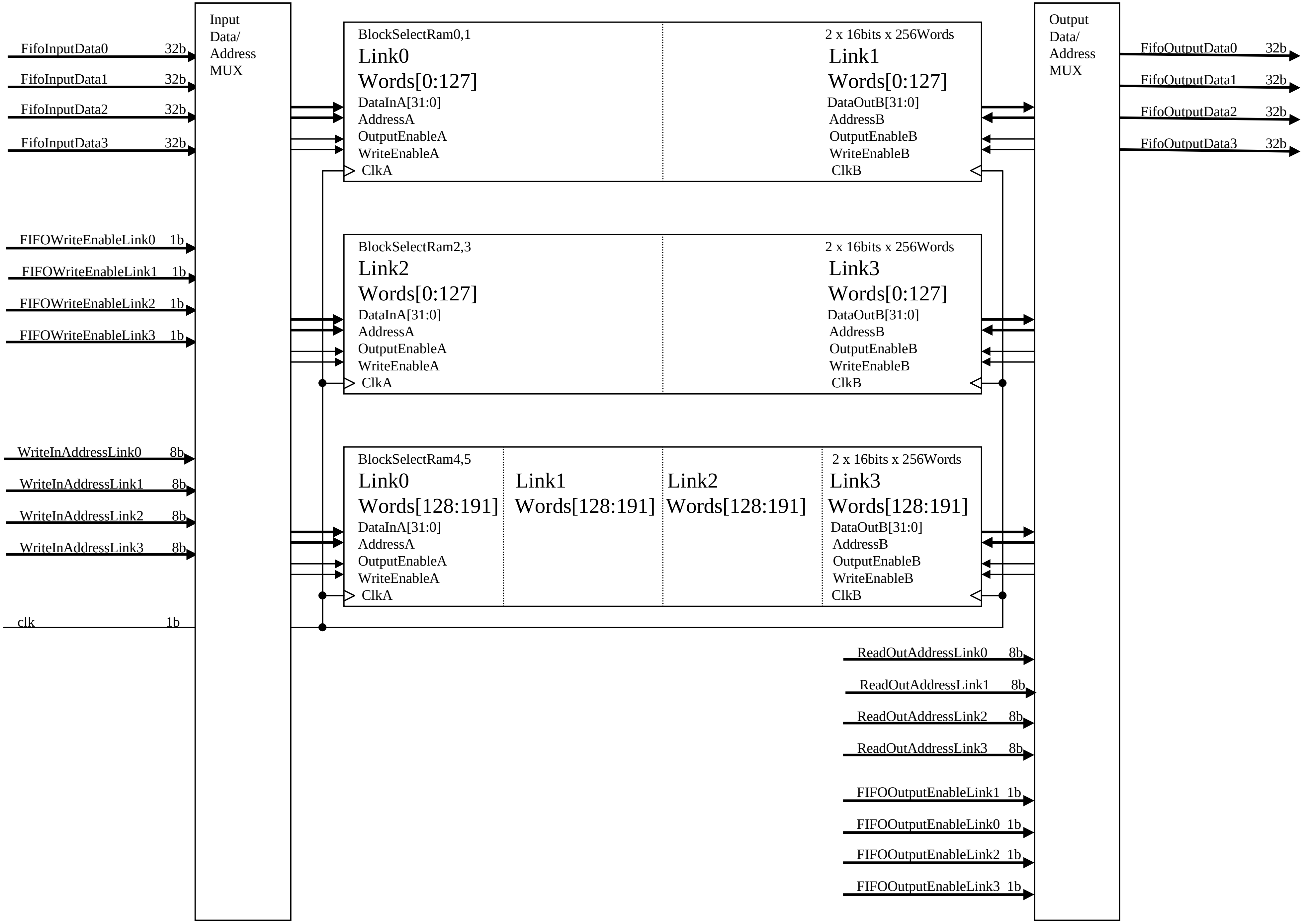
Model #2 Formatter FPGA: Operation State and Control Registers Block



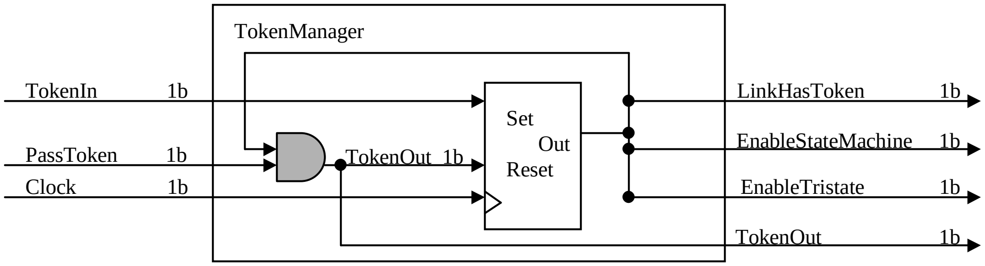
Model #2 Formatter FPGA: FIFO Buffer



Model #2 Formatter FPGA: 192Word Circular FIFO

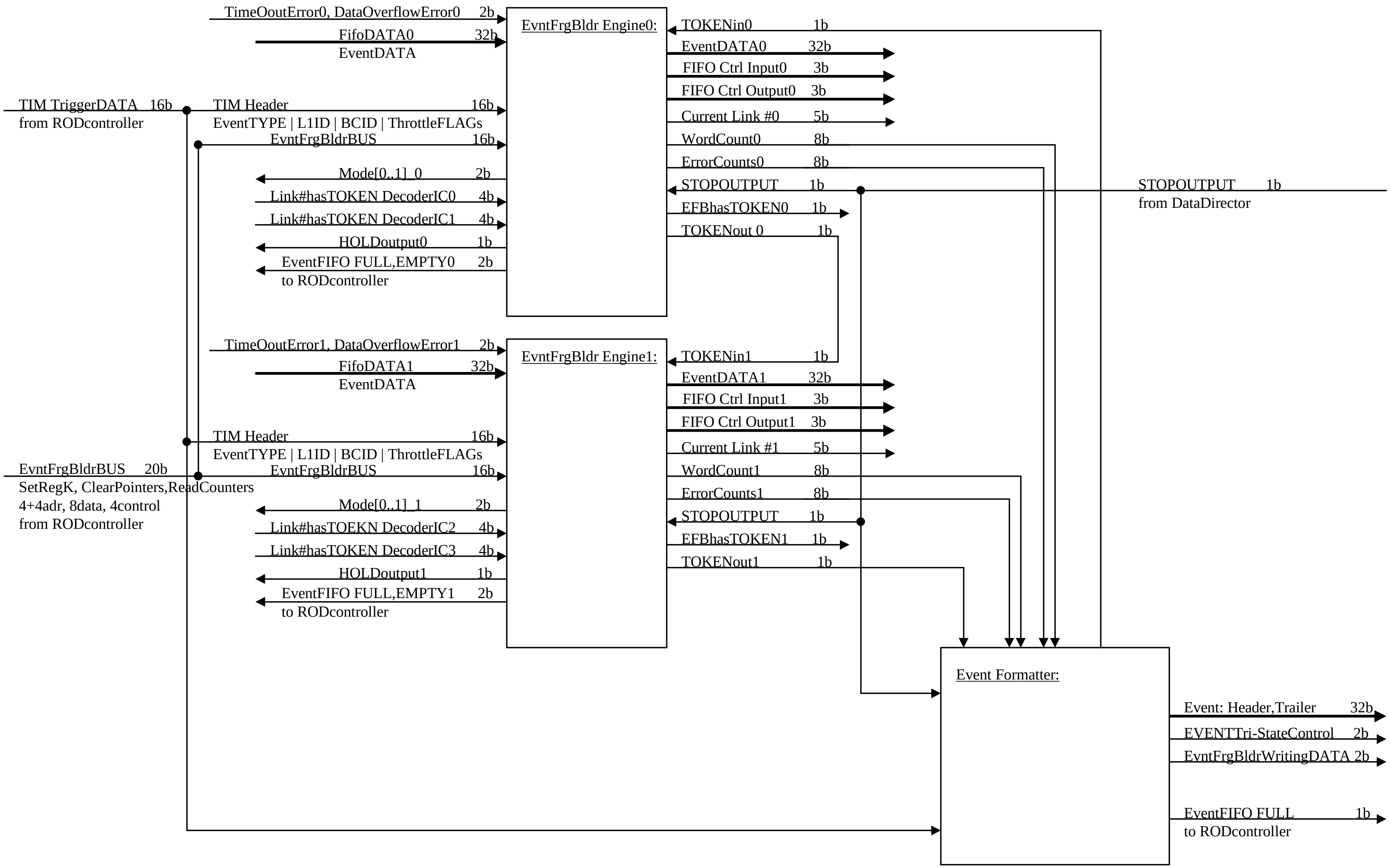


Model #2 Formatter FPGA: Token Manager

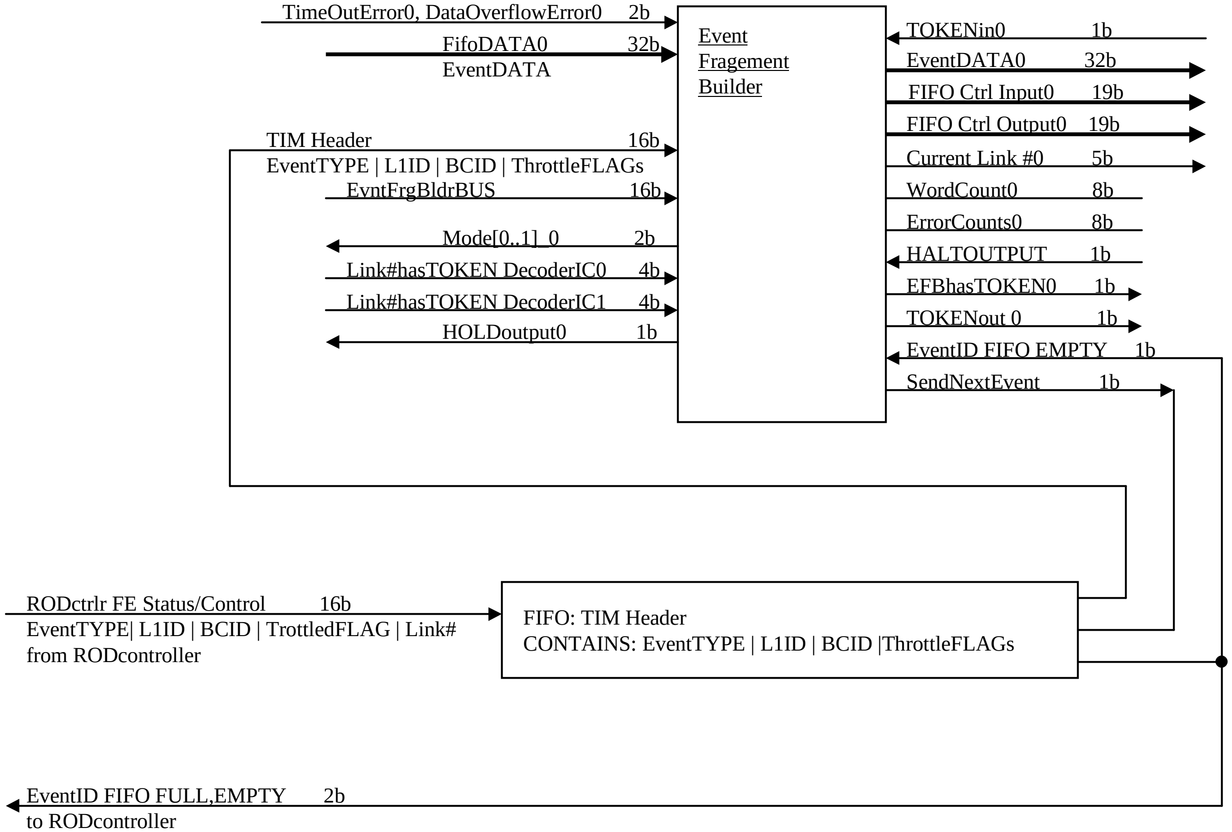


Model #2 Dual EventFragmentBuilder

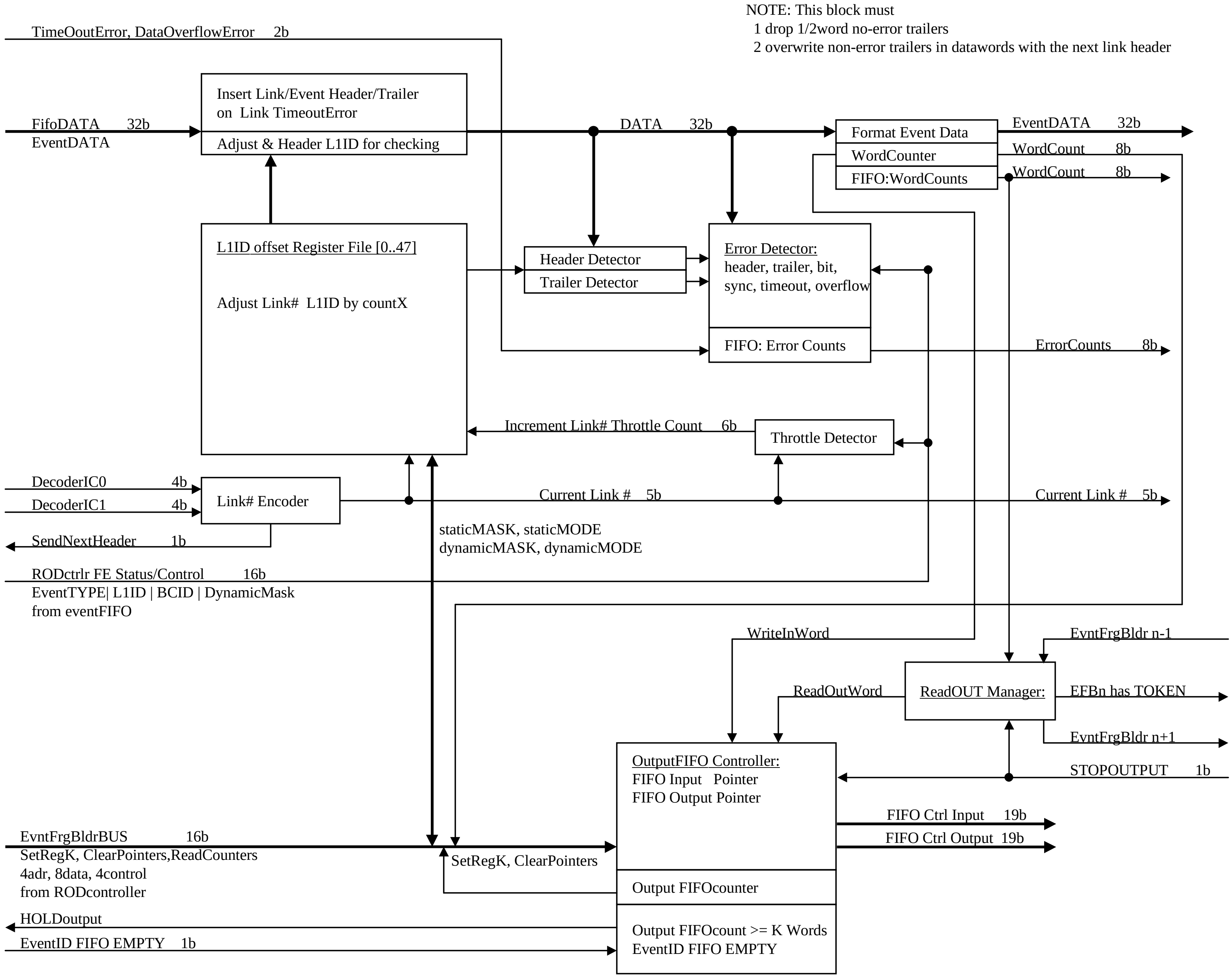
Note: XCV200fg-5 2352 14



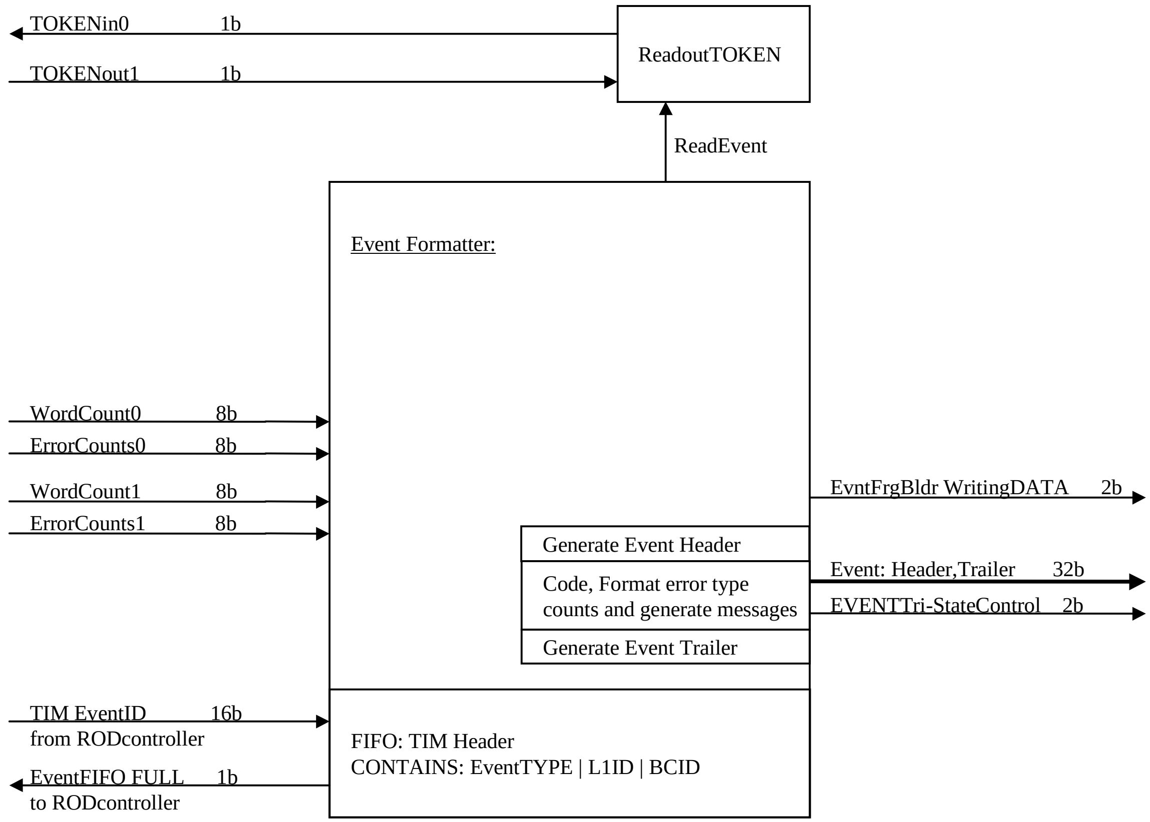
Model #2 GathererEngine preliminary



Model#2 Event Fragment Builder Engine



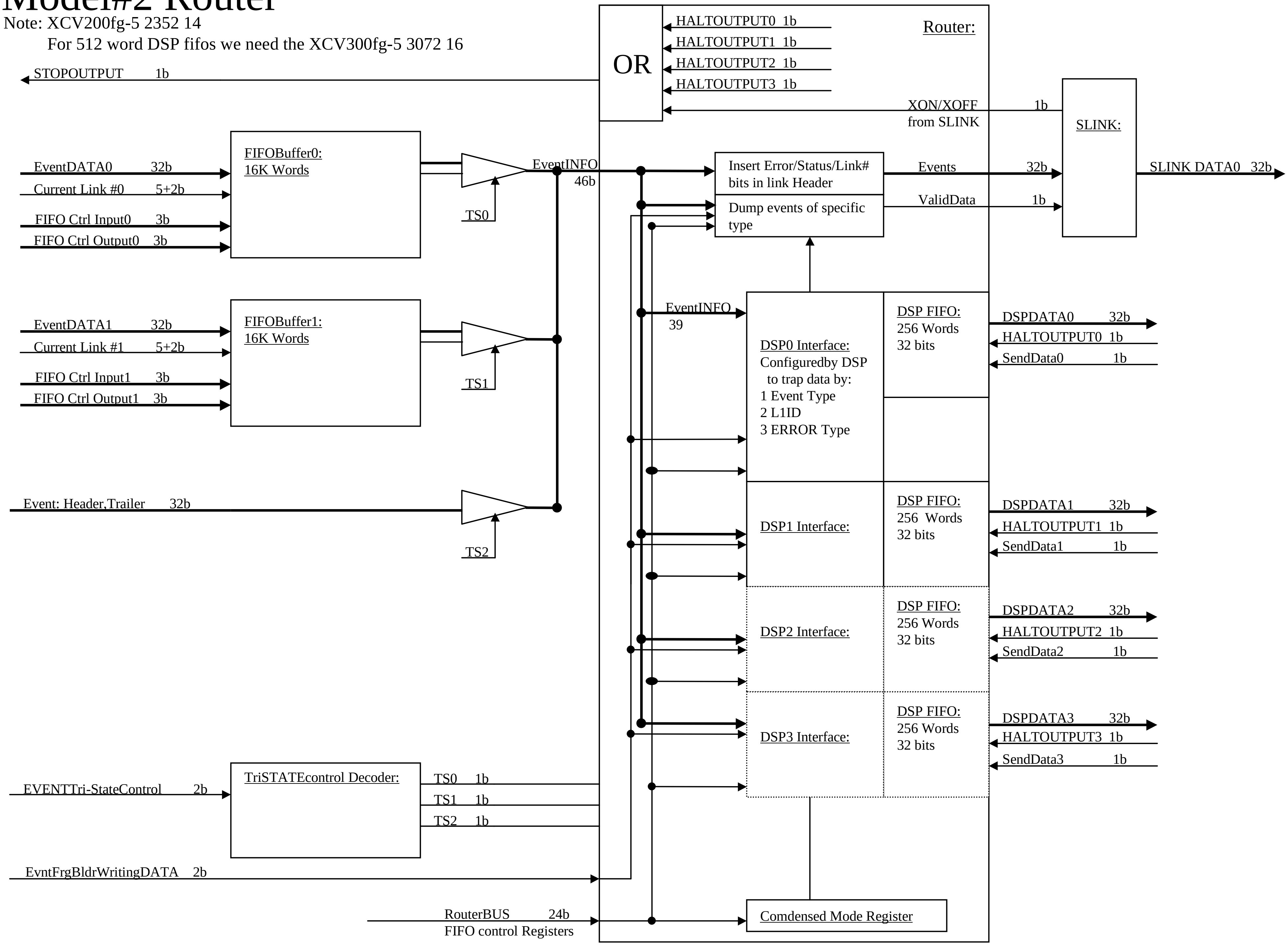
Model #2 EventFormatter



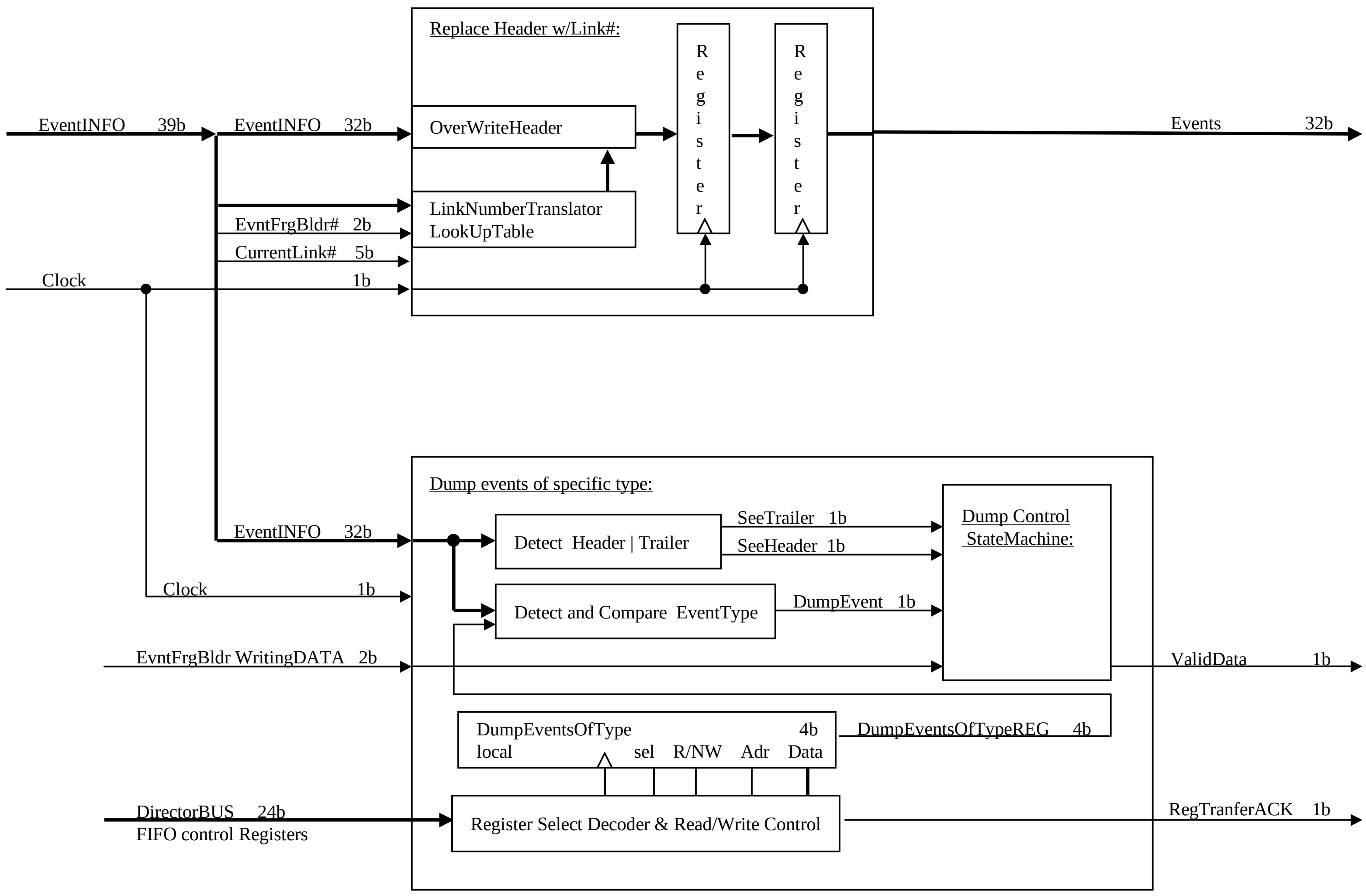
Model#2 Router

Note: XCV200fg-5 2352 14

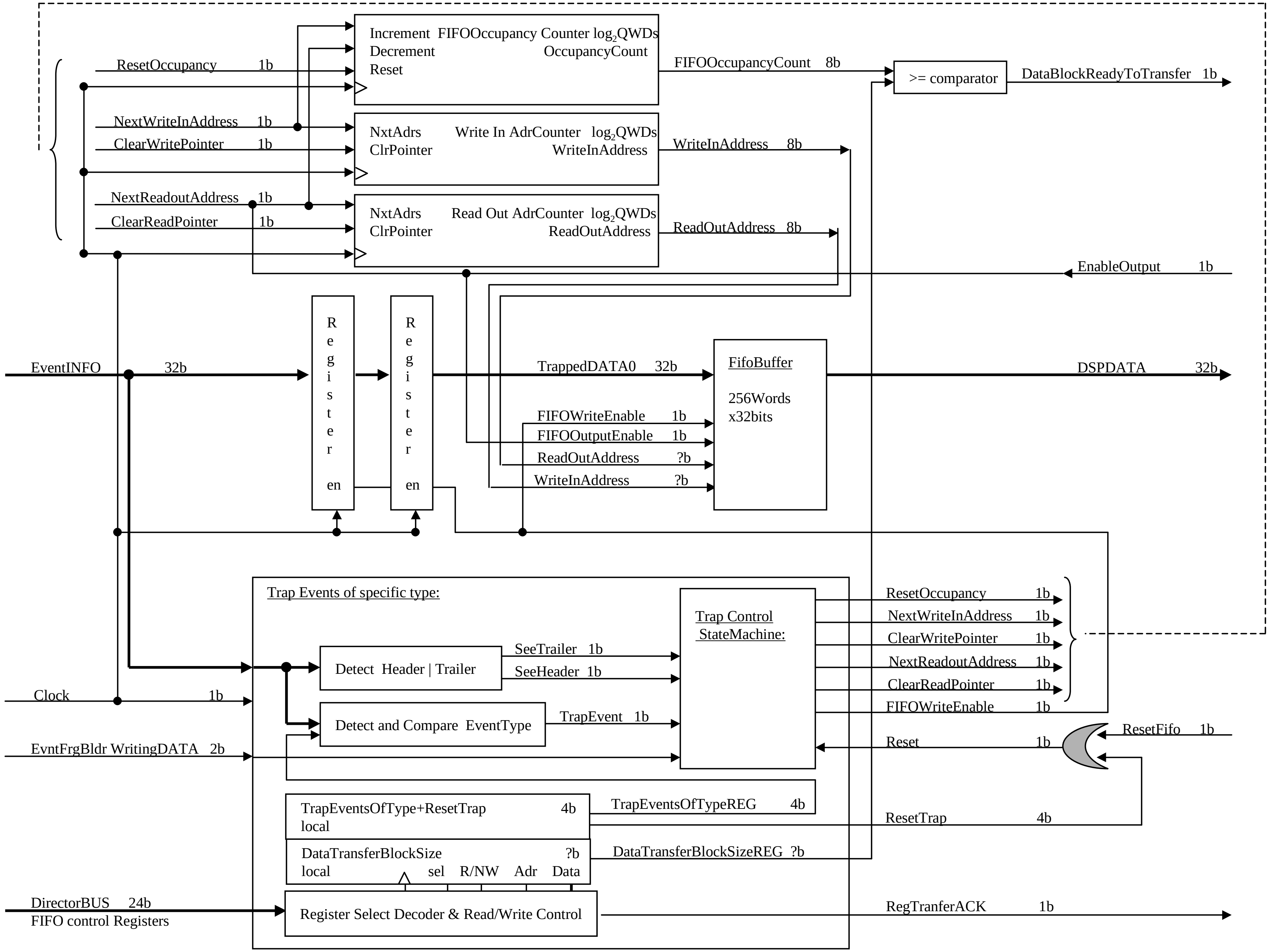
For 512 word DSP fifos we need the XCV300fg-5 3072 16



Model#2 Router: HeaderReplacer and DataDumper

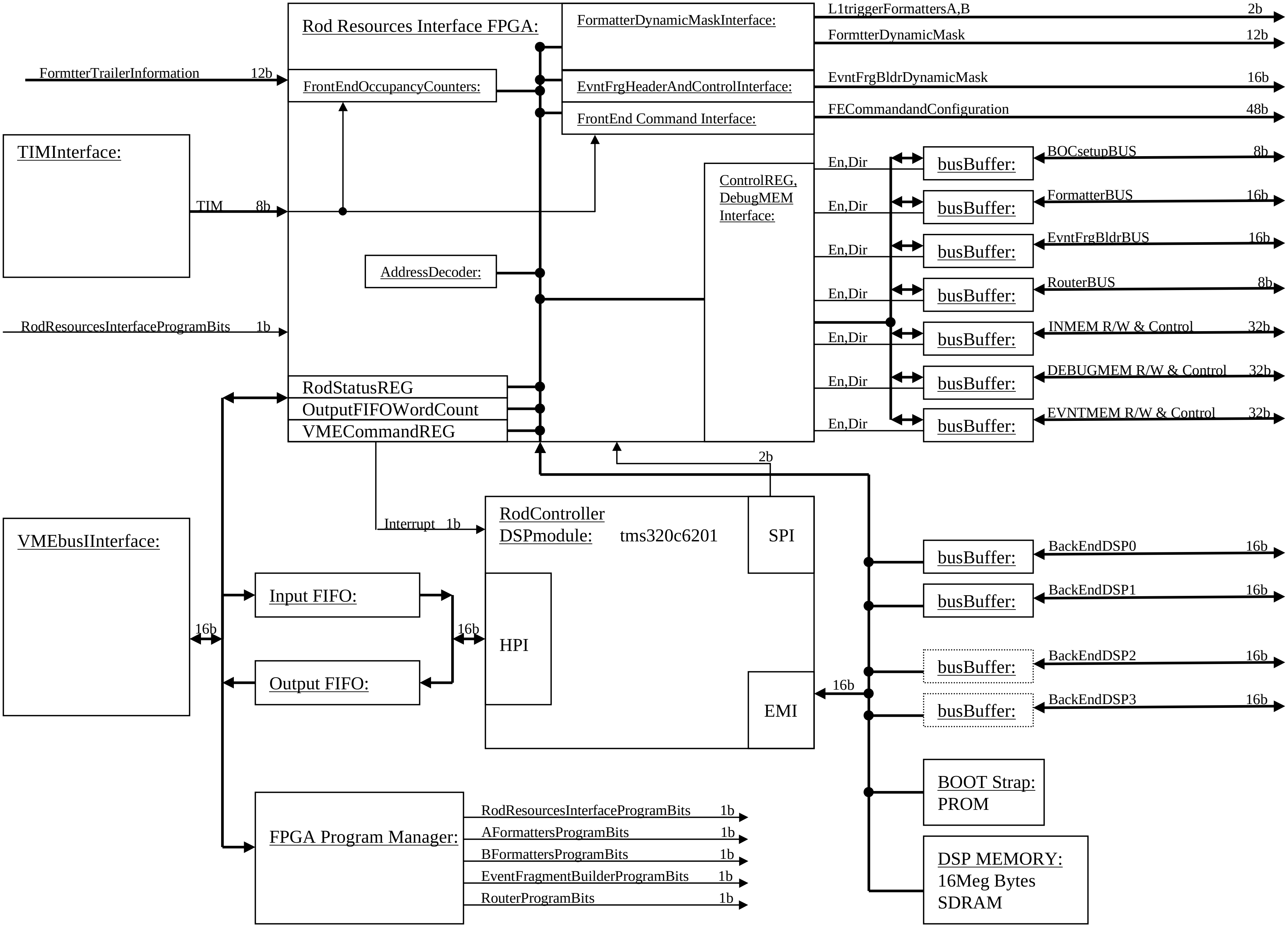


Model#2 Router: DSPInterface



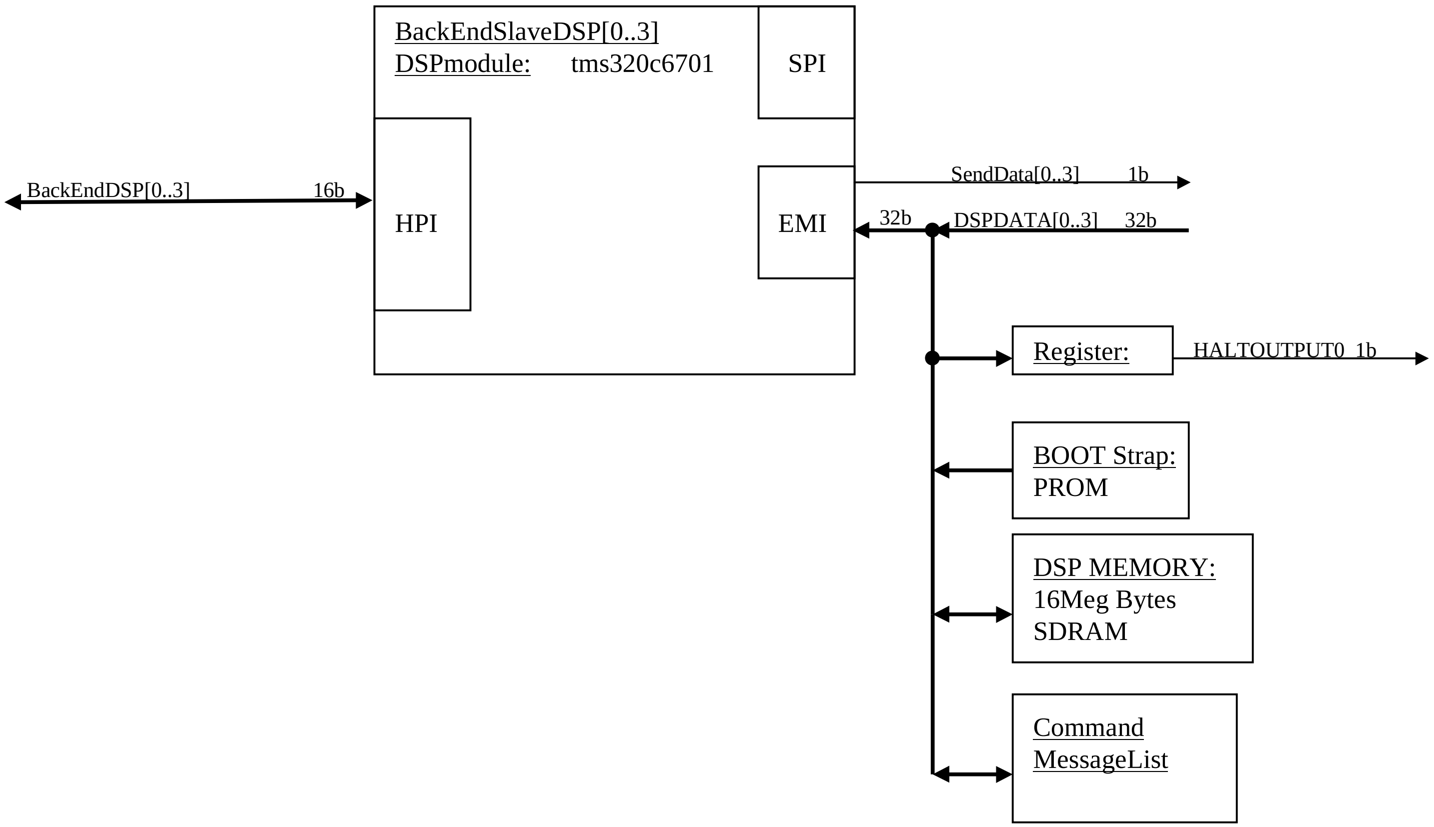
Model #2: ROD Controller Functional Block Diagram

Note: All bus size numbers indicate data bus size only, address and control signal have been omitted for clarity. XCV400fg-5 4800 20



Model #2: BackEnd Slave DSP 1 of 4

Note: Board resources are available for 4 DSP modules. Due to cost, only 2 are loaded.



Model#2 RODController: Formatter and EFB Dynamic Mask Encoders

FromatterFifo /Dynamic Mask Encoder

Inputs:
- FECommandPulse 1b
- OccupancyReadoutBUS 22b
  16data+4adr+2ctrl

Outputs:
- TIM TriggerInformation 12b
  ReadLink,SkipLink,ReadThrough
  to FormatterFifos
- FormatterDynamicMaskFifoWriteEnable[0..7] 8b
- L1triggerFormattersA,B 2b

RodController Dynamic Mask to Event Fragment Builder

bit11 bit0

DynamicMask for links [11:0] 2 bits/link
DynamicMask for links [23:12] 2 bits/link
DynamicMask for links [35:24] 2 bits/link
DynamicMask for links [47:36] 2 bits/link
DynamicMask for links [59:48] 2 bits/link
DynamicMask for links [71:60] 2 bits/link
DynamicMask for links [83:72] 2 bits/link
DynamicMask for links [95:84] 2 bits/link

Event Fragment Builder Header/Dynamic Mask Encoder

Inputs:
- TIM EventTYPE 1b
  fast commands, trigger headers
  from TIM
- TIM EventID 1b
  trigger headers
  from TIM
- FECommandPulse 1b
- OccupancyReadoutBUS 22b
  16data+4adr+2ctrl

The TTC0-7 lines in the ROD TIM Interface document need the following changes (Lane).

TTC4 was 1 start bit + 24L1 ID bits + 12 BC ID bits (+trigger type)
should be 1 start bit + 24L1 ID bits + 12 BC ID bits
TTC5 was ROD Clear
Should be 1 start bit +8 trigger type bits.
TTC6 was unused
should be reserved for periodic reset.

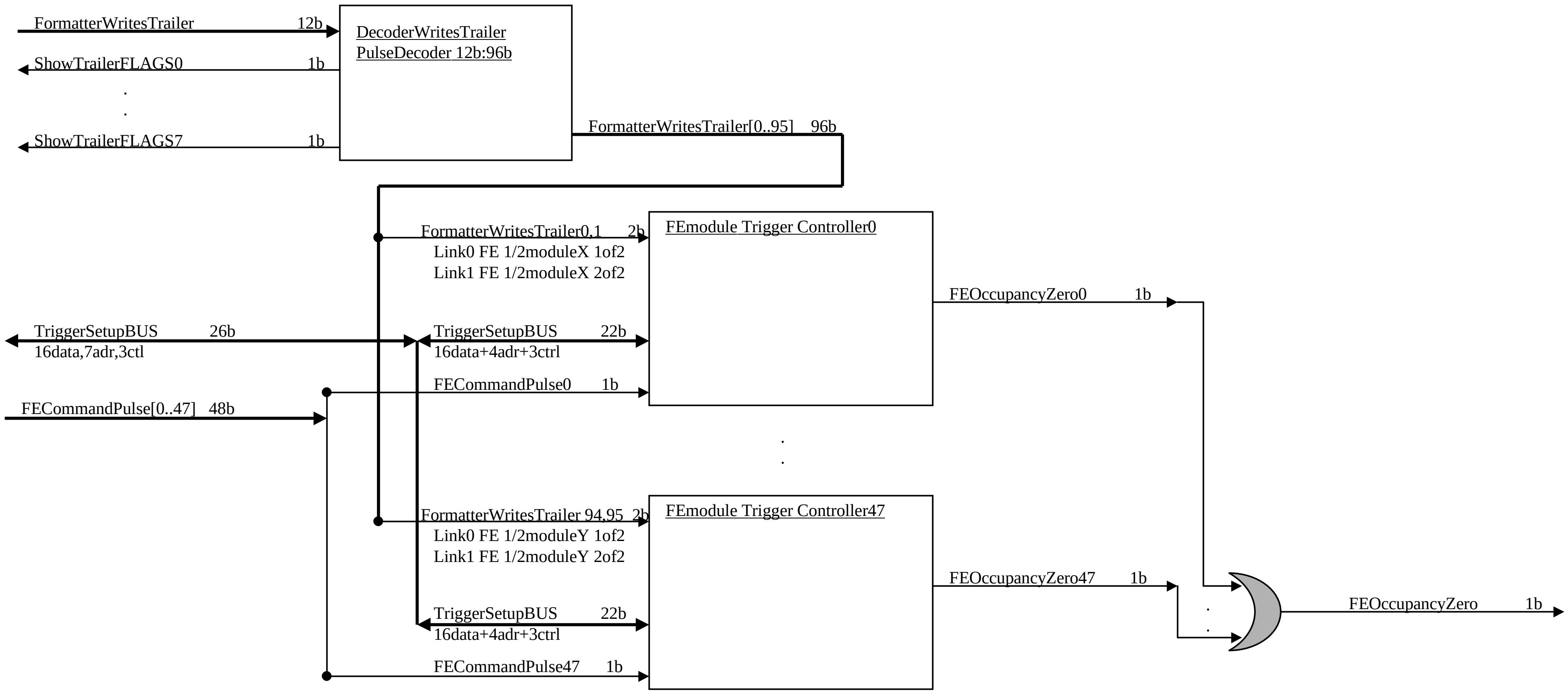
Outputs:
- TIM EventID 16b
  EventTYPE| L1ID | BCID | DynamicMask | Link#
  to EventFragmentBuilder
- EFBDynamicMaskFifoWriteEnable[0..7] 8b

TIM Event Packet to Event Fragment Builder

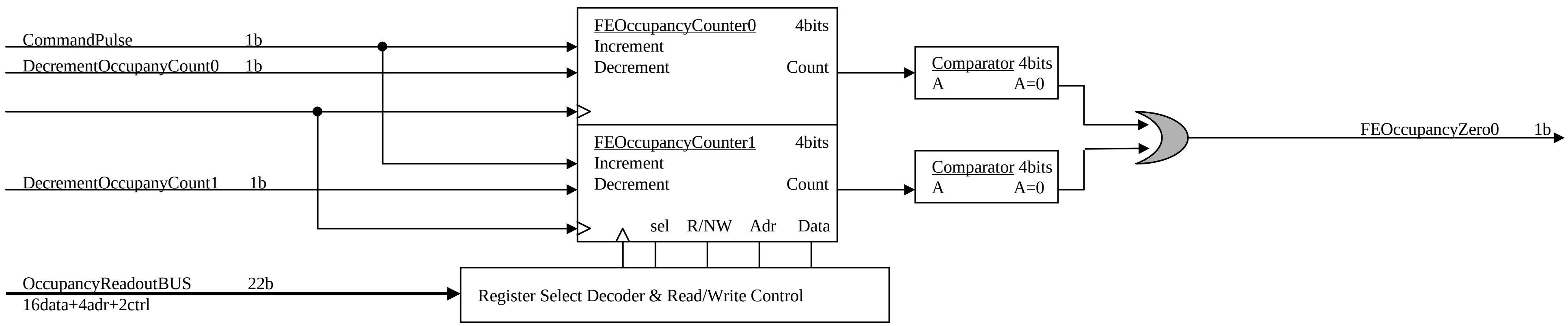
bit15 bit0

L1ID bits[15:0]--[15:0]
TriggerType bits[7:0]--[15:8] L1ID bits[23:16]--[7:0]
BCID[11:0]--[15:4] DetectorSpecificEventType[3:0--[3:0]
DynamicMask for links [7:0] 2 bits/link
DynamicMask for links [15:8] 2 bits/link
DynamicMask for links [23:16] 2 bits/link
DynamicMask for links [31:24] 2 bits/link
DynamicMask for links [39:32] 2 bits/link
DynamicMask for links [47:40] 2 bits/link
DynamicMask for links [55:48] 2 bits/link
DynamicMask for links [63:56] 2 bits/link
DynamicMask for links [71:64] 2 bits/link
DynamicMask for links [79:72] 2 bits/link
DynamicMask for links [87:80] 2 bits/link
DynamicMask for links [95:88] 2 bits/link

Model#2 RODController: Front End Occupancy Counters



Model#2 RODController: FETrigger Counter



Model#2 RODController: FETriggerCommands