OPERATOR'S MANUAL

MODEL 2132
HIGH VOLTAGE TO
CAMAC INTERFACE

LeCroy

Innovators in Instrumentation

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GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

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Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

PRODUCT DESCRIPTION

INTRODUCTION

The LeCroy Model 2132 is a single-width CAMAC module used to allow bi-directional communication between the CAMAC Dataway and the System 1440 or HV4032 or HV4032A mainframes. Please note however, that the 2132 should be used with the 1440 system or the HV4032 system. It cannot be used with both systems at once. Any combination of the HV4032 series mainframe may be used in the daisy chain. The system employs a five pair 20 mA current loop serial bus. Data are transmitted at 2400 BAUD using a modified ASCII code. Sixteen bit data words are transmitted as three bytes, each with its own parity bit. Checks for data transmission errors (parity) are accommodated by firmware at the addressed high voltage chassis or by hardware at the 2132.

The bus consists of two serial data pairs, two bus priority pairs and one pair to differentiate between CAMAC and TTY operation. A cable of up to 1000 feet maybe reliably employed between the 2132 and the first HV chassis. Up to 100 feet between chassis' may also be employed.

Using the 2132, all front panel operations can be performed remotely (high voltage hardware limit and HV gate are excluded). Commands are available to turn on, turn off, set and read voltage of any one channel or all channels in any one HV mainframe.

Because CAMAC is so much faster than the serial bus, 40 word memories are employed to buffer both the R and W lines. This allows the user to initiate a read only after all data are transferred, thus minimizing the dead time of the attendant computer. Completion of a routine data transfer to the 2132 sets a low priority LAM (L2) (HV4032A only). Error signaling uses a high priority LAM (L1). These LAMs may be detected by CAMAC Look-at-Me and identified through the CAMAC Read (R1 = L1, R2 = L2). A front-panel ERROR output is clamped to ground (open collector 300 mA sink) when any mainframe reports an error via the serial bus allowing the user to trigger an external alarm.

The response time of the HV mainframes depends upon the specific command issued. "Read One Voltage" commands require only a few msec in contrast with "Turn HV On", which requires approximately 20 seconds. For this reason, a Finished Response is returned after HV4032 has accomplished the task. Although this response can be disabled, it is strongly recommended that this feature be used

Communications between the CAMAC 2132 and the HV4032 mainframes are of several types. All communication from the 2132 to the HV4032 will be called COMMANDS, and all communication from the HV mainframes to the 2132 will be called RESPONSES. The HV mainframes will spontaneously respond to indicate a failed channel. Otherwise, the HV mainframes will respond only after receipt of a COMMAND from the 2132.

Conversely, most valid COMMANDS from the 2132 will be acknowledged by a RESPONSE from the addressed mainframe. Those commands having a defined response are called HANDSHAKE COMMANDS. These are outlined in Figure 1.

Any non-handshake command can generate a Finished response (user's option) for convenience of operation.

CAMAC COMMAND WORDS

TYPE[1]	WORD[2]	DESCRIPTION	RESULTING RESPONSE	INITIATING COMMAND
Command	C-M-0	Modify one channel voltage (Chan/Mainframe)	None (HV4032A waiting for T= 1 command)	–
Command	V-1	Set values[12]. Must follow a T=0, T=2, T=7, or T=12	T=11[8]	–
Command	X-M-2	Modify all 3.3 kV channel voltage (Mainframe select)	None (HV4032A waiting for N V=1 commands where N+ total number of 3.3 kV channels and empty channels.)	–
Command	C-M-3	Read true voltage of addressed channel	T=3	–
Response	V-3	True voltage (actual rear panel output in volts)	–	T=3 or T=4
Command	X-M-4	Read true voltage of all 32 channels	32 T=3 words[4]	–
Command	S-M-5[9]	HV ON/OFF Switch[9]	T=11[8]	–
Response	S-M-5[9]	HV ON/OFF Status[9]	–	T=9
Command	C-M-6	Restore addressed channel	T=11[8]	–
Command	X-M-7[3]	Preset all 3.3 kV channel (Mainframe select) if high voltage is off	None (HV4032A waiting for a T=1 command)	–
Command	C-M-8	Read demand value of addressed channel	T=8	–
Response	V-8	Demand value (in volts)	–	T=8 or 10
Command	X-M-9	Status request	T=9 and 5[5]	–
Response	C-M-9	Failed channel response[11]	–	T=9[6]
Command	X-M-10	Read demand value of all 32 channels	32 T=8 words[7]	–
Response	P-10	Response Identifying Pod complement	–	T=15
Command	S-M-11[9]	ENABLE/DISABLE finished (T=11) response	None	–
Response	X-M-11	Finished response	–	T=1,5,6 or 14
Command	N-M-12	Preset all 7 kV channels. N indicates voltage (N=0) or current (N=1).	None (HV4032A waiting for a T=1 command)	–
Response	X-M-12	Parity error (HV4032A Receiver)	–	Any
Command	N-M-13	Set individual voltage or current demands for all 7 kV channels. N indicates voltage (N=0) or current (N=1).	None (HV4032A waiting for X V-1 commands, where X=number of 7 kV channels.	–
Response	X-M-13	Overwrite error (HV4032A receiver)	–	Any
Command	C-M-14	Zero addressed channel	T=11[8]	–
Response	M-M-14[10]	Report of "Trip" condition (HV4032A only)	–	–
Command	X-M-15	Identify pod complement	T=10	–
Response	X-X-15	Transmission error (2132 receiver)	–	Any

Figure 1

Footnotes

(1) Command is a word transfer from the 2132 to the HV4032A. Response is a word or block of words transferred from the HV4032A to the 2132. It is always accompanied by one L2 (following the last word transferred if in a block).

(2) C = Channel address. CAMAC W16 to W11 for commands, R16 to R11 for responses.
X = Don't care. CAMAC W16 to W11 for commands, R16 to R11 for responses.
S = Switch, W11 (where W16 to W12 should be 0) for commands, R11 (where R16 to R12 are don't cares) for responses. W11 or R11 equal to "1" is ON, equal to "0" is OFF.
M = Mainframe address, CAMAC W10 to W5 for commands, R10 to R5 for responses (addresses 0 to 63 possible for HV4032, 0 to 16 must be used for the HV4032A, there should be no more than 16 mainframes per 2132).
V = Voltage, CAMAC W16 to W5 for commands, R16 to R5 for responses (0-4095 possible, HV4032A limits at 3300 for 3.3 kV pods and 3500 counts for 7 kV pods).
P = Pod type, 1 for 7 kV and 0 for 3.3 kV. Bit 2^7 corresponds to pod 0; bit2 for pod 7.0
0-15 = Tag (T), CAMAC W4 to W1 for commands, R4 to R1 for responses.

(3) HV must be OFF for command to be accepted.

(4) Expect 32 true voltages (actual rear panel output), channel 0 first, etc. with L2 on last (channel 32) data word only.

(5) Expect one T=9 word, no L2, for each failed channel in the module, followed by T=5 with an L2.

(6) Also can be transferred spontaneously at time of failure with an L2 and the high priority L1.

(7) Expect 32 demand values, channel 0 first, etc., with L2 on last data word only.

(8) Can be enabled or disabled by T=11 command.

(9) Status bits indicates:

2^0 = HV ON(1) / HV OFF(0)
2^1 = Calibrate(1) / Regulate(0)
2^2 = idle down(1) / Normal (0)
2^3 and 2^4 unused.

(10) Spontaneous transfer due to panic off or interlocking being asserted with L2 and the high priority L1.

(11) Failed channel responses are possible from channels 0 to 31. The 2 bit of C is set to indicate the initiator of a trip sequence.

(12) For 7 kV pods, the values entered and read through CAMAC correspond to the voltage or current according to: (CAMAC voltage value) = (Actual/2); (CAMAC current value) = (Actual x8).

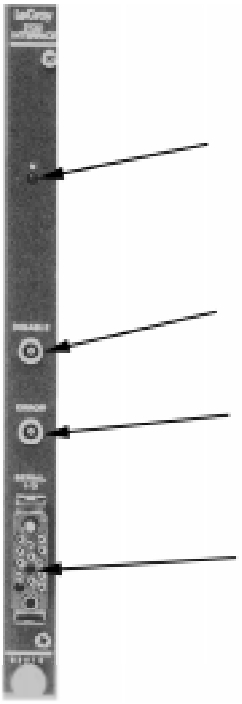
FRONT PANEL DESCRIPTION

Two LEMO type connectors are provided on the front panel of the Model 2132 (see Figure 2). DISABLE is an external inhibit of the low priority LAM (L2). This eliminates computer overhead for routine HV maintenance at critical times.

ERROR is an open collector 300 mA clamp to ground when a failure is detected at an HV4032. It is intended for use with an external alarm. Maximum V CC is 30 V.

The Serial I/O connector is an Amp Model 201298-1. It is compatible with the HVDC-14 (AMP 201297-1).

A LED on the front panel illuminate each time the 2132 is addressed.



N: LED indicates that 2132 has been addressed.

DISABLE: A clamp-to-ground inhibits Q and low priority LAM (L2) responses.

ERROR: An open collector 300 mA clamp-to-ground when a failure is detected from an HV4032A. Intended for use with an external alarm. Maximum Vcc is 30 V. System 1440 does not report errors through this line.

SERIAL I/O: Connector is compatible with HVDC-14 cable for use with 4032A or AD/CAM cable used with System 1440.

Figure 2

CAMAC OPERATION

The Model 2132 is a dual port device, communication with the HV mainframes serial daisy chain via a Universal Asynchronous Receiver Transmitter (UART) and with CAMAC via Dataway. Data words written into the 2132 from CAMAC are loaded into a 40-word deep FIFO and are available for CAMAC read out (Figure 3). Full buffering of both ports has been provided to allow efficient operation in spite of the drastic difference between the speed of the serial daisy chain and that of the computer.

Two levels of interrupt are employed by the 2132 system: High Priority (L1) and Low Priority (L2) LAMs (HV4032 only). The Low Priority LAM is used to indicate completion of data transmission from the HV4032 to the 2132 Interface. The L2 may be defeated by a TTY clamp-to-ground at the front panel DISABLE Input. In this way, routine responses from the HV4032s may be masked off when a LAM would be inconvenient. For

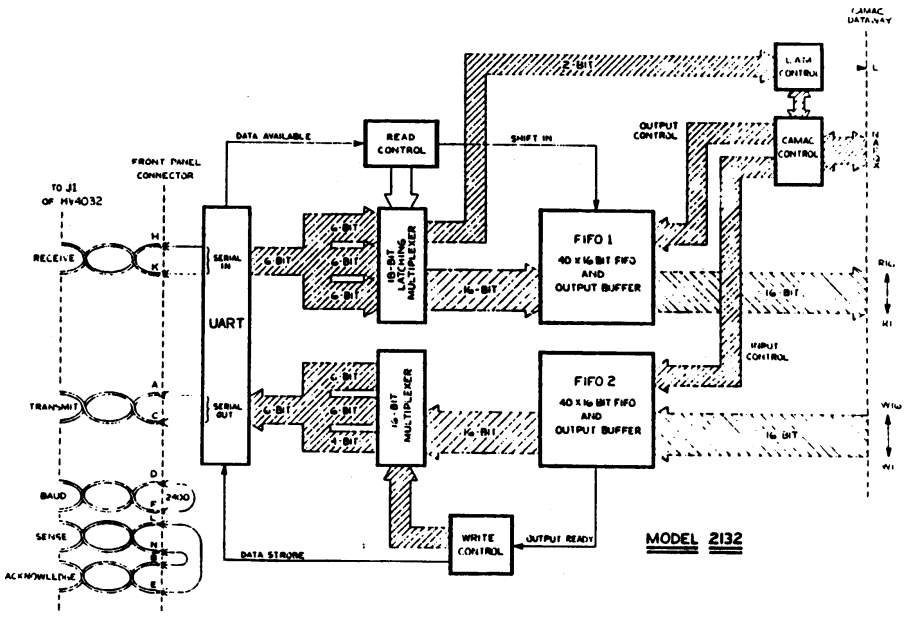
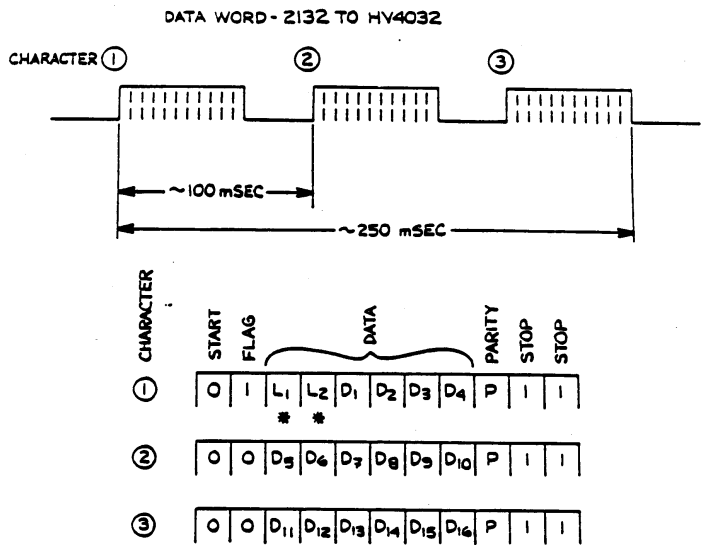


Figure 3

example voltage may be measured during data taking and read out, when the computer is inactive.

Data transmission of the Serial Daisy Chain is done at 2400 SAUD using a modified ASCII code. Sixteen bit command words written into FIFO 2 (Figure 3) are broken into three 6-bit characters. The UART adds one start bit, two stop bits, and a parity bit. The 2132 control circuitry adds a flag bit allowing the system to perform framing checks (Figure 4) for the HV4032. L1 and L2 are used for setting the LAM status on (but not for resetting it).



* L1 and L2 are bits indicating LAM 1 and LAM 2

Figure 4: Data transmission and character configuration

Eighteen data bits are transferred, two of which are used as LAM Status Bits only on transmission to the 2132. Data transfer from the 2132 to the HV mainframes is considerably slower than the corresponding response communication. Because of the computer error checking (parity, framing, etc.) the HV mainframe requires approximately 100 msec between characters, making the total transfer time approximately 250 msec/word. This timing is controlled by hardware within the 2132.

Responses are transmitted at the rate of 15 msec/word. THUS, TRANSMISSION OF 32 VOLTAGE SETTINGS REQUIRES APPROXIMATELY SIX (6) SECONDS. In contrast, reading back 32 voltages can be accommodated in 500 msec.

PROGRAMMING FOR THE HV4032A

Programming of the HV4032/2132 system involves a 16-bit word format. The constituent syllables that comprise the datawords are as follows:

M Mainframe address, M=0 used for addressing all units on the daisy chain (6 Bits)

C Channel number (6 Bits)

V Voltage (12 Bits)

T Control Tag (See Figure 1) (4 Bits)

S Software Switch (1-bit right justified in a 6-bit field)

The COMMANDS and RESPONSES are indicated in Figure 1. These words are written into the 2132 via CAMAC F(16) commands. A list of CAMAC function codes is given at the end of this Section.

Registers which have front-panel designations greater than 31 may be written into through CAMAC as follows:

CAMAC Channel Number	Front Panel Number
32	33
33	43
34	47
35	70
36	70c
37	99

The user software should keep track of values entered into these registers since there are no CAMAC commands to read them. Proper entry of information into these registers may be checked through the front panel.

A programming example flow diagram is given in Figures 5 to 10 to illustrate general procedure for operation of the 2132.

CAMAC clear (C or Z) is recommended after power up of the 2132. After this initialization it should not be necessary to clear the module again. Use of clear function may, in fact, cause erroneous data to be read out should it coincide with data transferred from an HV4032).

Data buffer (FIFO) clearing can be performed by generating read cycles F(2), until Q response equals zero. During normal read, F(2) should be continued until Q=0 to ensure all data available has been cleared.

A Q response following a write command, F(16), indicates that the 16-bit word had been accepted by the 2132. It will be transferred thereafter according to the timing set internally by hardware in the 2132 Interface.

The Finished Response can be used for non-handshake commands to inform the user when the command is completed the given example, the 33 words used to modify the voltage of 32 channels in mainframe 16 will be transmitted to the HV4032 at a rate determined by hardware in the

2132 Interface. The HV4032 will process this data, look for errors (parity), and send a Finished response on completion of the command. If the high voltage is ON the response will occur after the voltage have been modified. If the high voltage is OFF the response will be given upon receipt of the data.

After the high voltage ON command is used, a delay of approximately 20 seconds allowing voltage run-up will be experienced before the finished response will be given. (Response is generated when the microprocessor is no longer “busy”.) The user should modify his software for his convenience so that considerable computing time is not lost in waiting for this response. (Figure 9).

In generating commands to the HV4032 via the 2132 CAMAC Interface, care should be exercised in writing into the FIFO 2 (Figure 3). Though the buffer is 40 words deep it must be realized that the buffer data is transferred to the HV4032 at a much slower rate than the CAMAC dataway can write. Do not attempt to write more than 40 words at one time.

If several commands are to be given, i.e., modify 32 channels for more than one mainframe, wait for a response from the first mainframe before addressing the next.

A module zero address can be used to address all mainframes in a daisy chain. Never use this command where a response totaling more than 40 words will occur. For example, requesting 32 ADC voltages from all mainframes.

Error detection is performed by decoding the 16-bit response words. The lower order four bits will define the nature of the error, (i.e., 12 = parity, 13 = overwrite). A parity error implies a command to an HV4032 which was not recognized. This can be generated by any unit in a daisy chain as all units will see the command from the 2132, but only the HV4032 recognizing the address should respond to the command given.

Each of the three characters in a word has a parity bit which is checked before the data is processed. If a parity error is detected, the command will be aborted and the user will have to re-initiate the command.

An overwrite error will occur should a second character arrive before the first character is processed. The likelihood of this occurring is very small since the timing is controlled by hardware in the 2132 Interface. In the event that an overwrite error is detected, the command will be aborted and will necessitate re-initialization of the command as above. Both overwrite and parity are errors detected at the HV4032.

Transmission error is detected at the 2132 and includes either parity or overwrite error of a response.

PROGRAMMING FOR THE SYSTEM 1440

Computer interface to System 1440 is accomplished with a LeCroy 2132. The language linking them has been designed to minimize programming problems, however there are certain nuances that should not be forgotten.

1. The mainframe select command is residual. It remains active until another mainframe command is received. Obviously, if power is turned off the 1440 will not be able to respond, it will also lose its selected status when power is restored. Computer programs that are waiting for responses should expect this situation and be able to cope with it. Do not forget the mainframe select command when trying to re-establish communications. This situation can also occur if the 1447 is plugged in, the 2132 cable is disconnected, or the 2132 is turned off.

2. The 1440 may have mixed polarity and/or empty slots. This should be taken into account since programming a card to the wrong voltage will result in zero output. It is suggested that programming be done by card or single channel. These are convenient sizes to be compatible with both the 2132 buffer and the necessity to handle polarity and empty slots.

3. To aid in determining the mainframe configuration, the unit will generate a list of empty cards upon request. It the unit is full, a response indicating that it is full will be sent. If not full the response will be a variable length list (depending on setup). When is the list ended? There are two ways to handle this. One is to consider that it is certain to take less than 160 msec, between words. The other would be to issue some other command (enable finished response for example) and use that command's response as the list terminator.

4. LAMS. The 1440 generates an L1 with every transmission. This can be used to indicate that the 2132 has received data. Unfortunately, the LAM and the amount of data are uncorrelated. This raises the question of when to clear the LAM. This can be difficult since transfers occur in different sizes and the 2132 may be simultaneously issuing new commands. If polling is acceptable it is recommended that the LAM be ignored and allow the Q response from a F(2) to indicate valid data. Note that L2 is NEVER generated.

5. FIFOs. Both the 2132 and the 1445 arc FIFO buffered. This allows a burst of data to be transmitted at high speed, but then necessitates a delay to allow processing of that data. The 2132 will indicate FIFO full during a F16 by not returning a Q response. The 1445, being isolated from the host computer cannot give such an indication. Its buffer length exceeds that of the 2132 giving on level of protection. The best way to ensure that no data is lost is to transmit data in a handshaking mode. This means that data sent to the 1445 should be in blocks of less than 40 words, the last word being a command that generates a response.

   This response will then have the additional meaning of "FIFOs empty", thus ensuring proper operation. Normal program flow will

generally, but not always accomplish this. If necessary, the ENABLE FINISHED RESPONSE command is a handy way to get a response when nothing more than indicating FIFO empty is desired. The most likely situation to cause concern is down loading a set of voltages. This is where programming in card increments is convenient. The sequence of COUNT, WRITE, 16 voltages, ENABLE FINISHED RESPONSE, will fit into the 2132 buffer twice. First send one block of writes, then loop sending blocks followed by a wait for finished response. This gives maximum throughput while maintaining hand-shaking. Note that if this loop is to cross mainframes the mainframe select command should be included.

TRANSMITTING TO SYSTEM 1440

The data received by System 1440 is buffered to a depth of 40 commands. All mainframes receive all commands independently of whether they are selected or not. Those units not selected will not act upon the command. This means that consideration of the buffer depth does not include mainframe selection. The depth of the buffer has been set to accommodate the expected size of command bursts. For instance, in a setup of multiple units a burst of status requests may be issued without waiting for any response (buffer depth max. of 16). Since the size of the 2132 input and output buffers are also 40 there should be no difficulties involved. If the buffer size is ignored and the computer manages to overflow it any following commands will be lost.

RESPONSES FROM SYSTEM 1440

Output from System 1440 to the 2132 is only generated in response to a request. There is no spontaneous transmission. When requesting information from 1440 the buffer size of the 2132 must be taken into account. The count option in the commands to the 1445 can generate a block response of up to 257 words. The demand and measured i.d. responses have been included to assist in verifying that no data responses are lost. The suggested mode of operation is to limit the count to 39 (39 channels + 1 i.d. word fills 2132). If this is not done the 2132 must be read out fast enough to prevent overflow. This might be a reasonable approach if the LAM is used as an interrupt.

NOTE

Due to timing differences between the HV4032A/M and the 1440 System High Voltage Mainframes, it may be necessary to remove a 6.8 μf capacitor located on the 2132 PC board for operation with the 1440 mainframe. Since the 1440 system controller can transfer data at a higher rate of speed, the capacitor can be removed to allow the 2132 to transfer data faster. When a 2132 is shipped with a 1440 system, the capacitor is removed at the factory before shipment. If the 2132 is being bought separately for use with a 1440 System, it will be necessary to remove the capacitor. This 6.8 μf capacitor is located in the top right-hand corner of the PC board, between IC "BA" (7402) and IC "CA" (74LS123). On the schematic it is designated "C9" and can be located on sheet 4 of 7. The capacitor should be either de-soldered and removed from the PC board or clipped out with a pair of wire cutters. This capacitor should always be in place when the 2132 is used with the HV4032A/M mainframe.

SUMMARY OF CAMAC FUNCTIONS

F(0)•(A(0)+A(1))•N	Read LAM Register (R1=L1, R2=L2)
F(2)•(A(0)+A(1))•N	Read and advance buffer (data valid if Q=1)
F(9)•A(0)•N	Clear buffers, L1 and L2
F(16)•N	Write into output buffer (Q=1 if word is accepted at output buffer. Data transfer will then proceed to the HV)
F(27)•A(0)•N	Test L1
F(27)•A(1)•N	Test L2
F(10)•A(0)•N	Clear L1
F(10)•A(1)•N	Clear L2
F(10)•A(0)•N	Enable L1
F(26)•A(1)•N	Enable L2
F(24)•A(0)•N	Disable L1
F(24)•A(1)•N	Disable L2
Z•S2	Clear L1, clear L2, clear buffers, enable L1, disable L2
C•S2	Clear L1, clear L2, clear buffers

Note: The 1440 System does not utilize L2. All responses generate L1.

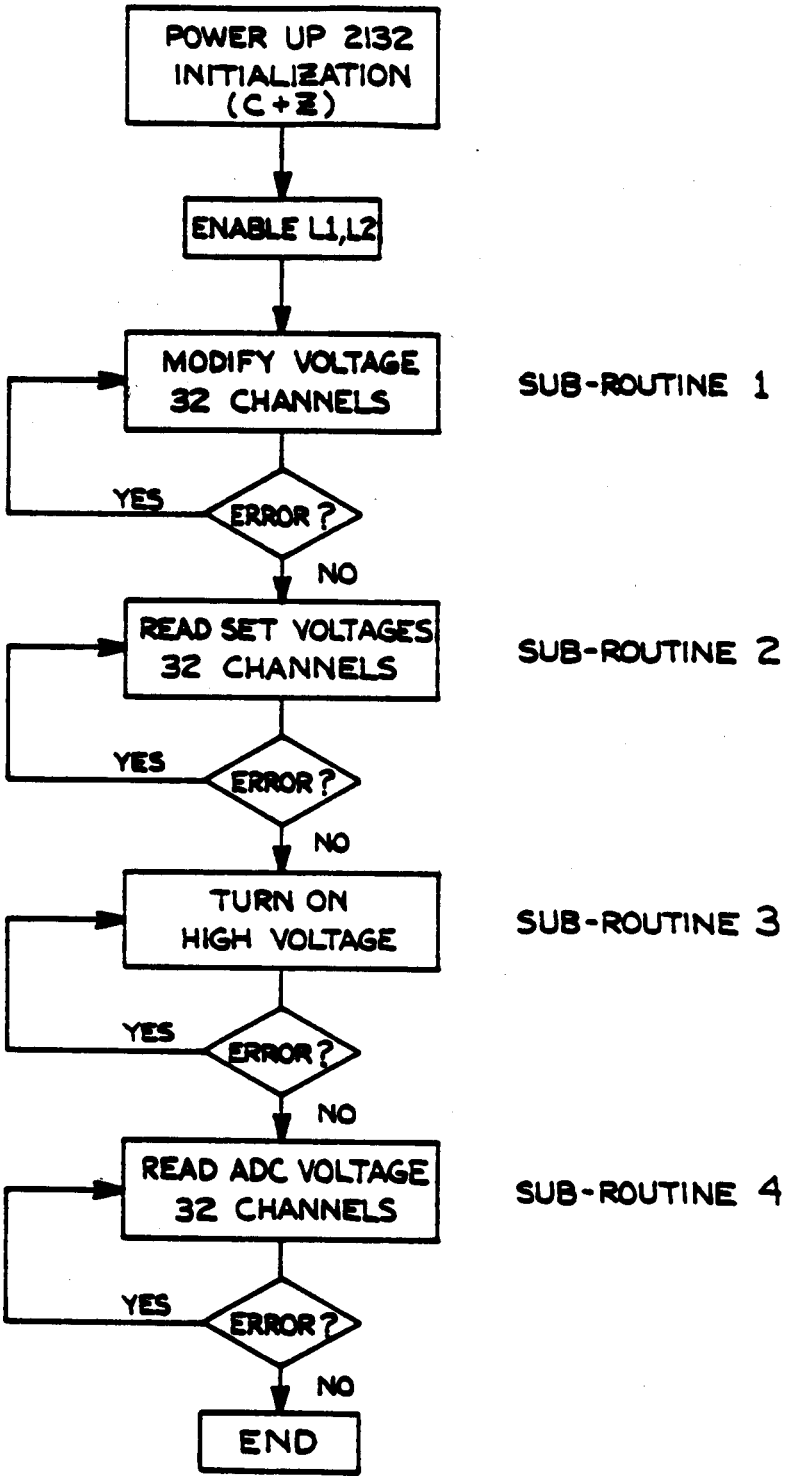


Figure 5: Model 2132 Programming

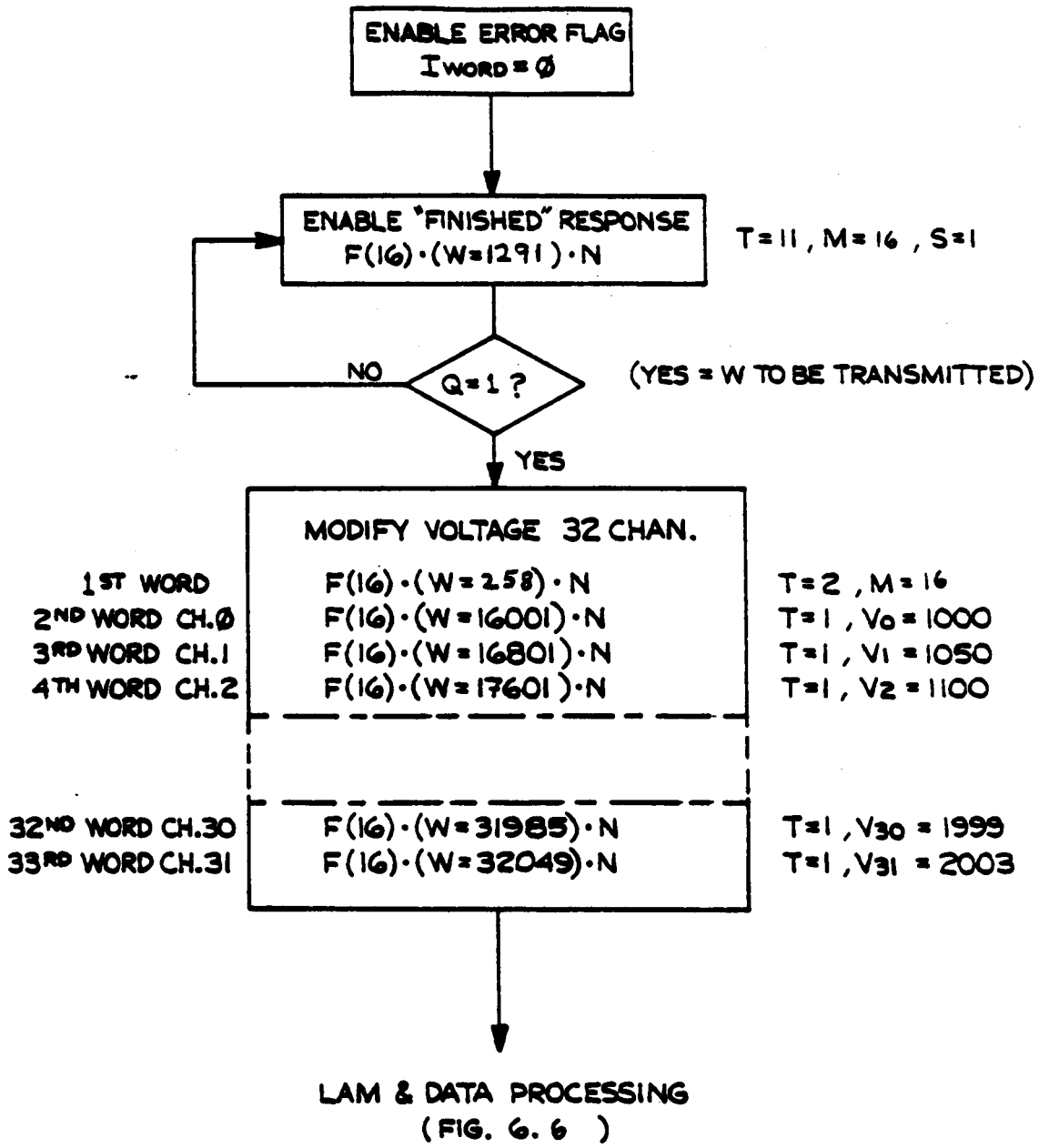


Figure 6: Sub-Routine 1; Modify Voltage, 32 Channels

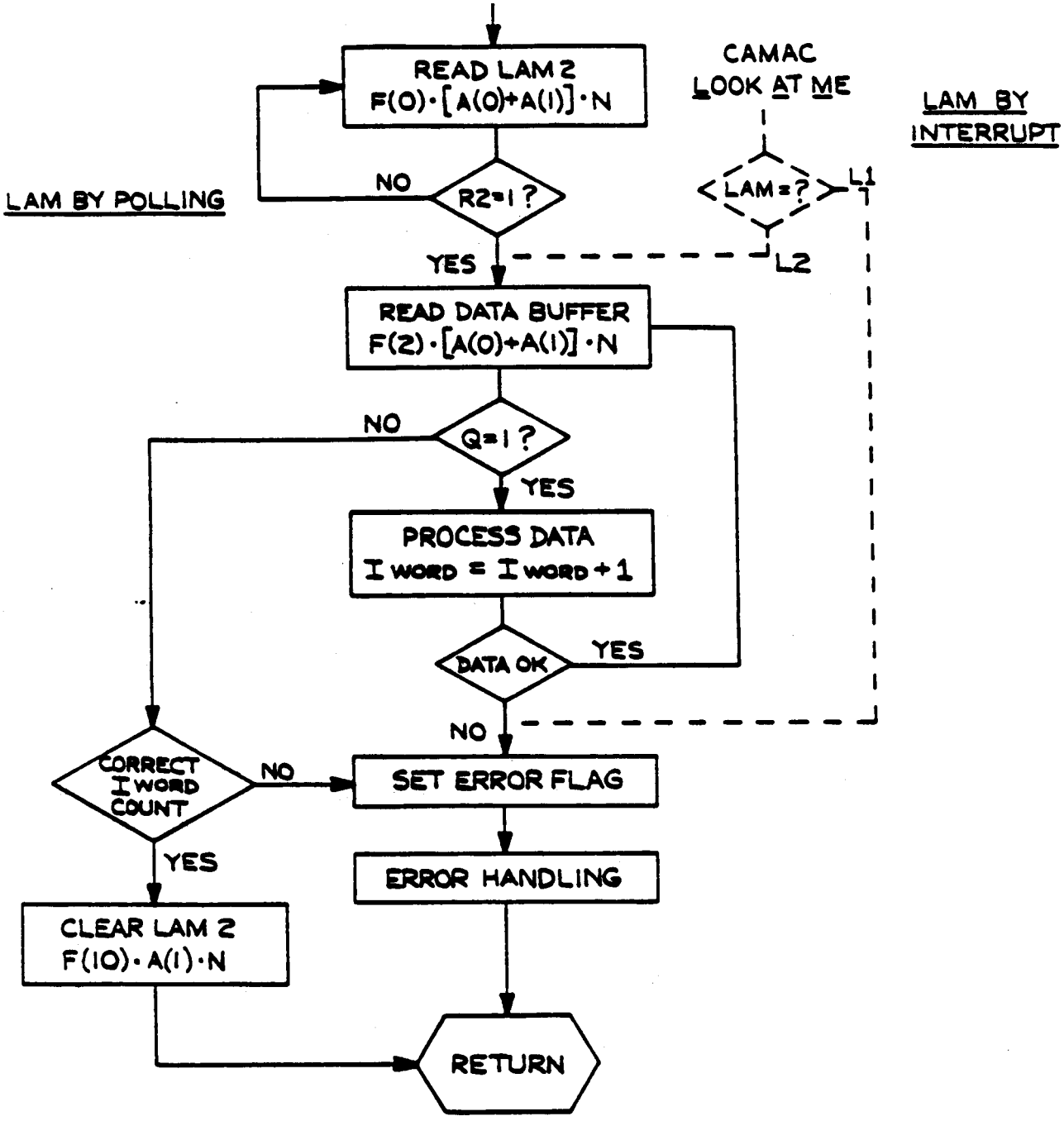


Figure 7: LAM & Data Processing

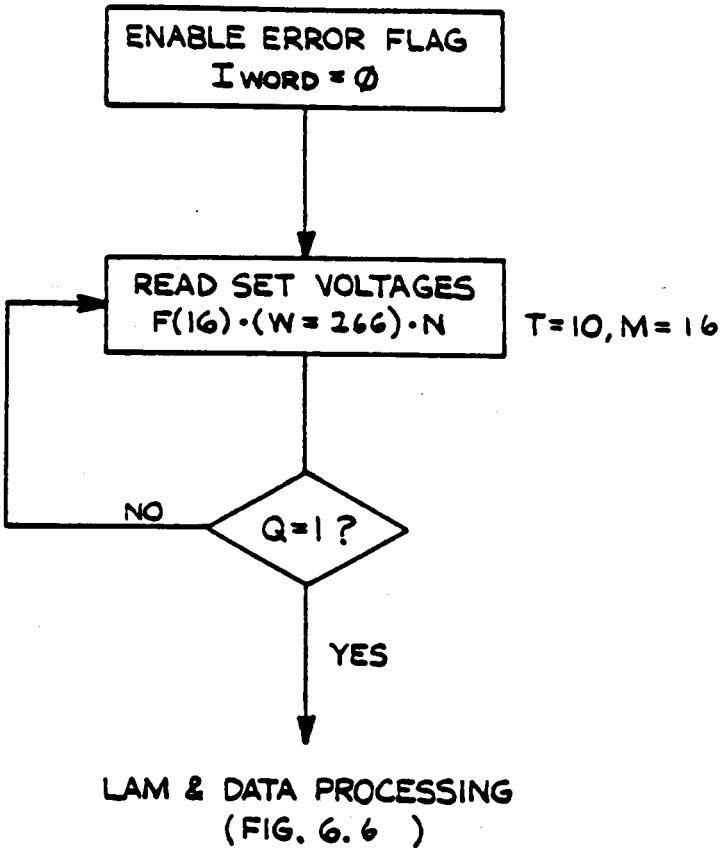


Figure 8: Sub-Routine 2; Read Set Voltage

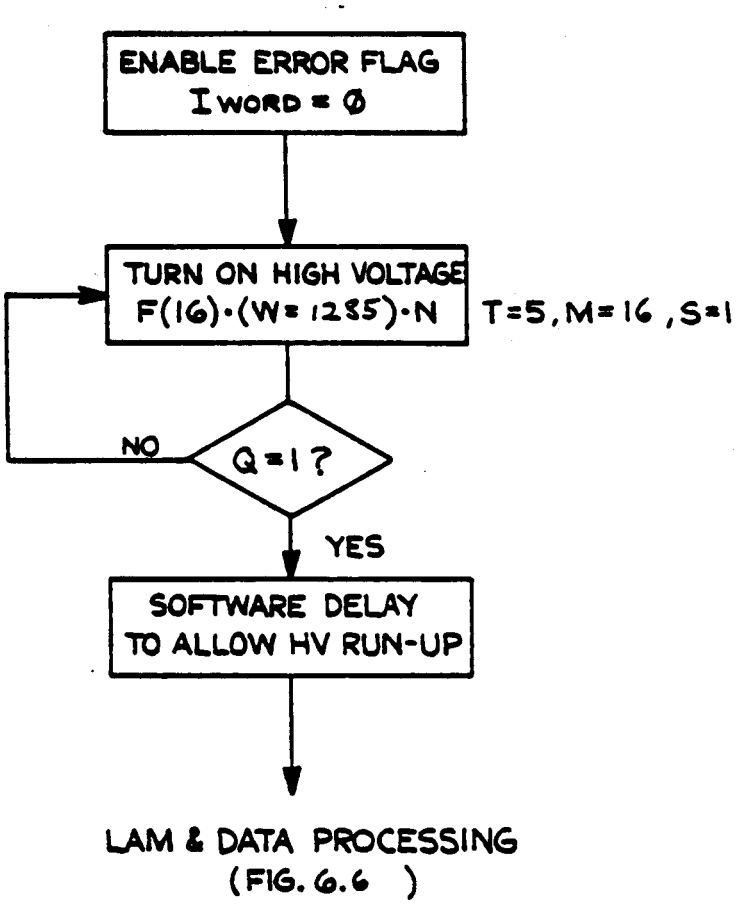


Figure 9: Sub-Routine 3; Turn On High Voltage

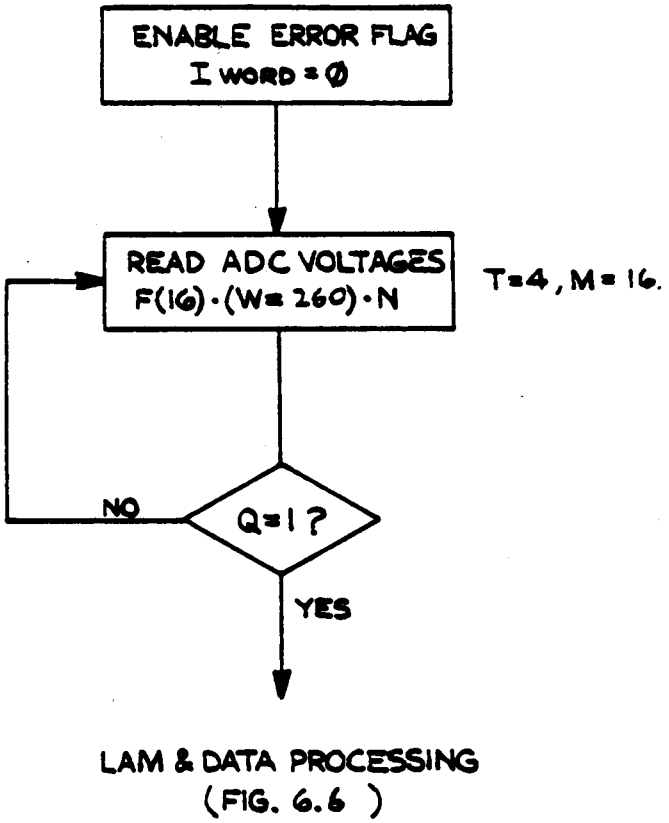


Figure 9: Sub-Routine 4; Read ADC Voltages, 32 Channels

Model 2132
Schematics and Parts List