Proposal for the continuation of the development of AFEII

J. Estrada, M. Johnson and P. Rubinov
Fermilab

For some time now, we have been developing a new front end board (AFEII) [1,2] for the operation CFT with bunch separation of 132 nsec. We now know that there is a very high probability that the Tevatron will never go to this mode of operation.

Since the results of the tests done with the prototype electronics are encouraging (see Refs. [2,3]) and the performance of the current front end board (AFEI) is not yet meeting the specifications, we are proposing in this note to continue the development of the AFEII in order to have a alternative to AFEI in case we can not make it operate within specifications.

In Section 1 the performance of the VLPC detectors in a high occupancy environment will be discussed. The problems seen in the current electronics and how this will affect the performance of the detector in a high luminosity environment are addressed in Section 2. Some additional advantages of AFEII are discussed in Section 3. In Section 4 we will present the proposal for a plan for continuing the development of AFEII.

1 The rate effect on the VLPC

The VLPC performance depends strongly on the rate at with it is being excited. This effect was studied at DØ in 1996 and, during production of the VLPC cassettes, every channel was characterized as a function of background rate in Lab3 [4].

For a fixed operating bias voltage the quantum efficiency (Q.E.) of the VLPC goes down as a function of background rate, as can be seen in Fig. 1. The bias voltage can the be raised to approximately compensate for this effect. On the other hand, if one looks at the gain dependence of rate shown in Fig. 2, one can see than the maximum gain that one can obtain for a given VLPC drops by approximately 30% as rate goes from 0 to 8 million photons per second. This means that as the luminosity increases, the rate of photo-electrons into the VLPC increases and the gain goes down significantly. The amount of charge seen by the front end electronics will decrease accordingly.

To understand how important this effect is one needs to estimate what will be the rate (R) of photo-electrons hitting the VLPC pixel, for difference occupancies. The is calculated as

$$R = \text{occupancy} \times \frac{1}{396 \text{ nsec}} \times < p.e. > \tag{1}$$

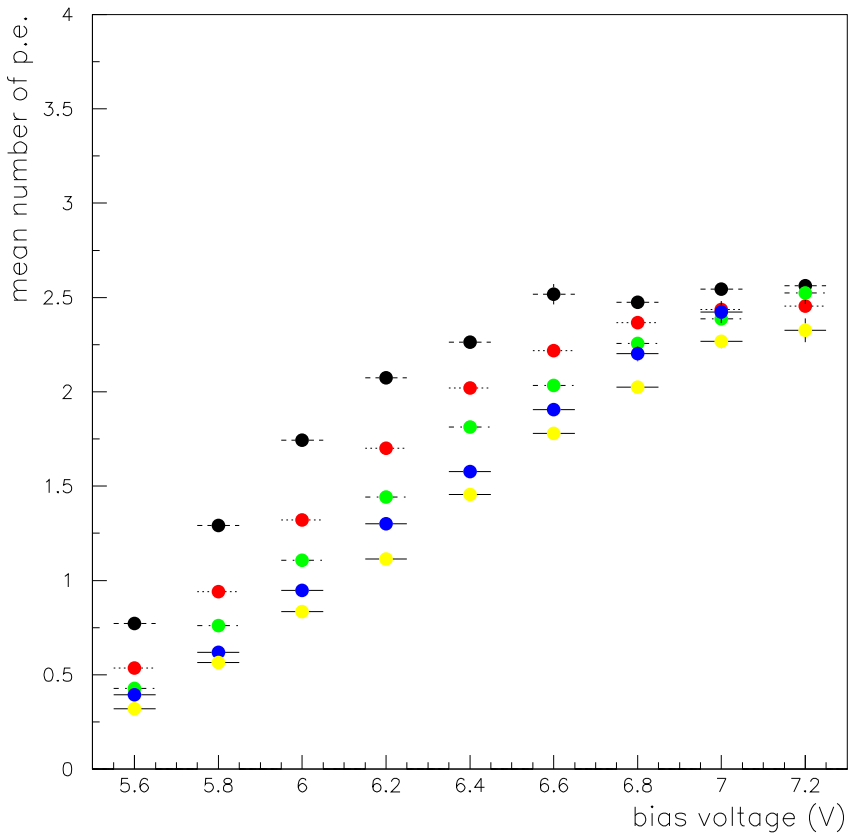

Fig. 1. Mean number of photo-electrons for a group of 64 VLPC channels (Cassette 12, module 1, RH), as a function of bias voltage. Black: 0 MHz, red: 2 MHz, green: 4 MHz, blue:6 MHz and yellow: 8 MHz.

where occupancy is the fraction of events in which a given channel will see a hit in the fiber, $< p.e. >$ is the mean number of photo-electrons in 1 hit and $\frac{1}{396} nsec^{-1}$ is the bunch spacing. Assuming $< p.e. >= 7$, we obtain a rate of 2MHz for 11% occupancy, Fig. 3 shows relative gain as a function of occupancy. From independent studies, extrapolating the current hit occupancy in the CFT to the luminosity levels expected in Run IIb, the occupancy of the CFT during Run IIb is estimated to be about 20% in average.

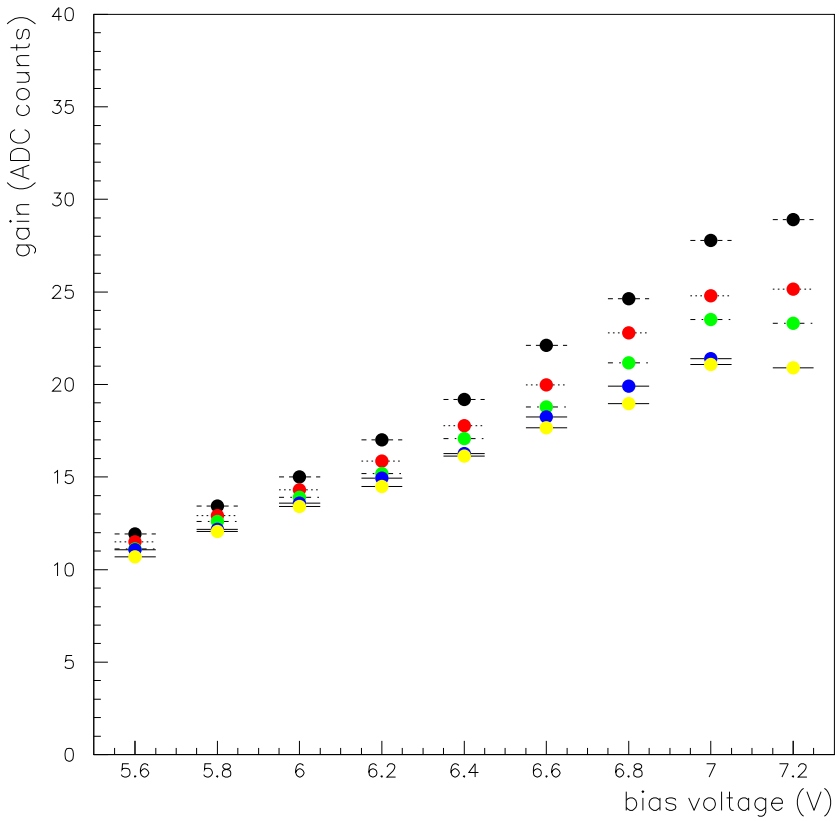

Fig. 2. Mean gain in ADC counts for a group of 64 VLPC channels (Cassette 12, module 1, RH), as a function of bias voltage. Black: 0 MHz, red: 2 MHz, green: 4 MHz, blue:6 MHz and yellow: 8 MHz. A significant reduction in the maximum gain is observed as the background rate increases.

2 The current electronics and the problems with the pedestals.

We have seen 2 kinds of problems with the pedestals in AFEI. a) split pedestals as shown in Fig. 4: instead of seeing one pedestal peak, some channels show two peaks in the pedestal distributions. b) pedestal dependence on bunch crossing as shown in Fig. 5: some channels have different pedestals for different crossings . Because these two problems we have to set our thresholds at 2.5 p.e. in order to get 1% occupancy with noise. It is possible that part of these problems will be solved by fine tuning the timing of the digital signals that control the operation of AFEI, a significant effort is being made

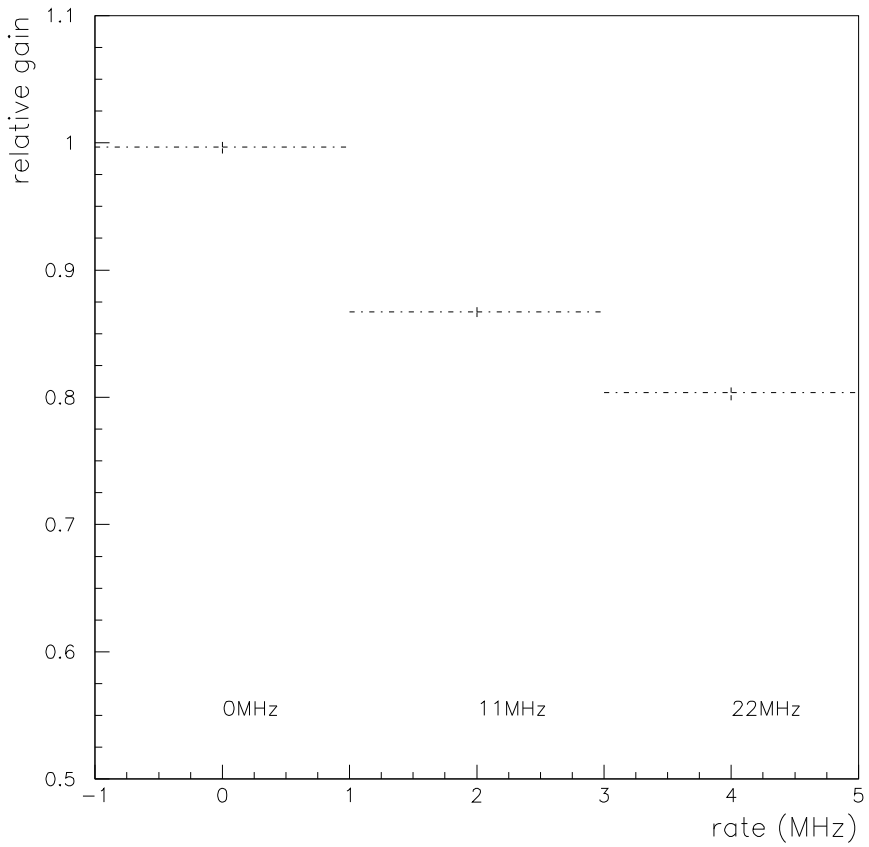

Fig. 3. Maximum gain as a function of background rate and equivalent hit occupancy.

to achieve this, but it is also possible that some of these problems are not going to be solved.

If the problems in AFEI are not solved we will see a significant degradation of our tracking efficiency (at L1 and offline) as the luminosity goes up. For example a threshold set at 2.5 p.e. for 0 MHz rate will correspond to a 3.1 p.e. threshold at 4 MHz (assuming a 20% gain reduction as seen in Fig.3, which means that the hit efficiency goes from 97% to 93% at 20% occupancy. The tracking efficiency requiring hits in 7 out of the 8 layers of the fiber tracker goes from 98% at 0% occupancy to 91% at 20% occupancy, as can be seen in Fig.6.

So far, every test we have done indicates that these problems are not going to be there for the AFEII. This will reduce the threshold setting to about 1.5 p.e. at 0% occupancy, and this threshold will move 1.9 p.e. at 20%

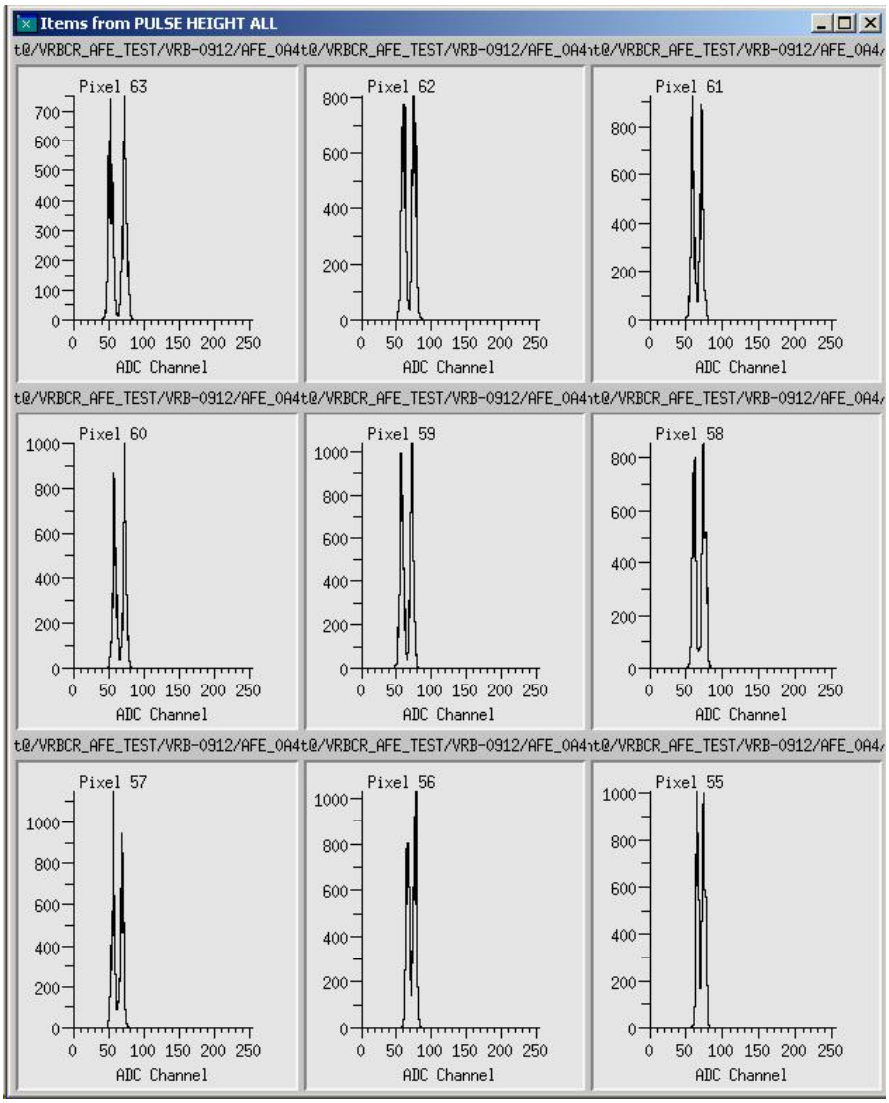

Fig. 4. A sample of split peds on a few consecutive channels. These plots are typical for channels that display split pedestals, although not all channels do. A 1 p.e. signal is on the order of 10 counts on this scale.

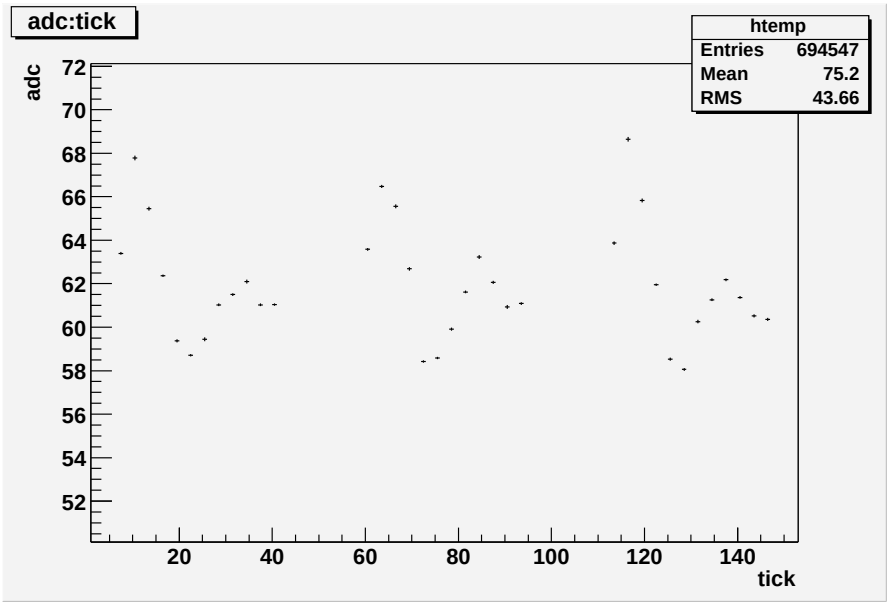

Fig. 5. A profile histogram of the average ADC counts vs. tick number. The ADC values are an average taken over the entire CFT. A 1 p.e. signal is on the order of 10 counts on the Y axis for this scale.

occupancy. As seen in Fig. 6 this reduces significantly the effect that the drop in gain has over the tracking efficiency.

3 Additional advantages of AFEII.

The are additional advantages of going to a new front then board, those are listed here.

- Detector deadtime
  The deadtime for AFEI is given by the time we require to digitize and read the information in the board with the highest occupancy. The readout clock in the AFEI (that sends the data from AFEI to Sequencer) runs at 53 MHz per byte. A board with 40% occupancy means hit in 205 channels, in addition to this the 64 channels on the VSVX (discriminator information) have to be readout for every board, making a total of 269 channels. The readout of each channel requires 2 clock cycles (2 bytes per channel), which means a deadtime of about $\frac{2\times 269}{53MHz} = 10.15$ μsec, this means that the maximum L1 rate will be 99KHz.
  With the new board this deadtime can be reduced in a number of ways. 1) No VSVX, making the timing $\delta = 7.7$ μsec. 2) In addition we could

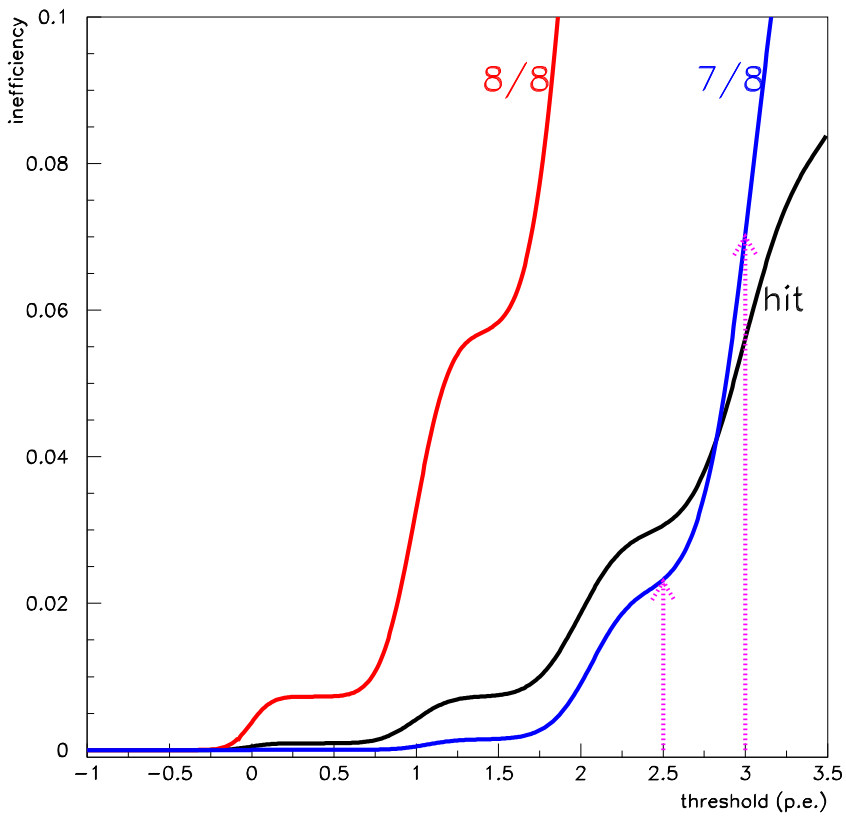

Fig. 6. Black: hit inefficiency as a function of threshold. Red: tracking inefficiency as a function of threshold requiring hits on 8 out of 8 layers of the detector. Blue: tracking inefficiency as a function of threshold requiring hits on 7 out of 8 layers of the detector. The effect of the gain reduction due to rate will move our threshold from 2.5 p.e at 0% occupancy to 3.0 p.e. at 20% occupancy, this translates into a significant increase in the tracking efficiency.

reduce the number of bits of analog information sent to the Sequencer, loosing the two LSB will gives us a dead time of $\delta = 6.8$ μsec . 3) Finally the new front end chip will allow the detector to take one event while the previous event is reading out. Without the extra buffer the fraction of the time the detector running a L1 rate τ^{-1} cannot process trigger is $F_{busy} = \frac{\delta}{\tau}$, with an extra buffer the fraction of time the detector cannot process a L1 trigger is F^2_{busy} (for this deadtimeless option we need other changes in the DØ DAQ chain).

- Replacement parts for AFEI
  Most likely some of the 200 AFEI boards that we have installed in the detector will develop problems with time that will require the replacement

of some parts, this could become an issue because we have a limited amount of replacement parts for the SVXIIe chips. We currently have on the order of 10 spare SVXIIe chips ready for installation into an MCM, we also have about 30 non-working MCMs with good SVXIIe chips that could be extracted if more spares are needed. If we need even more, we will have to use the 50 wafers at SiDet (125 SVXIIe in each wafer and 85% yield) that could be diced.
Until now 31 SVXIIe chips had to be replaced in the 200 AFEI boards. This means that, if the SVX chips continue to fail at this rate, we do not have the number of spares that we need to have a fully instrumented detector until the end of RunIIb unless we dice the extra wafers at SiDet. Building new AFEII boards will solve this problem.

- Timing readout possibility
The TriP chip (in AFEII) gives the possibility of adding timing information to the hits in the CFT. This possibility is discussed in Ref. [2]. The improvement in the tracking performance has not yet been evaluated by the tracking experts at DØ but if the CFT could be sliced in z with the timing information, a reduction in the fake tracks for high luminosity environment could be achieved.

4 Plan for continuing with AFEII development

We propose is the continuation of the AFEII effort until we have a clear picture of what will be the final performance of the AFEI.

We think that, in order to make the project still compatible with the rest of the schedule for the experiment and complete the installation of AFEII before the beginning of Run IIb, we need to have a AFEII prototype by the end of 2003. For this reason we need to start layout of the AFEII in spring 2003.

We propose an evaluation of the performance of AFEI and the prototype AFEII in December 2003. Based on this comparison, we propose to make a decision on what front end electronics we want to use for the CFT for RunIIb.

In this plan, there is very little impact to the AFEI team until the end of 2003, and the effort in solving the problems in this board will continue with the same emphasis until this time. After that, if we decide to go ahead with AFEII, the effort to keep improving the performance of AFEI will be less.

5 Resources required for continuing with AFEII development

We present an estimate for the resources required to continue the proposed development through roughly the end of calendar year 2003. These estimates are based on conversations with J. Anderson and others and the experience of the authors with AFEII development so far.

The cost of development is money, required to procure parts and printed circuit boards and labor, for the completion of the design, layout, assembly and testing. Because of the similarity between AFE and AFEII, there are natural people to perform the work. To the extent possible, we have attached the appropriate names to the task listed under the labor resources.

- M and S– The cost per prototype board is estimated to be on the order of $1600.00 per board for parts and labor for boards assembled by the vendor, or $1200.00 if the boards are assembled in house. This estimate includes the availability of some parts previously purchased. An extra $ 3000.00 should be considered for setup.
- Labor– design The engineering time to complete the board is approximately is one month of work time for J. Anderson. The schedule would require the work to be completed in a matter of 4 to 5 months, so 20 to 25% time commitment. This estimate includes the inefficiency inherent in spending less than 100% effort on the task.
- Labor– layout The layout time to complete the board is estimated to be two months of work for J. Franzen. The schedule would run concurrently with the design work, so this would represent about a 50% of the effort.
- Labor– assembly If the assembly is performed in-house, the time to complete the board is estimated to be 80hrs (two weeks) for a skilled technician.
- Labor– testing The testing of the AFEII to verify functionality and expected performance would be approximately 4 months of calendar time for P. Rubinov and J. Estrada, assuming and effort of approximately 50% of total available time.

Under ideal circumstances we would build 10 prototype AFEII boards. This number could be reduced somewhat to save on money and or labor. The minimum quantity needed to have some confidence in the performance of the new design is, in our judgment, 4 boards. The cost of the boards on a per board basis does not change. The design and layout time are not affected by the quantity of boards. The assembly time is simply 2 weeks per board and the testing time could be reduce slightly (20%) if the number of boards is reduced from 10 to 4.

References

1. B. Hoeneisen and P. Rubinov, "Design of the new MCM", DØ Note 3898.
2. J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, "MCMII and the TriP chip", DØ Note 4009.
3. J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, "Characterization of the TriP chip at 132 nsec using a modified AFE1c board", DØ Note 4076.
4. V. Buescher, F. Canelli, D. Cho, B. Davis, J. Estrada, G. Ginther, A. Schwartzman, N. Sen and P. Yoon, "Testing and Characterization of the VLPC cassettes", DØ Note 3975.