SUB MICRON AREA Nb/AlO_x/Nb TUNNEL JUNCTIONS FOR SUBMM MIXER APPLICATIONS

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Abstract

In this paper, we report on a fabrication process developed for submicron area tunnel junctions. We have fabricated Nb/AlO_x/Nb tunnel junctions with areas down to 0.1 μm^2 using these techniques. The devices have shown excellent performance in receiver systems up to 500 GHz and are currently in use in radio astronomy observatories at 115, 230, and 500 GHz.

The junctions are fabricated using a variant of the self-aligned-liftoff trilayer process[1] with modifications for electron beam lithographic patterning of junction areas. In brief, the technique involves patterning submicron holes in PMMA using electron beam lithography. The negative of this pattern is formed by thermal deposition and liftoff of chromium metal using this PMMA stencil. The chromium pattern is transferred to an underlying polyimide film using oxygen RIE. Junctions are formed by RIE using a gas mixture containing CCl_2F_2 and electrically isolated with thermally evaporated silicon monoxide. Contact wiring and coupling/tuning structures are patterned by RIE.

Introduction

SIS tunnel junctions can be modeled as a nonlinear resistor in parallel with a shunt capacitor. A good figure-of-merit of the high frequency performance of these devices is

the ratio of the capacitive reactance to the real resistance (ωRC). The RC product, for SIS tunnel junctions, is determined by the tunnel barrier thickness and is independent of the device area. The junction area is chosen to provide the best impedance match to the mixer embedding circuit and is usually a compromise between minimizing the capacitance while maintaining a reasonable real impedance. In the best case, the embedding circuit can tune out the capacitance and the junction area is chosen to make the rf-resistance match the real part of the embedding circuit impedance (approximately 50 - 100 Ω). For small RC devices, the resistance-area product is small so that achieving the appropriate resistance using a single junction requires submicron areas. Series arrays or other novel coupling mechanisms may relieve the constraint on submicron areas, however, designing these elements may require a greater understanding of the high frequency characteristics of devices and materials than is currently available. We have chosen to use single junctions in the hope that the simplicity in understanding the high frequencies behavior of the mixers may outweigh the complexity associated with the fabrication of submicron devices. Since their development[2], high quality Nb/AlOx/Nb tunnel junctions represent the only all refractory SIS technology in use in radio astronomy receiver systems. This is primarily due to their nearly ideal tunneling characteristics and physical robustness. In this paper we describe techniques for fabricating submicron devices.

Tunnel Junction Fabrication

The tunnel junction fabrication process is similar to the self-aligned-liftoff process used to fabricate refractory tunnel junctions employing optical lithography[1,3]. The primary difference arises from the need to use higher resolution lithography in the tunnel junction patterning and to maintain this resolution throughout the fabrication process. The process steps are shown schematically in figure 1.

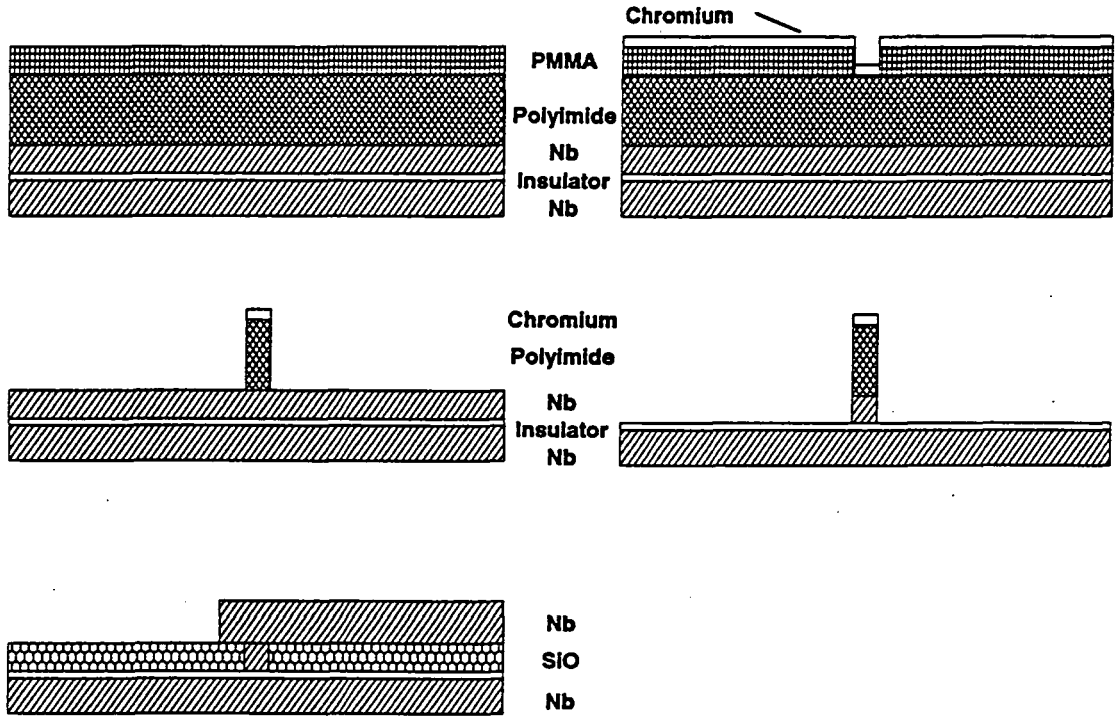

Figure 1. Submicron fabrication process schematic. (a) After trilayer deposition , wafers are spin coated with 400-600 nm of polyimide and 120 nm PMMA. (b) Chromium metal is thermally deposited. (c) Oxygen RIE of polyimide. (d) RIE of Nb counter electrode in $CCl_2F_2+CF_4+O_2$ gas mixture. (e) Deposition of SiO, lift-off, and wire electrode deposition and patterning.

a. $Nb/AlO_x/Nb$ Trilayer Deposition

The $Nb/AlO_x/Nb$ trilayer is deposited in-situ in a high vacuum system (base pressure 1.3 x 10^{-7} Pa) by magnetron sputtering. The substrates are oxidized silicon or quartz and are heat sunk to a thermal mass but not actively cooled during deposition. The large scale features of the trilayer are formed by lift-off using AZ5214 photoresist (AZ Hoechst) and image reversal. The Nb base and counter electrodes are approximately 160 nm and 120 nm respectively. The barrier is formed by depositing 6-10 nm of aluminum followed by an in-situ oxidation in an argon/oxygen gas mixture in a manner similar to that described by Morohashi et al.[3]. During this step the total process gas pressure is maintained constant by throttling the vacuum pump. A dc-plasma is formed during the oxidation process by applying approximately -500V to an aluminum ring placed in the system. This plasma has

been found to reduce oxidation times, but does not effect the quality of the barrier. After the Nb counter electrode deposition, 30 nm of gold is deposited on the trilayer to act as a contact layer.

b. Junction Patterning

The etch mask used to form the tunnel junction is patterned by electron beam (e-beam) lithography using a JEOL JBX-5 lithography system with a minimum spot size of 8 nm. The lithographic stencil must be robust enough to withstand Reactive Ion Etching (RIE) and provide a means to subsequently lift-off the SiO isolation layer. The high resolution e-beam resist, PMMA, is not suitable as the final RIE mask because it lacks the required etch resistance. Techniques have been developed which transfer the e-beam written pattern into polyimide while maintaining the required resolution[4]. The wafer is spin coated with a polyimide[5] film approximately 400 - 600 nm thick. Following a hot plate bake to drive the solvents from the polyimide, the wafer is spin coated with 120 nm of PMMA. It is then exposed in the e-beam lithography system to form holes in the PMMA film with the required junction dimensions. Chromium metal is thermally evaporated onto this stencil and the PMMA is removed in acetone, leaving metal where there were holes (polyimide is not soluble in acetone). The resulting pattern is etched in a parallel plate RIE system using oxygen gas to remove polyimide from areas of the wafer not protected by chromium. The RIE of polyimide is highly anisotropic, however, it is sensitive to surface contamination such as dust or material resputtered from the electrodes of the etcher and care must be taken to provide a clean environment for this process step. An SEM micrograph of an etch test pattern is shown in figure 2. The square etch stencils consisting of Cr(30nm) on Polyimide(550nm) have dimensions of 1.5, 1.0, 0.5, and 0.25 μm on a side. The minimum area is .06μm^2.

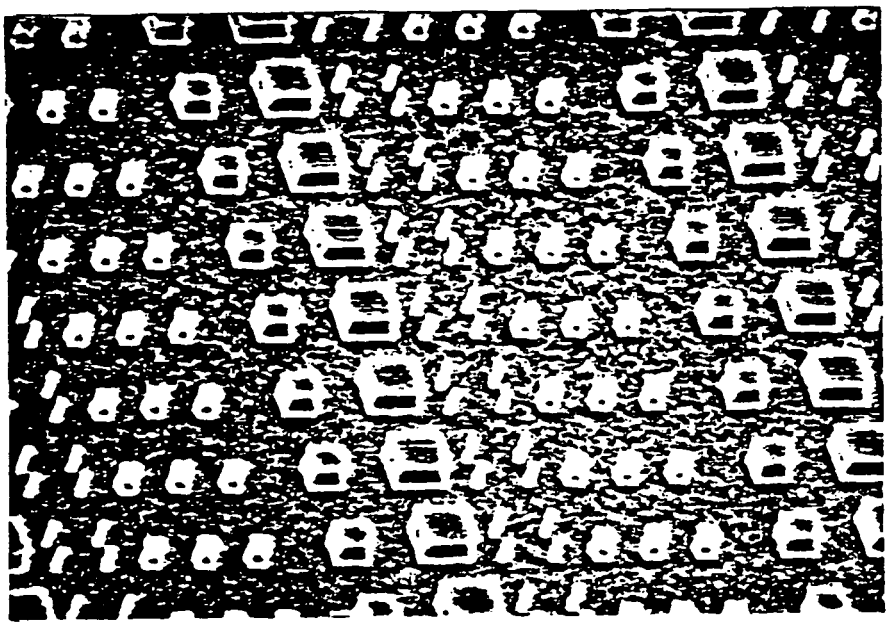

Figure 2. Test patterns etched in polyimide using oxygen RIE . The smallest features are $0.06\mu m^2$.

c. Junction Etch

The tunnel junction is formed using RIE by first etching the gold contact layer and then the Nb counter electrode. The gold is sputter etched using argon gas. Techniques for anisotropically etching Nb had to be developed. An etch profile for a submicron line patterned in an Nb film using a standard etch process (CF_4+20% O_2 ,4 Pa pressure, and 0.27 W/cm^2 power density) is shown in figure 3. The isotropic component of this etch mixture is clearly too large to be used in the fabrication of submicron devices. Anisotropy occurs in RIE when the etch mechanism requires predominantly normal incident ion impact energy to proceed[6]. Etching of Nb in CF_4/O_2 , however, occurs via a spontaneous rather than ion assisted reaction of fluorine and fluorine radicals with Nb. We have found a technique which achieves the required anisotropy. Etching with a gas mixture containing CCl_2F_2 produces very good etch anisotropy, which may be attributed to the a nonvolatile $NbCl_x$ product which forms on the sidewalls. Figure 4 shows the etch rate of Nb and NbN using mixtures of $CCl_2F_2+CF_4+O_2$. For these measurements, the total pressure was 4

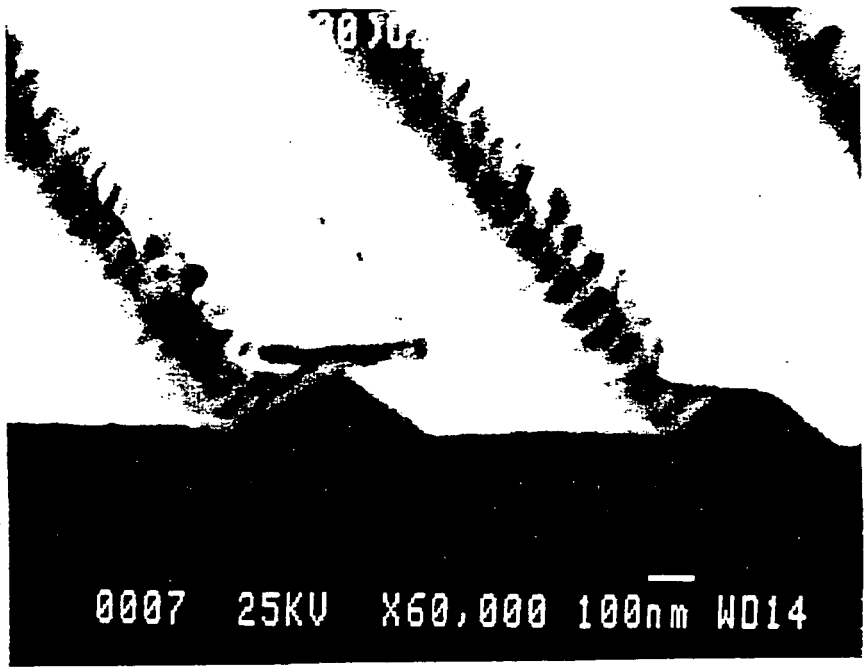

Figure 3. Submicron Nb lines etched by RIE using CF_4+O_2. The large undercut of the Nb line below the 0.4μm chromium etch stencil is evident.

Pa, the power density was 0.27 W/cm^2 and the oxygen flow was constant at 2 sccm, while the CCl_2F_2/CF_4 ratio was varied. The etch is highly anisotropic for mixtures containing greater than 60% CCl_2F_2 in $CCl_2F_2+CF_4$. Mixtures rich CF_4 exhibited isotropic etching. The region with approximately 20% to 50% CCl_2F_2 content was characterized by low etch rates and polymer formation. Shown in figure 5 is the etch profile of Nb achieved using 62% CCl_2F_2 in ($CCl_2F_2+CF_4$) and similar sample etched in CF_4+O_2. Structures etched in the CCl_2F_2 gas mixture show very little undercut while CF_4+O_2 produced a large undercut.

d. Electrical Isolation

Following the etch the counter electrode to form the junctions, a electrical isolation layer of SiO is deposited with the etch mask in place . The SiO is thermally deposited from a baffled source. To achieve good edge coverage, the samples are placed at a fixed angle

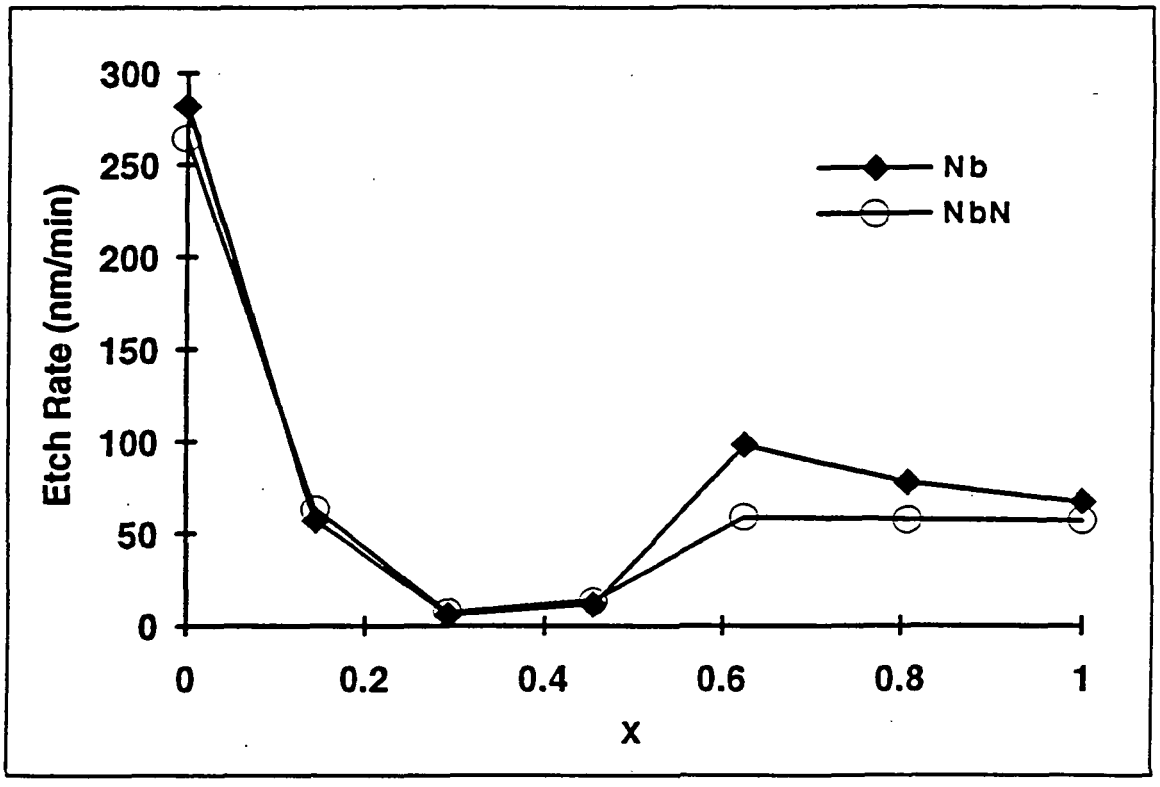

Figure 4. RIE etch rate for Nb and NbN as a function of gas composition. The etch gas consists of $85\%(x\ CCl_2F_2+(1-x)CF_4)+15\%O_2$.

relative to SiO flux and rotated during the deposition. Flux angles for normal incidence to approximately 60 degrees have been evaluated. Angles of 5-15 degrees have been found to provide a good compromise between side wall coverage and clean lift-off. SiO film thicknesses are typically 150-250 nanometers depending on the application. The polyimide and SiO are removed from the junction areas using dichloromethane solvent. A short RIE etch in oxygen is used to remove polyimide residues after the lift-off step.

e. Contact Wiring

Mixer elements are completed by depositing 250-350 nm of Nb by magnetron sputtering. The wire layer is patterned lithographically and etched using a RIE process similar to the one used for the junction etch. A typical current-voltage characteristic for a tunnel junction fabricated by this process is shown in figure 6. This device is 0.25 μm^2 in area and has a critical current density of 7.7 kA/cm^2.

Summary/Conclusions

In this paper, we have described techniques developed for the fabrication of submicron area tunnel junctions in refractory materials. The process described is applied specifically to the fabrication of $Nb/AlO_X/Nb$ tunnel junctions, however, much of the technology has also been used to fabricate NbN/MgO/NbN tunnel junctions[7] and is relevant to other submicron fabrication tasks. This process extends the self-aligned lift-off process used to fabricate refractory tunnel junctions using optical lithography. The primary new features are the use of electron beam lithography to form a submicron pattern in PMMA and the transfer of this pattern into chromium by lift-off. The chromium pattern is transferred into polyimide using oxygen RIE and the resulting Cr/polyimide is used to etch the trilayer counter electrode using a highly anisotropic RIE gas mixture containing CCl_2F_2. $Nb/AlO_X/Nb$ tunnel junctions with areas down to 0.1 μm^2 have been fabricated using these techniques. Mixer elements have been fabricated using this process for both wave guide[8,9,10] and quasi optically coupled[11,12,13] receiver systems. In wave guide receiver systems with operating frequencies up to 500 GHz, the capacitance associated with the submicron area $Nb/AlO_X/Nb$ devices is small enough so that the mixer block rf-embedding circuit provides enough tuning to achieve excellent performance (receiver noise temperatures, $T_R(DSB) = 180K$ at 485 GHz)[14] without integrated tuning structures. In principle junction areas can be scaled down further, however, in order to do so the junction relaxation times must also be scaled down so that the real part of the junction impedance in the correct range. The junction relaxation time (RC) is determined by the insulator barrier thickness, with thinner barriers producing smaller RCs. The limit for a given insulator barrier is determined by the thinnest barrier that can be achieved while maintaining suitable junction characteristics. It has been our experience with $Nb/AlO_X/Nb$ tunnel junctions, that the I-V characteristics degrade significantly for critical current densities of

greater than 15kA/cm^2 (RA≈ 12 Ω μm^2). For junctions with this current density, a 100 Ω junction has an area of ≈ 0.12 μm^2.

Acknowledgements

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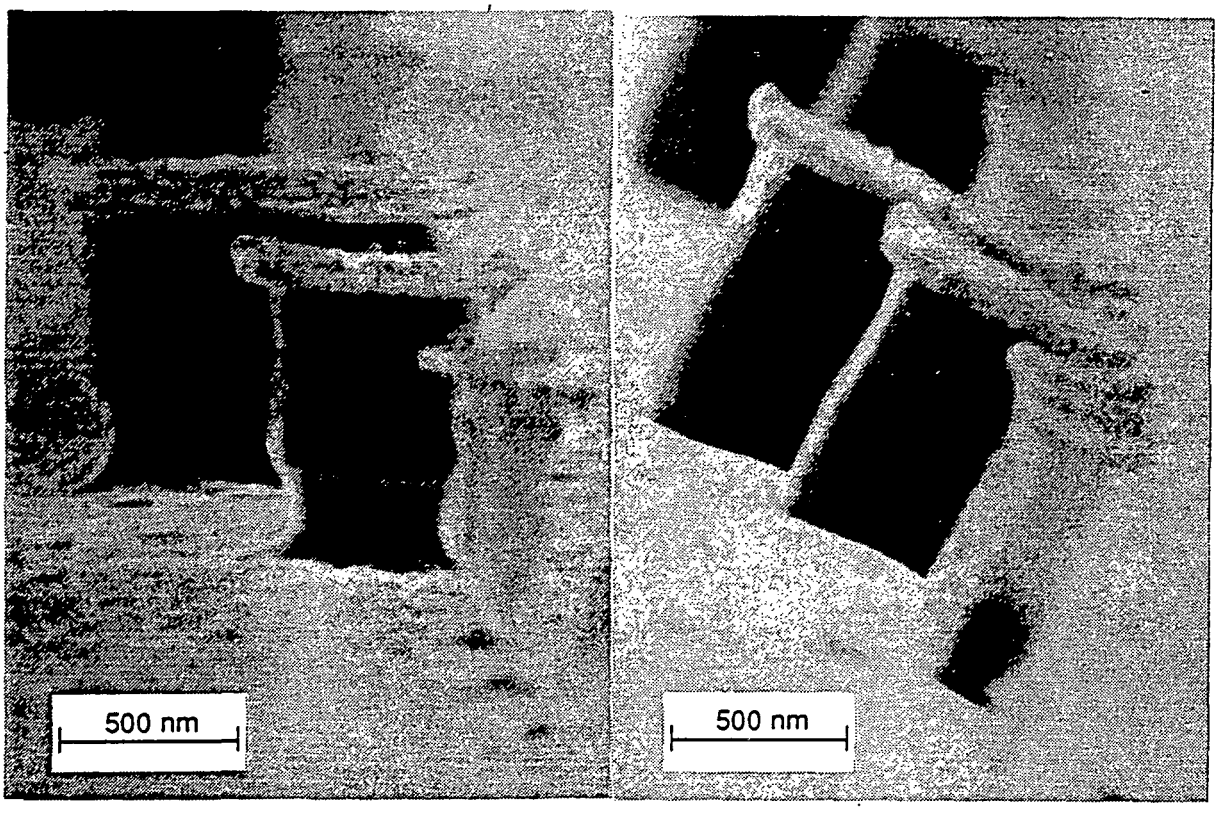

Figure 5. SEM micrographs showing etch comparrisons between CF_4+O2 (left) and CCl_2F_2+CF_4+O_2(right). The RIE mask is Cr(30 nm)/Polyimide(550 nm) patterned by e-beam lithography and oxygen RIE. The Nb film (400 nm thick) etchs anisotropically in the CCl_2F_2 containing etch gas.

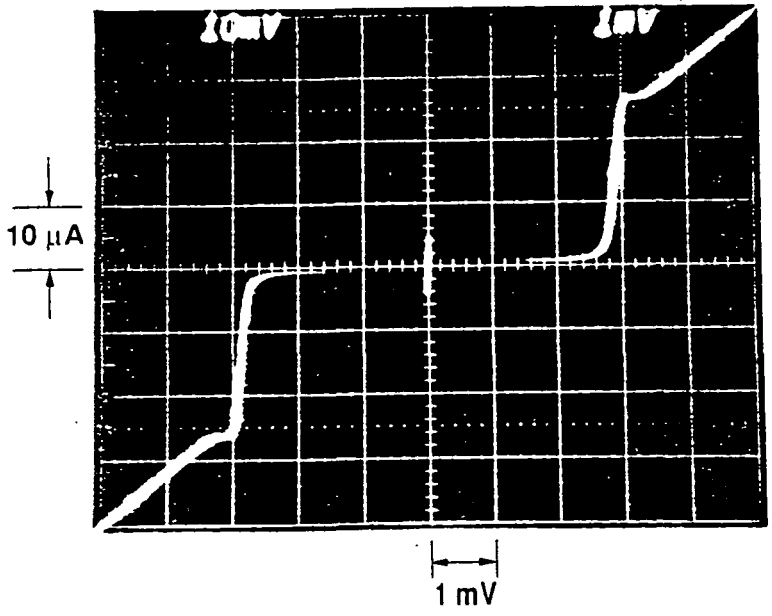

Figure 6. Typical tunneling current-voltage characteristic for a Nb/AlOx/Nb junction taken ar 4.2K. The junction area is 0.25 mm^2 and the critical current density is 7.7 kA/cm^2 .