SVX II Silicon Strip Detector Upgrade Project

TEST PORT CARD

--PRELIMINARY--

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1. GENERAL INFORMATION

This document describes the "TEST PORT CARD", hereafter referred to as TPC. The TPC is a prototype version of the Port Card to be used on the SVX II readout system. This module interfaces with the Test Fiber Interface Board (TFIB), the SVX Test Acquisition and Readout module (STAR), and with the prototype boards used to mount SVX II ICs. The STAR, TFIB, TPC, and SVX II hardware will be integrated on a VME test stand that uses the MVME 162 processor board to exercise and test the SVX II ICs and to allow the development and testing of the next generation of the SVX detector for CDF. In addition this test stand will be used to understand the performance of the SVX II IC and to develop a better understanding of the requirements for the final system.

1.1 System Introduction

The SVX II readout system is designed to perform an event data readout of the silicon detector for CDF. The front-end electronics is based on the SVX II IC. To get a better understanding of the SVX II IC and the readout system, refer to the appropriate documentation [1]. A block diagram of the hardware that makes up the test stand electronics is shown in Figure 1. The following paragraphs provide a simplified description of the test hardware.

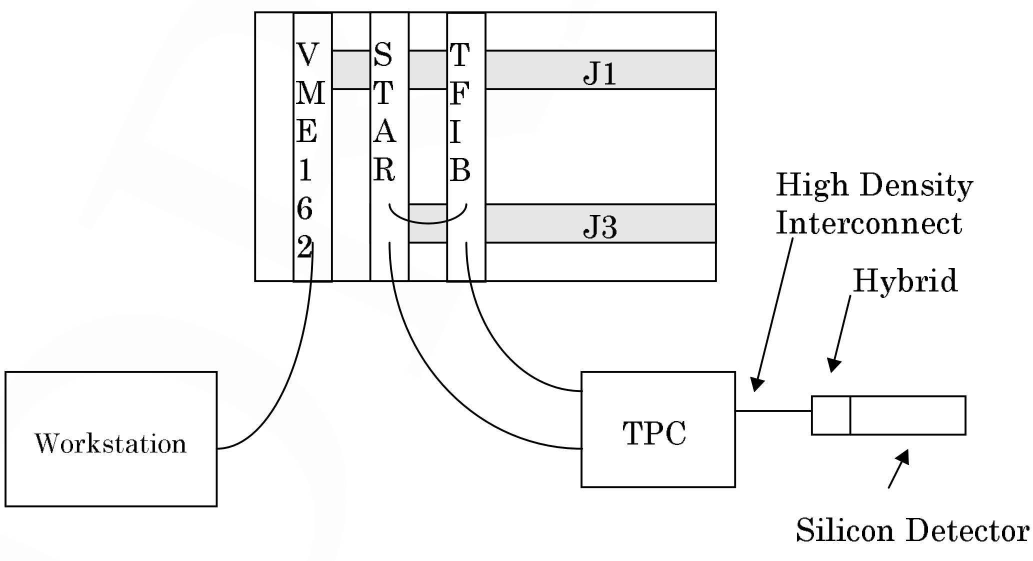

Figure 1: SVX II Test Stand Hardware

The SVX II IC implements 32 storage cells per channel and 128 channels per IC. The per channel storage capacity of the SVX II IC allows the L1 trigger to make a decision without stopping the analog acquisition of the silicon detector. At the front-end, SVX II ICs are mounted on a hybrid, and for readout purposes they behave like a single source of data. On a L1 accept (L1A), the readout control electronics instruct the SVX II ICs to stop analog acquisition, digitize the appropriate analog cell, and to transmit the samples above a pre-programmed threshold to the STAR module.

The STAR module provides the upper level functions to interface the data acquisition system to the trigger system. In this role, the STAR will accept level 1 accepts or a trigger command. Given this information, the STAR will instruct the data acquisition system to readout an event. It accomplishes this operation by sending commands to the TFIB module. The STAR/TFIB interface implements a variety of commands needed to control the test stand hardware [2,3]. In addition, the STAR module implements an event buffer to store data transmitted from the SVX II ICs in response to the readout command. The TFIB accepts high level commands from the STAR from which it generates a series of low level commands that are to be executed by the TPC. Once the data acquisition is completed, the VME CPU reads the event data from the STAR memory and transfers it to the workstation. Also, the TFIB implements the logic used to download and readout the SVX II configuration information.

1.2 Description Of Component

The TPC described in this document is a prototype design that will be used on the prototype version of the SVX II data acquisition system. This design allows the testing many of the features to be implemented on the final version of the Port Card. As previously mentioned, the TPC will be integrated on a test stand with the TFIB and STAR modules to fully exercise the SVX II ICs and to allow the development and testing of the next generation of SVX detector for CDF.

2. THEORY OF OPERATION AND OPERATING MODES

2.1 Basic Features & Operation

A block diagram of the TPC is shown in Figure 2. As shown the TPC interfaces with the TFIB, the STAR, the SVX II HDI (i.e. HDI/Hybrid), and with a workstation. The design and development of the TPC becomes a complicated task given the limited timing information on the SVX II IC and the final requirement that it will reside in a radiation environment. With this in mind, a rad-hard Xilinx FPGA currently under design by Harris has been selected to implement the TPC Controller (TPCC). For the initial design, an equivalent non rad-hard Xilinx part will be used. The use of a programmable device to implement the main control

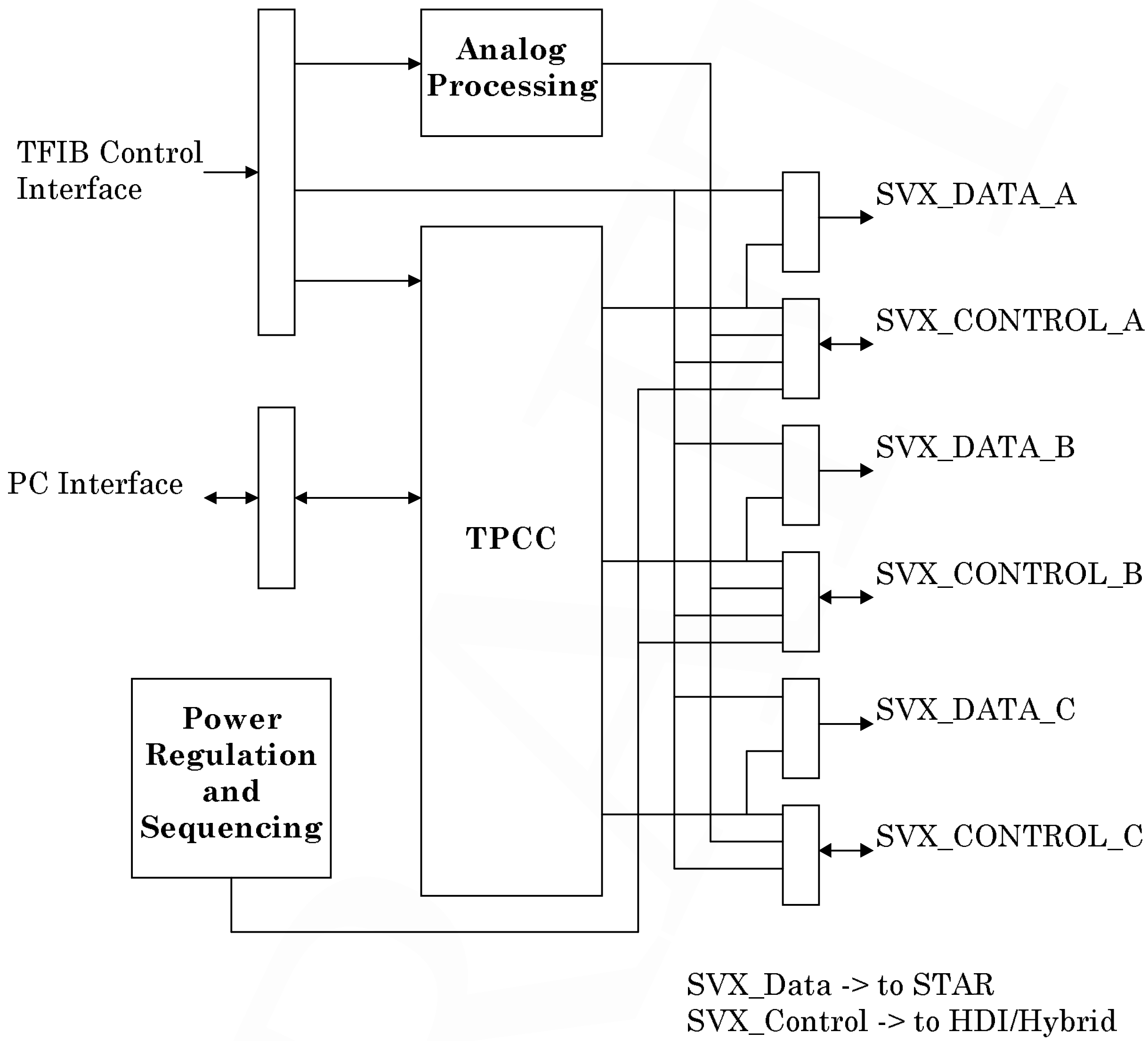

Figure 2: TPC Block Diagram

functions of the TPC allows for the implementation of changes as the data acquisition demands them. The initialization and programming of the TPCC on the TPC is done by the TFIB under VME control. In addition the TPC implements a PC link to download programs and diagnostics to the TPCC.

The basic functions and features of the TPC are provided on the following list:

- Implements three ports of initialization, control, and data readout for SVX II ICs (i.e. SVX_CONTROL_A, SVX_CONTROL_B, and SVX_CONTROL_C) as shown in Figure 2.
- During SVX II IC initialization, selects the appropriate port to download data.
- Executes control commands transmitted by the TFIB.
- Buffers the SVX clock and drives the SVX II ICs.
- Recognizes the end of readout from the SVX II ICs (EOR) and inserts an EOR control word into the readout data stream.
- Transmits SVX II event data with associated clock to the STAR.
- Regulates the power supply used by the SVX II ICs and provides a variable regulator for the AVdd2.
- Implements power supply protection circuits to avoid damage to the SVX II ICs.
- Provides a serial interface to download the DACs used to generate the analog control signals used by the SVX II ICs.
- Implements several diagnostics functions to guarantee the integrity of the data paths.
- The main control configuration program on the TPCC is downloadable via the TFIB interface or with the personal computer interface.

Basically, the control of the SVX-II chips is split into the TFIB board and the TPC board. In this application, the TPC is an extension of the TFIB that provides local control to the SVX II ICs. The control functions have been divided between these two modules in such a way that the TFIB has been selected to execute what is called *high level commands,* and the TPC executes *low level commands*. This approach is taken to reduce the complexity of the TPC controller so that the commands can be implemented with the available resources in the FPGA part.

The control of the TPC and associated SVX ICs is implemented by a serial interface that includes three signals which are a serial command signal (**SR_Cmd**), a serial command clock (**SR_CLK**), and the SVX clock (**SVX_CLK**). In the TPC, the control functions are implemented by the TPC Controller (TPCC). The functions supported by the current implementations are SVX initialization and readout, enter acquisition mode, preamplifier reset, calibration inject, perform digitization/readout, and readback TPCC FPGA configuration. The TPCC implements a control sequence for each of the command codes. Once the command has been transmitted, the TFIB sequences the TPCC through the different states with the SR_CLK signal. Note that the TPCC requires a fix number of SR_CLK rising edges to complete the command execution before it can be ready to execute a new command. In addition the TFIB controls the state timing sequencing by controlling the time between clock edges. All the commands supported by the TPCC are implemented with a single FPGA configuration. The specific details of the TPCC implementation are provided later.

The TPC is also used during initialization to configure the SVX II ICs. To initialize the SVX II ICs, the TPC works in combination with the TFIB to download the configuration data into the SVX II ICs. For this application, the SVX II ICs are programmed for *initialization*. The sequence of steps to initialize the SVX II ICs is as follows:

- VME CPU downloads SVX II ICs configuration data into the TFIB.
- VME processor board requests download operation from the TFIB.
- TFIB sends the SVX II ICs initialization command to the TPC.
- The TFIB pulses the SR_CLK to advance the sequencer of the TPCC such that it can program the SVX ICs for configuration downloading.
- TFIB transmits serially the configuration data and pulses the SVX_CLK line.
- Repeat previous last step until downloading is completed.

In data acquisition mode, the TPC executes commands delivered by the TFIB. To emulate data acquisition mode, the TFIB implements a command FIFO that is downloaded via VME. In FIFO mode, the TFIB works independent of the STAR which allows isolated debugging of the TFIB, TPC, and SVX II ICs hardware. A detailed description of this hardware is provided in the TFIB document [2]. In either case, the data acquisition commands executed by the TFIB are *high level* commands. As previously mentioned, from these commands the TFIB generates a sequence on primitives and timing sequences that are passed to the TPC to be executed in synchronism with the TFIB. As an example, the following is the sequence of steps used to perform an event readout.

- The STAR sends, through the J3 back plane, a 53 MHz clock, sync, and a command to the TFIB. Detailed implementation of this interface is included in the STAR document [3].
- The TFIB interprets the command from the STAR and sends to the TPC the SVX-II clock, the serial command clock, and series of commands that implement the requested operation.
- The TPC controller delivers these commands and clocks to the SVX-II chips.

- SVX-II chips transmit the data to the TPC.
- The TPC converts the data to differential PECL and transmits it to the STAR.

This is only one example of control flow implementation on this data acquisition system. There are other commands initiated at the STAR and destined to the SVX II ICs. In principle the control flow for other operations is as described above.

The following sections provide a detailed description of the hardware features implemented on the TPC. Given that the main controller on the TPC is implemented on a Xilinx FPGA with limited resources and speed, preliminary timing information has been provided in appendix A4. With regard to event readout, design goals are being presented given the limited timing information available on the SVX II ICs.

2.2 TPC Main Controller (TPCC)

The block diagram for the TPCC is shown in Figure 3. The TPCC is the main controller on the TPC, and it is operated under tight control from the TFIB. The TPCC implements three major blocks: a command decoder, a state machine, and a state decoder used to drive the SVX II control lines. In general the execution of a command has three phases. First, the TFIB transmits the command using SR-CMD and SR-CLK. Second, the TFIB transmits the SR-CLK pulses to advance through the states that when decoded generate the appropriate SVX II control sequence. Also, during this phase the TFIB can transmit SVX-CLK pulses as required by the state. Finally, the TFIB transmits SR-CLK pulses to put the state machine in the state that interprets commands. The state tables for the implemented commands are provided in appendix A5. The state of the SVX control lines is determined by the sequencer state, and the timing between states is determined by time between SR-CLK edges. This implementation minimizes the demand for resources on the FPGA that implements the TPCC and also delegates all the detail timing needed by the SVX II IC to the TFIB.

Note that the timing of these operations is controlled by changing the timing between clock edges (i.e. the SR_CLK) transmitted by the TFIB. Also, the SVX_CLK is under TFIB control such that the appropriate SVX II clock is being transmitted as required by the operation. For example, after setting the SVX II ICs for acquisition mode, the TFIB will pulse the SVX_CLK for every beam crossing. Similarly, during digitization, the SVX_CLK will be at 53MHz and during readout at 26.5MHz. These last frequencies are instantaneous frequencies that change while the operations are taking place

The current plan for SVX II detector readout is based on three HDI/Hybrids ports per Port Card. To prototype this concept, the TPCC implements the required logic to connect to three chains of SVX II ICs as shown in Figure 3.

2.3 TPC CONTROLLER MICROCOMMANDS

The TPCC receives microcommands from the TFIB through the Serial-Command (SR-Cmd) and Serial Clock (SR-CLK) lines. The microcommands are loaded serially (MSB first) with the SR-CLK. The sequencer microcommands are executed by sending the microcommand (start bit + 3 bits) followed by several clocks (i.e. SR_CLKs) to cycle through the states. The number of SR_CLKs required to execute the microcommand after it has been downloaded is provided in Table I. The number of clocks (i.e. SR_CLK pulses) is dependent on the number of states used to implemented the microcommands. Note that these commands are independent of each other and that it is required to properly complete the execution of one command before another one can be requested. A non detailed timing diagram for the sequencer commands is shown in Figure A4.3.

2.3.1 TPC CONTROLLER MICROCOMMANDS DESCRIPTIONS

This describes the microcommands implemented by the TPCC. To establish a relation between these microcommands and the SVX II ICs, some of the signal names used in the SVX II IC Beginner's Guide were used [1]. In addition the microcommand description assumes that the user understands the operation of the SVX II IC.

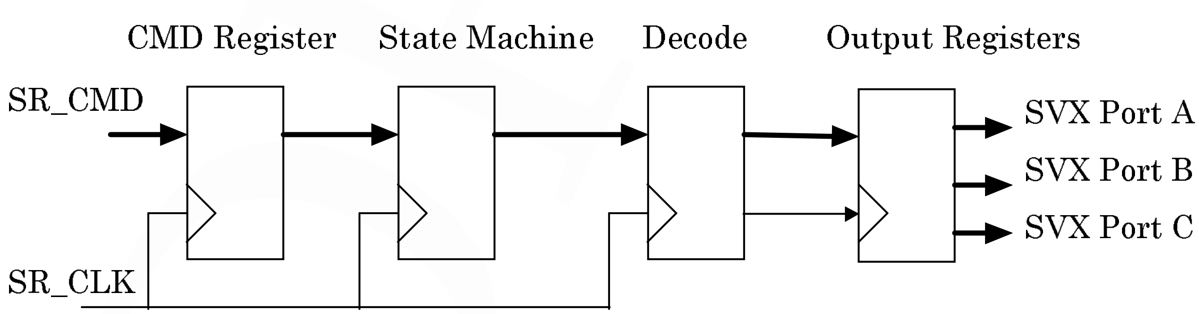

Figure 3: Test Port Card Controller Logic Block Diagram

CMD	Name	Description	Clocks
0	unused	unused	0
1	INIT	Enter the initialization mode	2 + 4 + 2
2	ACQ	Enter the acquisition mode	4
3	RSTPA	Reset the preamplifier	1 or 2
4	CALIN	Calibration inject	1 or 2
5	RDOUT	Perform digitization and readout	16
6	RBX	Read back FPGA configuration	2
7	unused	unused	0

Table I: Command Code Definitions

2.3.1.1 Initialize (INIT) microcommand

The initialize microcommand is used to load the configuration bit stream into the SVX II ICs. The microcommand is followed by two bits clocked with SR-CLK to select the HDI port to load. The next four SR-CLKs change the selected HDI chain of SVXII chips to the initialize mode. Once in the initialize mode, any data placed on the SR-CMD input is passed to the Serial Input of the first SVXII chip in the selected chain, and the Serial Output of the last SVXII chip in the chain is placed on the BUS1 line of the SVXII ICs. The configuration data is then clocked into the SVXII chain with the SVX_CLK. The last two SR-CMD clocks perform the SR-LOAD of the parameters into the chips and loops the serial output back to the serial input. The configuration data can then be clocked out of the SVXII chain with the SVX-CLK for read back verification. By driving BUS1, the TPCC makes the configuration data available to the TFIB (or STAR) on the SVX II data readout port (i.e. bit 1).

The following procedure is recommended for configuring the SVXII chips:

- Issue Acquire microcommand to place all chips in known state.
- Issue Initialize microcommand sequence to first HDI chain.
- Issue Acquire microcommand to place all chips back in known state.
- Issue Initialize microcommand sequence to second HDI chain.
- Issue Acquire microcommand to place all chips back in known state.
- Issue Initialize microcommand sequence to third HDI chain.
- Issue Acquire microcommand to place all chips back in known state.
- End of initialize procedure.

HDI Code	HDI Port
0	all
1	A
2	B
3	C

Table II: HDI Code Definition

2.3.1.2 Acquire (ACQ) microcommand

The acquire microcommand sets all SVXII chips in the HDI A, B and C chains to sample data from the detector. The acquire microcommand is followed by four SR-CLKs that sets all chains of SVXII chips into the acquire mode. This is the recommended default mode.

2.3.1.3 Reset the Preamplifier (RSTPA) microcommand

The RSTPA microcommand generates a PA-RST pulse to all SVXII chips on all chains. The RSTPA microcommand is followed by one SR-CLK that raises the BUS0 which is then interpreted by the SVXII ICs as preamplifier reset (i.e. PA-RST) when the chip is in acquire or initialize mode. Therefore, the command should be requested only when the SVXII ICs are in the appropriate mode. The PA-RST line is lowered by another SR-CLK which can be a individual clock or the first clock of another microcommand.

2.3.1.4 Calibration Inject (CALIN) microcommand

The CALIN microcommand generates a CAL-INJECT pulse on the BUS1 line to all SVXII chips on all chains. The CALIN microcommand is followed by one SR-CLK that raises the CAL-INJECT line. The CAL-INJECT line is lowered by another SR-CLK which can be an individual clock or the first clock of another microcommand. This command should only be generated when in acquire mode. This microcommand has no effect in the INIT or RDOUT modes.

2.3.1.5 Readout (RDOUT) microcommand

The RDOUT microcommand generates a pipeline readout, digitization, and data readout sequence to all SVXII chips on all chains. The RDOUT microcommand is followed by sixteen SR-CLKs that sequence the SVXII chips through the states required to perform these operations. Only the acquire or initialize microcommands should be executed after a RDOUT sequence. The RSTPA and CALIN commands have no effect in this mode.

2.3.1.6 Readout Back FPGA configuration (RBX) microcommand

The RBX microcommand generates a read trigger pulse to enable read back of the FPGA configuration information. When in this mode, the configuration data is clocked out on the BUS7 line with SR-CLK. It is recommended that the SVXII chips be put in acquire mode, but this command should work in any mode.

2.3.1.7 Additional Control

The interface between the TFIB and TPC implements a formal reset mechanism. To guarantee that the TPCC is in the state that interprets microcommands, the TFIB implements a command that sends SR_CLK (i.e. more than sixteen) to initialize the TPCC

2.4 TPC Analog Section

The TPC implements eighteen DACs to provide six calibration voltages, six ramp reference voltages and six ramp pedestal voltages. To minimize the amount of circuitry and support logic, the TPC uses three octal 12 bit DACs with a serial programming interface. Each HDI (i.e. A, B and C) will have six independent voltages (2 calibration, 2 ramp reference and 2 ramp pedestal) to supply independent sets of signals to the ϕ and z planes. Each HDI (i.e A, B and C) is feed with a separate DAC, leaving two unused DACs per package. The voltage range and resolution for the calibration, ramp reference, and ramp pedestal is provided in Table III. The resolution shown will degrade due to the presence of digital circuitry noise and power supply noise. In particular, this implementation relies on the software to program the ramp reference and ramp pedestal with the appropriate relation needed between these two voltages.

Signal	Min. Voltage	Max. Voltage	Resolution
Calibration	0V	5.0V	1.22mV
RAMP_REF (RF)	0V	3.5V	.85mV
RAMP_PED	0V	3.5V	.85mV

Table III: Analog Control Signal Voltage Range

2.5 SVX Power Supplies

The TPC provides power regulators for each of the four supplies used by the SVXII ICs (i.e. AVdd, AVdd2, DVdd and QVdd). All of the regulators are adjustable and provide a logic level shutdown input. The typical voltages for these supplies is provided in Table IV.

Supply	Vmin	V nominal	Vmax
AVdd		5.0V	
AVdd2	3.5V		5.0V
QVdd		5.0V	
DVdd		5.0V	

Table IV: SVX II Supplies

2.5.1 Power Sequencing and Protection

The current version of SVXII IC is sensitive to power up sequence on the AVdd, AVdd2, DVdd and QVdd. Failure of a supply can also cause damage to the ICs. To minimize the potential damage of the ICs, the TPC implements two types of power up sequencing mechanisms. The selection of which mechanism is use is done via a jumper. The recommended method uses a single switch that once it is moved to the on position will start a sequence to turn on the SVX II IC supplies. The sequence turns on one power supply at a time with a delay 10 ms. The second option associates a switch with each supply and the user controls the sequence directly from the switches.

In addition to the power up sequence, the TPC implements a monitoring circuit that will turn off the power supply whenever one of the supplies reaches a low threshold. The power shutdown operation does not implement power turnoff sequencing. It shuts down all supplies simultaneously (AVdd, AVdd2, DVdd and QVdd) and discharges the bypass capacitors with power FETs.

2.6 Diagnostic Features

The current design ideas for the TPC has limited features for testing it's internal operation. To assist during the development of the TPC, a computer port has been included that allows downloading and testing of the Xilinx FPGA.

2.6.1 Interface Specifications

This section describes the interfaces implemented by the TPC. The timing specifications for these ports are provided in Appendix A4. The TPC implements four interfaces: the TFIB command port, the SVX II control port, the SVX II data readout port, and the FPGA download and diagnostics port.

2.7 TFIB Command Port Interface

The main function of this port is to transfer commands from the TFIB to the TPC. These commands are decoded at the TPC, and the appropriate control is supplied to the SVX II ICs. Refer to Appendix A4 for timing examples for this interface. The interface implements the following signals: a serial command signal, a serial command clock, and the SVX II IC clock. These are unidirectional differential signals implemented with PECL levels.

This port also implements all of the signals required to download the DACs on the TPC and to readback the last value programmed.

2.7.1 TFIB Connector Pin Configuration

The TFIB command interface is implemented on a 40 conductor 100 mil pitch twist and flat cable. The differential signal pair consist of a "signal" and "signal*", where a 1 bit has the "signal" at it's most positive voltage and "signal*" at it's most negative voltage. The analog signals are also differential and intended for single power supply operation (i.e. one signal is a reference ground). The connector pinout is provided in Table V.

2.7.2 TFIB Connector Signal Description

This subsection provides a description of the signals implemented on the TFIB command connector. For simplification, only the "signal" name is referenced. The connector pin assignment is shown in Table V.

- **SVX_CLK:** PECL SVX II IC clock. This clock is buffered at the TPC and passed to the SVX II ICs.
- **SR_CLK:** PECL serial command clock used to clock the serial commands and also as the main clock for internal operations of the TPCC.
- **SR_Cmd:** PECL signal used to transmit commands to the TPC.
- **Cmd[1:6]:** PECL, spare set of command lines.
- **DONE_PROG*:** Signal to put FPGA into initialization mode.
- **D_CLK:** Serial clock for loading data into DACs.
- **D_IN:** Serial data for DACs.
- **D_SEL[1:0]:** DAC select lines.
- **D_LDAC:** Signal used to latch serially shifted data into selected DAC.
- **FSIN_IN:** Enable signal for DAC downloading.
- **D_DOUT:** Serial data retransmitted by selected DAC.
- **EN_XMT:** Flags data valid on D_DOUT signal.
- **CLK_OUT:** Clock for serial data D_OUT.

Pin Number	Signal	Pin Number	Signal
1	SVX_CLK	2	SVX_CLK*
3	NC	4	NC
5	SR_CLK	6	SR_CLK*
7	SR_Cmd	8	SR_Cmd*
9	Cmd[1]	10	Cmd*[1]
11	Cmd[2]	12	Cmd*[2]
13	Cmd[3]	14	Cmd*[3]
15	Cmd[4]	16	Cmd*[4]
17	Cmd[5]	18	Cmd*[5]
19	Cmd[6]	20	Cmd*[6]
21	DONE_PROG	22	DONE_PROG*
23	D_CLK	24	D_CLK*
25	D_DIN	26	D_DIN*
27	D_SEL0	28	D_SEL0*
29	D_SEL1	30	D_SEL1*
31	D_LDAC	32	D_LDAC*
33	FSIN_IN	34	FSIN_IN*
35	D_DOUT	36	D_DOUT*
37	EN_XMT	38	EN_XMT*
39	CLK_OUT	40	CLK_OUT*

TABLE V: TFIB Command Interface Pinout

The SR_CLK, SR_CMD and SVX_CLK are the signals used by the TPC to implement the control of the SVXII ICs. The use of these signals was described in previous sections. The DONE_PROG is a signal used to put the TPC FPGA into initialization mode. During initialization, the TFIB uses the SR_CMD and SR_CLK to download configuration data into the FPGA. The spare command signals, CMD[1:6], are included to allow for the implementation of a parallel command interface as may be allowed by the DOIM. The other signals in this connector are used to program the three octal DACs used on the TPC and to readback the digital data received by the TPC. A timing diagram for the downloading and the reading of the DACs is provided in appendix A.4.

2.8 SVX Control Port Interface

The TPC implements three ports to control three HDIs (i.e. clusters of SVX II ICs). The signaling for each of these ports is determined by SVX II IC specification [1]. The TPC implementation of this interface is defined by the SVX II IC test board developed at LBL. This is an interface that allows direct connection to the SVX II IC, and it will allow for the initial testing of the TPC. A 60 conductor connector is used at the TPC. It is anticipated that a adapter with a different connector will be designed to interface to the SVX II hybrids. There are three of these connectors on the TPC that are discriminated by indexing the signal names provided with A, B or C (refer to Figure 2).

2.8.1 SVX Control Port Connector Pin Configuration

The SVX II control connector is implemented on a 60 conductor 100 mil pitch connector. The same connector pinout is used for the three HDI ports implemented on the TPC. The connector pin assignment for HDI A is provided on Table VI. The connector for HDI B and C have equal pin assignments except that the specific signals are indexed with B or C respectively.

Pin Number	Signal	Pin Number	Signal
1	TNBR_A	2	GND
3	DA[7]	4	GND
5	DA[6]	6	GND
7	DA[5]	8	GND
9	DA[4]	10	GND
11	DA[3]	12	GND
13	DA[2]	14	GND
15	DA[1]	16	GND
17	DA[0]	18	GND
19	SVX_CLKA	20	GND
21	SVX_CLKA*	22	GND
23	GND	24	GND
25	DVdd	26	GND
27	CHG_MODE_A	28	GND'
29	AG	30	GND'
31	QVdd	32	GND'
33	MODE 1_A	34	GND'
35	MODE 0_A	36	GND'
37	AVdd	37	GND'
39	AGND	40	GND'
41	AVdd2	42	GND'
43	AGND	44	GND'
45	CAL_A1 (ϕ)	46	GND'
47	AGND	48	GND'
49	BNBR_A	50	GND'
51	NC	52	CAL_A2 (z)
53	RAMP_REF_A1(ϕ)	54	RAMP_REF_A2 (z)
55	RAMP_PED_A1(ϕ)	56	RAMP_PED_A2 (z)
57	AGND	58	AGND
59	AGND	60	AGND

GND' - Digital or analog ground NC - No Connection

Table VI: SVX Control Connector Pinout

2.8.2 SVX II Control Port Signal Description

The following is a description of the SVX control connector signals. The control signals for the SVXII IC (i.e. TNBR, DATA[0:7], CHG_MODE, mode 0 & 1 and BNBR) are driven by the TPCC under TFIB control. The analog control voltages are programmed by executing VME operations to the appropriate register on the TFIB (refer to [2]).

- **TNBR:** SVX II IC top neighbor signal.

- **DATA[0:7]:** This is a dual purpose bus. During normal operation this bus is used to control the SVX II ICs, and during data readout, the SVX II ICs use this bus to transmit data to the STAR.

- **SVX_CLK:** This is the PECL clock for the SVX II ICs.

- **DVdd:** Signals used to transmit the digital Vdd and digital ground for the SVX II ICs. The tolerances on this supply are to be determined.

- **CHG_MODE:** Signal used to strobe the mode specified by Mode[0:1].

- **AVdd :** Signals used to transmit the analog Vdd and the quiet Vdd supply used by the SVX II IC. Nominal value between these two pins is 5 Volts. The tolerances on this supply are to be determined.

- **Mode[0:1]:** Signals used to control the operation mode of the SVX II ICs.

- **AVdd2 :** Signal used to transmit the analog Vdd2 supply used by the SVX II IC. The nominal value for the supply will be set at the TPC with an anticipated range between 2 and 5 volts. Tolerance on this supply are to be determined.

- **CAL_A1, CAL_A2:** Signals used to transmit the calibration signal (with associated ground) to the SVX II ICs. The signal range is 0 to 5 volts.

- **BNBR:** SVX II IC Bottom Neighbor signal.

- **RAMP_REF 1 & 2:** Signal used to transfer the ramp reference for the ϕ and z planes. The voltage range for this signal is 0 to 3.5V volts.

- **RAMP_PEDESTAL 1 & 2**: Signals used to transfer the ramp pedestal for ϕ and z planes. The voltage range for this signal is 0 to 3.5V volts.

2.9 SVX Data Readout Port Interfaces

The following is a description of the SVX Data Readout Port connector signals. There are three of these connectors on the TPC that are discriminated by indexing the following names with A, B, or C (i.e. SVX_DATA_A, SVX_DATA_B and SVX_DATA_C) as shown in Figure 2. Each of these interfaces implement 8 unidirectional PECL differential data signals and a readout clock (i.e. 26.5 MHZ). The connector pin assignment is provided in Table VII.

Pin Number	Signal	Pin Number	Signal
1	DATA[0]	2	DATA*[0]
3	DATA[1]	4	DATA*[1]
5	DATA[2]	6	DATA*[2]
7	DATA[3]	8	DATA*[3]
9	DATA[4]	10	DATA*[4]
11	DATA[5]	12	DATA*[5]
13	DATA[6]	14	DATA*[6]
15	DATA[7]	16	DATA*[7]
17	CLK	18	CLK*
19	GND	20	GND

Table VII: SVX Data Readout Port Pin Assignment

2.9.1 SVX II Readout Port Signal Description

The following is a description of the SVX readout port signals. All the signals on this connector are implemented in PECL levels. They are "signal" and "signal*" and for the signal description provided below only the "signal" name is provided. A 1 bit has the "signal" at it's most positive level and "signal*" at it's most negative level.

- **DATA[0:7]:** This has two uses. First, it is used to transfer the event data from the SVX II ICs. Second, during SVX II configuration, the TPC will drive data of TNBR into DATA[1] (i.e. data shifted out of SVX ICs chain). Also, during readback of the FPGA configuration, data is placed on Data[7].

- **CLK:** The 26.5 MHz SVX II readout clock is driven into this line.

The CLK signal is a buffered version of the SVX_CLK received by the TPC, and there are no adjustments done at the TPC to align this clock with the SVX II data. It is assumed that the STAR and the TFIB will provide a delay adjustment to synchronize the data with the clock. For a timing diagram of this port, refer to Figure A4.4.

2.10 PC Interface

The PC interface is provided to facilitate the initial testing of the TPC. This port is compatible with the XChecker Universal Download/Readback Cable and Logic Probe supplied with the Xilinx's development software [5]. For more details, refer to Xilinx's documentation.

3. ELECTRICAL & MECHANICAL SPECIFICATIONS

3.1 Packaging & Physical Size

The TPC is designed as a standalone board with the interfaces described previously. The size of the board is approximately 7 in. by 10 in. .

3.2 PC Board Construction

The TPC PC board is made up of four power/ground planes and four signals planes. The thickness of the board is 93 mils. The layer stack for the PC board is shown in Appendix A7.

3.3 Power Requirements

The following table provides an estimate on the current requirements for the TPC. The current shown for the 6.5 volt power supply is for the case that the TPC is driving three hybrids with a total of 28 SVX II ICs.

Voltage	Current (max)	Usage
6.5_1V	0.5A	Analog section/SVX II supplies.
6.5_2V		SVX II ICs supplies
-6.5V	0.5A	Analog section.
5.0V	2.0A	TPC Digital section.

Table VIII: Power Supply Requirements for TPC

3.4 Cooling Requirements

To be determined.

4. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

4.1 Module Fusing & Transient Suppression

The current plan for the TPC is to be powered with three power supplies (a 6.5V, a -6.5V and a 5.0V). Note that the TPC has two separate 6.5V connections that are fused separately, but that are planed to be connected to the same supply. Based on table VIII and accounting for transient conditions, the 6.5V supply will be fused with a 0.5A fuse, the -6.5V with 0.5A fuse, and the 5.0V with a 2.0A fuse. In addition, transorbs are included to protect against overvoltage conditions on each power supply.

5. APPENDICES

5.1 A1: Parts List

5.2 A2: Schematics

5.3 A3: PAL, FPGA Equations

5.4 A4: Timing Diagrams

This appendix provides the timing diagrams for the different interfaces implemented at the TPC. Given the current state of the design, some of the timing specifications provided are not precise. This information will be provided as soon as the appropriate information becomes available.

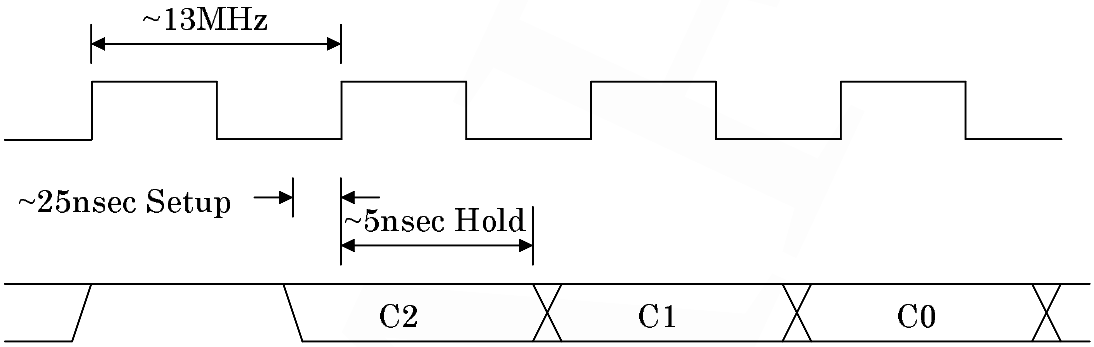

Figure A4.1: Serial Port Command Timing Diagram

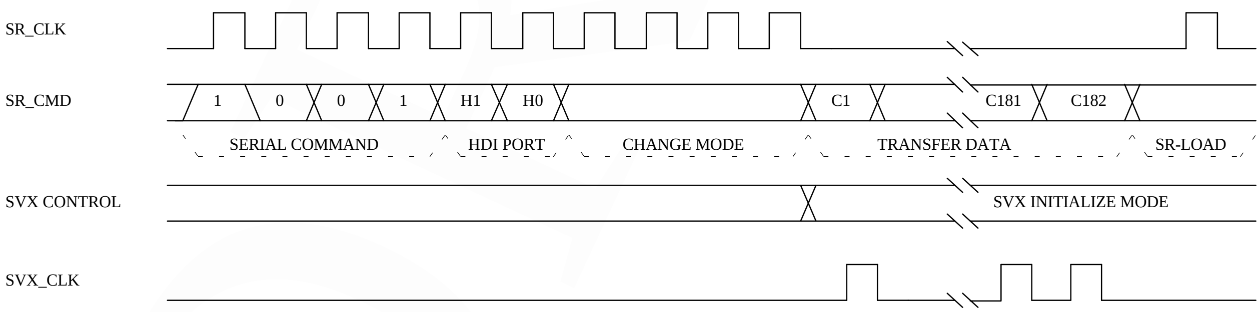

Figure A4.2: SVX IC Initialization Timing Diagram

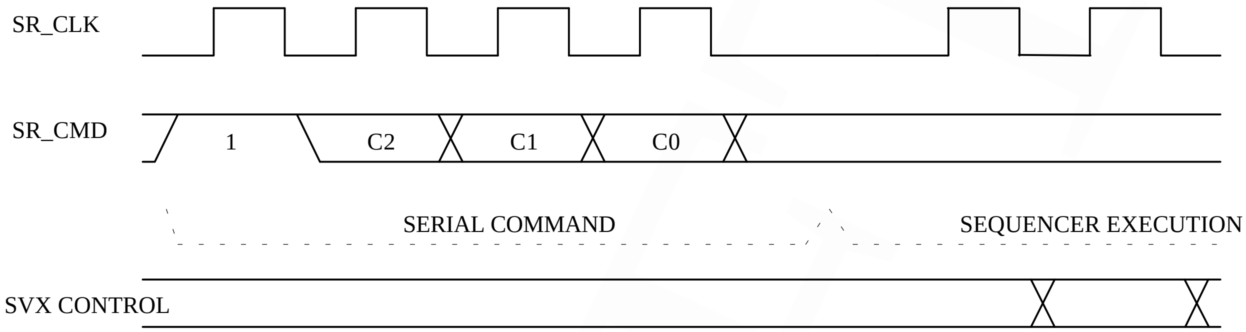

Figure A4.3: Sequencer Type Command Timing Diagram

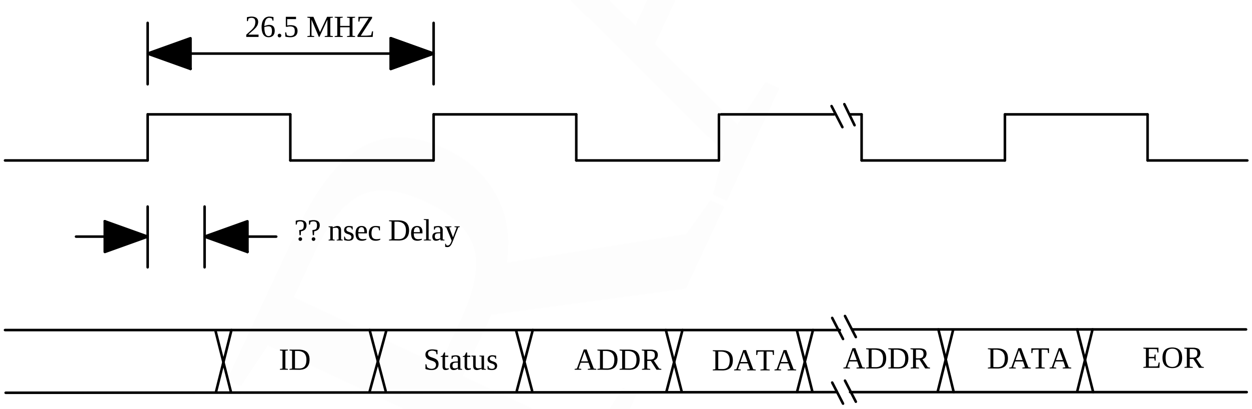

Figure A4.4: SVX Data Readout Timing Diagram

5.5 A5: TPCC State Transition Tables

STATE TABLE FOR INITIALIZE

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD	1	1	0	0	0											
MODE0	N	0	0	0	0											
MODE1	N	0	0	0	0											
BUS0	N	1	1	1	1											
BUS1	N	0	0	0	R											
BUS2	N	0	0	0	0											
BUS3	N	0	0	0	0											
BUS4	N	1	1	1	1											
BUS5	N	1	1	1	1											
BUS6	N	1	1	1	1											
BUS7	N	0	0	1	0											
BN/PO*					IN											
TN/PI*	N	N	D	D	D											

STATE TABLE FOR ACQUISITION

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD	1	1	0													
MODE0	N	1	1													
MODE1	N	0	0													
BUS0	N	0	0													
BUS1	N	1	1													
BUS2	N	1	1													
BUS3	N	1	1													
BUS4	N	1	1													
BUS5	N	1	1													
BUS6	N	1	1													
BUS7	N	0	0													
BN/PO*																
TN/PI*	N	T	T													

STATE TABLE FOR DIGITIZATION/READOUT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0
MODE0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
MODE1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
BUS0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	T	T
BUS1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	T	T
BUS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	T	T
BUS3	1	0	0	1	0	0	0	0	0	0	0	0	0	0	T	T
BUS4	1	1	1	1	1	1	1	1	1	1	0	0	0	0	T	T
BUS5	1	1	1	1	1	1	1	1	1	0	0	0	0	0	T	T
BUS6	1	1	0	0	0	0	0	0	0	0	0	0	0	0	T	T
BUS7	0	0	0	0	0	0	1	1	1	1	1	0	0	0	T	T
BN/PO*																
TN/PI*	T	T	T	T	T	T	T	T	T	T	T	T	T	T	0	0

STATE TABLE FOR PREAMPLIFIER RESET

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD																
MODE0																
MODE1																
BUS0	1	0														
BUS1																
BUS2																
BUS3																
BUS4																
BUS5																
BUS6																
BUS7																
BN/PO*																
TN/PI*																

STATE TABLE FOR CALIBRATION INJECT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD																
MODE0																
MODE1																
BUS0																
BUS1																
BUS2																
BUS3																
BUS4																
BUS5																
BUS6																
BUS7	1	0														
BN/PO*																
TN/PI*																

STATE TABLE FOR FPGA READBACK

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH-MD																
MODE0																
MODE1																
BUS0																
BUS1																
BUS2																
BUS3																
BUS4																
BUS5																
BUS6																
BUS7		R														
BN/PO*																
TN/PI*																

T = Tri-stated IN = INput D = Data out R = Readback data N = No change

5.6 A6: Termination Scheme for PECL Signals

This appendix provides the termination scheme used on the TPC for all the PECL signals.

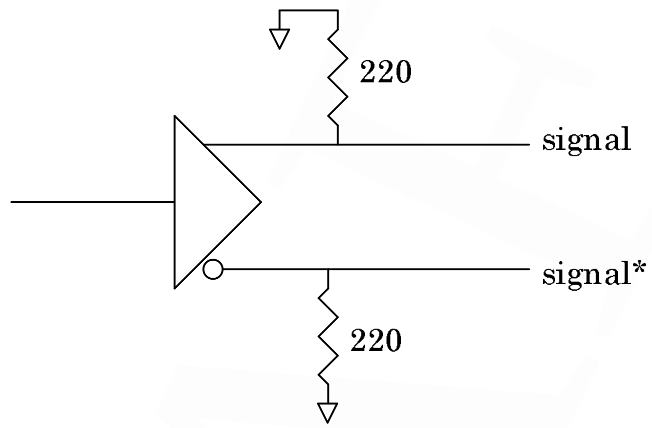

Figure A6.1: Termination Scheme for PECL signals driven by the TPC

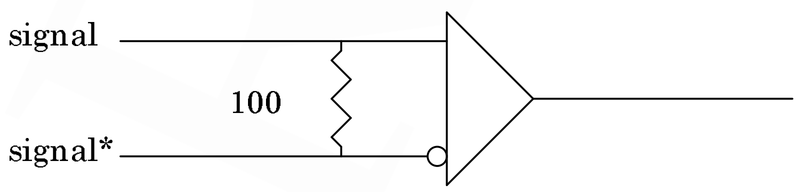

Figure A6.2: Termination Scheme for PECL Signals Received by TPC

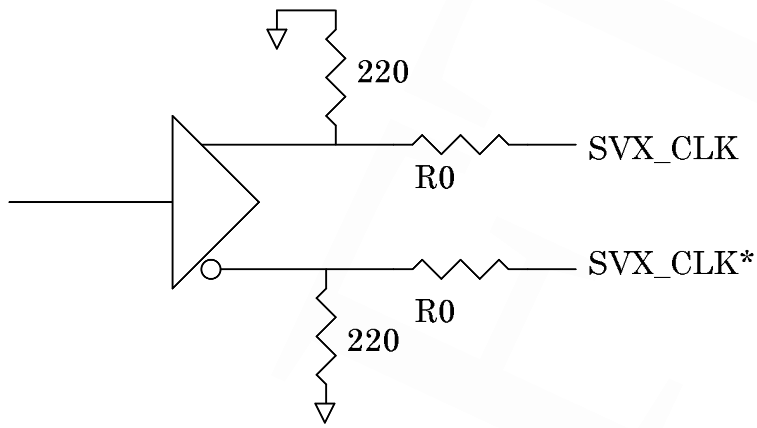

Figure A6.3: Termination Scheme for the PECL SVX Clock

6. References

[1] R. Yarema, el. al., "A Beginners Guide to SVX II", Fermilab document.

[2] S. Zimmerman, el. al., "Test Fiber Interface Board (TFIB)", " Fermilab document.

[3] J. Oliver, "Silicon Test Acquisition & Readout Module (STAR)".

[4] A. Cook, el. al., "Prototype Test Stand Crate Hardware", Fermilab document.

[5] Xilinx's Reference Guide III.