SVX4 Chip Specifications 5/30/01

A. General:

1. Input bonding pad pitch:	48μm
2. Overall Width:	6.250mm active area. Dicing streets as close as allowed by design rules.
3. Overall length:	< 11.925mm
4. Supply voltages:	2.25-2.75V analog, 2.25-2.75V digital.
5. Versions:	A version is the basic "conservative" version. B version adds on-chip bypassing and front to back combined power routing,
6. Bond pad layout:	Both version have same bond pad layout with some pads used only by CDF and others used only by D0.
7. Bond pads:	Except Front End inputs, no wirebond pad is to be smaller than 150x150um (cover layer opening). Probe pads not meant for wirebonding are exempt.
8. Maximum Supply Voltage:	3.5V

B. Preamp:

1. Input pulse polarity:	Positive
2. Gain (feedback capacitor):	3mV/fC
3. Gain uniformity (ch-to-ch):	5% or better
4. External load capacitance:	10pF to 50pF
5. Risetime 0-90%:	adjustable in a range that includes 60-100ns for any allowed load
6. Risetime adjustment:	4 bits minimum
7. Noise (ENC):	2000e or less for a 40pF load using double correlated sampling with 100ns integration t.
8. DC open loop gain:	>2500 (>95% charge collection from 40pF)
9. Linearity:	Linear response for pulses up to 20fC non-linearity < 0.25mV at output
10.Dynamic range:	>200fC
11.Reset + settling time:	<1μs for any initial condition
12.Reset offset voltage:	Internally set to a value TBD by designers, with external override capability.
13.Input protection diodes:	2uA DC capability to either rail. Current must not go to substrate.
14.Calibration injection:	40fF internal cap switched to input
15.Calibration charge control:	1 external analog reference voltage (other voltage is AVDD, not ground)
17. Input disable switch:	2 Config. Register bits. #1 disables control of reset switch for channel with calibration mask bit set. #2 determines whether reset switch is always closed or always open for disabled channels.
18.Input Device Current:	Adjustable with configuration bits as in SVX3 but with wider range (factor of 2).
19.Bypass capacitors:	Performance in SVX-II mode should be maintained with no external bypass capacitors closer than 10mm.

C. Pipeline:

1. Input Pulse polarity:	Negative
2. Voltage gain:	3 to 5
3. Gain uniformity:	5% channel to channel
4. Risetime, 0-90%:	10ns to 40ns (in that range, fixed)
5. Noise (ENC at preamp input)	<500e
6. Linearity:	linear response up to 20fC at preamp input
7. Dynamic Range:	To Be Confirmed: >40fC at preamp input
8. Reset Time:	<20ns for any allowed initial condition
9. Pedestal uniformity:	<500e at preamp input channel to channel <1000e at preamp input cell to cell
10. Bias:	Internally set with override bonding pad.

D. ADC:

1. Type:	Wilkinson with real time pedestal subtraction.
2. Voltage Ramp:	Rate adjustable with external resistor.
3. Ramp rate “trim” bits:	3 Bits, adding binary weighted capacitors to op-amp feedback. Largest capacitor is 4x the fixed feedback capacitor. These capacitors provide a range adjustment- no fine adjustment needed.
4. Ramp Linearity:	0.25% for rates between 0.1 and 1 V/us.
5. Ramp dynamic range:	1V
6. Ramp pedestal:	Same as in SVX3.
7. Counter:	8-bit Gray code, 106MHz rate.
8. Differential nonlinearity:	<0.5 LSB.
9. Bias:	Internally set with override bonding pad

E. Data output drivers:

1. Type:	Complementary with "resistor current sources"
2. Current source range:	2.5mA to 17.5mA in 2.5mA steps (3 bit adjust).
3. Rise and fall times:	>2ns and <4ns with nominal load.
4. Common mode:	VDD/2 nominal with T termination.
5: Load capability:	70ohm and 20pF.
7. Tri-state:	Outputs tristated in initialize (except if SR copy pad is bonded- see H7) and digitize modes.
8. Single ended use:	No additional requirements
9. Bi-directional:	All Bus pads will be bi-directional. Only some will be used of input as well as output by CDF, but all of them will be I/O for D0.
10. Output data skew:	>3ns between OBDV and any bus line and between any two bus lines.

F. TN/BN Pins:

1. Functions	The multiplexed functions of the SVX3 TN/BN pads will be separated in SVX4 to TN/BN and Priority in/out dedicated sets of pads.
2. Type, BN/TN:	"Open collector" I/O with internal pull-up.
3. Type, Priority in:	Differential receiver (2 bond pads) same as clock receivers, with added high Z common mode reference voltage (center tap of large resistance between power and ground).
4. Type, Priority out:	Differential driver (2 bond pads) same as

data bus outputs.

5. BN/TN Internal pull-up: >500 ohm
6. BN/TN Pull-down current: >10mA
7. BN/TN Modes: only active in digitize mode
8. Priority in/out Modes: Configuration register input/output during initialize mode. Priority passing during readout mode. Priority out high during digitize mode.
9. Bonding pads: This increases the number of bonding pads per chip by 4 (2 next to TN and 2 next to BN).

G. Configuration Register:

1. Type: Bit serial shift register.
2. Cell type: SEU tolerant shadow register.
3. Shadow register: Keep for SEU tolerance.
4. Clock: Register advanced with FE clock in initialize mode.
5. Length: no limit.
6. Preset: no preset.
7. layout rule: Do not place configuration register cells within 75um of a wirebond pad (they tend to be destroyed by missed wirebonds).
8. Bit order: LSB loads first on all fields.
9. Bit Assignment: Numbers are for illustration. Designers may add bias adjust or other system bits as needed.

0-127:	Calibration Mask
128:	Cal-inject signal polarity
129:	Input disable
130:	Disable mode (reset always on or off)
140-144:	Bandwidth bits (left room for 5)
145-147:	Input transistor current
148-153:	Pipeline depth
154:	Pipeline readout order
155-161:	Chip ID
162:	Real time pedestal subtraction Enable
163:	Last channel latch
164:	Channel 63 latch
165:	Read all
166:	Read Neighbors
167-170:	Ramp pedestal
171:	Ramp direction
172:	Comparator polarity
173-175:	Ramp range selection
176-183:	Sparsification threshold
184-191:	Counter Modulo
192:	First chip flag (see H.9)
193:	Last chip flag (see H.9)
192-194:	Output driver resistor select

H. Control Functions:

(*) Denotes desirable feature but not strictly required

1. Signal Functions: All control signals same function as SVX3 except as noted here.
2. Ramp and Counter Reset: Remove Counter Reset as an independent signal. In normal mode Counter Reset is to be tied to Ramp Reset. In Dynamic Pedestal Subtraction mode Counter Reset is internally generated as in SVX3.

3. Preamp Reset & Fe Clock: Preamp Reset should always function independently of FE Clock state. In SVX3 Preamp Reset can only go high while FE Clock is high.

4. PRD2 (*): It is desirable that PRD2 control only the acquisition of the reference capacitor pedestal, and that the action of returning a cell to the pipeline be automatically triggered by the end of digitization (The falling edge of DIGITIZE MODE is used to drive the MOVE DATA pipeline input)

5. Last channel SR bit: on=always latch chan. 127 (same "last chip flag" in SVX3).

6. Chan. 63 latch SR bit (*): on=always latch chan. 63 (doubles read out speed)

7. Bus 3 SR copy bond pad: copy Priority out in initialize mode to Bus 3 output if pad is bonded to ground (and enable output bus in init. mode)

8. extra L1A: Additional L1A pulses (beyond 4) should be ignored by the pipeline logic.

9. OBDV (data valid) control (*): OBDV must be driven by 1 chip per daisy chain at all times to prevent data transmission errors. This can be accomplished in SVX4 with 2 configuration register bits: First Chip (FC) and Last Chip (Different from item 5). OBDV control is given by the following logic table

Pri. In	Pri. Out	FC	LC	OBDV
H	H	L	L	disabled
H	L	L	L	disabled
L	H	L	L	ENABLED
L	L	L	L	disabled*
X	H	H	L	ENABLED
X	L	H	L	disabled*
H	X	L	H	disabled
L	X	L	H	ENABLED

*OBDV is to be disabled one BE_CLOCK cycle after Pri. Out is lowered (same as in SVX3). [In the present CDF silicon system it was necessary to add logic to the port cards to implement this function, because the SVX3 does not have the FC and LC bits.]

10. Readout Mode Pad: Add an output pad to make the "Readout Mode" internal signal available

11. D0 Mode pad: A special bond pad, if left un-bonded will set the chip in D0 mode. This will multiplex I/O signals onto all Bus lines and gate the Pipeline Clock off during digitize and readout operations.

12. Test outputs: Buffered preamp and pipeline outputs for one channel, Comparator output for 1 channel, Ramp probe point, RTPS comparator buffered input And output- all as in SVX3. Additional probe points as needed to fully test performance.