CALORIMETER ELECTRONICS FOR THE D0 UPGRADE

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ABSTRACT

The Calorimeter Electronics for the D0 Upgrade is described with particular emphasis on the front-end analog signal processing and analog storage. The proposed electronics design is driven by the timing and luminosity changes at the Fermilab Collider. The reduction of the time between beam crossings from 3.5usec to 396ns requires new electronics to integrate and shape the signal for sampling. We describe the changes in cabling, preamp electronics and shaping electronics to deal with this challenge. During the 2usec delay for a level 1 decision, the signals are held and buffered using a custom Switched Capacitor Array. SCA design and test results are presented. After buffering, the signal is digitized using the present ADC and data acquisition system.

1. Introduction

The Fermilab accelerator upgrade increases both the luminosity and frequency of $p\bar{p}$ collisions. There is a dramatic reduction in the time between crossings from 3.5 μsec to 396 nsec. D0 calorimetry will meet this challenge with the current calorimeter and new electronic instrumentation.

A brief description of the current calorimeter follows[1] . The calorimeter is a sampling calorimeter consisting of uranium and liquid Argon in three cryostats. The signals from the read-out boards are connected with 30 ohm coax to the inner side of the printed circuit feed-through boards which bring the signals out of the cryostat. A short run of twist and flat cable connects the outer side of the feed-through to charge integrating preamps. The output of the preamp is shaped by a RC differentiation of 33 μsec and RC integration of 250 ns on the BLS (baseline subtractor) boards. The baseline and peak are sampled, and held. The difference is taken and buffered. To achieve 15 bit dynamic range, low level signals are amplified by a factor of eight. The voltage levels are multiplexed to 12 bit 10V ADCs in the moveable counting house.

Retention of the calorimeter imposes several constraints. The ionization of the liquid Argon results in a current pulse which linearly ramps to zero from its initial value in 430ns. The capacitance load of the calorimeter cells range from 300 pF to 5 nF. The internal cable will remain 30 ohm coax. Thus, the signal emerging from detector will remain unchanged, imposing the full burden of the accelerator upgrades on the calorimeter electronics. How is this challenge met?

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* Representing the D0 collaboration.

2. Analog Front End: The Preamp

The location of the preamps, between the cryostat and muon magnet, is a region of limited space and, during the run, limited access. This mandates a reliable design and reliable production to achieve a high level of quality control. This was achieved in the current detector. Therefore, we only add minimally to the current design the straightforward conventional changes needed to meet our new time scale requirements.

The full signal path from the detector modules to the preamp will consist of equal lengths of 30 ohm cable (the last 10ft of twist & flat cable is replaced). The input impedance of the preamp will be 30 ohm instead of the current 45 ohm. Reflections are minimized.

The preamp itself remains a charge integrating preamp with a 5.5pF feedback capacitor. A second stage is added with a pole-zero cancellation and gain of three. This stage drives the 110 ohm twist & flat output cable through a 110 ohm back-termination resistor. The overall preamp gain is 0.27V/pC.

The reduction in shaping times (2usec to 400ns) increases the electronic noise ($\propto 1/\sqrt{t}$). We therefore double the number of JFETs (SK369V) in parallel to reduce noise by $\sqrt{2}$ resulting in a overall increase of 1.6. The uranium noise, currently dominates the electronic noise by a factor of two -- which will be reduced by a factor of 2.3 as this varies $\propto \sqrt{t}$. Pile-up studies show a noise increase of about 1.3. Thus, the overall noise performance at 10^{32} will be comparable, to the current noise at the luminosity of 10^{31}.

The detector's capacitance range from 300pF to 5.0nF, together with the 30 ohm cable, gives rise times that vary from 9ns to 150ns. The time constant in our Sallen-Key shaping circuit (to be discussed shortly) is 150ns. We therefore add a pole-zero compensation circuit to the preamp which cancels the RC integration pole created by the detector module and cable/input impedance (fig. 1). Different flavor preamps will be equipped with different compensation filters appropriate for the various detector cells. Tests with prototypes show preamp signal uniformity on the 2% level will be achieved instead of the 33% spread with no compensation.

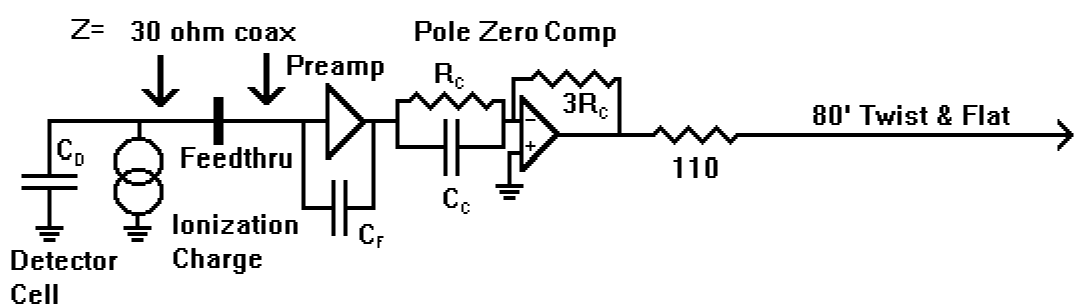

Fig. 1 Calorimeter Front-End Electronics

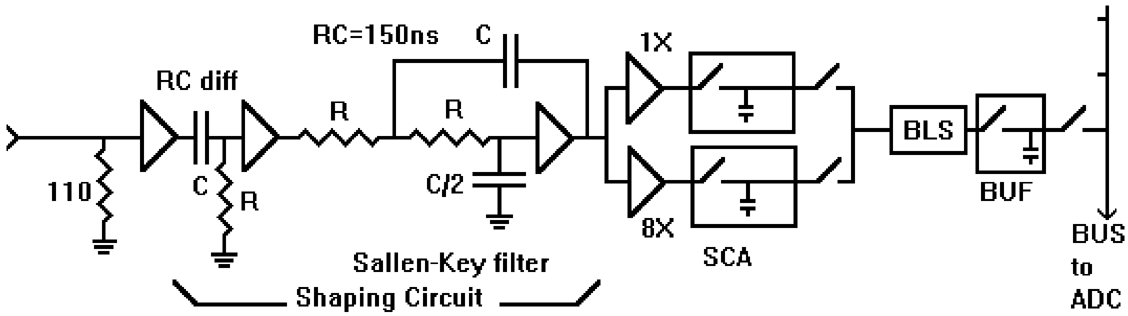

Fig. 2 Shaping Circuit, Sample and Hold SCA, Baseline Subtract, Buffer and Multiplex

3. Signal Shaping: The Sallen-Key Filter

The signal is shaped and peaks in 400ns. The shaping circuit consists of a RC differentiation followed by a Sallen-Key filter (see fig.2). This gives a unipolar signal. The unit step response of the shaping circuit is $4e^{-at}\sin^2(at/2)$. However, for the preamp integrated signal of our detector, the filter output is shown below (see fig. 3) for the input charge (3.7pC) that gives a preamp output of 1V. The time constant is 150ns. To achieve a 15bit dynamic range with a 12bit ADC, both 1X and 8X amplified signals are stored. These signals and the baseline are sampled and held by the switch capacitor array discussed below. For events that pass the level one trigger, the signal and base stored in the SCA are accessed. The baseline is then subtracted and the result buffered.

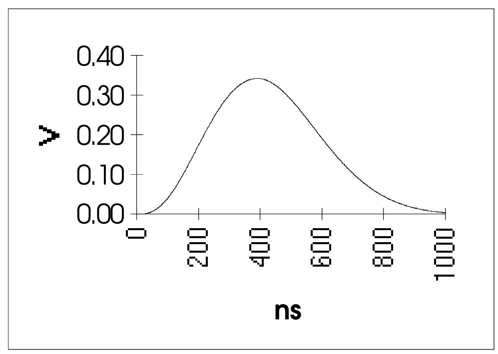

Fig. 3 Filter Output & SCA input

4. Analog Storage: The Switched Capacitor Array

The level one trigger requires two microseconds. During this time several events will be received and must be pipelined until a level one decision is made. The storage of these analog signals is achieved with a custom integrated circuit originally developed for use at the SSC by LBL[2]. The switched capacitor array (SCA) will have 12 channels with 48 memory cells per channel using 1.2 micron double-metal double-poly technology. Each sample and hold cell has CMOS gates and a polysilicon capacitor with independent access for dual port I/O. The symmetric switching reduces switching charge to first order. The cell can be randomly accessed in read and write modes. During the read mode, the charge in the cell is connected to the feedback of the output op-amp buffer.

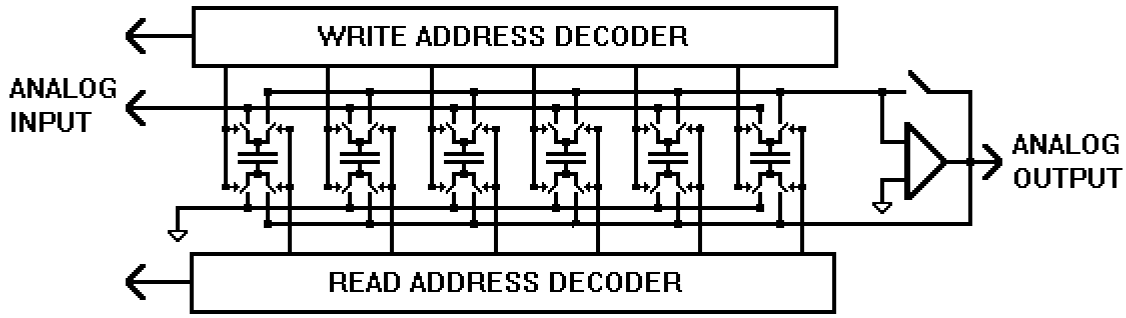

Fig. 4 Switch Capacitor Array (SCA) custom IC

To achieve 12 bit accuracy, cell to cell, noise and uniformity must be less than 1mV. This has been shown by tests performed on samples using 2 micron technology (Table 1). Cost is estimated at $24 per SCA.

The accelerator upgrade demands can be met by D0 calorimetery with new preamps, shaping, and SCA storage ICs. The changes can achieve the signal to noise and bandwidth requirements necessary for future runs.

Table 1 Switch Capacitor Array (SCA) custom IC measurements and specs

	2 micron measurements	1.2 micron specs
Noise	<0.26mV	<0.3mV
Uniformity	0.56mV p-p	0.15mV p-p
Linearity	<0.35%	<0.10%
Capacitor	~8.5pF	~15pF
RC time	7ns	~12ns
Cap droop rate	2uV/ms	< 100uV/ms
Crosstalk	0.1%	<0.5%
Voltage range	40mV to 4.8V	40mV to 4.8V
Max sample rate	8MHz for 12 bits	9MHz for 12 bits
Max readout rate	200kHz for 12 bits	500kHz for 12 bits
Op-Amp settling time	1.5us for 12 bits	1.0us for 12 bits
Number of channels	12	12
Cells per channel	48	48
Power per chan	<10mW	<10mW
Stability	20 ppm/day	25 ppm/day

References

1. R.D. Schamberger, *Nuclear Physics B* (Proc. Suppl.) **23A** (1991) p.191
2. S.A. Kleinfelder, M. Levi, O. Milgrome, *Nuclear Physics B (*Proc. Suppl.*)* **23A** (1991) p. 382.