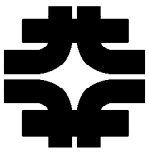


Fermi National Accelerator Laboratory

D-Zero Detector Central Fiber Tracker (CFT) Axial Project Readout Electronics

Central Tracker Trigger (CTT) Mixer System Diagnostic Procedures

Date: April 1st, 2002
Revision Date: March 18th, 2003

N. George Wilcer, S. Marco Rapisarda, M. Tomoto

Document # ESE-D0-020401

Table of contents

1. Introduction 5
2. Subrack Controller 6
Figure 2.1, Subrack controller simplified block diagram. 6
2.1 Use of board Controller 1553 Interface 7
2.1.1 Read Subrack Controller Status Word 7
Table 2.1, Read Subrack Controller status word. 7
Figure 2.2, Subrack Controller (DFEC) Status Word. 7
2.1.2 Read from Subrack Controller Memory 7
Table 2.2, Read from Subrack Controller memory. 7
2.1.3 Write to Subrack Controller Memory 8
Table 2.3, Write to Subrack Controller memory. 8
2.1.4 Writing and executing a sequence of Subrack Controller Commands 8
Table 2.4, Write and executing a sequence of Subrack Controller commands. 8
3. Diagnostic Procedure 9
3.1 Use of slow monitoring serial bus 9
Table 3.1, Slow Monitoring information read back procedure. 9
Figure 3.1, Mixer Board Slow Monitoring information 9
Table 3.2, Example of Board Status Block read back. 10
Figure 3.2, Slow Monitoring Diagnostic Procedure flow 11
4. Procedures 12
4.1 Board procedures 12
4.1.1 Read a board-controller register 12
Table 4.1, Read a Board Controller register 12
4.1.2 Write to a board-controller register 12
Table 4.2, Write to a Board Controller register 12
Figure 4.1, broadcast control for writes operations 13
4.1.3 Board devices access structure 13
Figure 4.2, Board device access structure 13
4.1.4 Read device registers 14
Figure 4.3, Read from device registers 15
4.1.5 Write to device registers 16
Figure 4.4, Write to device registers 18
4.1.6 Board reset 19
Table 4.5, Mixer board reset command sequence 19
Figure 4.5, Mixer board reset 19
4.1.7 Reset Board Controller History Information 19
Figure 4.6, Reset board controller history information 19
4.1.8 Read Mixer Board configuration status and device's firmware ID 20
Figure 4.7, Read configuration status and device's firmware ID 20
4.1.9 Erase Mixer Board Configuration 20
Figure 4.8, Erase mixer board configuration 20
4.1.10 Configure mixer board 21
Figure 4.9, configure mixer board 21
Table 4.6, Configuration Files denomination. 21
Table 4.7, Mixer# and Subrack slot#. 22
4.1.11 Read board controller firmware revision date and board serial number 22
Figure 4.10, Read board controller firmware revision date and board serial number 22
4.1.12 Read/Write test 23

Figure 4.11, Read/write test 23
4.1.13 Reset Board History Information 23
Figure 4.12, Reset Board History Information 23
4.1.14 Taking a snapshot of Mixer Board status 24
Figure 4.13, Mixer Board status snapshot 24
4.2 Input Links procedures 25
4.2.1 Read input links error status 25
Figure 4.14, Read input links error status 25
4.2.2 Read input links status 26
Figure 4.15, read input links status 26
4.2.3 Reset Mixer Board input links status history 27
Figure 4.16, Reset input links status history 27
4.2.4 Input Links Control 28
Figure 4.17, Input Links control procedure. 28
Figure 4.18, Input Links Control register 28
4.2.5 Input Links Control bits masking 29
Figure 4.19, Input Link Control Bits Mask Register 29
Figure 4.20, Command bits generation, timing and denomination. 29
Table 4.8, Example of command sequence to mask control bits on the input links. 30
Figure 4.21, input links control bits masking 31
4.2.6 Monitoring mode 7 masking 32
Figure 4.22, monitoring mode 7 masking 32
4.2.7 Input Links Control bits status 33
Figure 4.23, read input links control bits status 33
4.2.8 Embedded Command Bits Status 34
Figure 4.24, Read Embedded Command Bits status. 34
4.3 Backplane Devices Procedures 35
4.3.1 Reset Backplane Devices History 35
Figure 4.25, reset backplane devices history. 35
4.3.2 Readback Mixer Board clock/SYNC status 36
Figure 4.26, Read Clock/SYNC Status and History. 36
4.3.3 Reset Mixer Board clock/SYNC status history 36
4.4 Output links devices procedures 37
4.4.1 Output link FIFO read 37
Figure 4.27, Read content of an output link FIFO. 37
4.4.2 Output link FIFO Write 38
Figure 4.28, Write content of an output link FIFO. 38
4.4.3 Output Link FIFO reset 38
4.4.4 Output link FIFO Configuration 39
Figure 4.29, Output link FIFO configuration 39
4.4.5 Triggering of Output Links FIFO 40
Figure 4.30, Triggering of Output Link FIFO. 40
4.4.6 Use of Output Links FIFOs 40
Figure 4.31, Use of Output Links FIFOs. 40
4.4.7 Reset Output Links History Information 41
Figure 4.32, Reset output links history information 41
4.4.8 Output links Control Bits Masking 42
Table 4.9, Example of command sequence to mask control bits on the output links. 42
Figure 4.33, Output links control bits masking 43
4.4.9 Output Links Control 44
Figure 4.34, Output links control 44

4.5 System procedures 45
4.5.1 Mixer System reset 45
Figure 4.35, Mixer System reset 45
4.5.2 Mixer System Extended Reset 46
Figure 4.36, Mixer System extended reset 46
4.5.3 Mixer System power-up initialization 47
Figure 4.37, Mixer System Power-up initialization 47
4.5.4 Mixer System configuration erasing 47
Figure 4.38, Mixer System configuration erasing. 47
4.5.5 Broadcast configuration of the mixer system 48
Figure 4.39, broadcast configuration of the mixer system 48
5. Use of the LEDs Monitoring Mode 49
Figure 5.1, Front panel LEDs and LEDs monitoring mode 49
Figure 5.2, Mode of Operation register 49
Figure 5.3, Monitoring Mode Register 50
Figure 5.4, Monitoring Status Registers 50
Figure 5.5, Monitoring Status History Registers 50
Table 5.1, Monitoring Mode change 51
Figure 5.6, Monitoring Mode change 51
Figure 5.7, Enable/Disable LEDs to show monitoring mode 51
Figure 5.8, Read monitoring status and status history 52
6. Problem reporting 53
6.1 Report a problem to mixer system support 53
6.2 Report a problem to AFE system support 53
7. References 54

1. Introduction

This document describes the use of the diagnostic features and provides the recommended procedures to operate the mixer system.

More information on the D0 CTT Mixer System is provided in a separate document [Ref.4d].

2. Subrack Controller

Details provided in separate document [Ref. 4d].

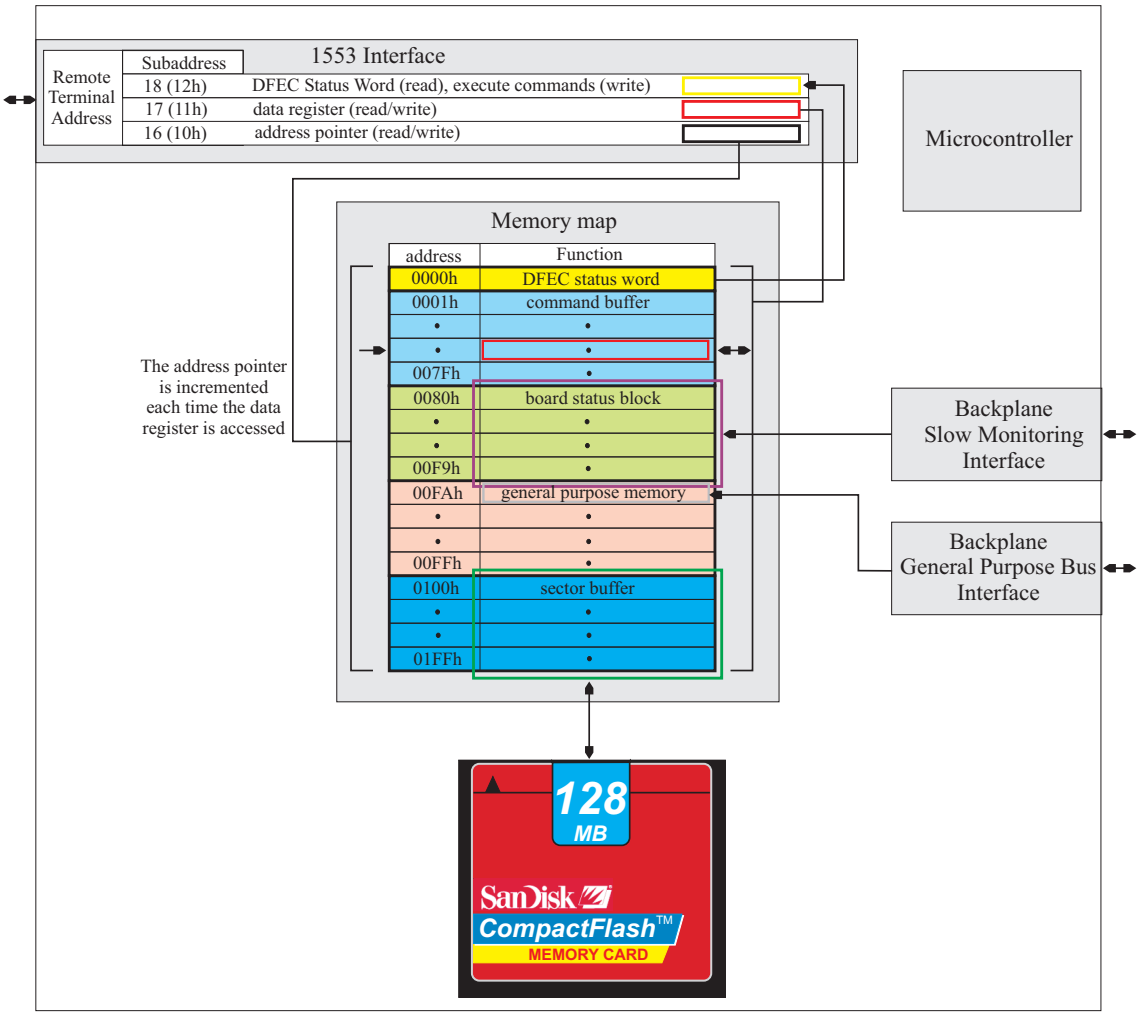


Figure 2.1, Subrack controller simplified block diagram.

2.1 Use of board Controller 1553 Interface

2.1.1 Read Subrack Controller Status Word

Table 2.1 provides the command sequence to read the Subrack Controller (DFEC) status word. The status word contains the information on the current status of the subrack controller (BUSY, HALT, IDLE) and the type of error in the case an error occurred in executing the last command.

Command to 1553 Remote Terminal	1553 Remote Terminal subaddress	Number of words	Notes
Read	18 (0x12)	1	Readback Subrack Controller Status Word.

Table 2.1, Read Subrack Controller status word.

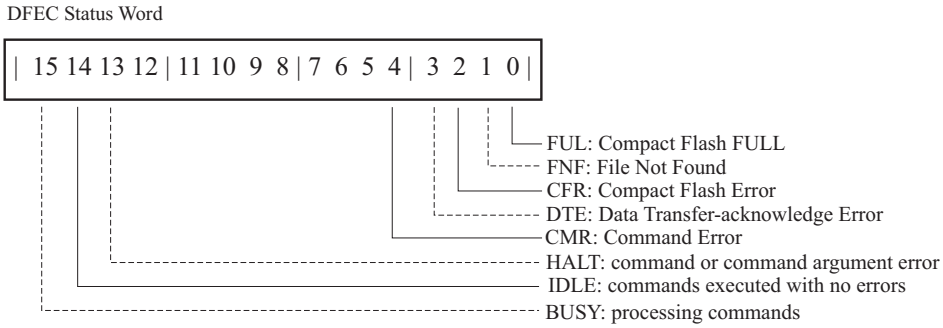


Figure 2.2, Subrack Controller (DFEC) Status Word.

2.1.2 Read from Subrack Controller Memory

Command to 1553 Remote Terminal	1553 Remote Terminal subaddress	Number of words	Notes
Write	16 (0x10)	1	Write the memory address in the subrack controller address pointer register.
Read	17 (0x11)	n	Read the subrack controller data register. The content of the address pointer register is automatically incremented each time the data register is accessed.

Table 2.2, Read from Subrack Controller memory.

2.1.3 Write to Subrack Controller Memory

Command to 1553 Remote Terminal	1553 Remote Terminal subaddress	Number of words	Notes
Write	16 (0x10)	1	Write the memory address in the subrack controller address pointer register.
Write	17 (0x11)	n	Write to the subrack controller data register. The content of the address pointer register is automatically incremented each time the data register is accessed.

Table 2.3, Write to Subrack Controller memory.

2.1.4 Writing and executing a sequence of Subrack Controller Commands

Command to 1553 Remote Terminal	1553 Remote Terminal subaddress	Number of words	Data	Notes
Write	16 (0x10)	1	0x0080	Write the address of the top location of the command buffer in the address pointer register.
Write	17 (0x11)	n	<command 1> <…> <command m>	Write to the subrack controller data register. The data will be written in the command buffer starting from location 0x0080.
Write	17 (0x11)	1	0xA1	Write to the subrack controller data register. 0xA1 is the "End of List" command and must always be placed at the end of a command sequence to stop the subrack controller from fetching and executing commands.
Write	16 (0x10)	1	0x0080	Optional step (command sequence verification) Write the address of the top location of the command buffer in the address pointer register.
Read	17 (0x11)	n	…	Optional step (command sequence verification) Verify that the read back sequence matches the sequence of commands <command 1> … <command m>.
Write	18 (0x12)	1	0x00	Write to subaddress 18 (0x12) to have the Subrack Controller to execute the command sequence stored in the command buffer.
Read	18 (0x12)	1	<status word>	Read back Subrack Controller status word. Verify the Subrack Controller status is IDLE or BUSY. Continue read back until the state is IDLE to confirm the execution of the entire sequence of commands without errors.

Table 2.4, Write and executing a sequence of Subrack Controller commands.

3. Diagnostic Procedure

3.1 Use of slow monitoring serial bus

Detailed information on the mixer system subrack controller is provided in [Ref.1f].

The mixer board status information is continuously collected from the mixer boards by the Mixer System subrack controller over a custom serial bus. The information is stored in the subrack controller memory space and is made accessible through the MIL-STD-1553 Remote Terminal interface. The mixer board status information read back from each mixer board is shown in Figure 3.1.

Table 3.1 provides the command sequence to read back the slow monitoring board status information from the Mixer System subrack controller memory.

Figure 3.1 shows the information provided in the Mixer Board slow monitoring word, detailed description of the word is provided in a separate document [Ref.4d].

Command to 1553 Remote Terminal	1553 Remote Terminal subaddress	Number of words	Notes
Write 0x0080	16 (0x16)	1	Point the address pointer to the top of the Board Status Block memory space (0x0080-0x00F9)
Read	17 (0x11)	20	Read back Board Status Block Memory. The first word provide the status information of the mixer board in slot# 2, the 20th word of the mixer board in slot# 21.

Table 3.1, Slow Monitoring information read back procedure.

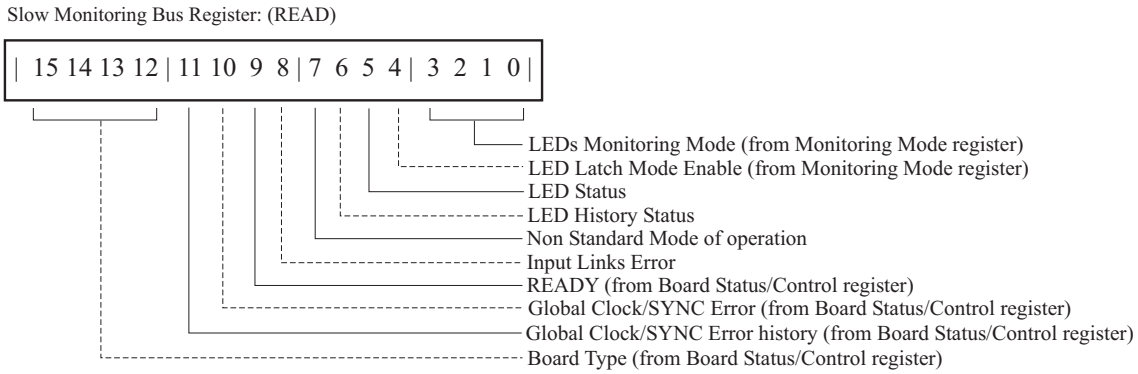


Figure 3.1, Mixer Board Slow Monitoring information

Subrack Controller Memory Address (Board Status Block)	Mixer Subrack Slot#	Read back data	Notes
0x0080	2	0x**D**22C b**1101**_0010_0010_1100	The board type is 0xD (mixer board).
0x0081	3	0xD**2**2C b1101_00**1**0_0010_1100	The board is fully configured (all 16 devices).
0x0082	4	0xD2**2**C b1101_0010_00**1**0_1100	All the bit in the LED Status Register are high (the logic AND is '1')
0x0083	5	0xD22**C** b1101_0010_0010_**1100**	The board is in LED monitoring mode 12 (0xC, default at power up).
0x0084	6	0x**F**FFF b**1111**_1111_1111_1111	The board type is not correct (should always be 0xD => the board is not responding correctly or is missing.
0x0085	7	0xD**E**2C b1101_1**1**10_0010_1100	The board has a Global Clock/SYNC error => the board is not using the correct source for the global Clock/SYNC or the SYNC used doesn't respect the correct protocol.
0x0086	8	0xD**F**2C b1101_1111_0010_1100	Beside having a Global Clock/SYNC error as the board in slot #7 this board has also an input link error => at least one of the 16 input links has a clock/sync error.
0x0087	9	0xD**E60** b1101_**1110**_0**11**0_**0000**	The board has a Global Clock/SYNC error, is in LED monitoring mode 0 (input links clock and DLL status), the bits in the LED Status registers are all high but there is a change in LED status reported in the LED Error Status History registers. No input link error is reported.
0x0088	10	0xD**9**CC b1101_100**1**_1100_1100	The board is not fully configured (READY bit is low).
…	…	…	…
0x0093	21	0xD b1101_0000_0000_0000	

Table 3.2, Example of Board Status Block read back.

Figure 3.2 shows the suggested diagnostic procedure flow. The flow is based on the information collected from the slow monitoring system; this data is used to define two levels of error (critical and severe) and one level of warning (alert). The flow diagram reports for each error and alert an ordered list containing, in order of precedence, the possible procedures to be used to investigate the problem. The procedures marked with an (+) are specified in this document.
A critical error is defined as one that affects the system in disrupting both the data flow and the system diagnostic. A severe error is one that just disrupts the data flow and makes the data unreliable. Alerts are used to warn about the board being accessed, being operated in a mode which can impair the data flow and when errors are reported form the input links diagnostic.

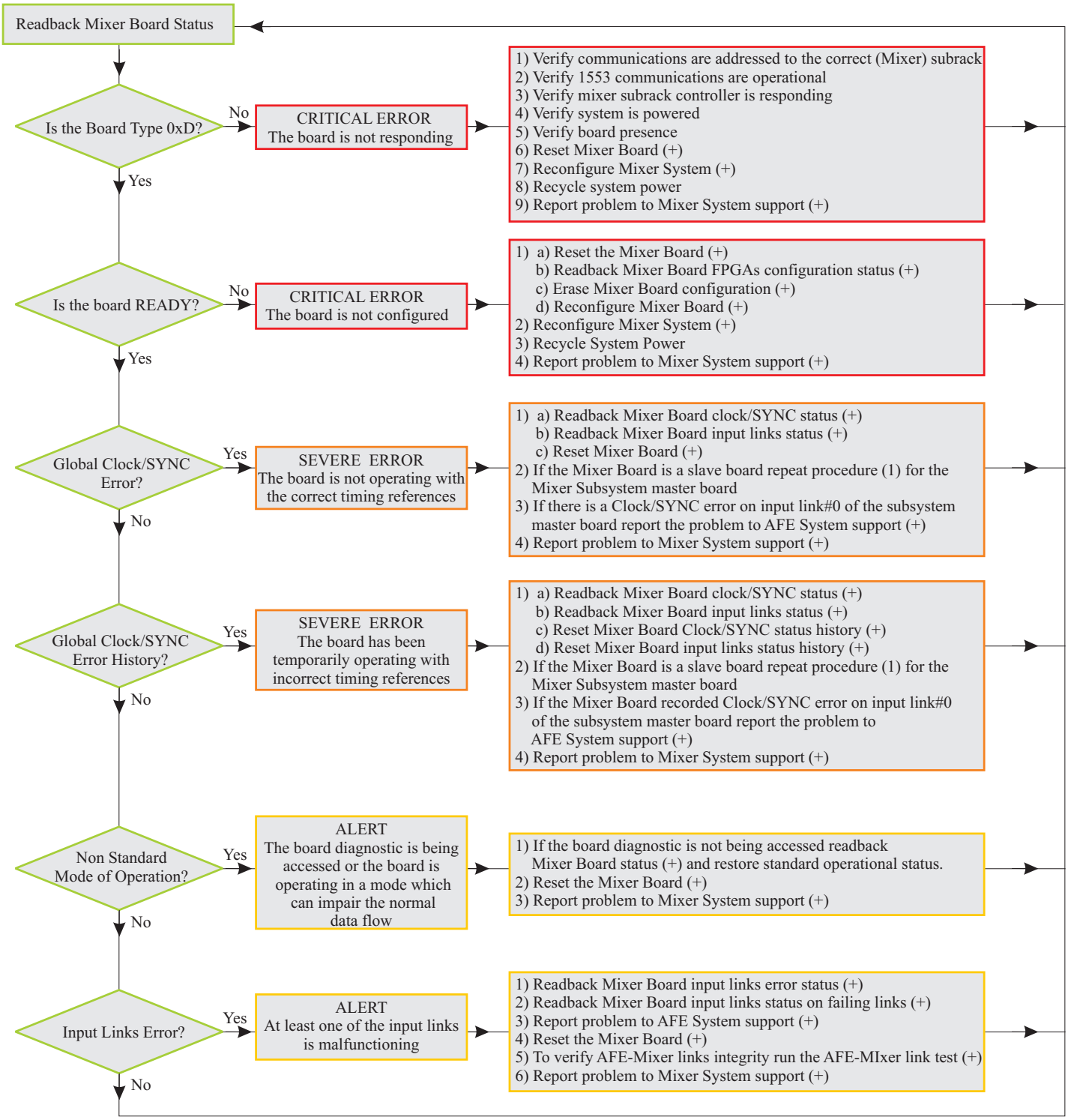


Figure 3.2, Slow Monitoring Diagnostic Procedure flow

4. Procedures

4.1 Board procedures

4.1.1 Read a board-controller register

Subrack Controller command (0x)	Notes
<22><00><offset><slot>	Read the content of the board controller register having address <offset> on the mixer board in slot <slot>. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <offset>: board register address, from 0x00 to 0x1F. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte will be available in the subrack controller General Purpose Memory at location 0x00FA.

Table 4.1, Read a Board Controller register

4.1.2 Write to a board-controller register

Subrack Controller command (0x)	Notes
<12><data><offset><slot>	Write the byte <data> to the board controller register having address <offset> on the mixer board in slot <slot>. <12>: subrack controller command "write byte to backplane". <data>: data byte to be written. <offset>: board register address, normal addressing range from 0x00 to 0x1F. The most significative three bit of the <offset> byte are using for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

Table 4.2, Write to a Board Controller register

The write operation can also be targeted to a particular set of mixer boards using the broadcasting control (see Figure 4.1).

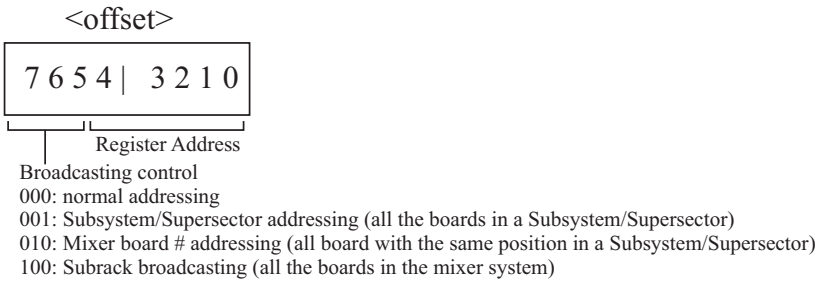


Figure 4.1, broadcast control for writes operations

4.1.3 Board devices access structure

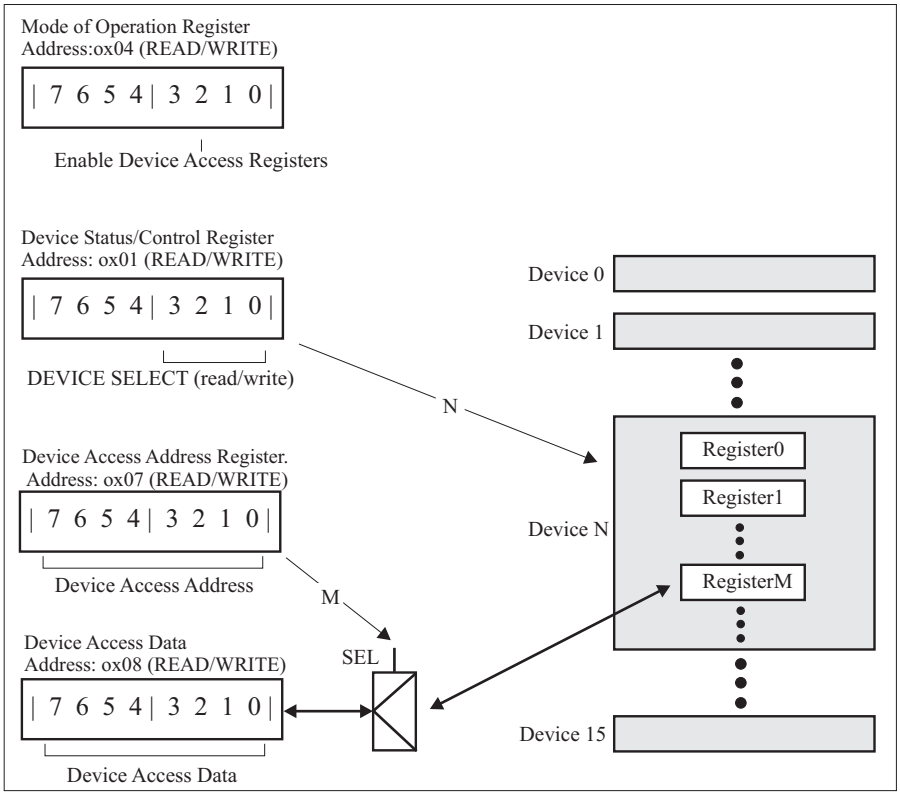


Figure 4.2, Board device access structure

4.1.4 Read device registers

Step#	Subrack Controller command (0x)	Notes
1	<22><00><04><slot>	Read the content of the Mode of Operation register. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <04>: <offset> byte, Mode of Operation register address. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte <MOreg_data> will be available in the subrack controller General Purpose Memory at location 0x00FA.
2	<12><data_a><04><slot>	Enable Device Access Registers (default is disabled) in the Mode of Operation register. <12>: subrack controller command "write byte to backplane". <data_a>: <MOreg_data> OR <04>. Is the logic OR of the byte obtained from the previous operation (<MOreg_data>) and the mask used to enable the Device Access Registers (<04>). <04>: <offset> byte, Mode of Operation register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
3	<12><0x0,device><01><slot>	Point the Device Status/Control Register to a specific device. No masking is required. <12>: subrack controller command "write byte to backplane". <0x0,device>: 0x0 followed by 4 bit device address, from 0x00 to 0x0F. <01>: <offset> byte, Device Status/Control register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
4	<12><register><07><slot>	Point the Device Access Address Register to a specific register inside the device. No masking is required. <12>: subrack controller command "write byte to backplane". <register>: Device's internal register address. <07>: <offset> byte, Device Access Address register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

5	<22><00><08><slot>	Read the content of the Device Access Data register. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <08>: <offset> byte, Device Access Data address. If broadcasting control was used in the preceding writing operations this step should be repeated for each of the boards belonging the subset of boards accessed by the broadcasting. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte <devreg_data> will be available in the subrack controller General Purpose Memory at location 0x00FA.
7	<12><data_c><04><slot>	Disable Device Access Registers in the Mode of Operation register. <12>: subrack controller command "write byte to backplane". <data_c>: <MOreg_data> AND <bxxxxx0xx>. Is the masking of the byte obtained from step#1 (<MOreg_data>) and the mask used to disable the Device Access registers (<bxxxxx0xx>). <04>: <offset> byte, Mode of Operation register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

Table 4.3, Read from device registers

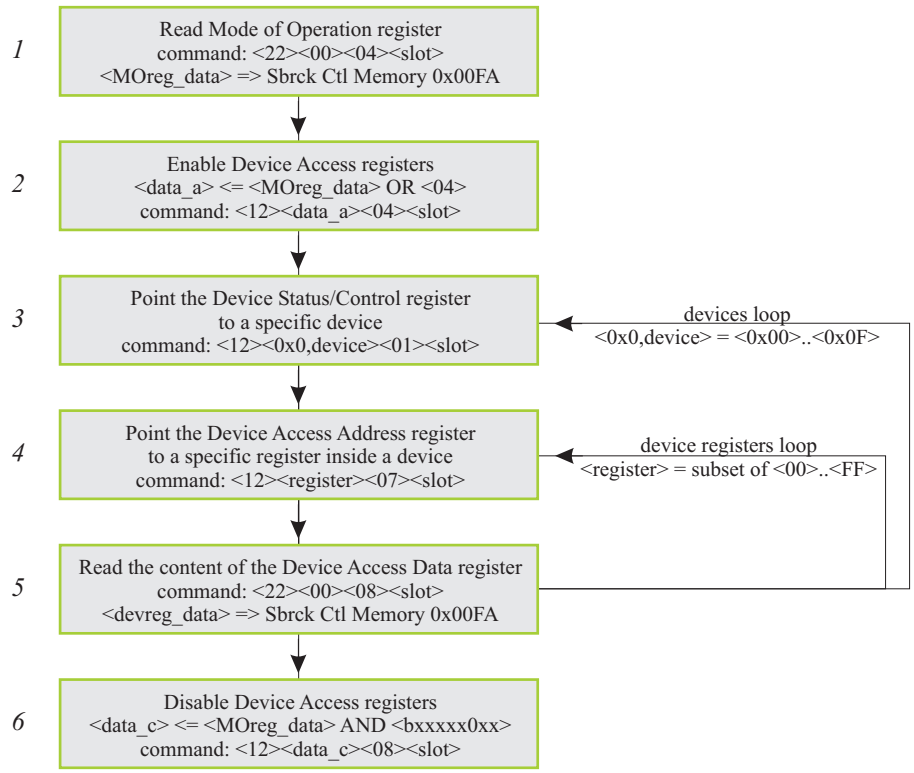


Figure 4.3, Read from device registers

4.1.5 Write to device registers

The write operation follows all the steps of the read operation. The difference is that the result of the read is OR-ed with the desired mask and then used in one more step to write back the desired content to the device register.

Step#	Subrack Controller command (0x)	Notes
1	<22><00><04><slot>	Read the content of the Mode of Operation register. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <04>: <offset> byte, Mode of Operation register address. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte <rdbk_dataA> will be available in the subrack controller General Purpose Memory at location 0x00FA.
2	<12><data_a><04><slot>	Enable Device Access Registers (default is disabled) in the Mode of Operation register. <12>: subrack controller command "write byte to backplane". <data_a>: <rdbk_dataA> OR <04>. Is the logic OR of the byte obtained from the previous step (<rdbk_dataA>) and the mask used to enable the Device Access registers (<04>). <04>: <offset> byte, Mode of Operation register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
3	<12><0x0,device><01><slot>	Point the Device Status/Control Register to a specific device. No masking is required. <12>: subrack controller command "write byte to backplane". <0x0,device>: 0x0 followed by 4 bit device address, from 0x00 to 0x0F. <01>: <offset> byte, Device Status/Control register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
4	<12><register><07><slot>	Point the Device Access Address Register to a specific register inside the device. No masking is required. <12>: subrack controller command "write byte to backplane". <register>: Device's internal register address. <07>: <offset> byte, Device Access Address register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

5	<22><00><08><slot>	Read the content of the Device Access Data register. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <08>: <offset> byte, Device Access Data address. If broadcasting control was used in the preceding writing operations this step should be repeated for each of the boards belonging the subset of boards accessed by the broadcasting. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte < devreg_data > will be available in the subrack controller General Purpose Memory at location 0x00FA.
6	<12><data_b><08><slot>	Write to the Device Access Data register. <12>: subrack controller command "write byte to backplane". <data_b>: <devreg_data_new>. devreg_data_new is the byte obtained from the previous operation (<devreg_data>) after having applied the desired changes. <08>: <offset> byte, Device Access Data register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
7	<12><data_c><04><slot>	Disable Device Access Registers in the Mode of Operation register. <12>: subrack controller command "write byte to backplane". <data_c>: <rdbk_dataA> AND <bxxxxx0xx>. Is the masking of the byte obtained from step#1 (<rdbk_dataA>) and the mask used to disable the Device Access registers (<bxxxxx0xx>). <04>: <offset> byte, Mode of Operation register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

Table 4.4, Write to device registers

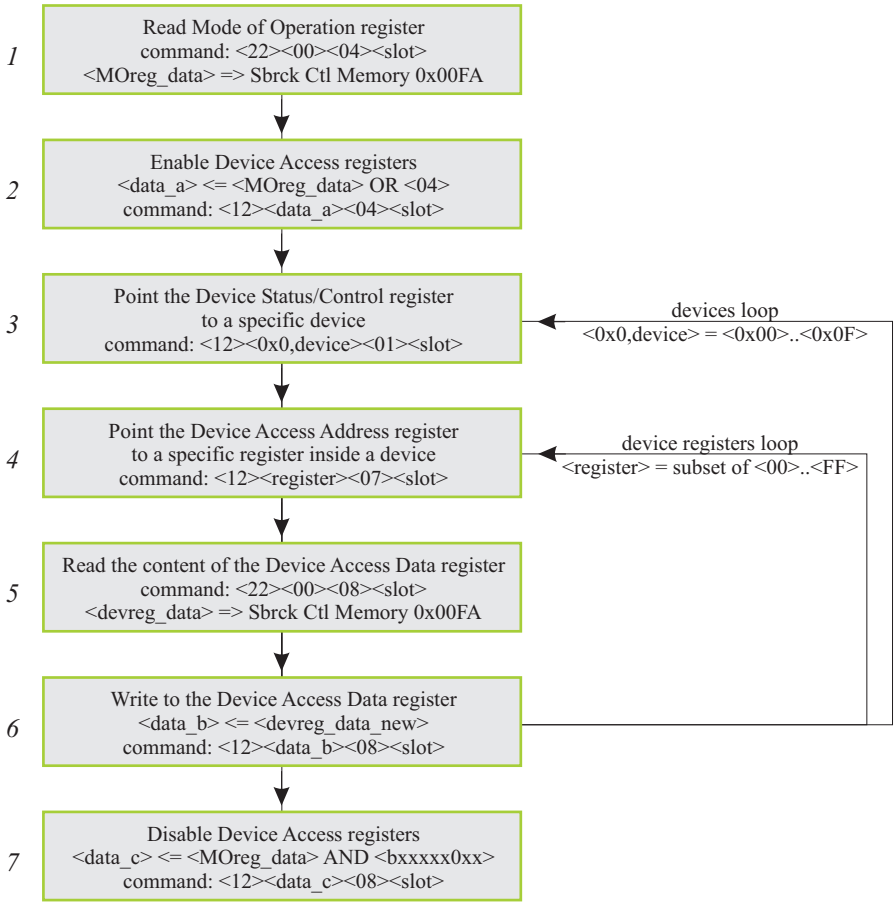


Figure 4.4, Write to device registers

4.1.6 Board reset

This procedure will reset to the default value/state all the registers and state machines on the mixer board. Due to the fact that some state machines may take several clock cycles to go to normal operation not all the history information after a board reset is reliable. After a reset it is suggested to reset history information (procedure described in paragraph 4.1.13). When a master board is reset the operation should be followed by the reset of all the slave boards in the same supersector. Paragraph 4.5 describe the procedure to reset the mixer system.

Step#	Subrack Controller command (0x)	Notes
1	<12><02><00><slot>	<12>: subrack controller command "write byte to backplane". <02>: <data> byte, set high the reset bit in the board status/control register. <00>: <offset> byte, board status/control register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
2	<12><00><00><slot>	<12>: subrack controller command "write byte to backplane". <00>: <data> byte, set low the reset bit in the board status/control register. <00>: <offset> byte, board status/control register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

Table 4.5, Mixer board reset command sequence

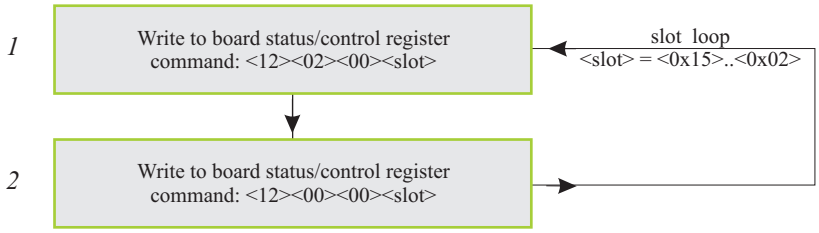


Figure 4.5, Mixer board reset

4.1.7 Reset Board Controller History Information

This procedure will reset the history information on the board controller FPGA.

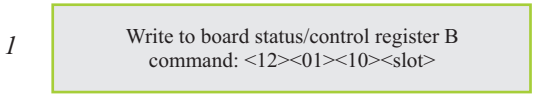


Figure 4.6, Reset board controller history information

4.1.8 Read Mixer Board configuration status and device's firmware ID

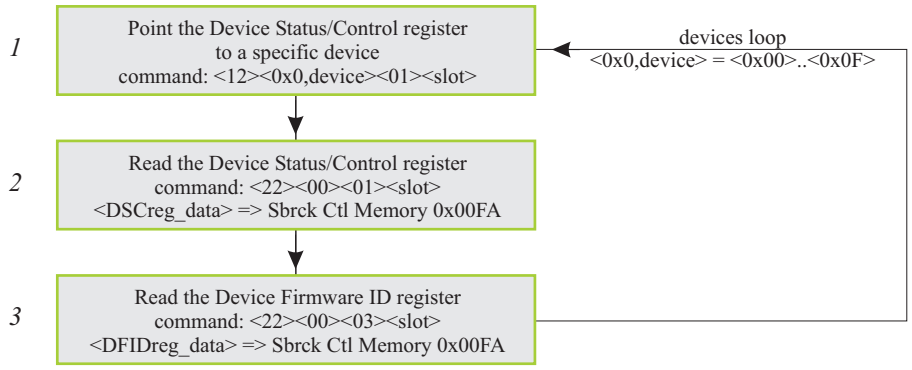


Figure 4.7, Read configuration status and device's firmware ID

4.1.9 Erase Mixer Board Configuration

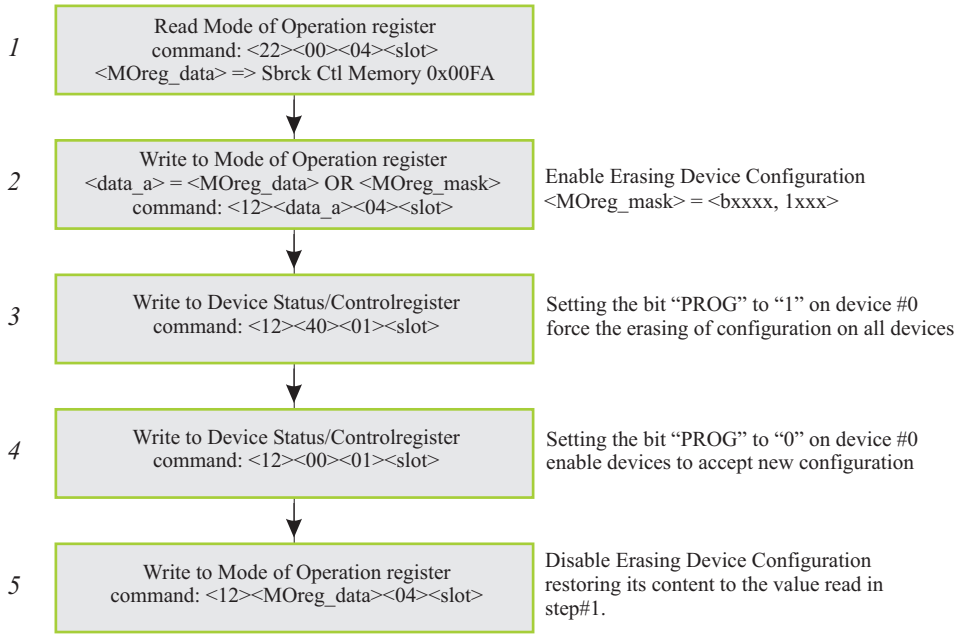


Figure 4.8, Erase mixer board configuration

4.1.10 Configure mixer board

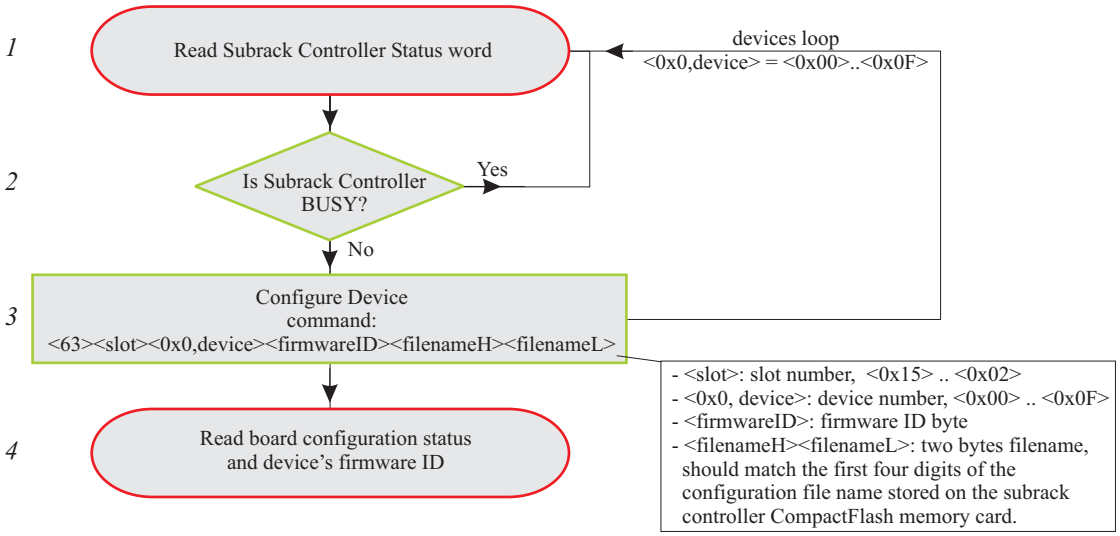


Figure 4.9, configure mixer board

Step 1 is described in paragraph 2.1.1. Step 4 is described in paragraph 4.1.8.

Device #	Device Type	Schematic device#, device name	Mixer#1 files	Mixer#2 files	Mixer#3 files	Mixer#4 files
0	Spartan XL	U2, DFE1 YP (Outlink 5).	0200_PC.bin	0300_PC.bin	0400_PC.bin	0500_PC.bin
1	Spartan XL	U1, DFE1 RB (Outlink 6).	0201_PC.bin	0301_PC.bin	0401_PC.bin	0501_PC.bin
2	Spartan XL	U10, DFE1 OG (Outlink 4).	0202_PC.bin	0302_PC.bin	0402_PC.bin	0502_PC.bin
3	Spartan XL	U11, DFE0 RB (Outlink 3).	0203_PC.bin	0303_PC.bin	0403_PC.bin	0503_PC.bin
4	Spartan XL	U19, DFE0 OG (Outlink 1).	0204_PC.bin	0304_PC.bin	0404_PC.bin	0504_PC.bin
5	Spartan XL	U18, DFE0 YP (Outlink 2).	0205_PC.bin	0305_PC.bin	0405_PC.bin	0505_PC.bin
6	Virtex	U31, LINK_IN 13-15.	0206_PC.bin	0306_PC.bin	0406_PC.bin	0506_PC.bin
7	Virtex	U45, LINK_IN 4-6.	0207_PC.bin	0307_PC.bin	0407_PC.bin	0507_PC.bin
8	Virtex	U46, LINK_IN 1-3.	0208_PC.bin	0308_PC.bin	0408_PC.bin	0508_PC.bin
9	Virtex	U32, LINK_IN 10-12.	0209_PC.bin	0309_PC.bin	0409_PC.bin	0509_PC.bin
10	Virtex	U47, LINK_IN 0.	020A_PC.bin	030A_PC.bin	040A_PC.bin	050A_PC.bin
11	Virtex	U48, Backplane Left Driver.	020B_PC.bin	030B_PC.bin	040B_PC.bin	050B_PC.bin
12	Virtex	U33, LINK_IN 7-9.	020C_PC.bin	030C_PC.bin	040C_PC.bin	050C_PC.bin
13	Virtex	U12, Backplane DFE0 receiver.	020D_PC.bin	030D_PC.bin	040D_PC.bin	050D_PC.bin
14	Virtex	U5, Backplane DFE1 receiver.	020E_PC.bin	030E_PC.bin	040E_PC.bin	050E_PC.bin
15	Virtex	U6, Backplane Right Driver.	020F_PC.bin	030F_PC.bin	040F_PC.bin	050F_PC.bin

Table 4.6, Configuration Files denomination.

Mixer#	Subrack slots
1	**02**, 06, 10, 14, 18
2	**03**, 07, 11, 15, 19
3	**04**, 08, 12, 16, 20
4	**05**, 09, 13, 17, 21

Table 4.7, Mixer# and Subrack slot#.

4.1.11 Read board controller firmware revision date and board serial number

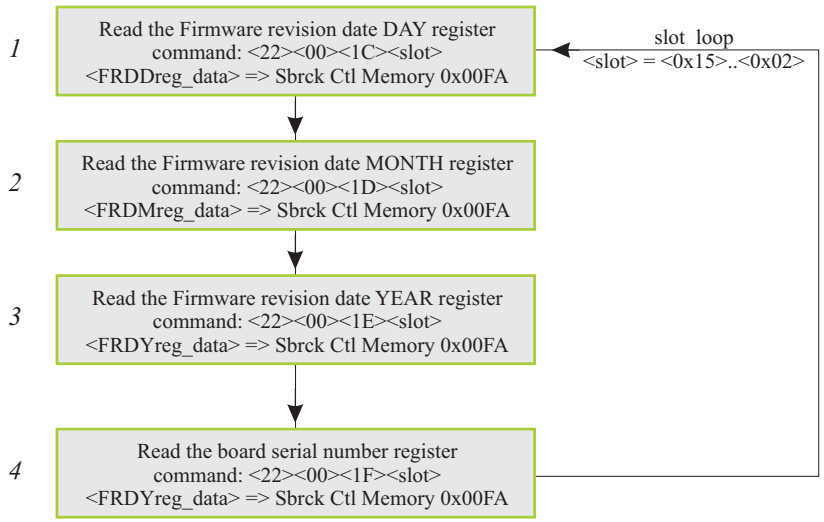


Figure 4.10, Read board controller firmware revision date and board serial number

4.1.12 Read/Write test

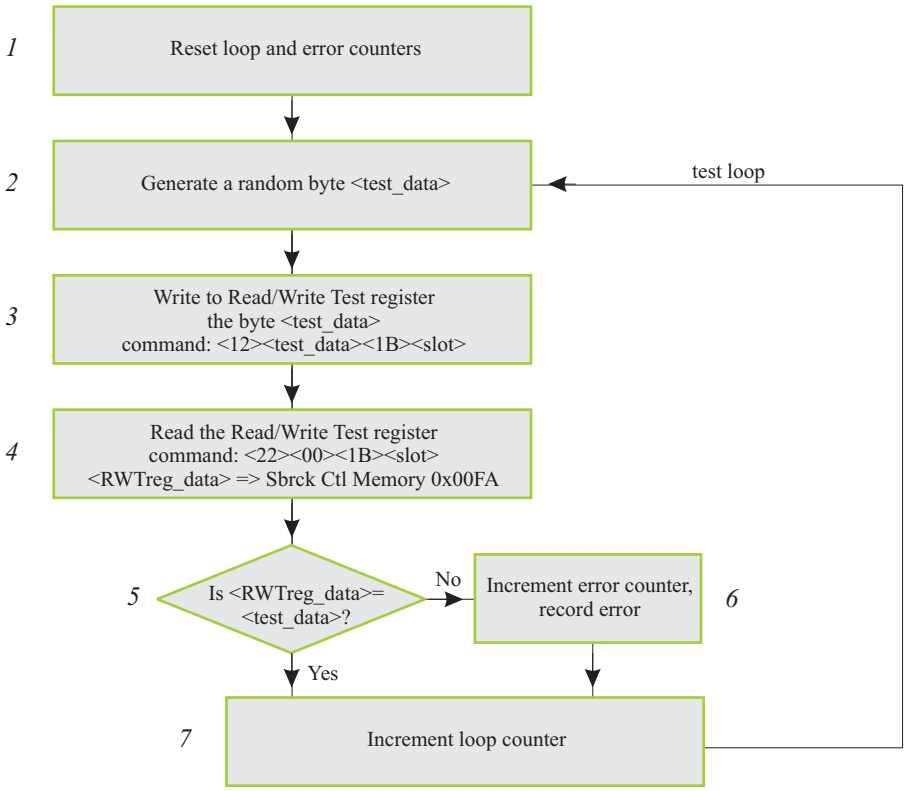


Figure 4.11, Read/write test

4.1.13 Reset Board History Information

The reset of the history information on a mixer board follow few steps to operate on the several devices on the board. The procedure can be generalized to the mixer system or to a subset of it using broadcasting of the commands.

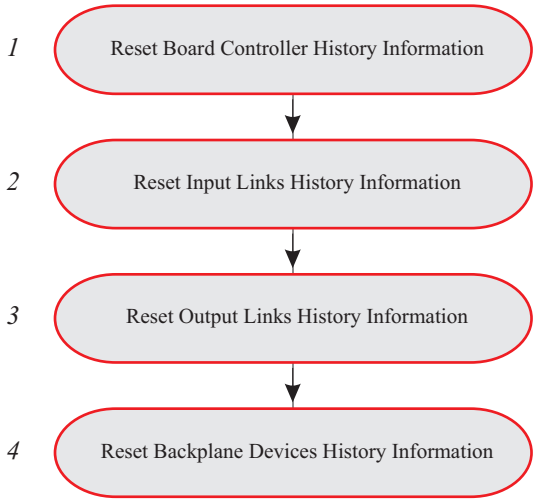


Figure 4.12, Reset Board History Information

Step 1 is described in paragraph 4.1.7. Step 2 is described in paragraph 4.2.3.
Step 3 is described in paragraph 4.4.7. Step 4 is described in paragraph 4.3.1.

4.1.14 Taking a snapshot of Mixer Board status

Taking a snapshot of mixer board status consists in reading all the board controller registers and all of the device registers. This can be done using the procedures described previously in Paragraphs 4.1.1 (for step 1 in Figure 4.13) and 4.1.4 .

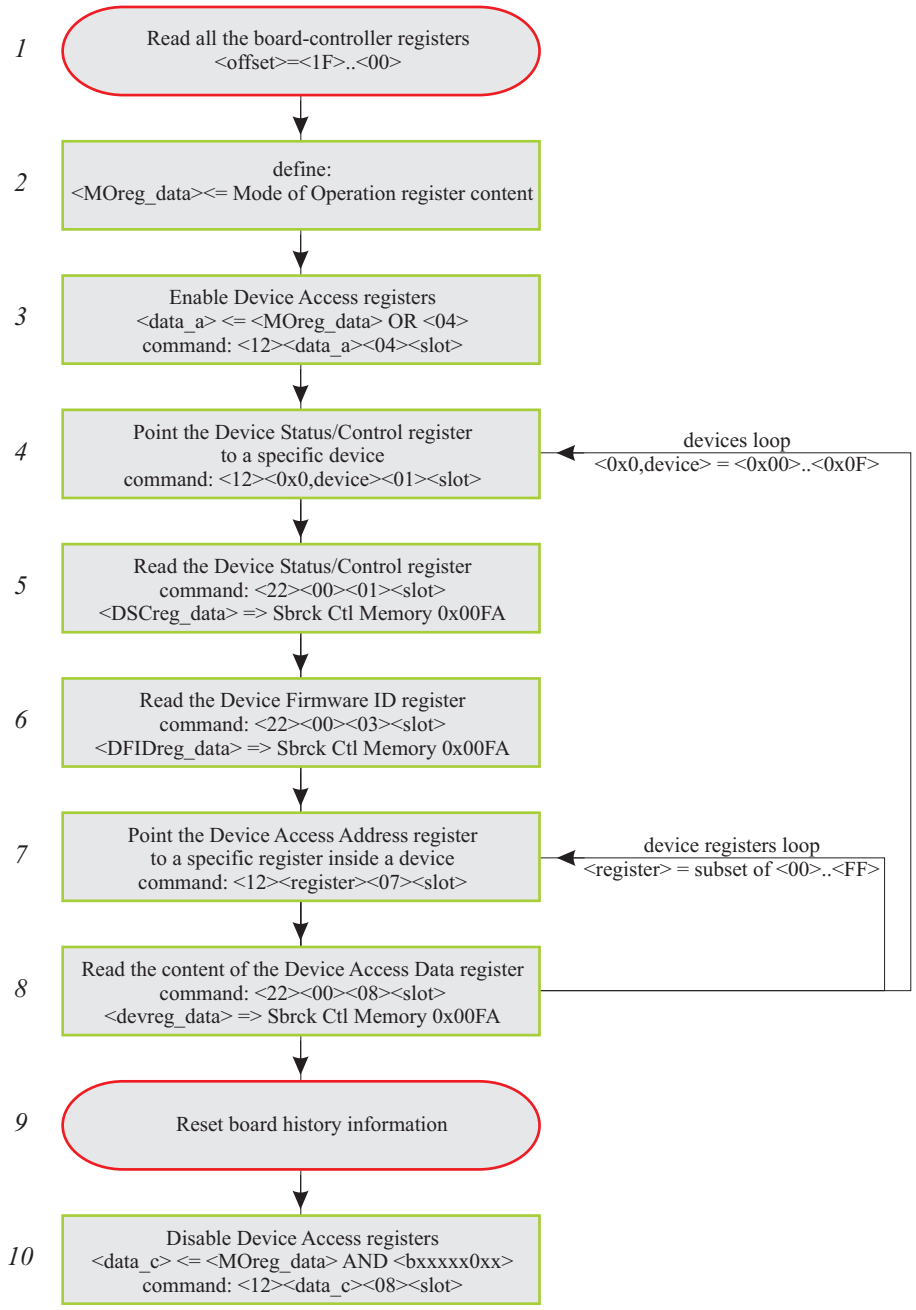


Figure 4.13, Mixer Board status snapshot

The read of the output links FIFOs is not included in the procedure. One exception is the procedure to read the content of the Device Status/Control register and the Device Firmware ID register. The content of these registers reflect the status/information of the device pointed by the four less significative (device select) bits of the Device Status/Control register.
It is suggested to erase all the history information after each snapshot (step 9 in Figure 4.13, the procedure is specified in paragraph 4.1.13). At the next snapshot this will provide useful insides on what happened on the board (i.e. loss of input links clock/frame-marker/frame-synchronization, etc.).

4.2 Input Links procedures

4.2.1 Read input links error status

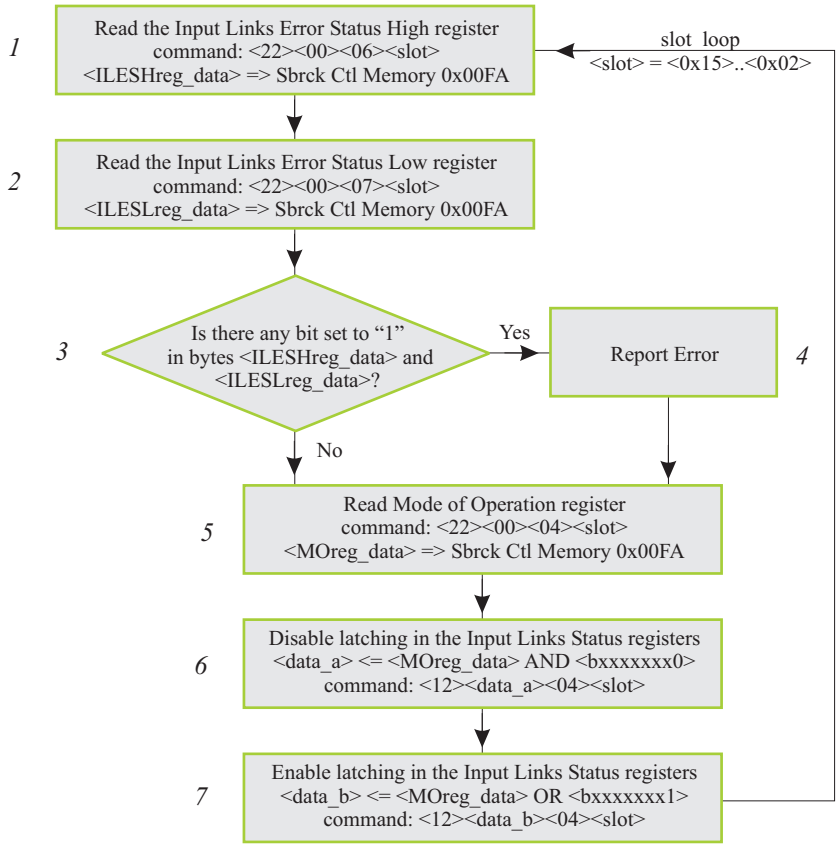


Figure 4.14, Read input links error status

4.2.2 Read input links status

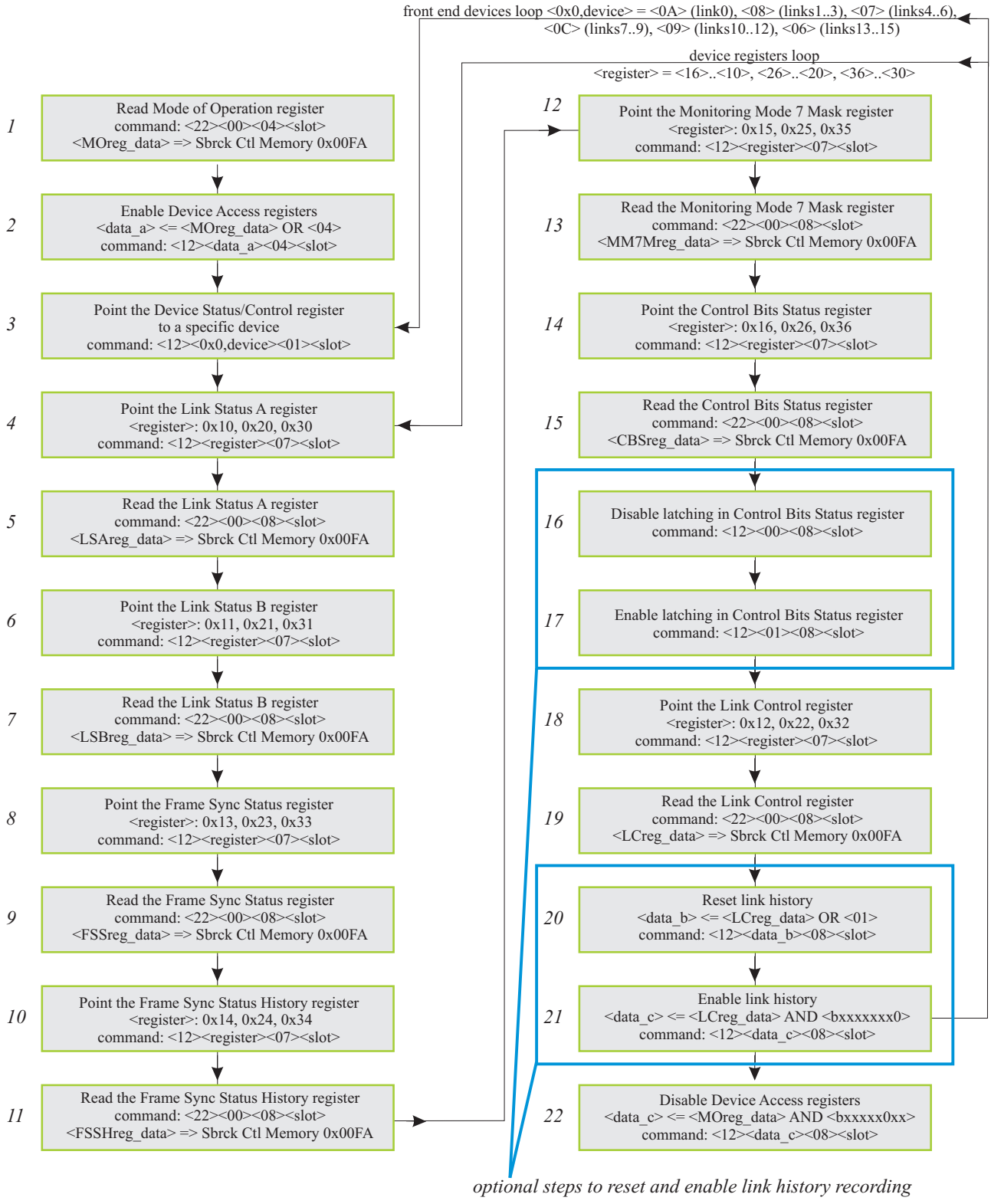


Figure 4.15, read input links status

4.2.3 Reset Mixer Board input links status history

Steps 4, 5, 6 are used to reset the control bits history information stored in the Control Bits Status registers.

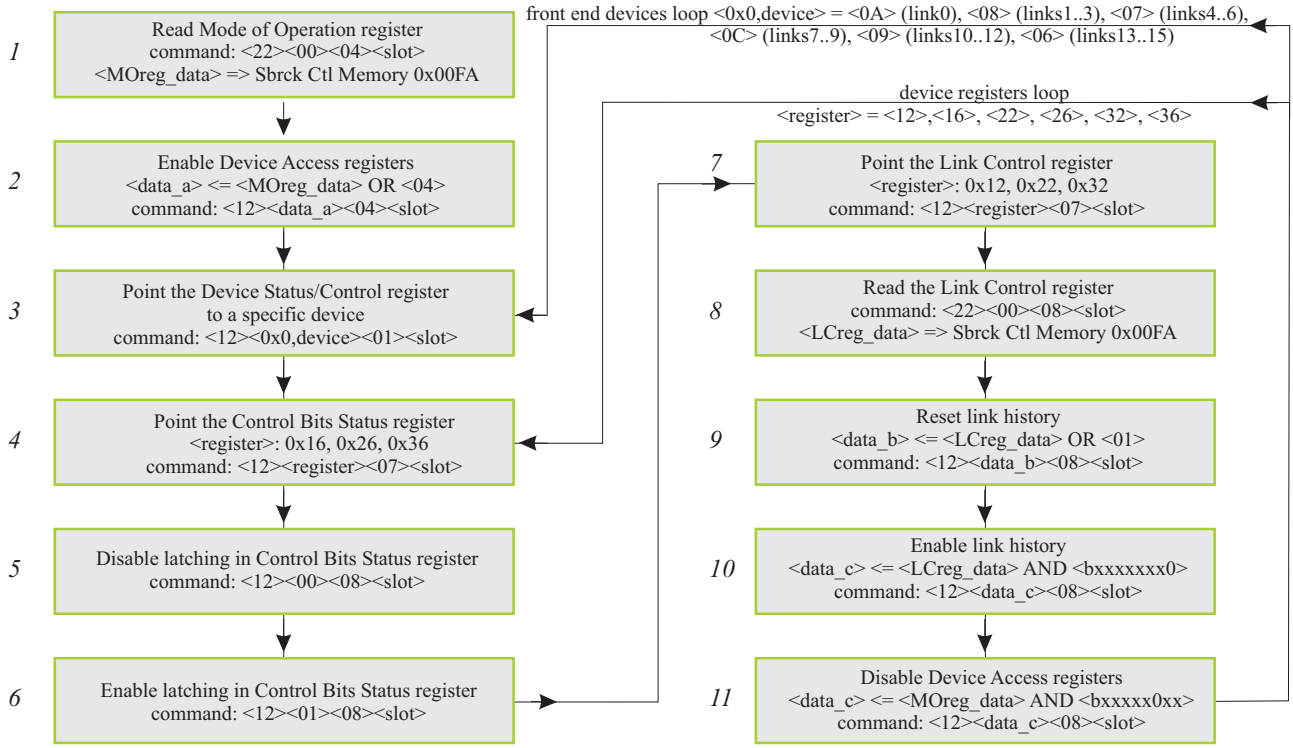


Figure 4.16, Reset input links status history

4.2.4 Input Links Control

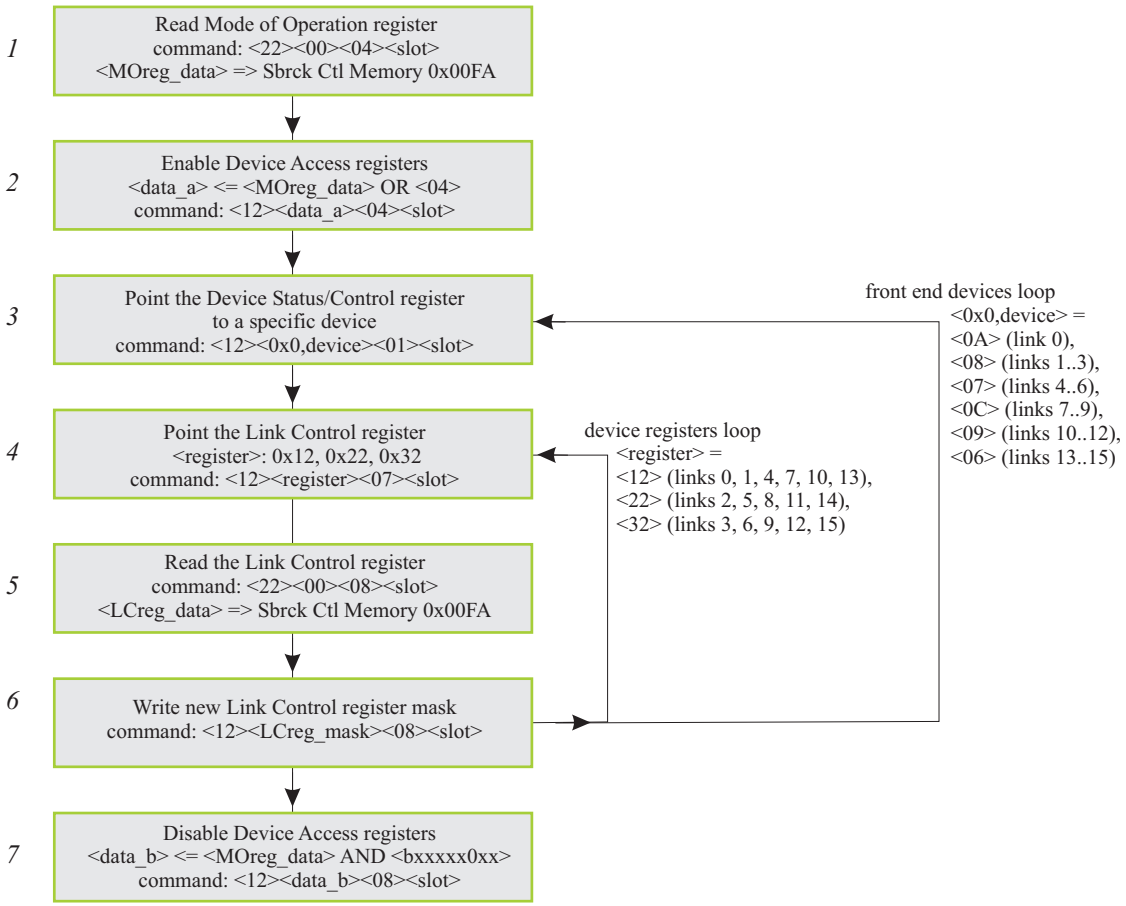


Figure 4.17, Input Links control procedure.

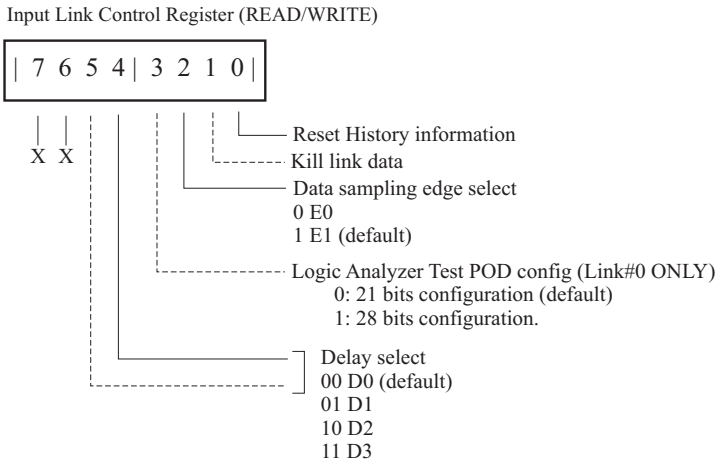


Figure 4.18, Input Links Control register

4.2.5 Input Links Control bits masking

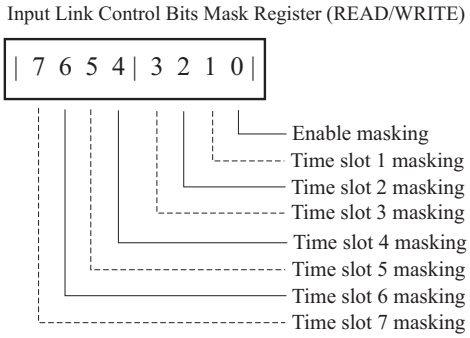


Figure 4.19, Input Link Control Bits Mask Register

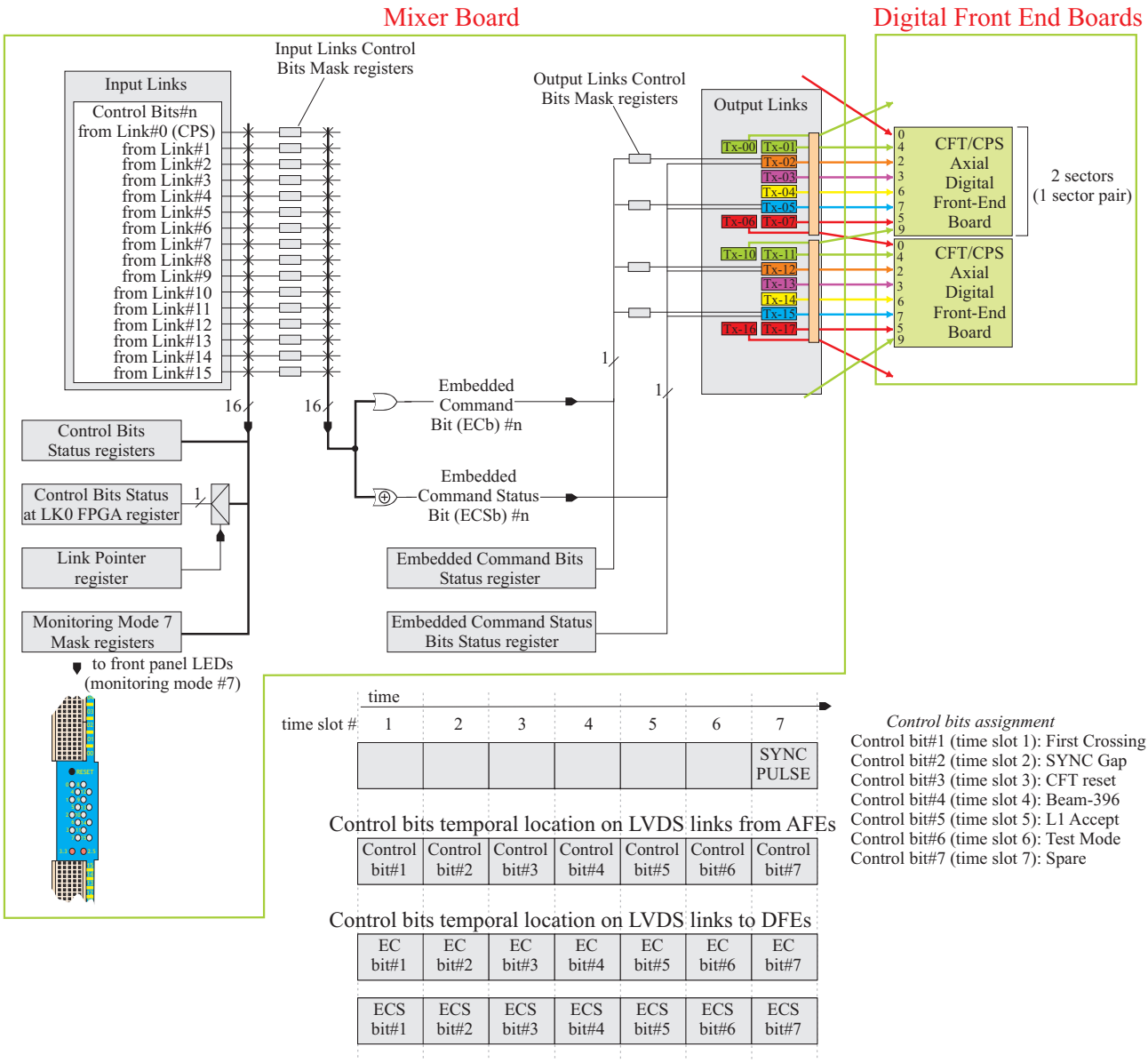


Figure 4.20, Command bits generation, timing and denomination.

command (0x)	Notes
<12><17><84><02>	Write 0x17 to the Mode of Operation Register of all mixer boards in the subrack (subrack broadcast) to enable Device Access Registers.
<12><0A><81><02>	Write byte 0x0A to the Device/Status Control register in all mixer boards (subrack broadcast). Sets the device select pointer to device 0x0A.
<12><reg_addr><07><slot>	Write byte <reg_addr> to the Device Access Address register (address <07>) of the mixer board in slot <slot>. This set the Device Access Address register to point inside device 0x0A to the register having address <regaddr>. <regaddr> depends on the input link on which the control bits mask is to be modified: <40>: Link#0 Control Bits Masking register <41>: Link#1 Control Bits Masking register <42>: Link#2 Control Bits Masking register <43>: Link#3 Control Bits Masking register <44>: Link#4 Control Bits Masking register <45>: Link#5 Control Bits Masking register <46>: Link#6 Control Bits Masking register <47>: Link#7 Control Bits Masking register <48>: Link#8 Control Bits Masking register <49>: Link#9 Control Bits Masking register <4A>: Link#10 Control Bits Masking register <4B>: Link#11 Control Bits Masking register <4C>: Link#12 Control Bits Masking register <4D>: Link#13 Control Bits Masking register <4E>: Link#14 Control Bits Masking register <4F>: Link#15 Control Bits Masking register <07>: <offset> byte: board Device Access Address register address. The most significative three bits of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
<12><cb_mask><08><slot>	Write <cb_mask> to the Device Access Data register of the mixer board in slot <slot>. The byte <cb_mask> will be written to the register pointed by <reg_addr> in the device 0x0A. This will mask the control bits on input link specified by <reg_addr>. <cb_mask> is the control bit mask and should be chosen depending on the control bits to be asked (see Figure 4.19 and Figure 4.20). <00>: masking disabled (equivalent to no masking) <FF>: masking enabled, no bit is masked <01>: all control bits are masked <DF>: only control bit at time slot 5 (L1 Accept) is masked. <08>: <offset> byte: board Device Access Data register address. The most significative three bits of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
	Repeat the last two commands as needed to mask the control bits on all the desired links.
<12><13><84><02>	Write 0x13 to the Mode of Operation Register of all mixer boards in the subrack (subrack broadcast) to disable Device Access Registers.
<A1><00>	End of list command. Stop the subrack controller execution of the commands in the command buffer.

Table 4.8, Example of command sequence to mask control bits on the input links.

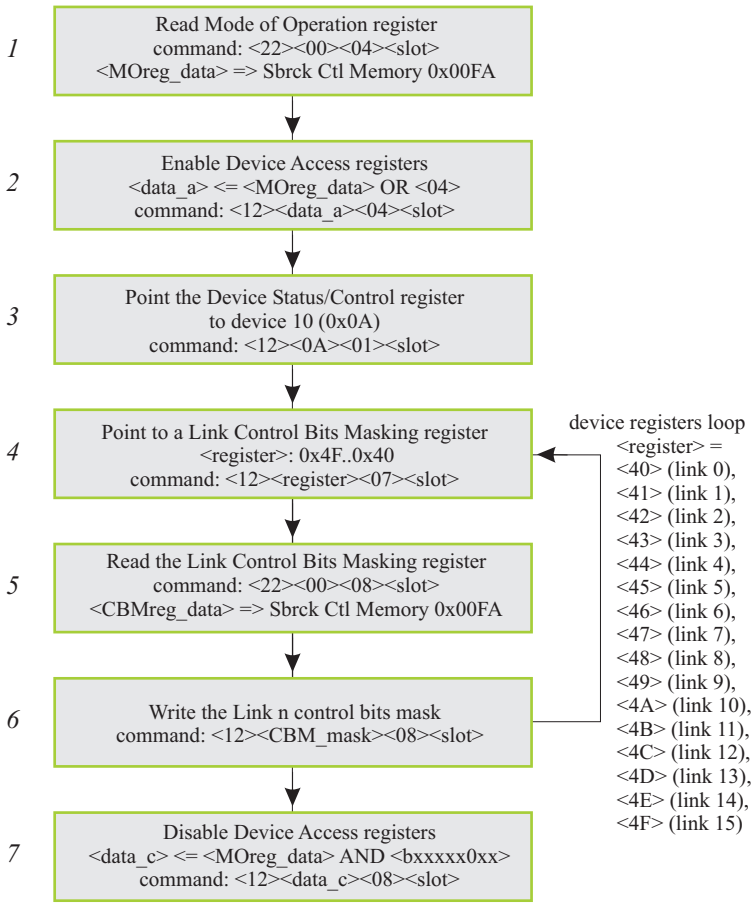


Figure 4.21, input links control bits masking

4.2.6 Monitoring mode 7 masking

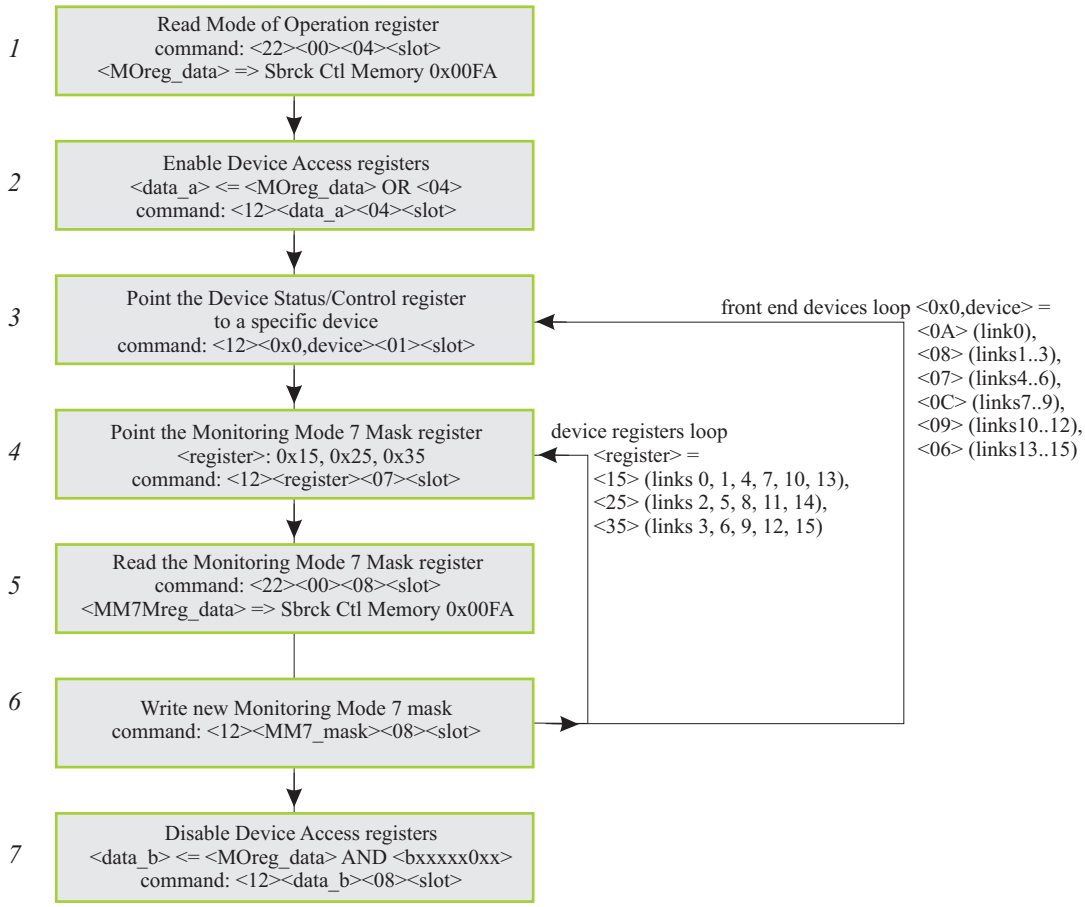


Figure 4.22, monitoring mode 7 masking

4.2.7 Input Links Control bits status

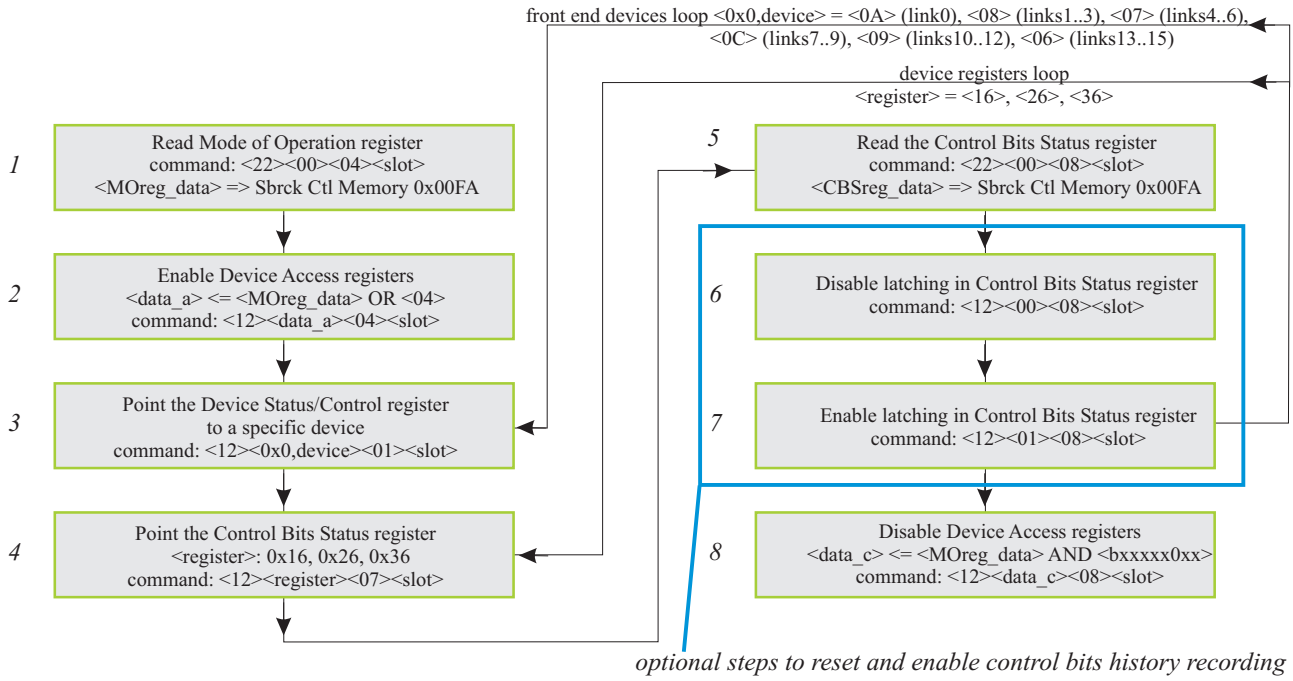


Figure 4.23, read input links control bits status

4.2.8 Embedded Command Bits Status

This procedure will allow to verify the status of the Embedded Command Bits (see Figure 4.20).

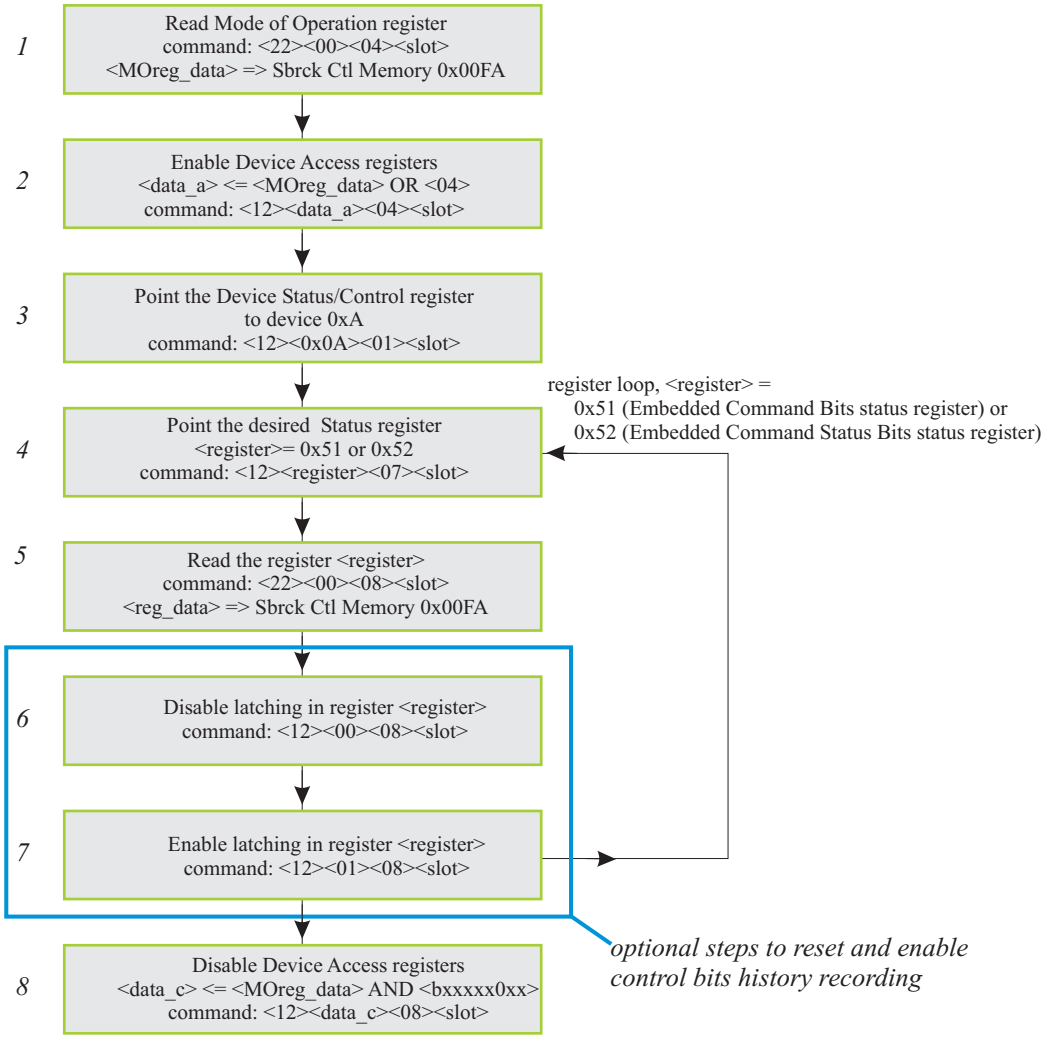


Figure 4.24, Read Embedded Command Bits status.

4.3 Backplane Devices Procedures

4.3.1 Reset Backplane Devices History

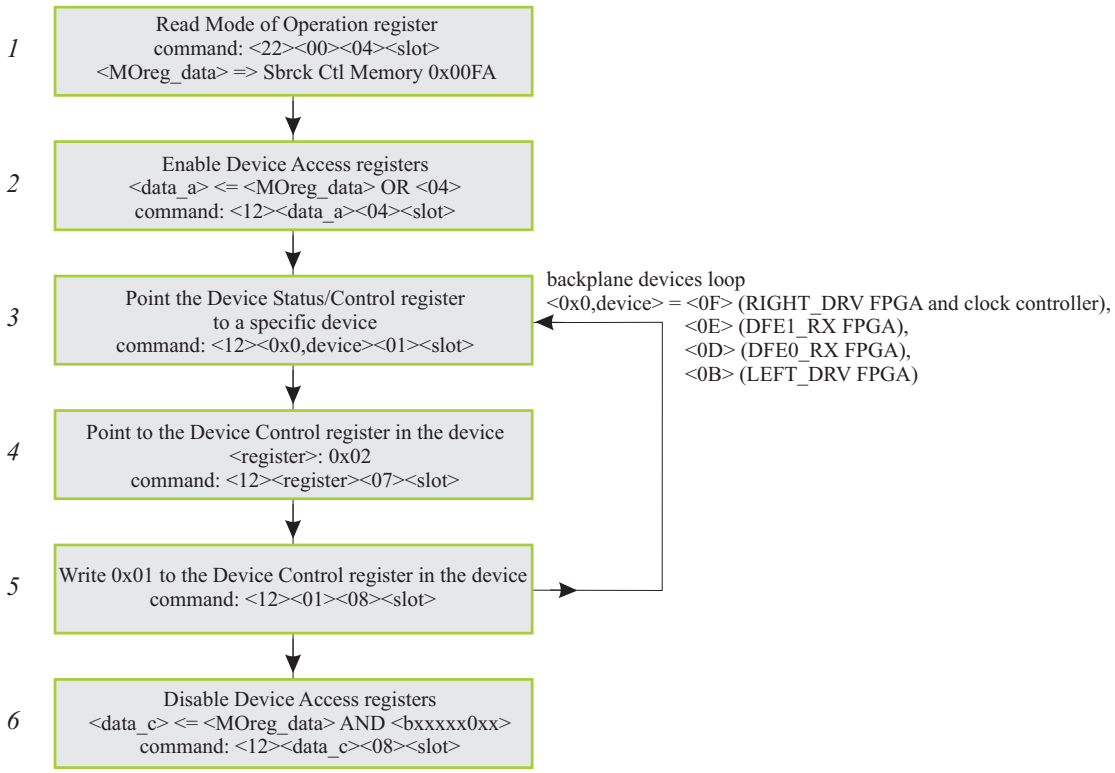


Figure 4.25, reset backplane devices history.

4.3.2 Readback Mixer Board clock/SYNC status

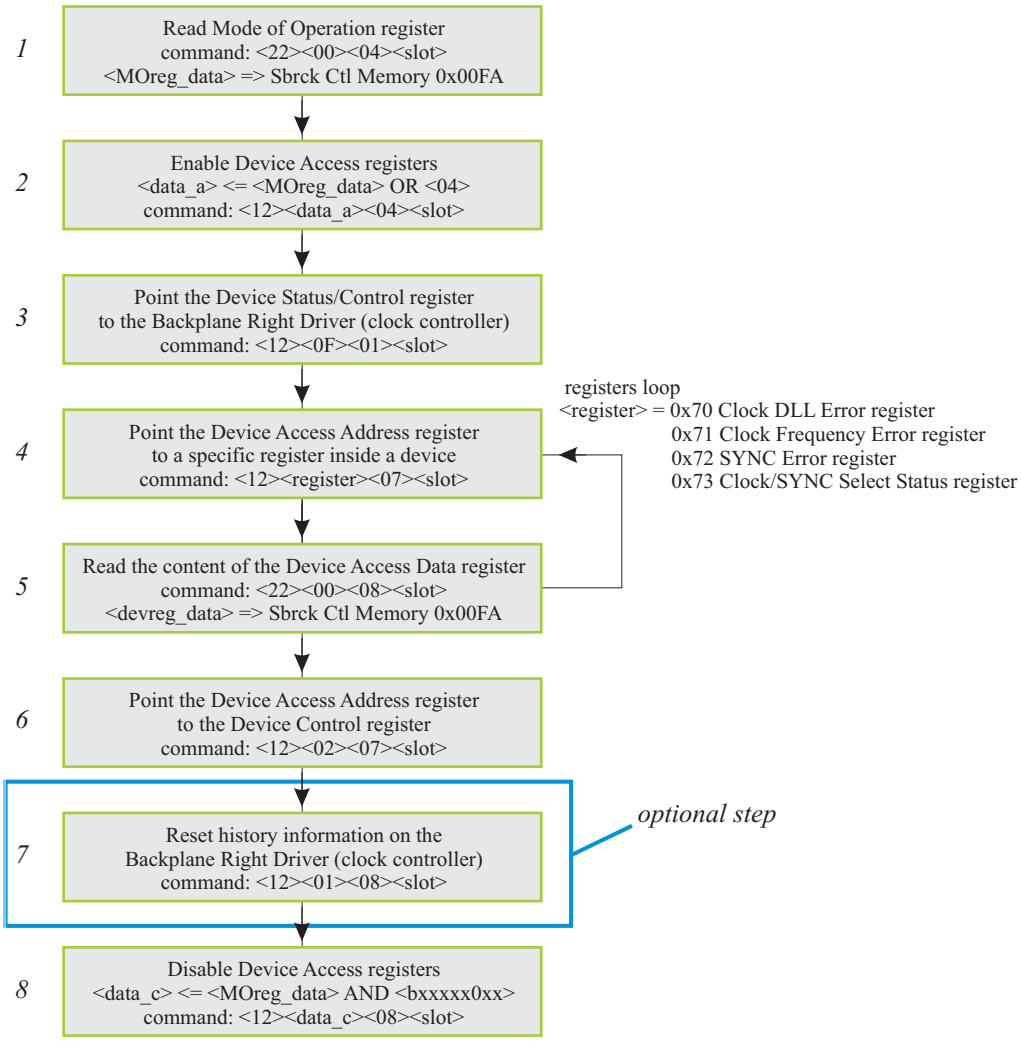


Figure 4.26, Read Clock/SYNC Status and History.

4.3.3 Reset Mixer Board clock/SYNC status history

The procedure to reset the clock and SYNC history on the mixer board is the same specified to reset history information on backplane devices (paragraph 4.3.1) applied to the Backplane right driver device (board controller).

4.4 Output links devices procedures

4.4.1 Output link FIFO read

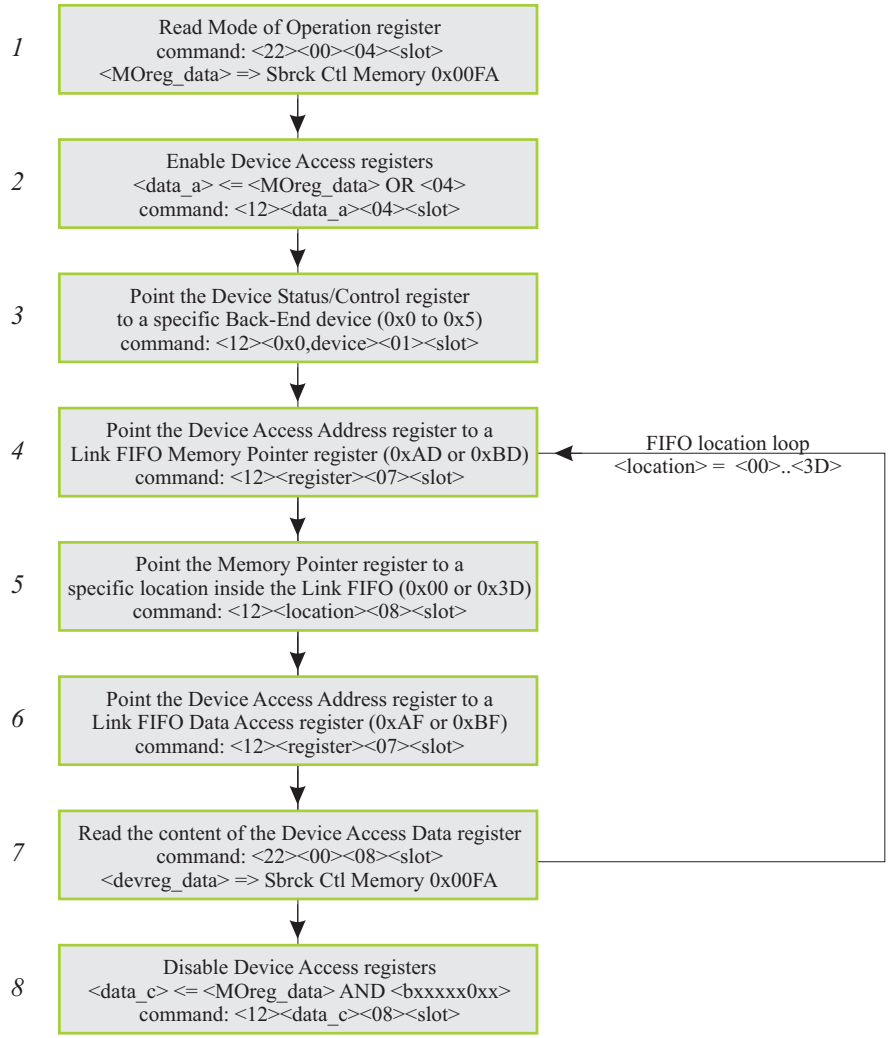


Figure 4.27, Read content of an output link FIFO.

4.4.2 Output link FIFO Write

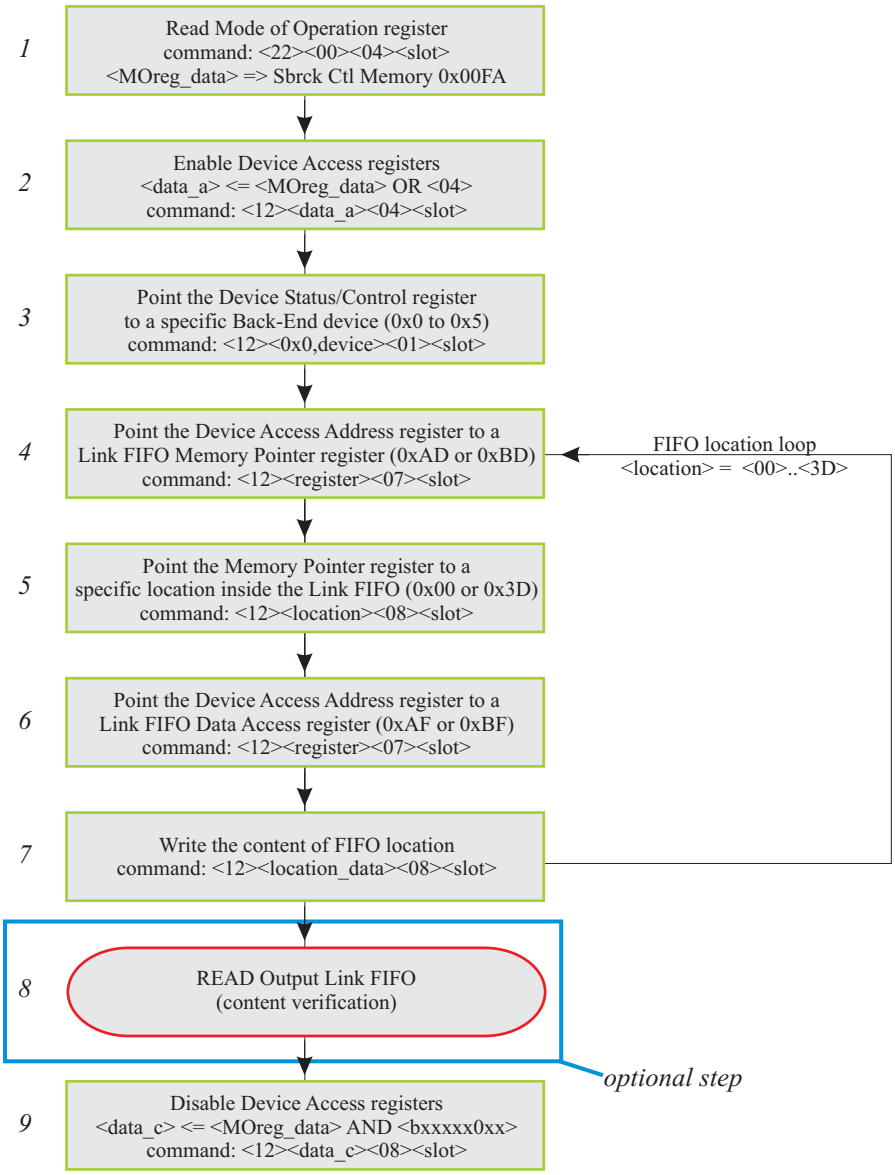


Figure 4.28, Write content of an output link FIFO.

Step 8 is specified in paragraph 4.4.1.

4.4.3 Output Link FIFO reset

Consist in the same procedure described in paragraph 4.4.2 for the output link FIFO write using <location_data> = 0x00.

4.4.4 Output link FIFO Configuration

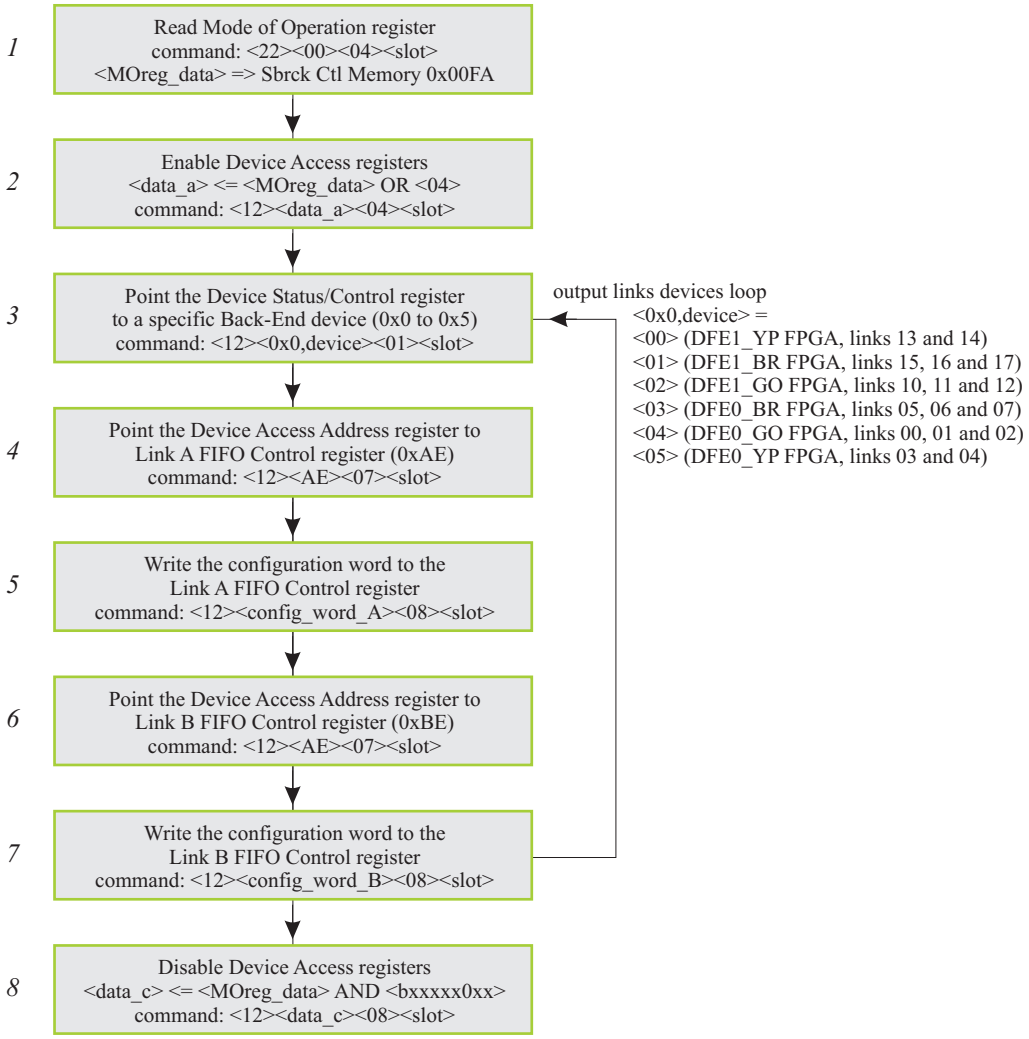


Figure 4.29, Output link FIFO configuration.

4.4.5 Triggering of Output Links FIFO

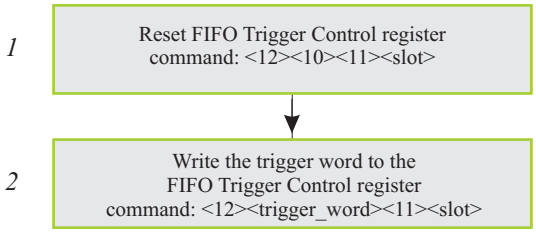


Figure 4.30, Triggering of Output Link FIFO.

4.4.6 Use of Output Links FIFOs

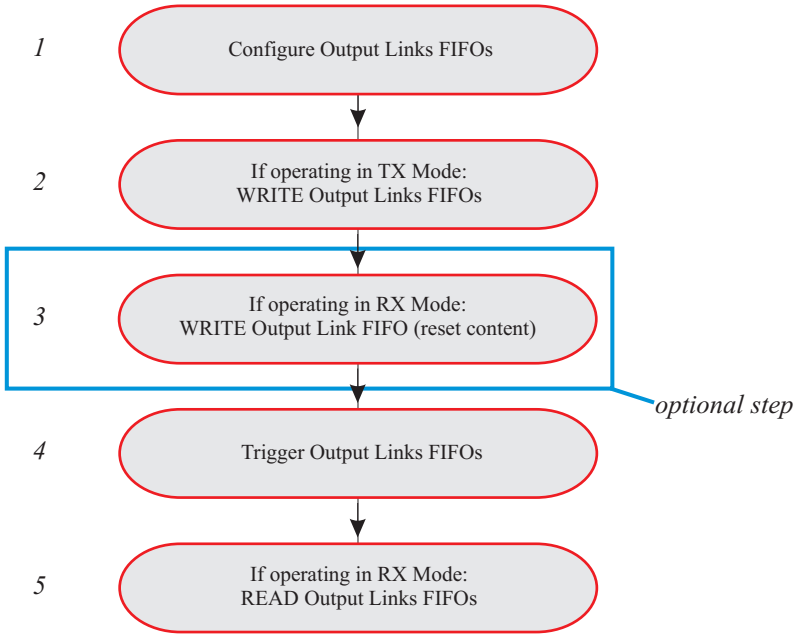


Figure 4.31, Use of Output Links FIFOs.

Step 1 is specified in paragraph 4.4.4. Step 2 and 3 are specified in paragraphs 4.4.2 and 4.4.3. Step 4 is specified in paragraph 4.4.5. Step 5 is specified in paragraph 4.4.1.

4.4.7 Reset Output Links History Information

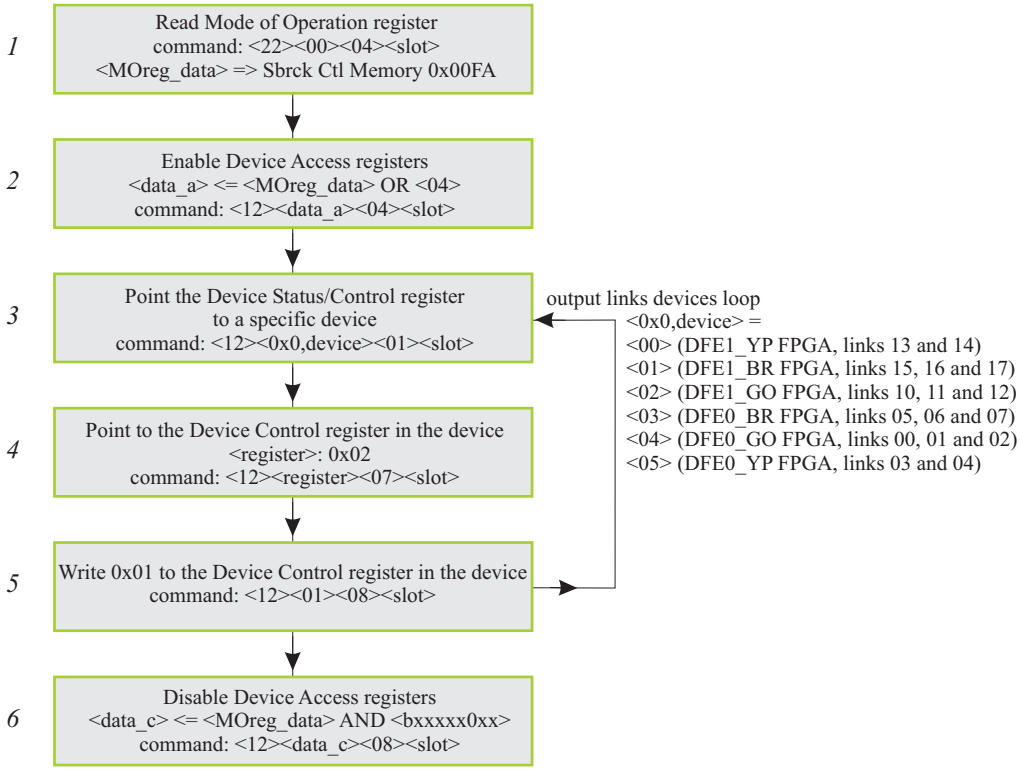
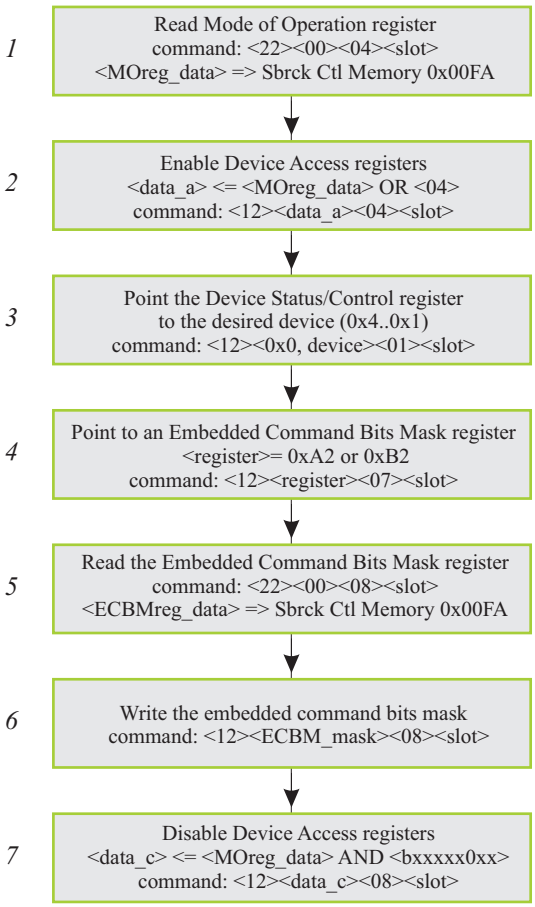


Figure 4.32, Reset output links history information

4.4.8 Output links Control Bits Masking

command (0x)	Notes
<12><17><84><02>	Write 0x17 to the Mode of Operation Register of all mixer boards in the subrack (subrack broadcast) to enable Device Access Registers.
<12><0x0,device><81><02>	Write byte <0x0, device> to the Device/Status Control register in all mixer boards (subrack broadcast). Sets the device select pointer to a particular device. There are 4 output links carrying control bits: Output link 02 (orange) is on device 0x4 (DFE0 Green Orange FPGA) Output link 05 (blue) is on device 0x3 (DFE0 Blue red FPGA) Output link 12 (orange) is on device 0x2 (DFE1 Green Orange FPGA) Output link 15 (blue) is on device 0x1 (DFE1 Blue red FPGA)
<12><reg_addr><07><slot>	Write byte <reg_addr> to the Device Access Address register (address <07>) of the mixer board in slot <slot>. This set the Device Access Address register to point inside the chosen device to the register having address <regaddr>. <regaddr> depends on the ounput link on which the control bits mask is to be modified: <B2>: Link#02 Embedded Command Bits Mask register <A2>: Link#05 Embedded Command Bits Mask register <A2>: Link#12 Embedded Command Bits Mask register <B2>: Link#15 Embedded Command Bits Mask register <07>: <offset> byte: board Device Access Address register address. The most significative three bits of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
<12><cb_mask><08><slot>	Write <cb_mask> to the Device Access Data register of the mixer board in slot <slot>. The byte <cb_mask> will be written to the register pointed by <reg_addr> in the device <device>. This will mask the control bits on output link specified by <reg_addr>. <cb_mask> is the control bit mask and should be chosen depending on the control bits to be asked (see Figure 4.19 and Figure 4.20). <00>: masking disabled (equivalent to no masking) <FF>: masking enabled, no bit is masked <01>: all control bits are masked <DF>: only control bit at time slot 5 (L1 Accept) is masked. <08>: <offset> byte: board Device Access Data register address. The most significative three bits of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.
	Repeat the last three commands as needed to mask the control bits on all the desired links.
<12><13><84><02>	Write 0x13 to the Mode of Operation Register of all mixer boards in the subrack (subrack broadcast) to disable Device Access Registers.
<A1><00>	End of list command. Stop the subrack controller execution of the commands in the command buffer.

Table 4.9, Example of command sequence to mask control bits on the output links.



Output link	Device	ECB Mask reg. address
02 (orange)	0x4 (DFE0_GO FPGA)	0xB2
05 (blue)	0x3 (DFE0_BR FPGA)	0xA2
12 (orange)	0x2 (DFE1_GO FPGA)	0xB2
15 (blue)	0x1 (DFE1_BR FPGA)	0xA2

Figure 4.33, Output links control bits masking.

4.4.9 Output Links Control

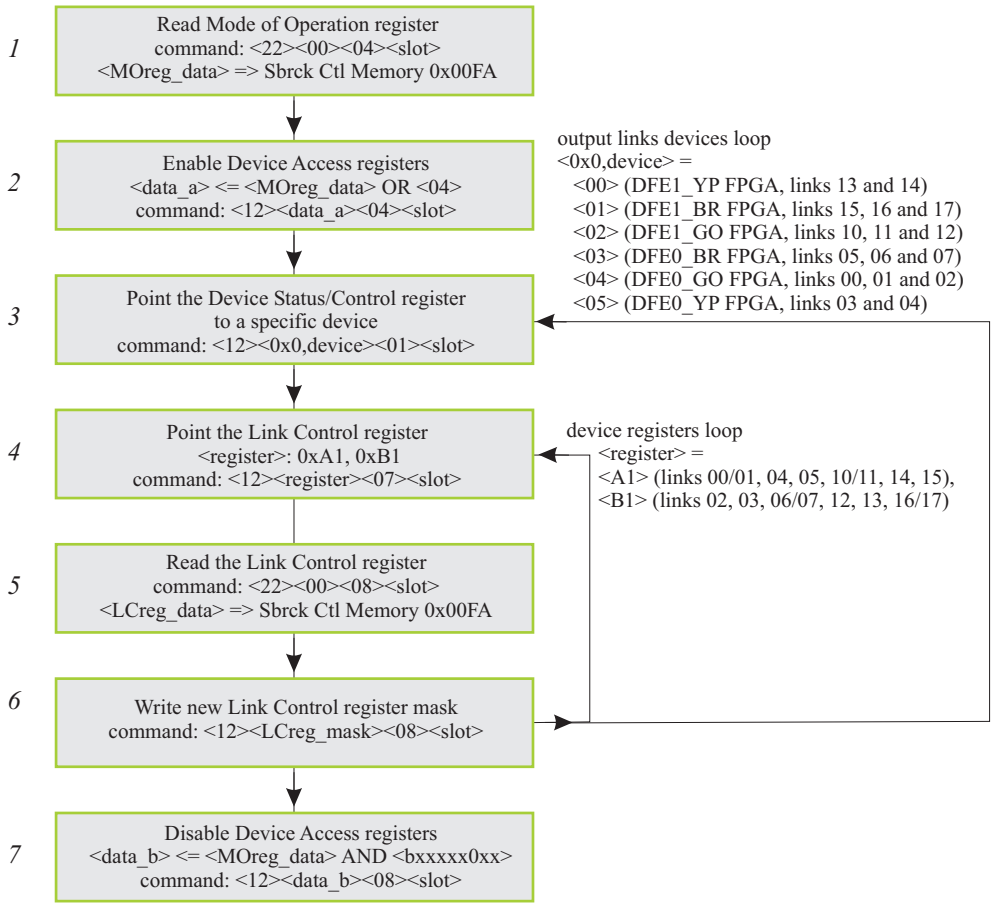


Figure 4.34, Output links control

To be noted that the output links LVDS transmitters clock can be disabled for all the output links at once using the Board Controller's Mode of Operation register.

4.5 System procedures

4.5.1 Mixer System reset

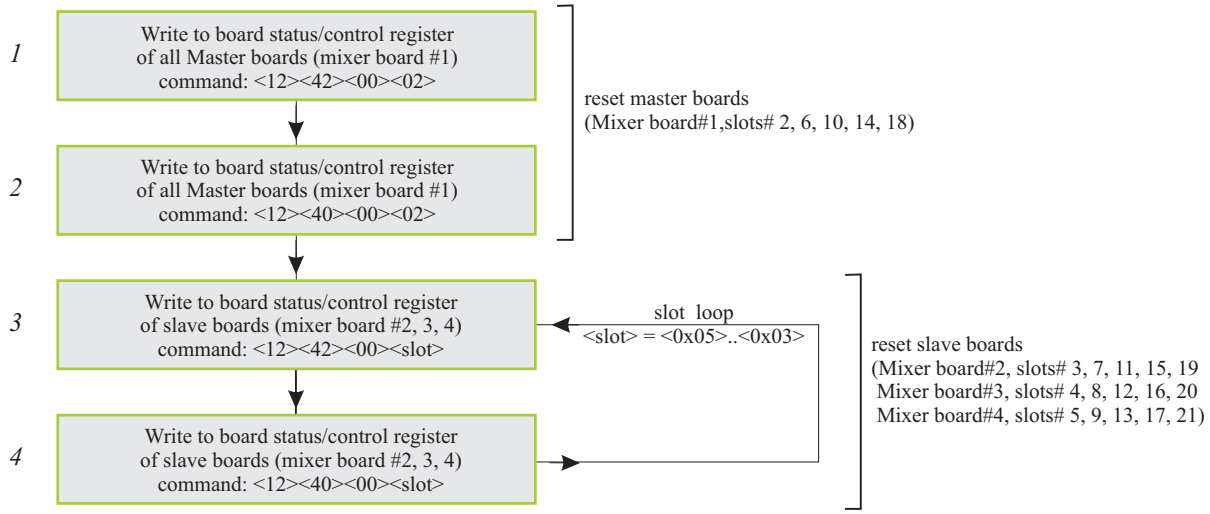


Figure 4.35, Mixer System reset

4.5.2 Mixer System Extended Reset

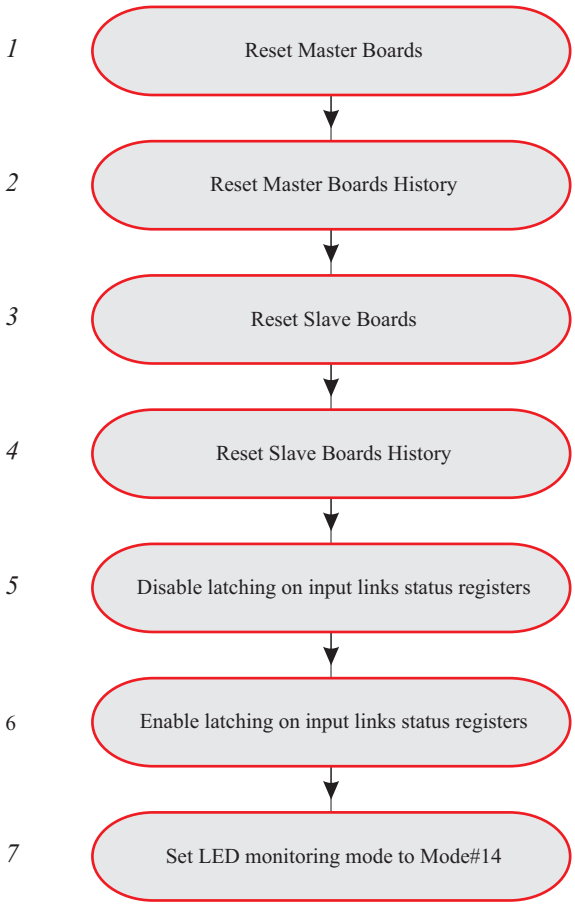


Figure 4.36, Mixer System extended reset

Steps 1 and 2 specified in paragraph 4.1.6. Steps 2 and 4 specified in paragraph 4.1.13.
Steps 5 and 6 consist in the sequance of steps from 5 to 7 of the procedure specified in 4.2.1.
Step 7 is specified in Figure 5.6.

4.5.3 Mixer System power-up initialization

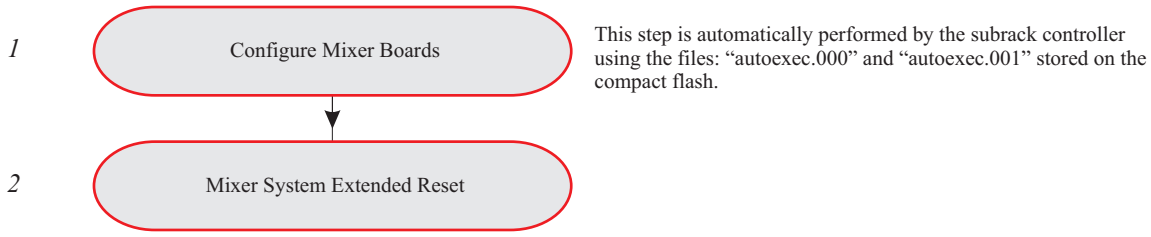


Figure 4.37, Mixer System Power-up initialization

Step 1 is automatically performed by the subrack controller using the command sequances stored in the “autoexec.000” and “autoexec.001” files.

Step 2 is specified in paragraph 4.5.2.

4.5.4 Mixer System configuration erasing

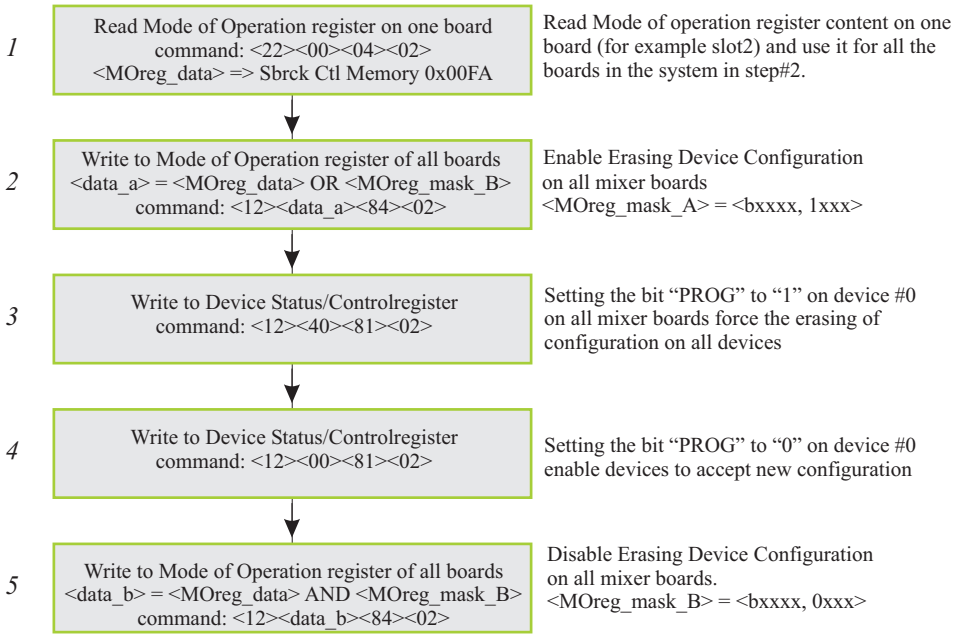


Figure 4.38, Mixer System configuration erasing.

4.5.5 Broadcast configuration of the mixer system

The procedure is illustrated in Figure 4.39 and follows the same steps used to automatically configure the mixer system at power-up. The command sequence used at power-up is stored in two "autoexec" command files on the subrack controller Compact Flash memory card. Steps 2 and 3 are not used for automatic power-up configuration but are needed when issuing commands remotely. The firmware ID byte can assume any value and at the moment no convention has been established for the mixer system. Step 6 is described in procedure XYZ and is used to verify that the successful configuration of the mixer system.

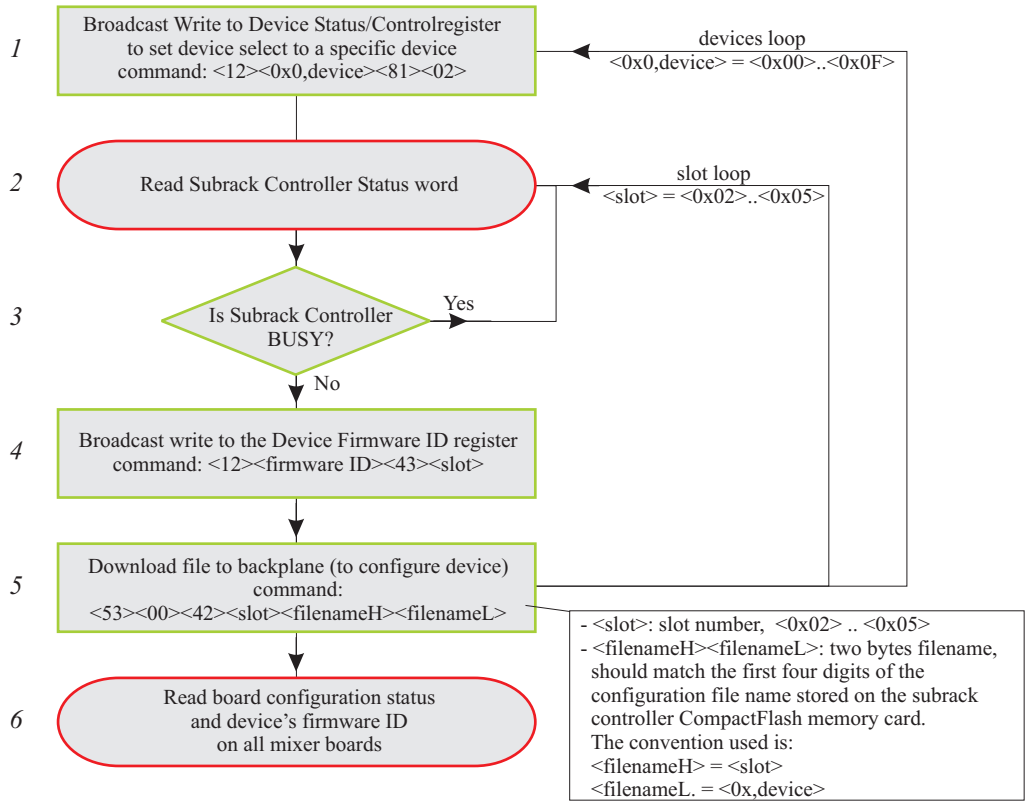


Figure 4.39, broadcast configuration of the mixer system

5. Use of the LEDs Monitoring Mode

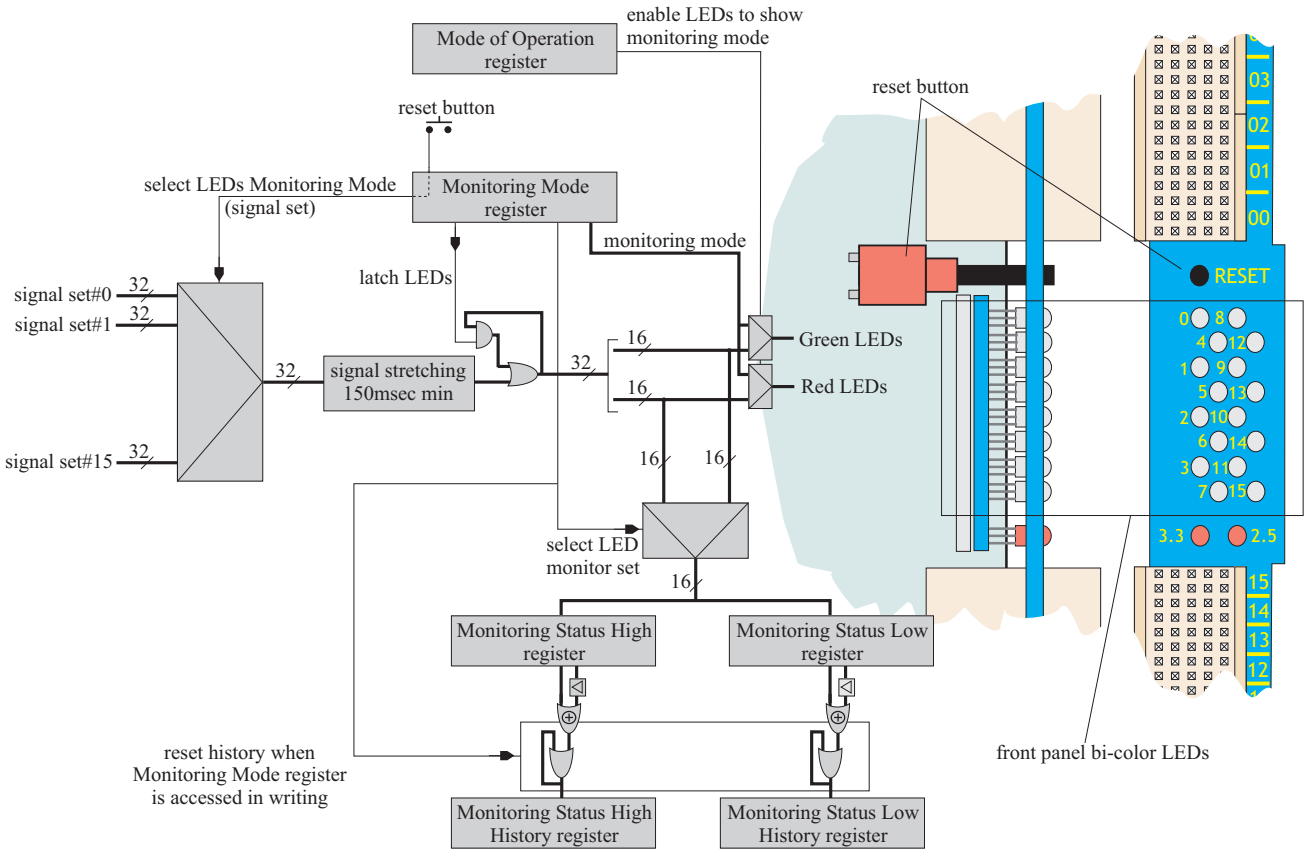


Figure 5.1, Front panel LEDs and LEDs monitoring mode

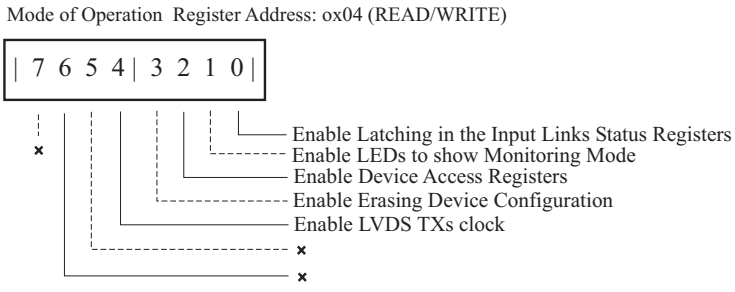


Figure 5.2, Mode of Operation register

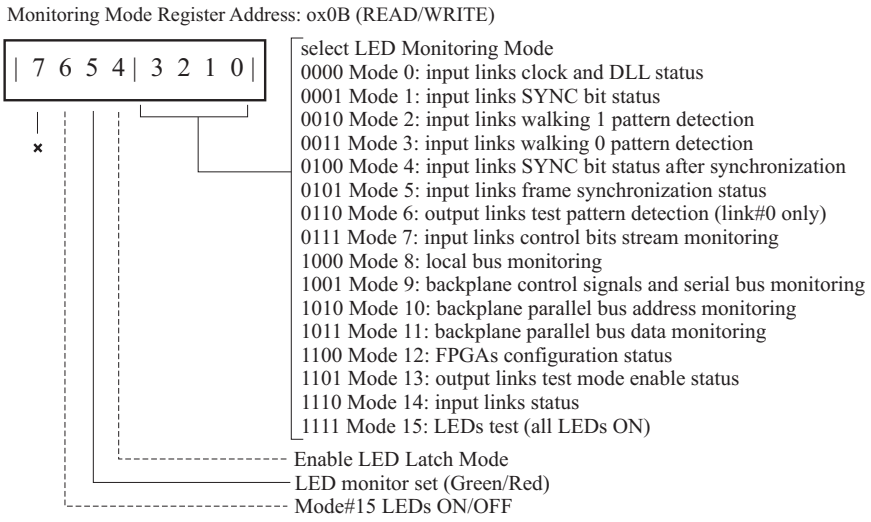


Figure 5.3, Monitoring Mode Register

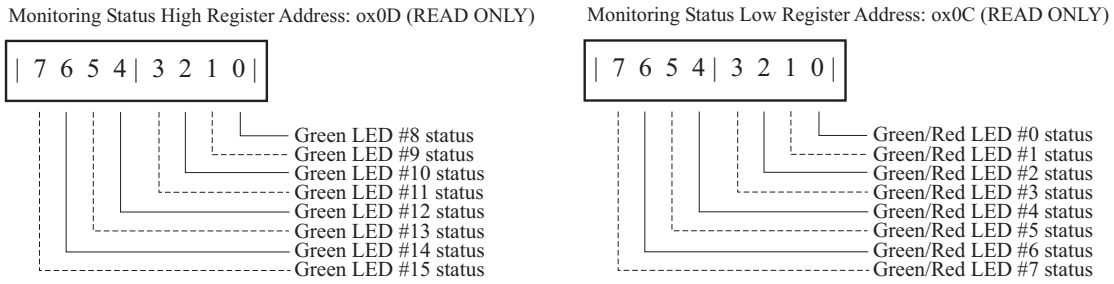


Figure 5.4, Monitoring Status Registers

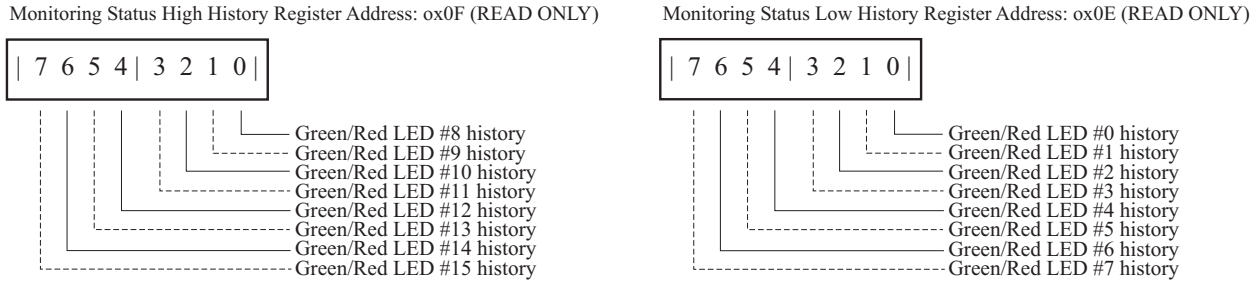


Figure 5.5, Monitoring Status History Registers

1	<22><00><0B><slot>	Read the content of the Monitoring Mode register. <22>: subrack controller command "read byte from backplane". <00>: unused byte. <0B>: <offset> byte, Device Access Data address. <slot>: mixer subrack slot number, from 0x02 to 0x15. The read data byte <MMreg_data > will be available in the subrack controller General Purpose Memory at location 0x00FA.
2	<12><data_a><0B><slot>	Write to the Monitoring Mode register. <12>: subrack controller command "write byte to backplane". <data_a>: (<MMreg_data> AND <bxxxx0000>) OR < MMreg_mask >. Is the logic AND of the byte obtained from the previous operation (<MMreg_data>) and <bxxxx0000> to reset the four least significative bits to "0". The result is then ORed with the desired mode: <MMreg_mask> = <b0000, mode>. In <bxxxx0000> the "bxxxx" are four non-care bits meaning that the AND operation is not performed on them and "mode" are four bits representing the desired monitoring mode. The four bxxxx bits can be replaced by a different set of bits to enable/disable some of the monitoring features such as "Enable LED latch Mode", select the "LED Monitoring set (green/red)", turn the LEDs ON/OFF in monitoring mode #15, see Figure 5.3. <0B>: <offset> byte, Monitoring Mode register address. The most significative three bit of the <offset> byte can be used for broadcasting control (see Figure 4.1). <slot>: mixer subrack slot number, from 0x02 to 0x15.

Table 5.1, Monitoring Mode change

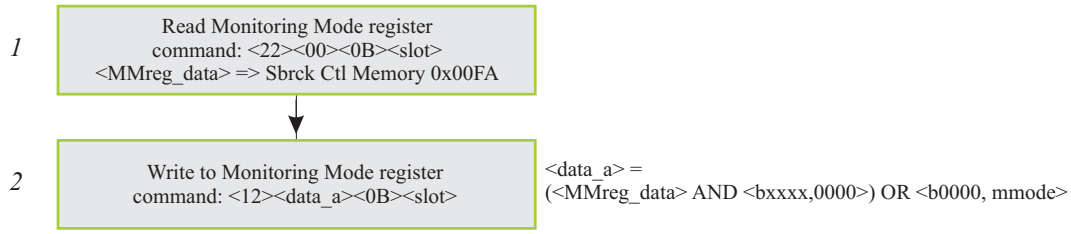


Figure 5.6, Monitoring Mode change

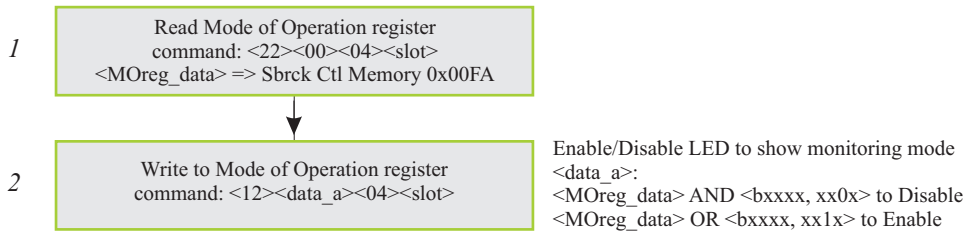


Figure 5.7, Enable/Disable LEDs to show monitoring mode

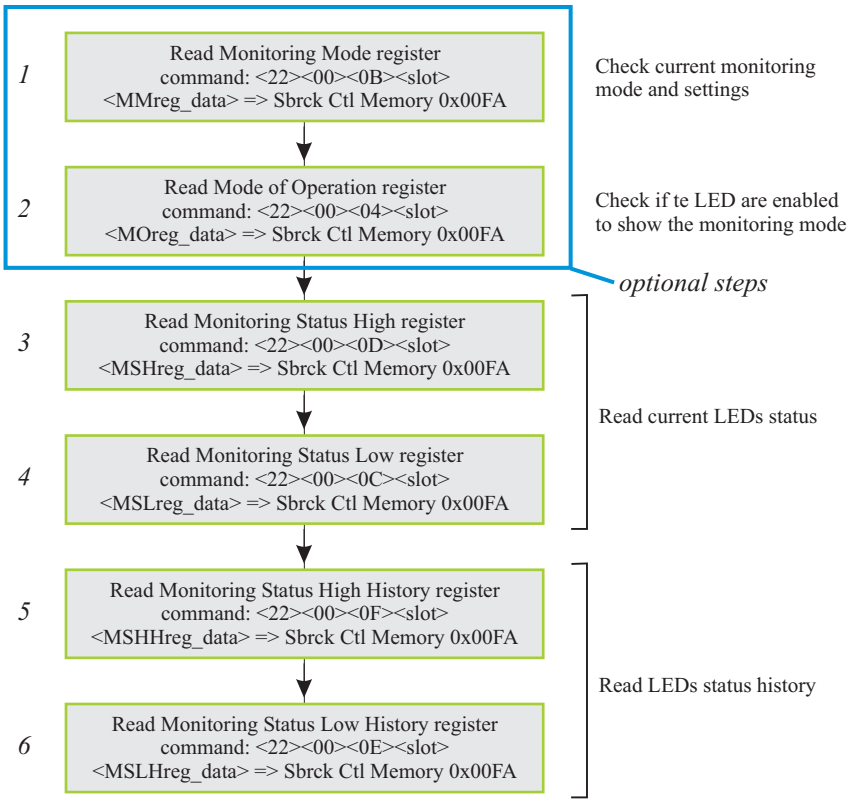


Figure 5.8, Read monitoring status and status history

6. Problem reporting

6.1 Report a problem to mixer system support

Stefano M. Rapisarda
E-mail: rapisard@fnal.gov
Phone: (630) 840-6559.

Neal G. Wilcer
E-mail: wilcer@fnal.gov
Phone: (630) 840-2749.

Computing and Engineering for Physics Application Department
Electronics Systems Engineering Section
Names and emails available on the ESE Section web page:
http://www-ese.fnal.gov/

6.2 Report a problem to AFE system support

George Ginther
E-mail: ginther@fnal.gov
Phone: (630) 840-6337.

Fred Borcherding
E-mail: fredb@fnal.gov
Phone: (630) 840-3164.

John T. Anderson
E-mail: janderson@fnal.gov
Phone: (630) 840-8885.

7. References

[1] Jamieson T. Olsen,

a) "Digital Front End Mother Board register map", Engineering Note 2000-01-28a.

b) "DFE and Mixer Board Registers ", Engineering Note 2000-01-28a.

c) "DFE backplane address/data bus protocol", Engineering Note 2000-03-28a.

d) "DFE slow monitoring custom serial bus specification", Engineering Note 2000-01-31a.

e) Digital Front End Controller (DFEc) Board: http://d0server1.fnal.gov/users/jamieson/www/projects/dfec/index.html

f) "DFE Crate Controller (DFEC) Command Structure and 1553 Interface Specification", Engineering Note 2001-04-16a.

Information available on the internet: http://d0server1.fnal.gov/users/jamieson/www/index.html

[2] Robert D. Angstad, technical documentation. Information available on the internet: http://d0server1.fnal.gov/users/angstadt/www/datapump/datapump.htm

[3] John T. Anderson,

a) "D-Zero Central Fiber Tracker 8-MCM Analog Front End Board, Design Specification", January 7, 2000.

Information available on Internet: http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/default.html.

[4] Mixer System documentation

a) Neal Wilcer, John Anderson, Stefano Rapisarda "Central Tracker Trigger (CTT) Mixer System Backplane Description & Power Distribution Specification", July 4, 2000. Document#: ESE-D0-000704.

b) Makoto Tomoto, "Note on cable mapping from AFE to Mixer", October 26, 2001.

c) Central Tracker Trigger (CTT) Mixer System Test Procedures.

d) Central Tracker Trigger (CTT) Mixer System.

The mentioned documents and several others are available on Internet: http://www-ese.fnal.gov/D0_CTT_Mixer/