Integrated Device Technology, Inc.

HARDWARE FIX FOR 77201 REV. C3 AND REV. D SAR ERRATA

TECHNICAL NOTE TN-29

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ABSTRACT:

This tech note is to describe the hardware used to fix the following items in the errata dated June 18, 1996:

#9 When the timer rolls over before the 77201 is initialized

#14 Intolerance of controllers that are non-compliant to the PCI spec.

DETAIL DESCRIPTION:

Errata #9: The timer rolls over before the 77201 is initialized.

This situation will cause the 77201 to generate a TSI (Transmit Status Indicator) in the TSQ (Transmit Status Queue). This is accomplished by DMAing the timer rollover indicator into host memory at the TSQ address. If the 77201 is not initialized with a proper TSQBA (Transmit Status Queue Base Address) register with a non-zero value, the 77201 will write the TSI to host memory location zero. This may cause some operating systems to crash.

The hardware fix requires a Quickswitch to isolate the 77201 PCI bus request line ($\overline{\text{SAR\_REQ}}$ in the diagram) from the PCI bus at PCI power-up reset. This effectively disables DMAs by the SAR. When the device driver initializes the 77201 (including the TSQBA register), it should enable the $\overline{\text{SAR\_REQ}}$ signal by writing to the utility bus with $\overline{\text{UTL\_CS1}}$ = 0, $\overline{\text{UTL\_CS0}}$ = 1, and UTL_AD0 = 1. Also, when the 77201 device driver is un-loaded, $\overline{\text{SAR\_REQ}}$ can be turned off by writing to the utility bus with $\overline{\text{UTL\_CS1}}$ = 0, $\overline{\text{UTL\_CS0}}$ = 1, AND UTL_AD0 = 0.

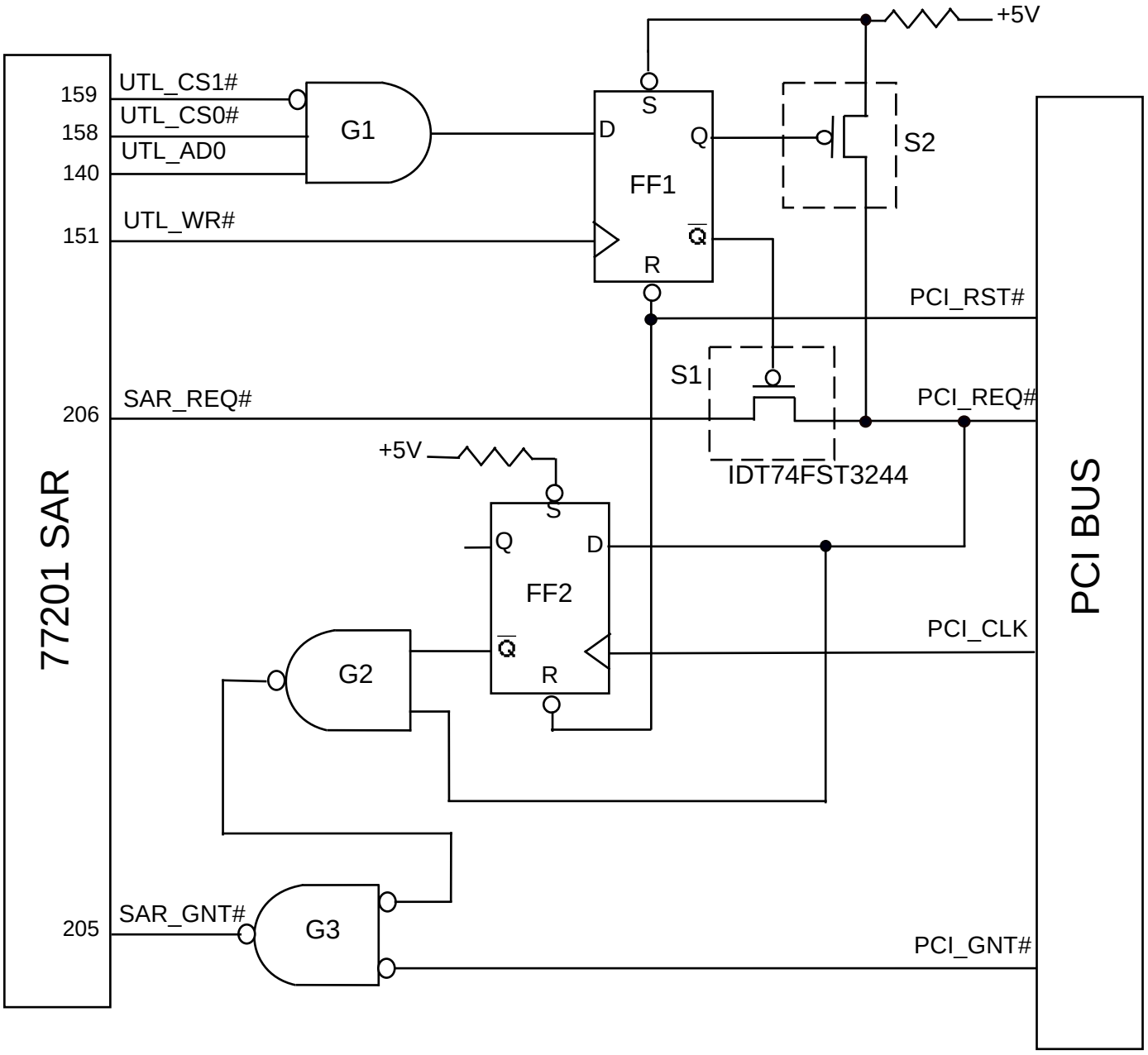
Hardware used in the diagram to accomplish this function is: S1, S2, FF1 and G1.

Errata #14: Intolerance of controllers that are non-compliant to the PCI spec.

Some PCI chip sets arbiters do not take away PCI $\overline{\text{GNT}}$ until one PCI clock after $\overline{\text{REQ}}$ becomes de-asserted. This delayed de-activation of the $\overline{\text{GNT}}$ will make the 77201 a park master according to the PCI Spec. To optimize the PCI bus utilization, the 77201 could start a PCI cycle when it is a park master (in the next PCI clock - the same time that the $\overline{\text{GNT}}$ is being de-activated). Correct operation should allow the 77201 to complete the transfer. Some controllers have been observed to violate this function (e.g. the new low-end versions of the Power Macintosh and the IBM DX4-100 model 330).

To allow tolerance to these non-compliant controllers, hardware consisting of an OR-gate to block off $\overline{\text{GNT}}$ to the 77201 one PCI clock after the $\overline{\text{REQ}}$ becomes de-asserted (this additional clock is required by the non-compliant PCI chip set to take away $\overline{\text{GNT}}$).

Hardware used in the diagram: FF2, G2 and G3.



77201 REV. C3 and D External Hardware Fix

Note: all components except the IDT74FST3244, can be put inside a single PLD. An alternate part to IDT74FST3244 is the IDT74FST6800, which combines the S1 and S2 internally to cut down the PCI bus loading.

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