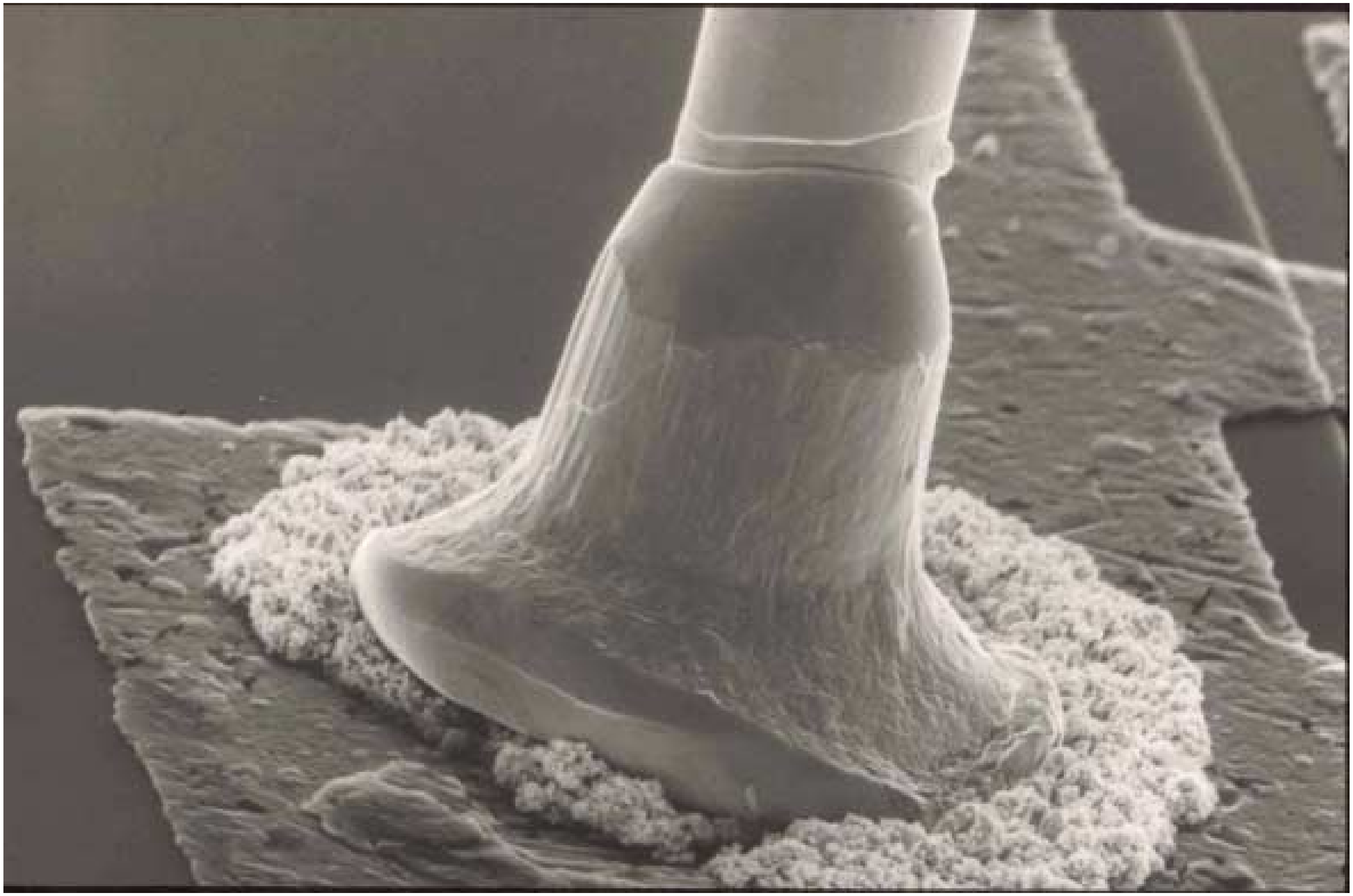
Metallurgical Interconnections for High/low Temperature Extreme Environments in Microelectronics.

George G. Harman, NIST Fellow-E
National Institutes of Standards and Technology
Gaithersburg, MD 20899 <george.harman@nist.gov>

- *What kind of interconnections are of Interest? (some only briefly reviewed)*
- **For Chip I/Os**: Bond Pads/adhesion, Wire-bonds, Flip-Chips, and Die Attach
- Other: TC, Parallel-gap Welds, Seam Welders for Package lids, Solder (hard and soft-low temp), etc.

Gold-Aluminum Intermetallic Compound and Kirkendall Voiding-(Prototype for bimetallic interconnect failures)



Plague and Plague-Corrosion Failures

A) CLASSICAL FAILURES

- a) High Electrical Resistance or Open Circuits
- b) Weak Bond Adherence
- c) Brittle Bond Heels

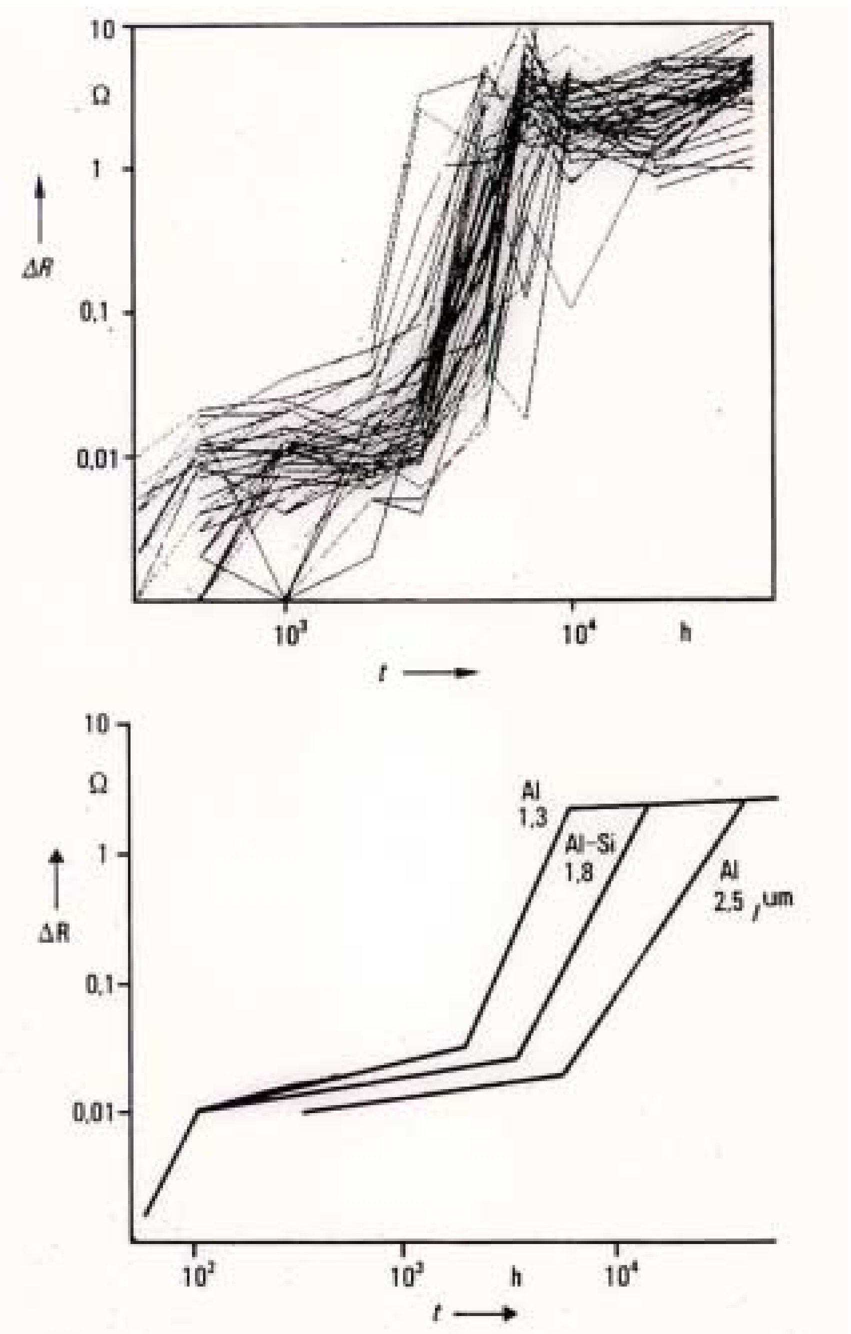
B) CONTAMINATION-INDUCED PLAGUE-LIKE FAILURES

- a) Epoxy and other Organics
- b) Halogens from Many Sources
- c) Other Reactive Species

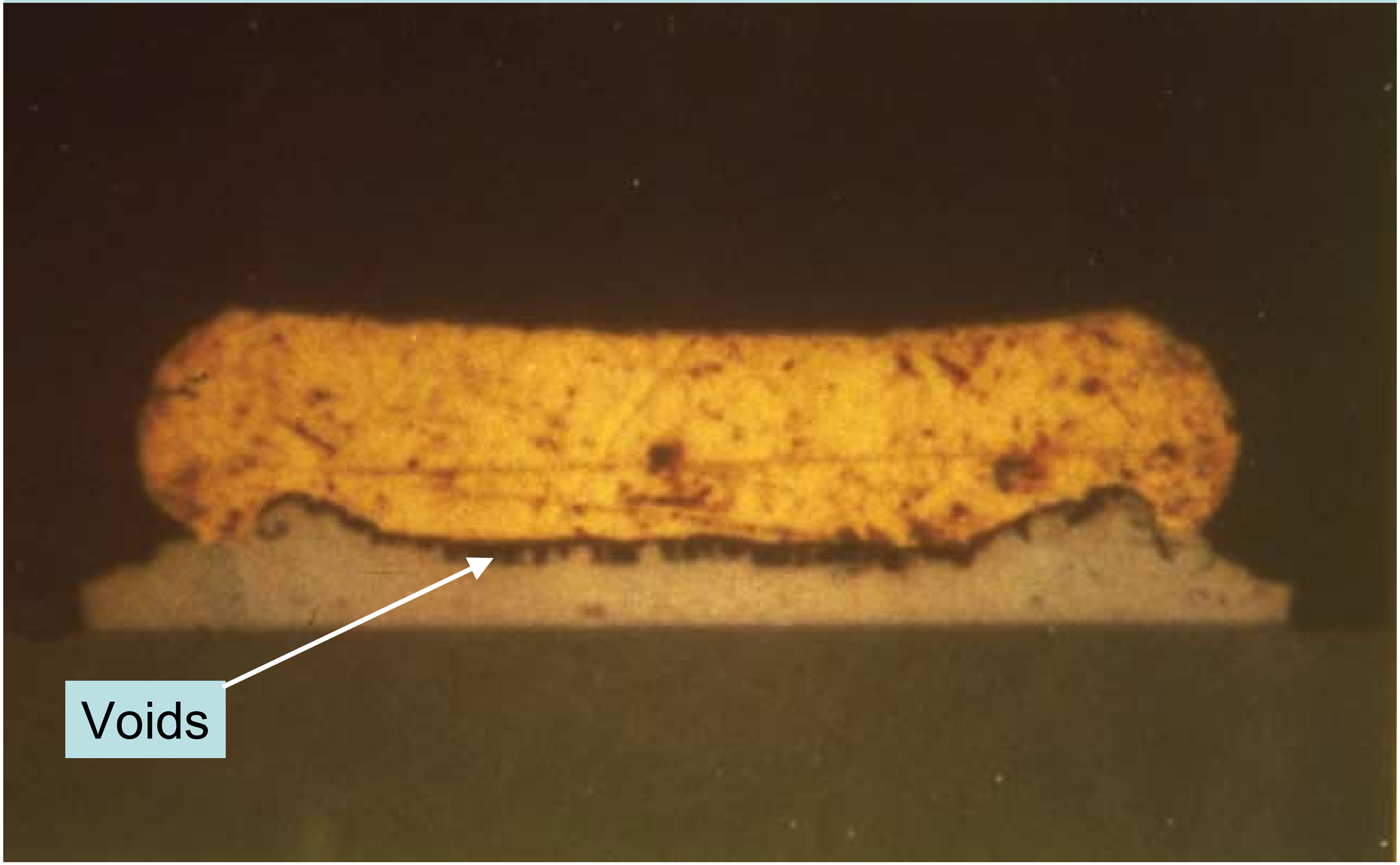
Resistance Increase of Au Ball Bonds on Al

- Curves of Contact-resistance-change for Different Test Groups at Test Temperature of 200˚C.

- (Initial contact resistance are typically ~ a few milliohms)

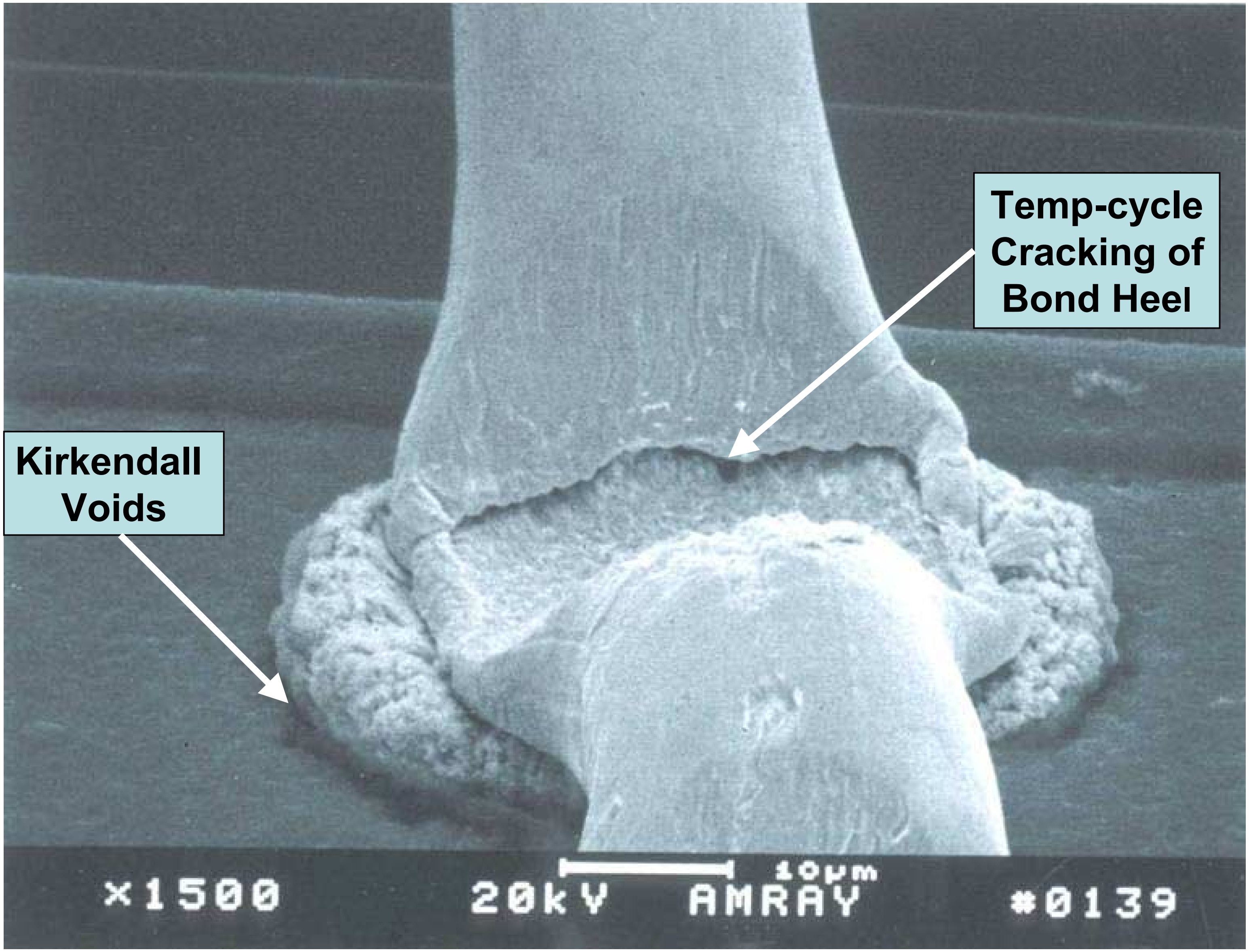


A Line of Voids *Under* a Gold Ball Bond



Voids

Au Stitch-bond on Al Pad, Showing Kirkendall Voids and Temp-cycle Cracks



Temp-cycle Cracking of Bond Heel

Kirkendall Voids

Au-Al Intermetallic Growth Rates

- The Growth Rate, ***x***, is Parabolic

$x = Kt^{1/2}$, ***where t* is time,**

(The 5 Phases Each Have Different Rate Constants, ***K***.)

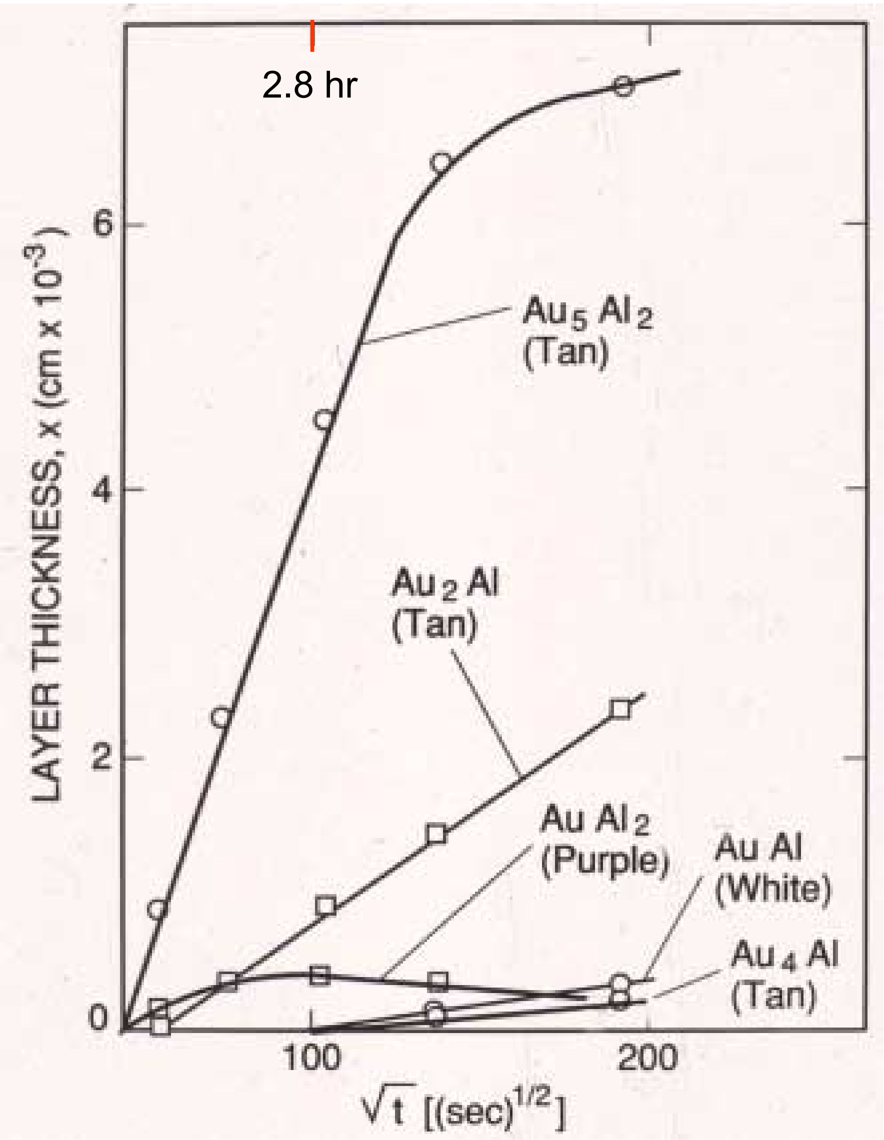
- The Usual ***Arrhenius Equation*** is:

$$K = Ae^{-E/RT}$$

Where: **E** is the activation energy for layer growth,
R is the molar gas constant,
T is the absolute Temperature in Deg. Kelvin.

(Crude Rule of thumb is that the reaction rate ~ doubles every 10☞C)

The Layer Thickness of Five Intermetallic Phases *vs.* the Square Root of Time at 400˚C



Al-Au Phase Diagram (intermetallics in color)

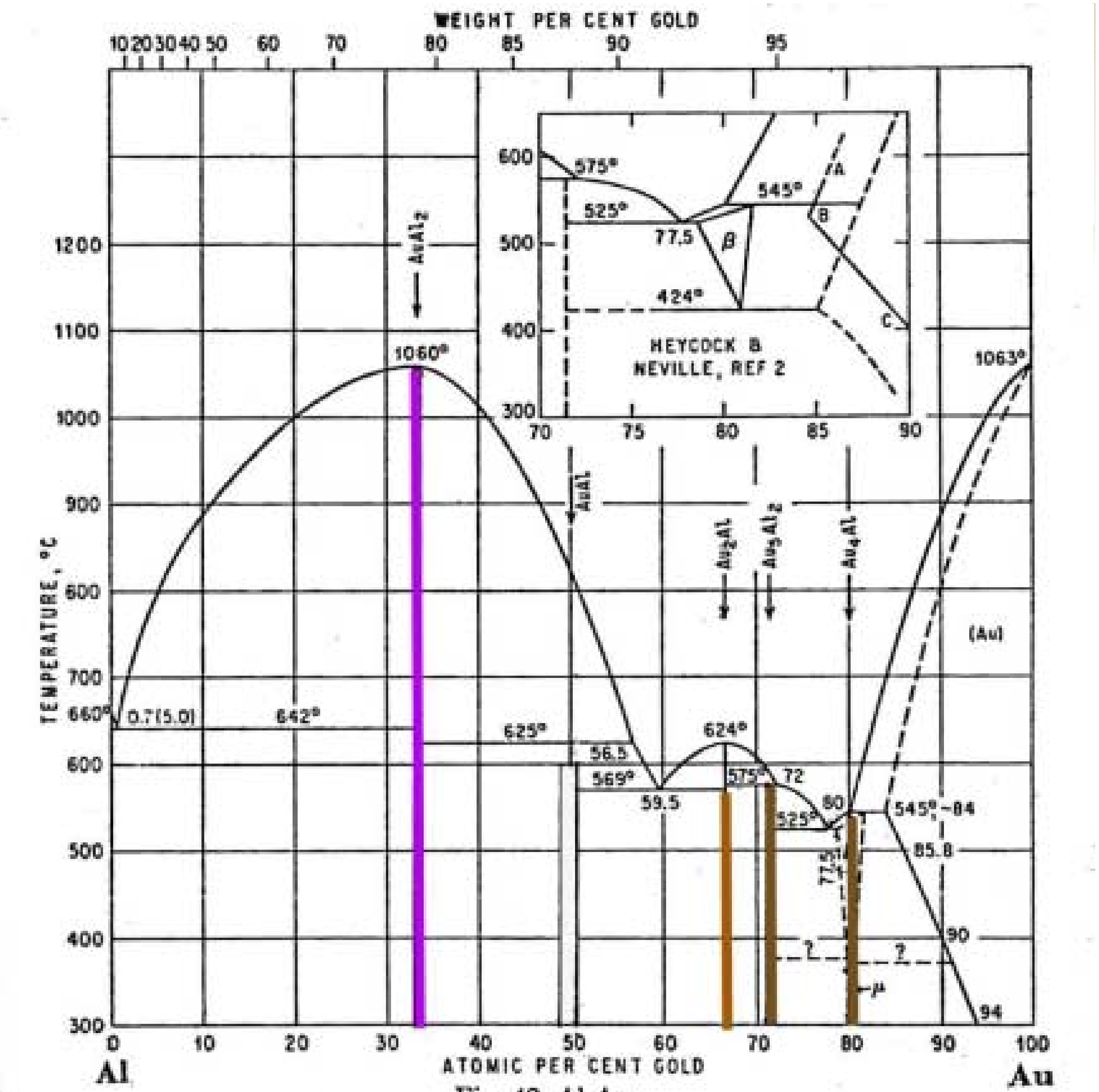
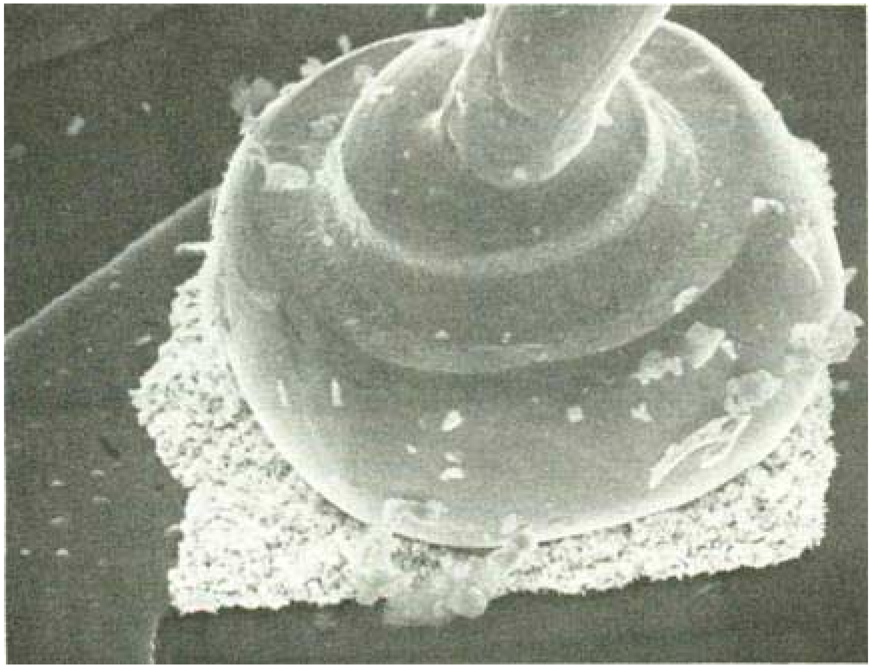


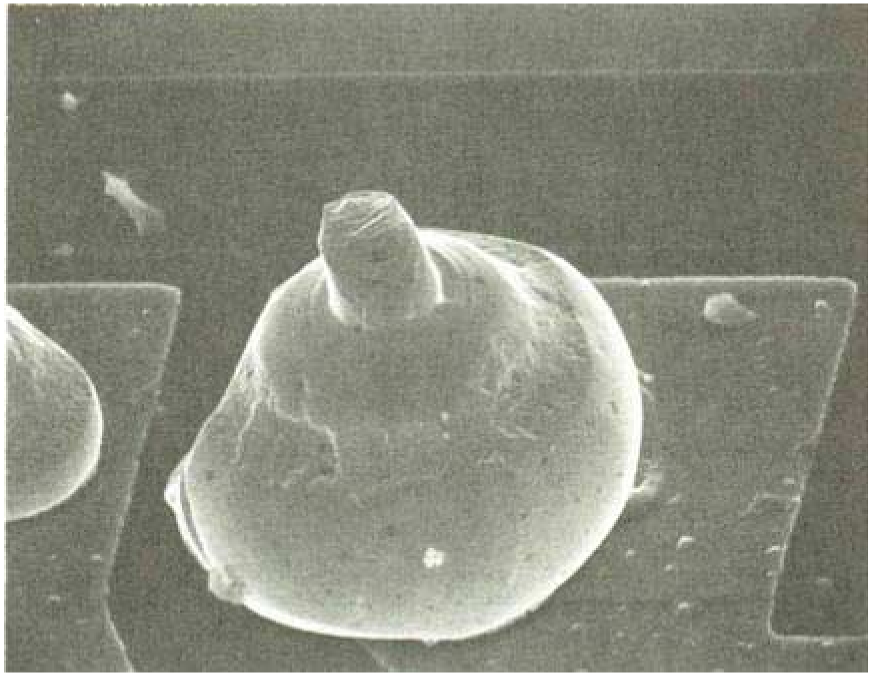
Fig. 42. Al-Au

HTE Possibilities for using H_2 Atmosphere for Au-ball Bonds on Al (Heated 400 °C for 1 hr), *but H_2 could leak to vacuum*) [Shia & Ficalora]

(also, Al bonds to Pd-doped thick film Au.)



Heated in Argon or Air

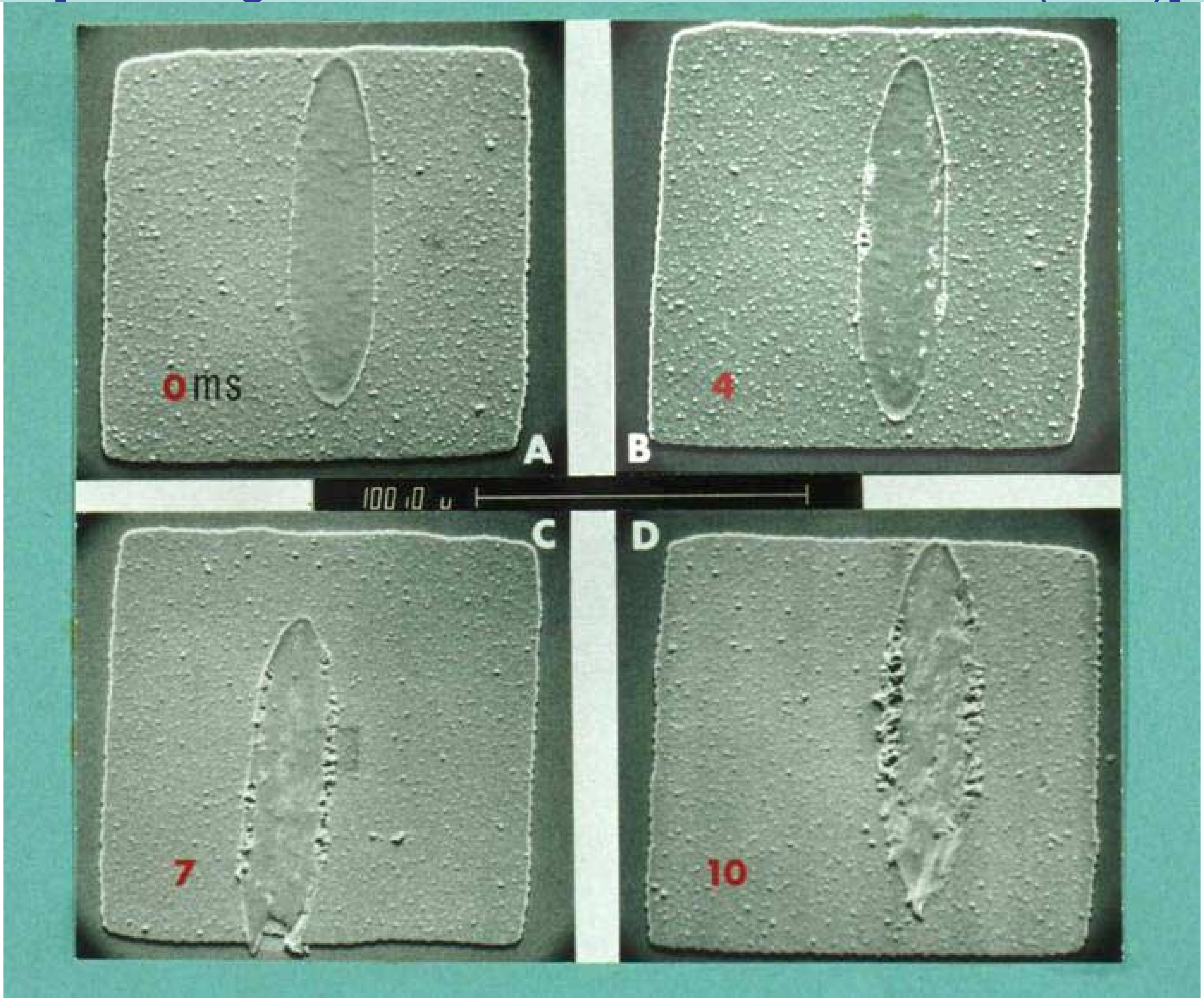


Heated in Hydrogen

All welds start as disconnected Microwelds

Al Wedge-Bond Initial Formation Process.

[Bonding Time indicated in Milliseconds (Red)]



Poorly made Au-Bond on Al-Pad, after 300˚C, 1-Hour Bake

Plague and Plague-Corrosion Failures

A) CLASSICAL FAILURES
  - a) High Electrical Resistance or Open Circuits
  - b) Weak Bond Adherence
  - c) Brittle Bond Heels

B) CONTAMINATION-INDUCED PLAGUE-LIKE FAILURES
  - a) Epoxy and other Organics
  - b) Halogens from Many Sources (cause corrosion)
    Cl, Fl, etc. can regenerate themselves after corroding Al

Corrosion at Low and at High Temperatures is Different from that in Normal Ambients

There is no liquid H_2O in either extreme environment (however, some Space environments [e.g., Mars] do cycle through the liquid H_2O zone! So normal corrosion is possible there-(2000 to 5000** ppm H_2O in hermetic package can cause Cl corrosion of an Au-Al interface on Mars or of Al metallization)-**NASA Specs—

- At Low Temperatures Chemical Reaction Rates Slow Down (by the Arrhenius relationship).

- In Both HTE & LTE, however, corrosive species (e. g., Cl, F, etc.) can react with Al to form chlorides, etc. **CLEAN! Remember, these are built in an Earth environment.**

The Mechanism of Chlorine Corrosion of AL

- **The corrosion mechanism consists of the adsorption of Cl^{-}** on the oxide-solution interface under the influence of an electric field (caused by the electric double layer at the oxide-solution interface and/or the galvanic couple of the bond) in competition with OH^{-} or H_2O molecules for surface sites on the hydrated oxide surface. This is followed by the formation of a basic hydroxychloride aluminum salt with aluminum oxide cations on the hydrated oxide surface:

- $Al(OH)3 + Cl^{-} \rightarrow Al(OH)_2 Cl + OH^{-}$. (1)

- Once the surface oxide is dissolved, the underlying Al reacts with the Cl^{-} by the equation

- $Al + 4Cl^{-} \rightarrow Al(Cl)_4^{-} + 3e^{-}$. (2)

- The $Al(Cl)_4$ will then react with the available water by the reaction

- $2AlCl_4^{-} + 6\ H2O \rightarrow 2Al(OH)_3 + 6H^{+}\ 8Cl^{-}$. (3)

- **This process liberates the Cl^{-} ion**, which is then available **to continue** the corrosion process via equations (1) and (2). In addition, the gold ball bond on aluminum produces a galvanic couple which can accelerate corrosion by acting as the driving force for the aluminum oxidation reaction. The region near the bond is an area of higher chloride ion concentration (compared to the overall surface) because of the reduction reaction of **Cl_2** by the gold electrode.

Electrochemical Series [Selected Reactions]
(can cause rapid electrochemical reactions)

<u>REACTION</u> **Standard Reduction <u>Potential (Volts)</u>**

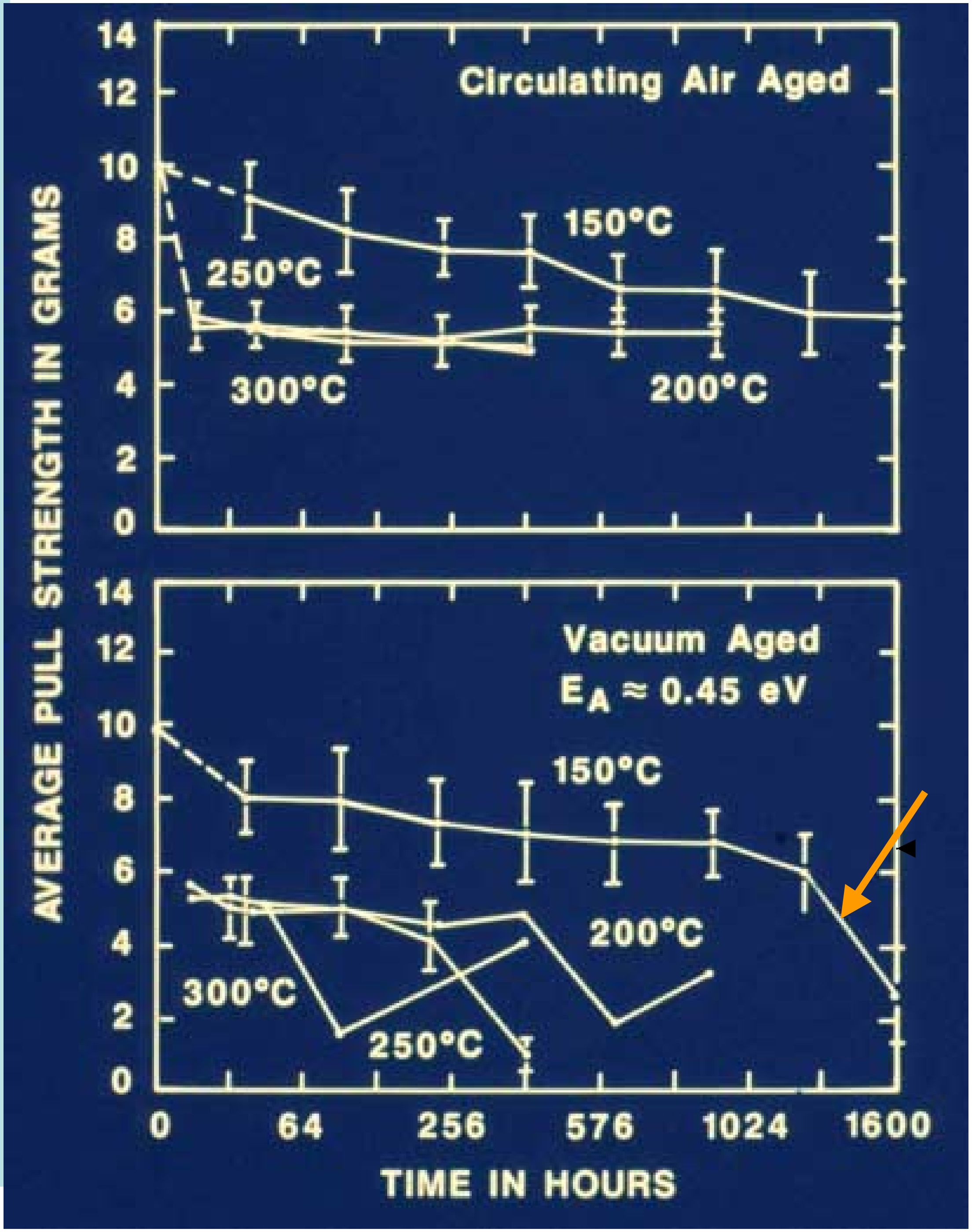
- $\mathrm{Au^{+} + e}$ ⌖ Au ---------------- 1.69
- $\mathrm{Au^{+++} + 2e}$ ⌖ $\mathrm{Au^{+}}$ ---------------- 1.4
- $\mathrm{AuCl_4^{-} + 3e}$ ⌖ $\mathrm{Au + 4\,Cl^{-}}$ ---------------- 1.0
- $\mathrm{Al^{+++} + 3e}$ ⌖ Al ----------------—1.66
- $\mathrm{Cu^{+} + e}$ ⌖ Cu ---------------- 0.52
- $\mathrm{Ag^{+++} + 2e}$ ⌖ $\mathrm{Ag^{+}}$ ---------------- 1.9
- $\mathrm{Ni^{++} + 2e}$ ⌖ Ni ----------------—0.26
- NOTE: THIS TABLE IS ONLY INDICATIVE.
- *The e-chem series is measured with respect to the potential of a standard hydrogen electrode. However, for bond pads, there may be* ***water*** *and especially* ***voltages*** *present, which can cause worst case reactions on chips*

Non Gold-Aluminum Interconnection Systems

1). Aluminum-copper
2). Gold-copper
3). Palladium-Aluminum or Gold
4). Aluminum-Nickel
5). Aluminum-Silver (bad news!)
6). Gold-Gold **(the best!)**

- Al-Al, Au-Ag, Noble Metal Combinations

Degradation (in Different Ambients) of Aluminum Wire Bonds on Copper with Temperature (note degredation in vacuum—**the Space environment!**)

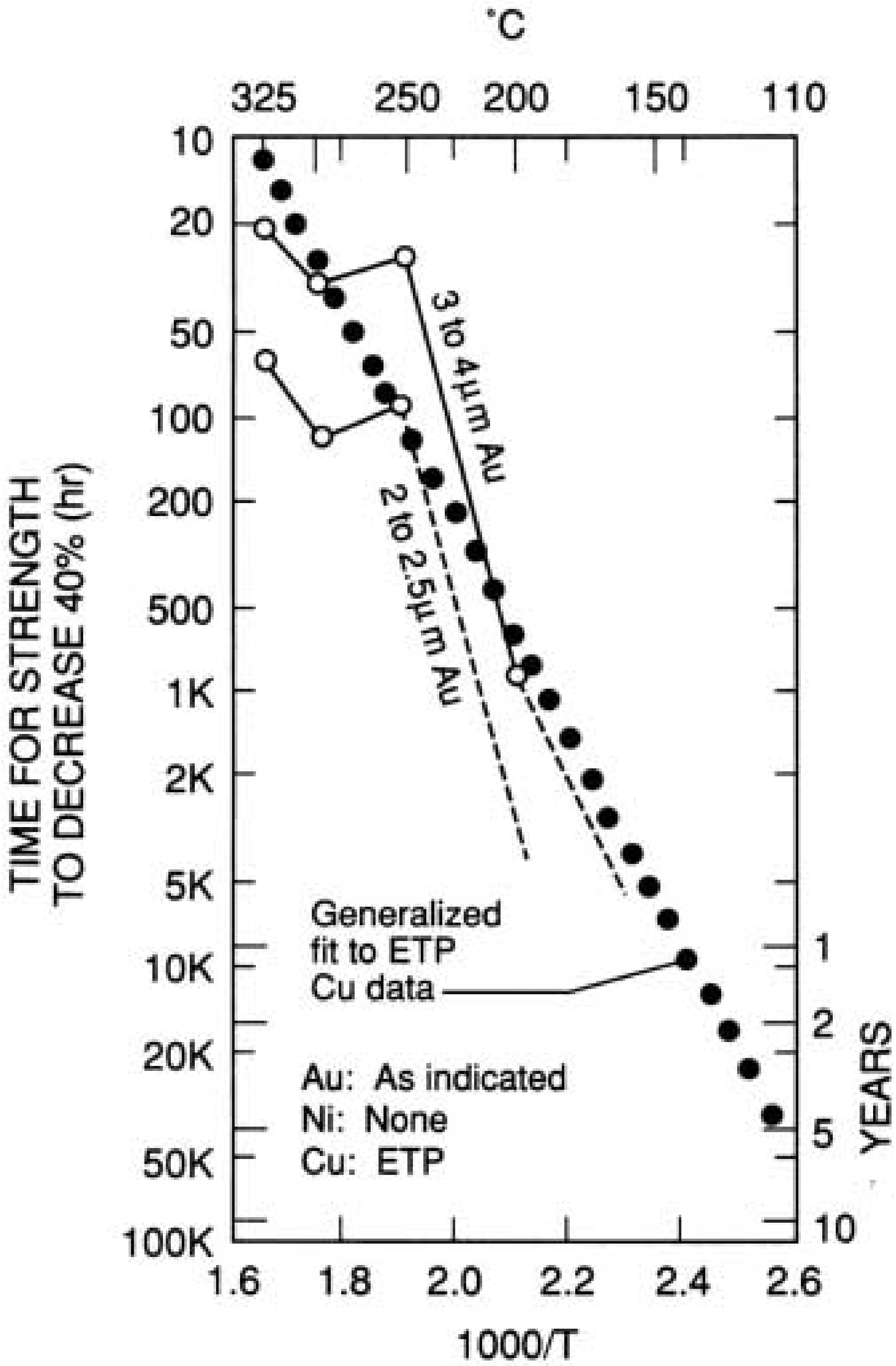


Reliability of the Gold-Copper Interface

Note: ***this metallurgy is not appropriate for long-term HTE***

Temperature Dependence of Time-to-Decrease Au-Cu Bond-strength 40% Below the as-bonded Strength.

(The dotted line ●● is the generalized fit to the data. After Hall, et. al.)



THE PALLADIUM—GOLD and—ALUMINUM WIRE BOND SYSTEM

Uses

1. Au-Ball and Al-Wedge Bonding to Pd-Plated Lead Frames & Packages.

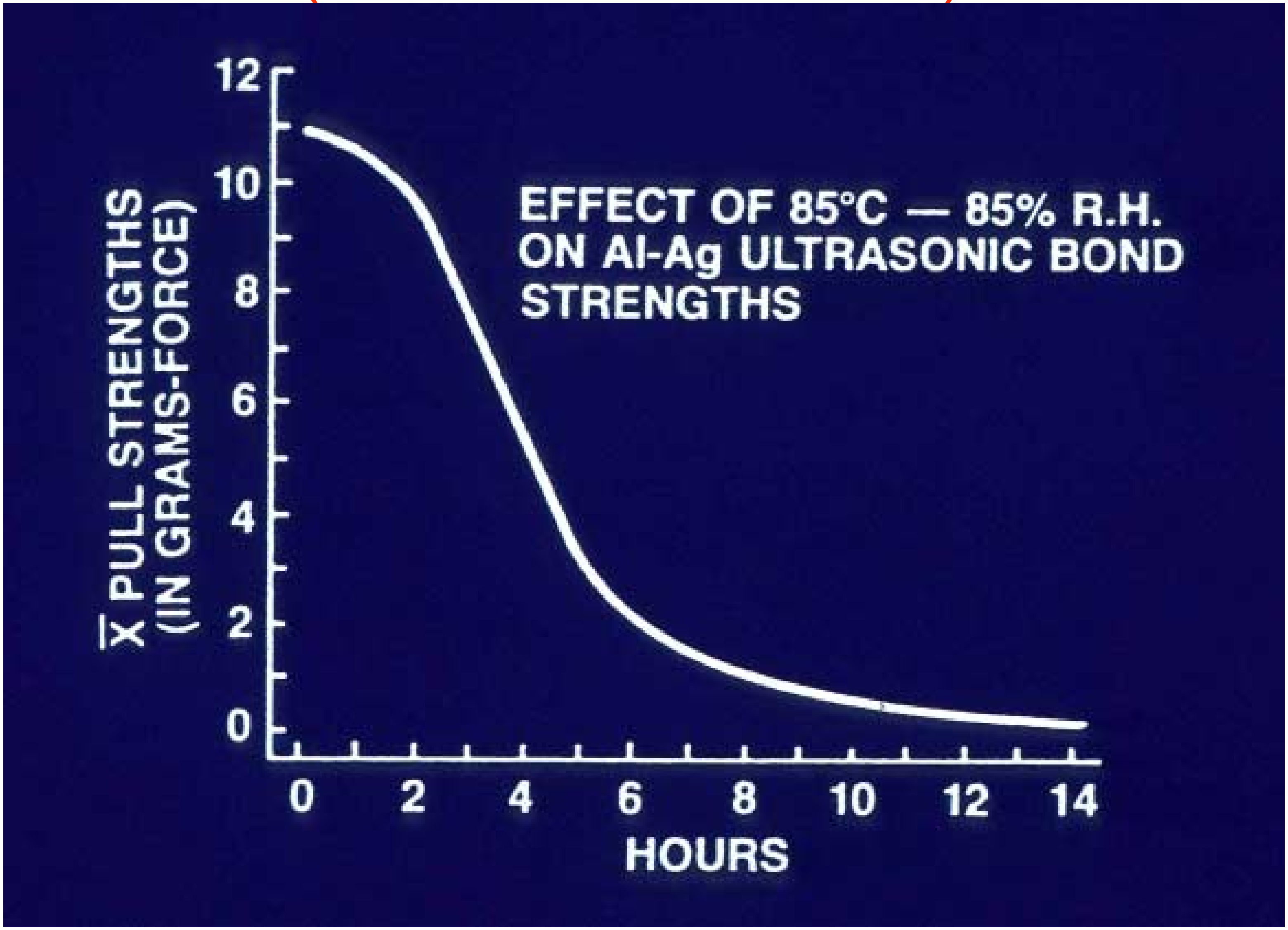
Advantages

1. Pd (0.076 µm—3µ") is Plated Over Ni (1.5µm—60µ") to Cu Leadframes.
2. Gold-Crescent, and Aluminum-Wedge Bonds to Thin Palladium Films are Reported to Have NO Bond Reliability Problems. (Some Fine Pitch Solderability Bridging Problems are Reported.)
3. Pd Has High Surface Free Energy—Good Adhesion

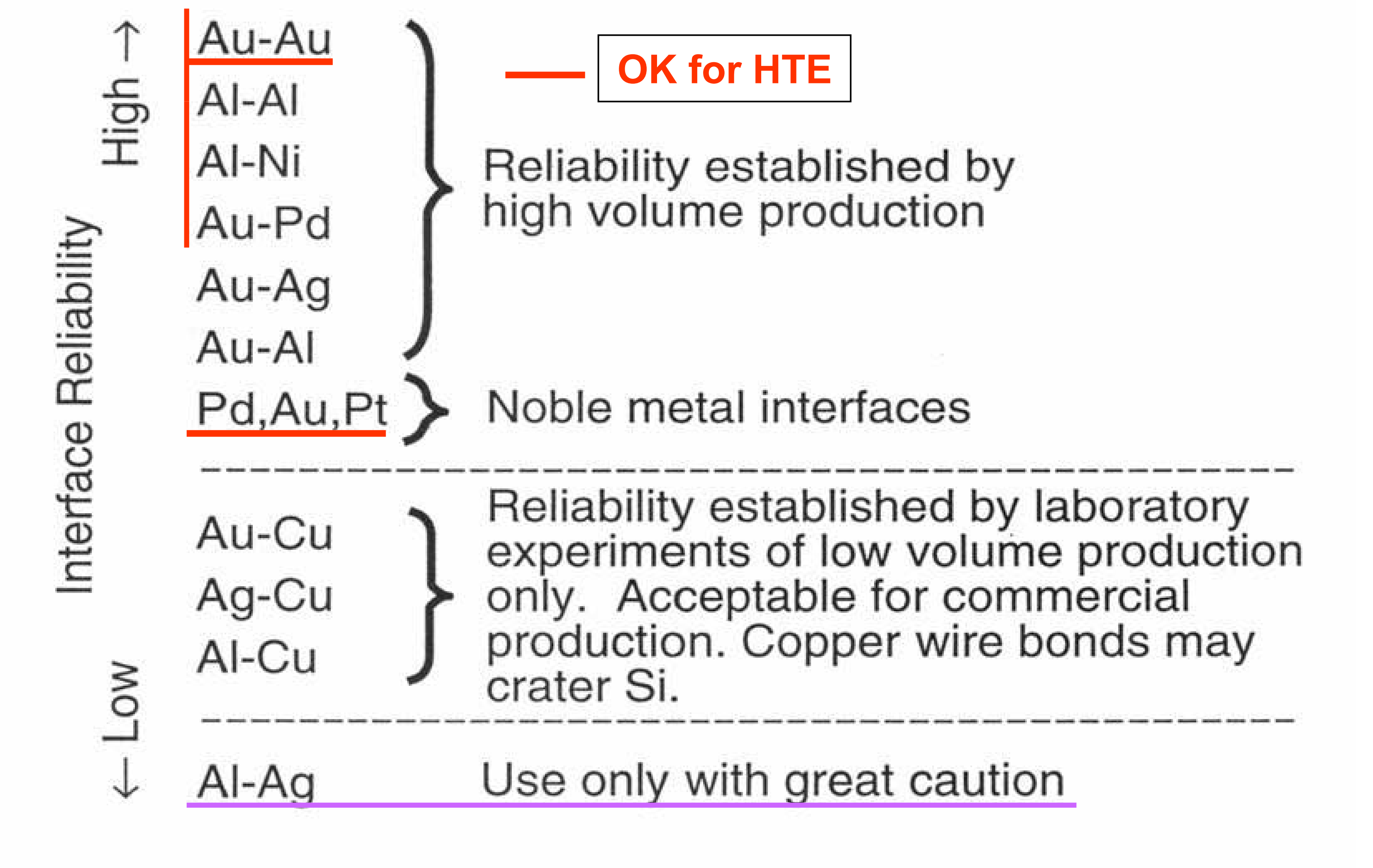
- ____________

Decrease in Pull Strength of the Ag-Al Bond during Temperature-Humidity testing

(Do not use for HTE!)



All Interfaces OK for LTE, RED OK for HTE



OK for HTE

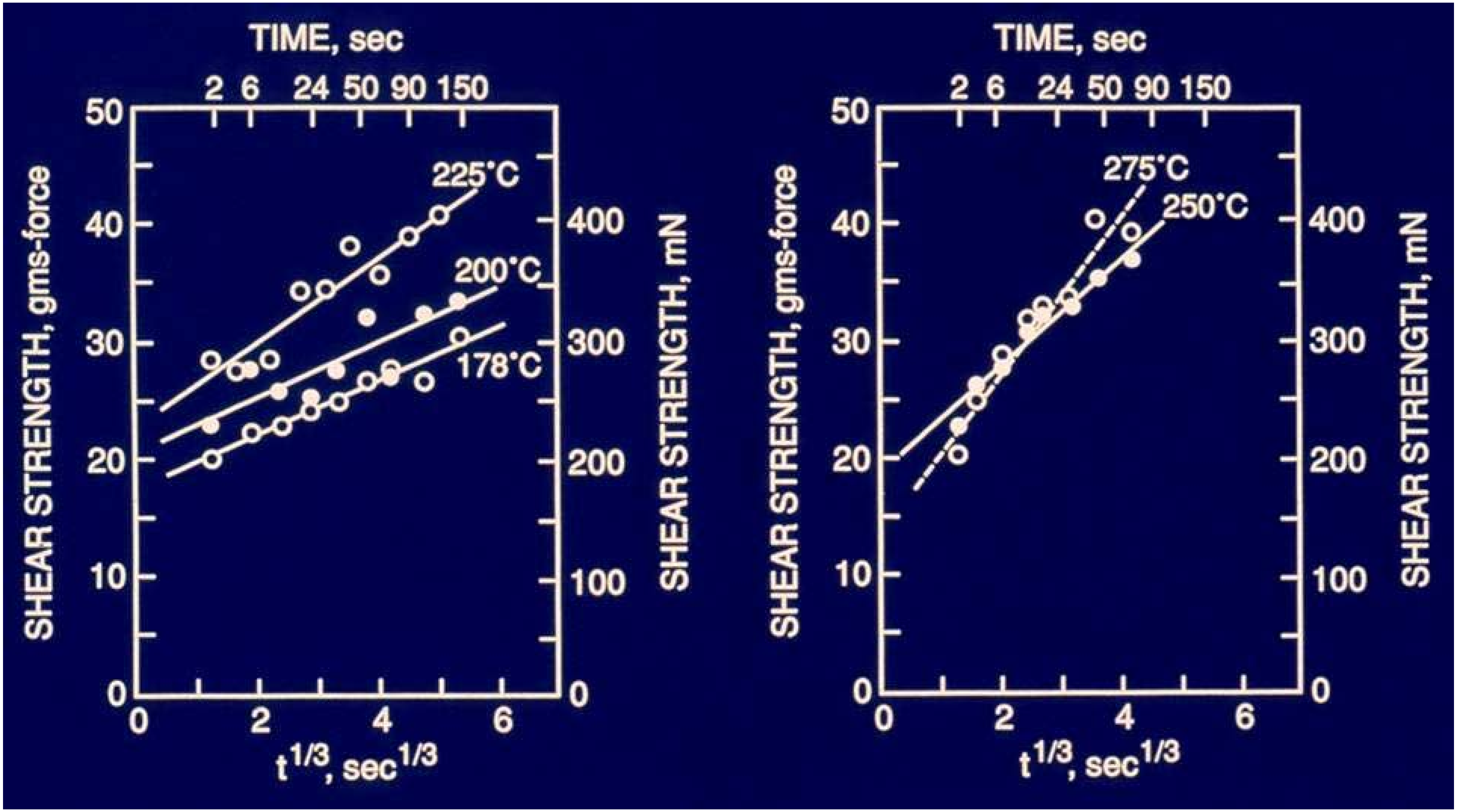
Interface Reliability

High ↑

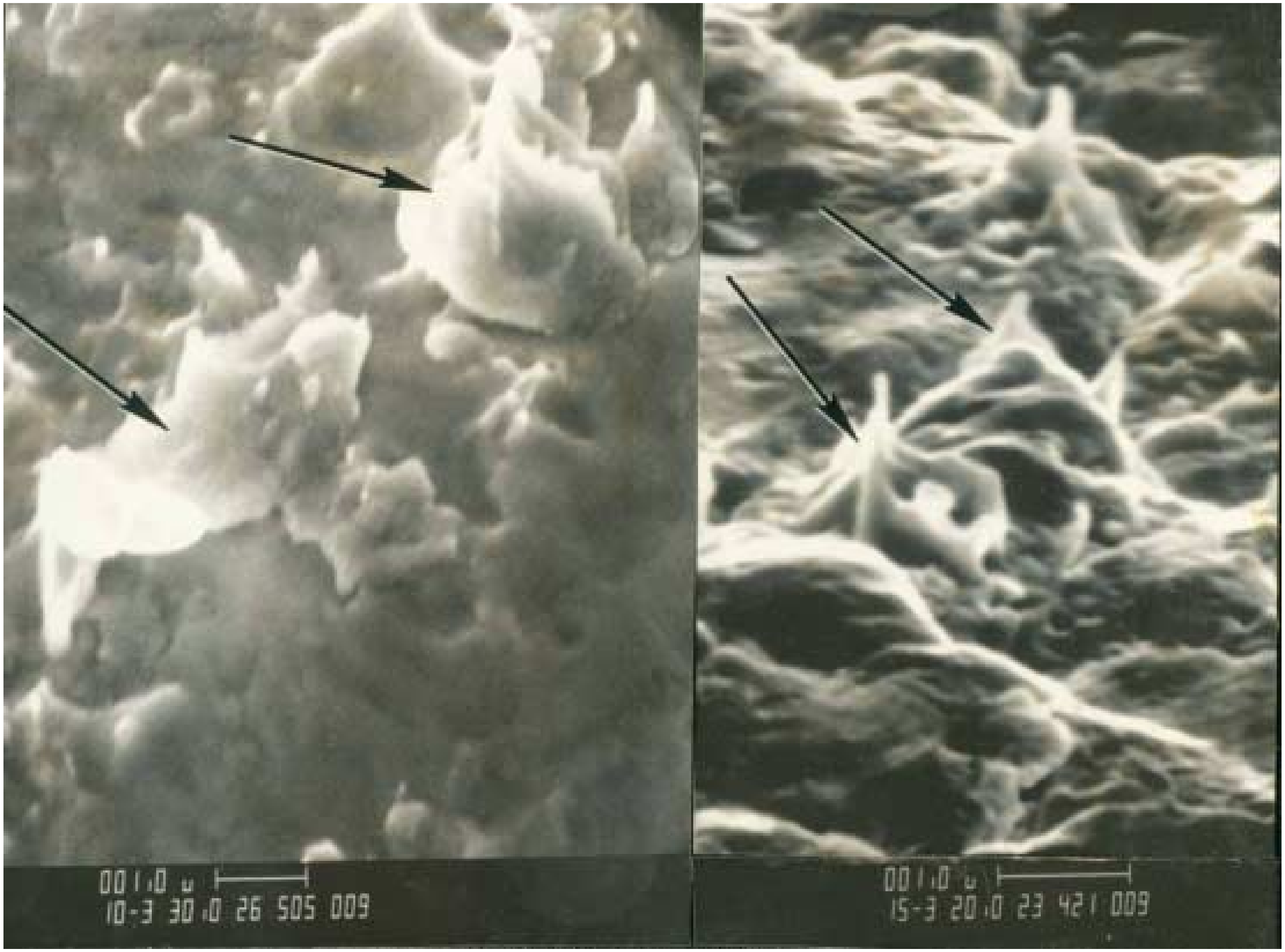
Au-Au	Reliability established by high volume production
Al-Al	
Al-Ni	
Au-Pd	
Au-Ag	
Au-Al	
Pd,Au,Pt	Noble metal interfaces
Au-Cu	Reliability established by laboratory experiments of low volume production only. Acceptable for commercial production. Copper wire bonds may crater Si.
Ag-Cu	
Al-Cu	
Al-Ag	Use only with great caution

Low ↓

Organic Contaminated Gold-Gold Bond-Interface-Strength Improves with Post-bond Heat Treatment



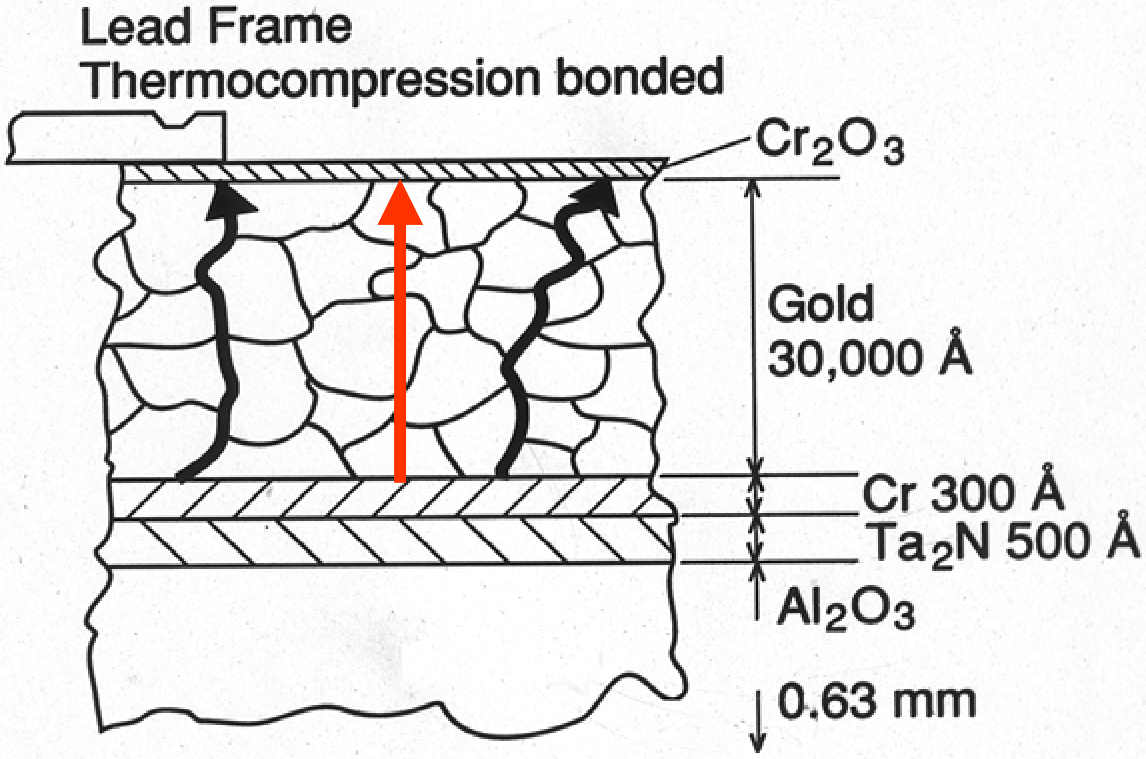
Microwelds on Failed Gold-gold Bond Interfaces: (Au Interfaces with **inorganic** oxide contaminants improve minimally with temp/time)



How do Inorganic Contaminants get on Au Surfaces

Grain Boundary →, and ***Bulk*** →

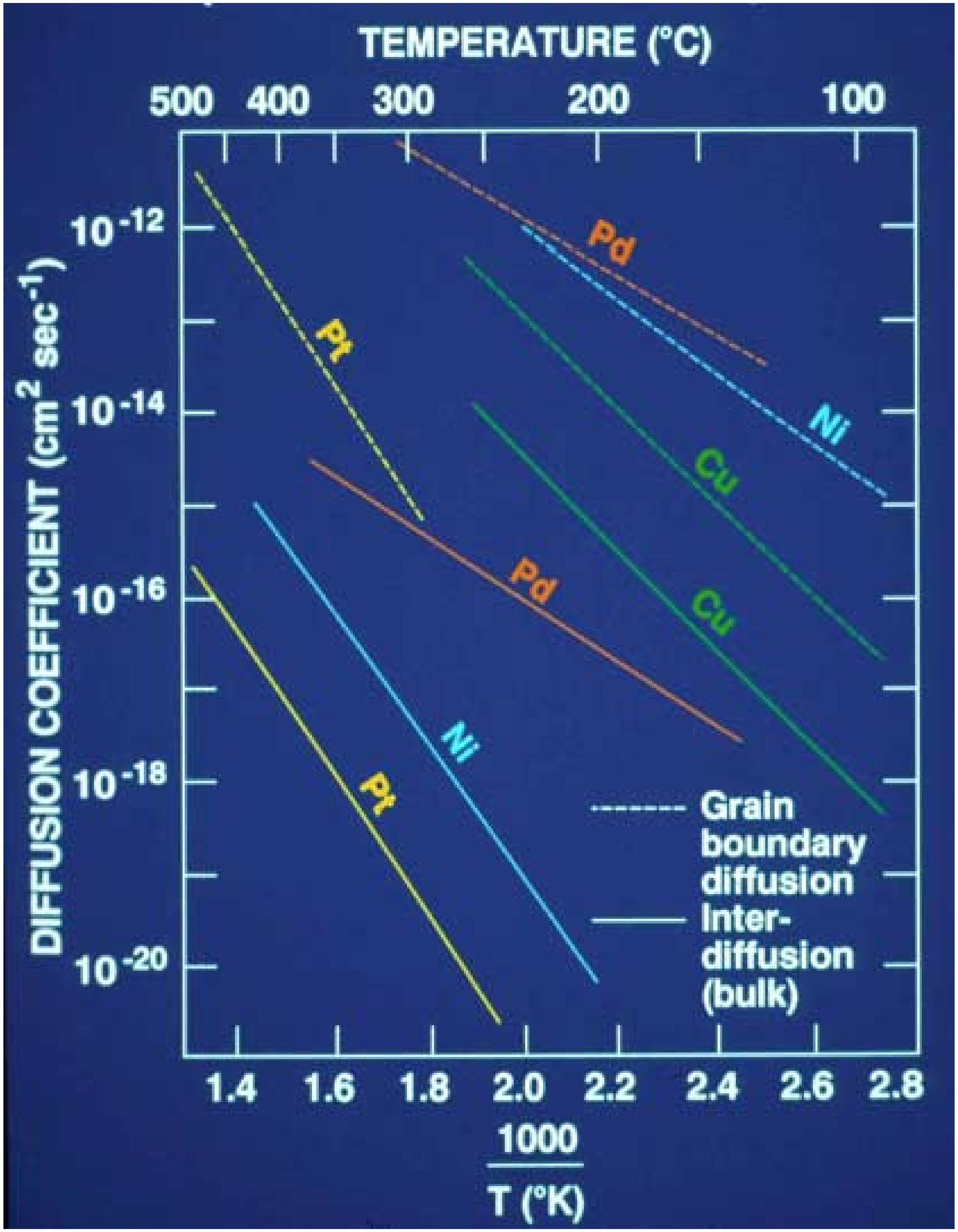
(Diffusion up Through Gold)



Hybrid microcircuit geometry with Cr_2O_3 layer on the surface.
The arrows indicate possible diffusion paths.
(after Nelson & Holloway)

An Arrhenius Plot of Diffusion Coefficients for Metal Couples with Gold as the Top Layer, (demonstrating how much faster grain boundary diffusion is- compared to bulk).

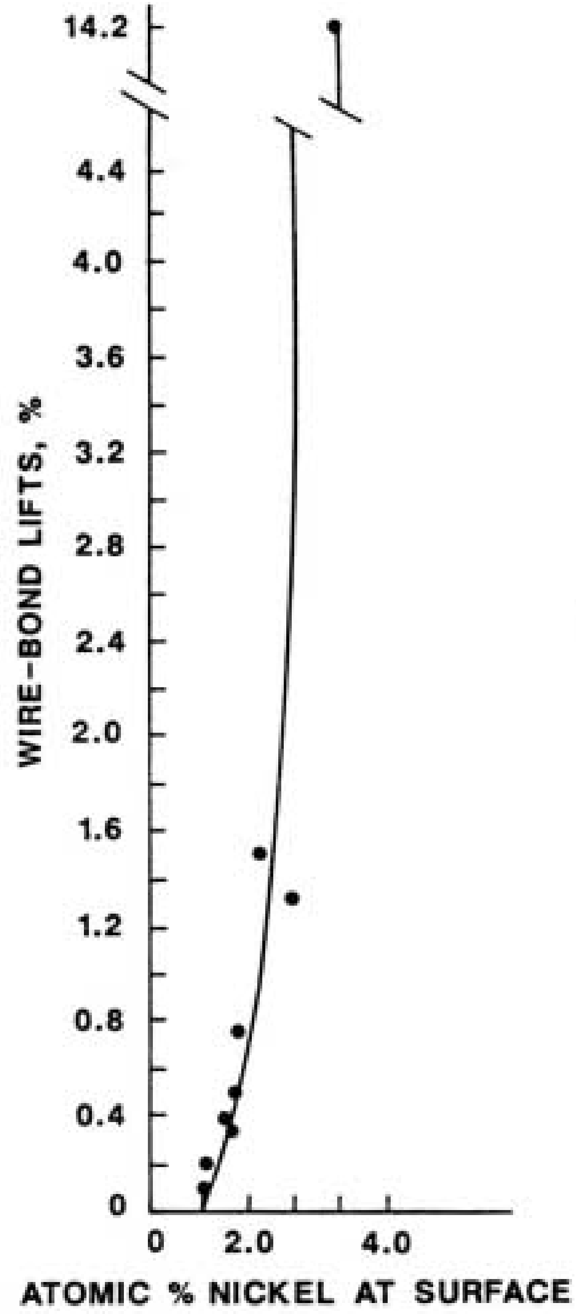
(After Hall)



The Decrease of Au Bondability to Surfaces Contaminated with Soft Oxides (Ni, Cu, etc.)

- Thermocompression Gold Wire-Bond Lifts *vs.* Auger Atomic Percent of Nickel

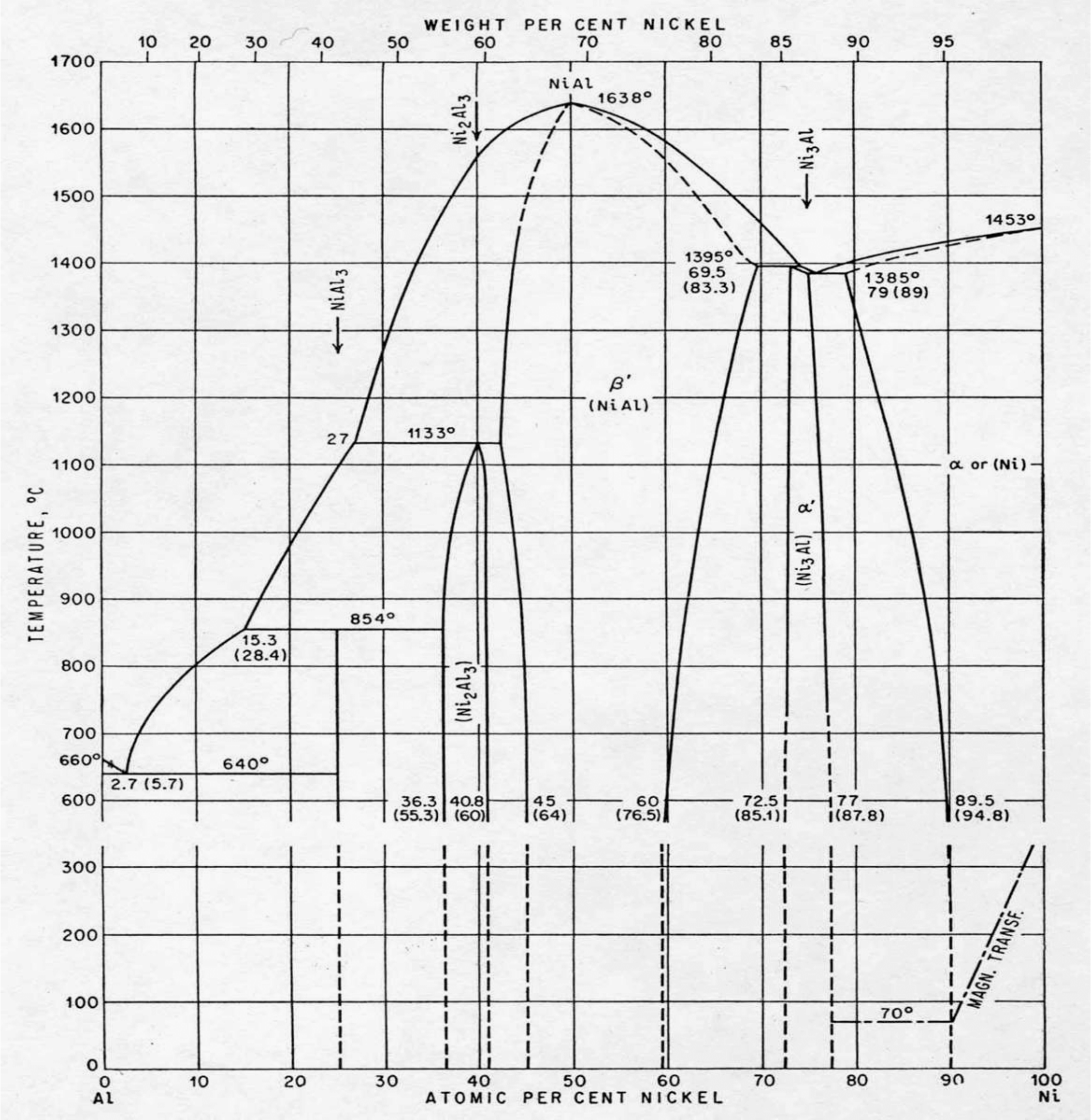
  (as oxide) on the Plated Gold Surface



Nickel-Aluminum Phase Diagram

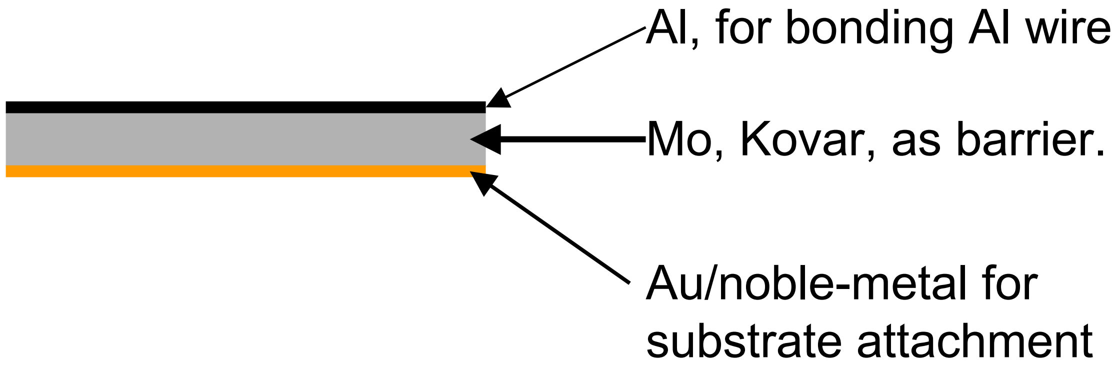
(Note the high temperature melting-point intermetallics)

Al-Ni interfaces have demonstrated reliability for >100 hr at 300 °C with only a 1% increase in interface resistance. (Palmer)



Some Alternatives to Normal Wire Bonding for Interconnecting High-Frequency, High-Temperature Devices Using Barriers

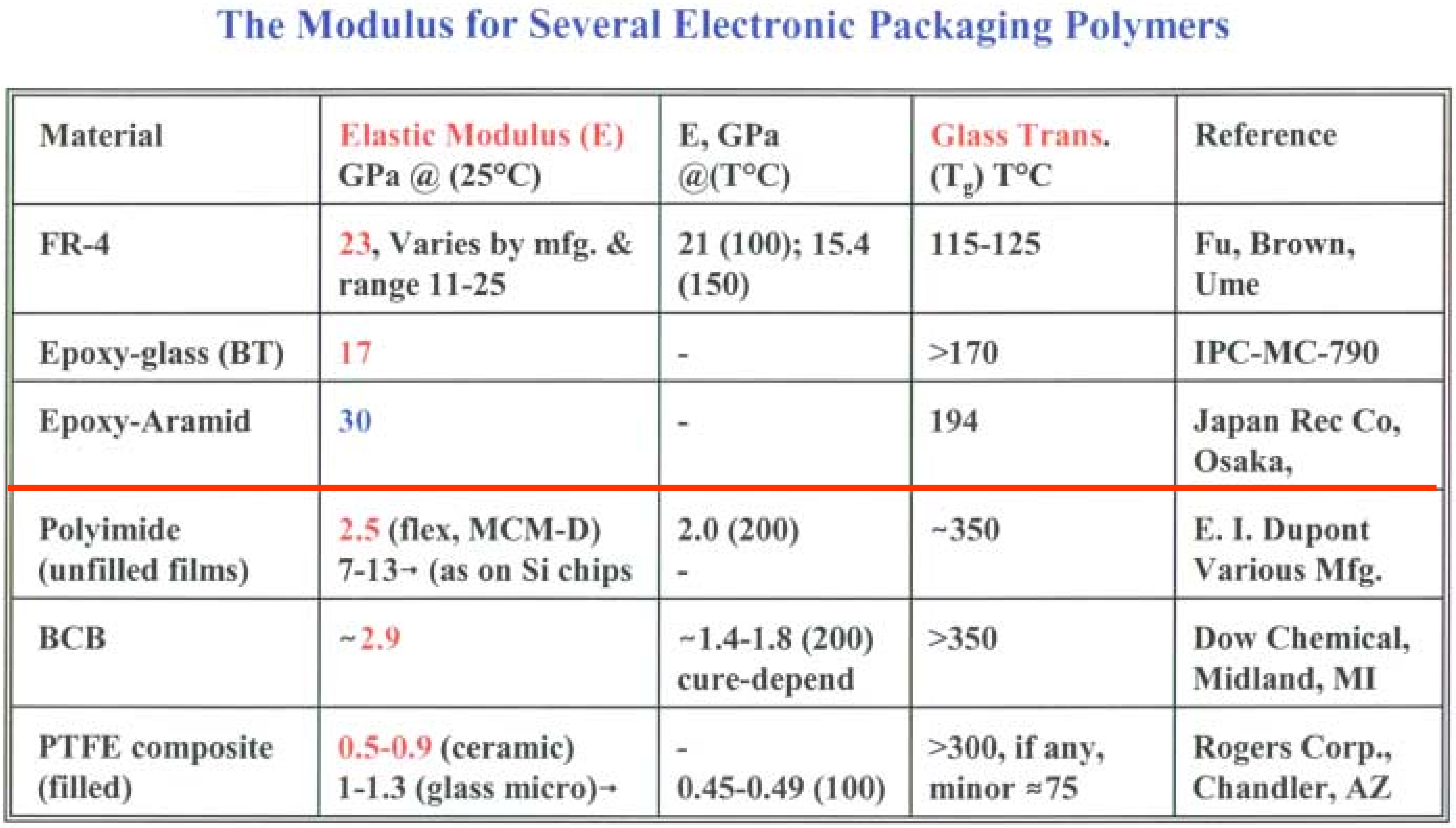
- Thermosonic or Thermocompression Au Ribbon-Wire
- Stud/ball-bumps, flip-chipped and TC Bonded to Noble Metal Pads on high Temperature Substrates
- Using Au/Ta/Al on chips, moly-tabs, or other tri-metallic barriers to avoid diffusion/intermetallics (TC bonded to thick-film Au).>300 ºC for hundreds of hours.
- **Example:**



Al, for bonding Al wire

Mo, Kovar, as barrier.

Au/noble-metal for substrate attachment



The Modulus for Several Electronic Packaging Polymers

Material	Elastic Modulus (E) GPa @ (25°C)	E, GPa @(T°C)	Glass Trans. (T_g) T°C	Reference
FR-4	23, Varies by mfg. & range 11-25	21 (100); 15.4 (150)	115-125	Fu, Brown, Ume
Epoxy-glass (BT)	17	-	>170	IPC-MC-790
Epoxy-Aramid	30	-	194	Japan Rec Co, Osaka,
Polyimide (unfilled films)	2.5 (flex, MCM-D) 7-13→ (as on Si chips	2.0 (200) -	~350	E. I. Dupont Various Mfg.
BCB	~2.9	~1.4-1.8 (200) cure-depend	>350	Dow Chemical, Midland, MI
PTFE composite (filled)	0.5-0.9 (ceramic) 1-1.3 (glass micro)→	- 0.45-0.49 (100)	>300, if any, minor ≈75	Rogers Corp., Chandler, AZ

Materials below red line may be considered for HTE—problems of metal adhesion? Outgassing not resolved?

Low Dielectric Constant Materials with Tg>350ºC (weight loss at 425 ºC, 8 hours-available)

<400C
>450 C

>350 C

450 C

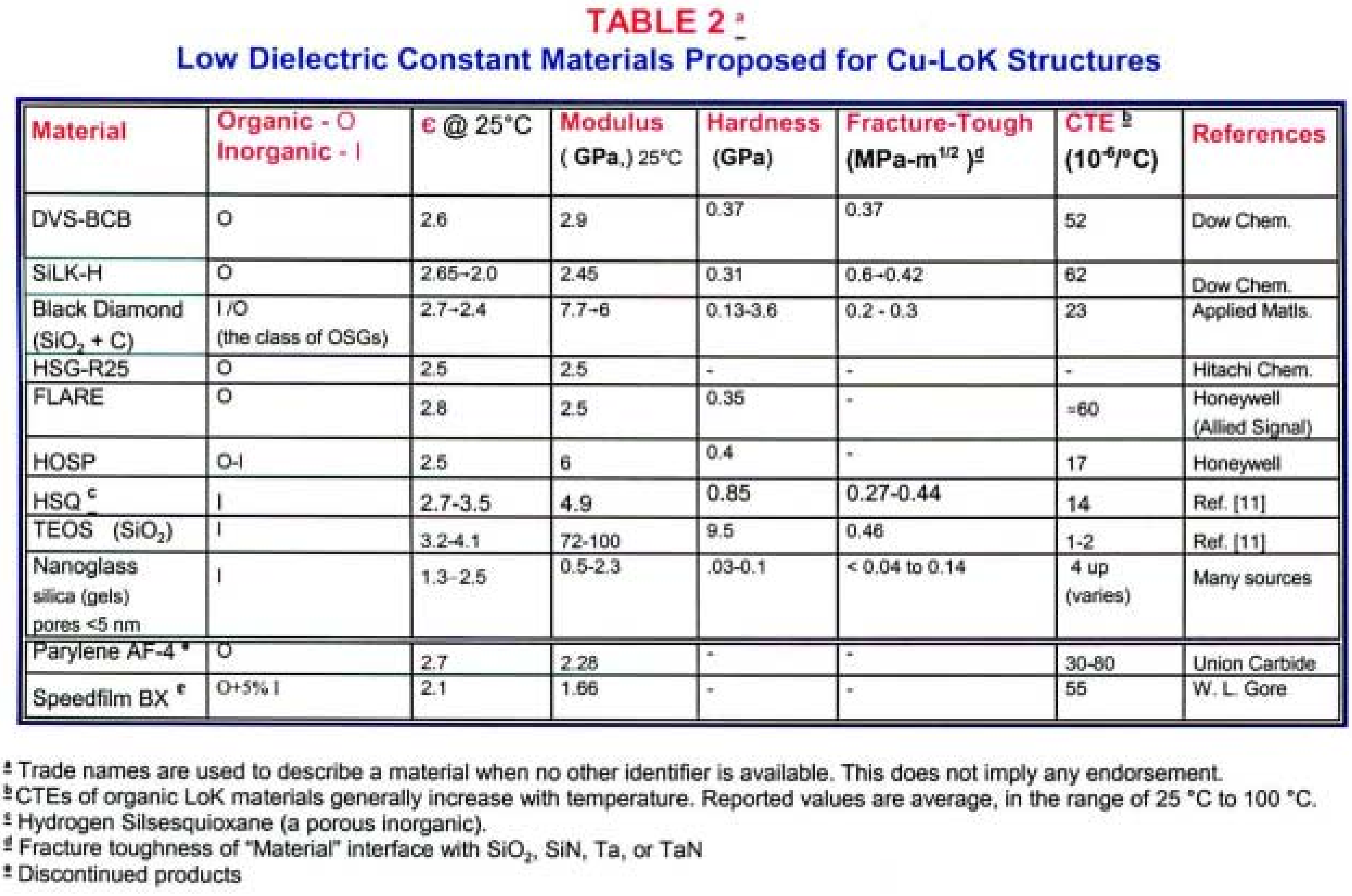


TABLE 2 [a]

Low Dielectric Constant Materials Proposed for Cu-LoK Structures

Material	Organic - O Inorganic - I	ε @ 25°C	Modulus (GPa,) 25°C	Hardness (GPa)	Fracture-Tough (MPa-m$^{1/2}$)[d]	CTE [b] (10^{-6}/°C)	References
DVS-BCB	O	2.6	2.9	0.37	0.37	52	Dow Chem.
SiLK-H	O	2.65→2.0	2.45	0.31	0.6→0.42	62	Dow Chem.
Black Diamond (SiO_2 + C)	I /O (the class of OSGs)	2.7→2.4	7.7→6	0.13-3.6	0.2 - 0.3	23	Applied Matls.
HSG-R25	O	2.5	2.5	-	-	-	Hitachi Chem.
FLARE	O	2.8	2.5	0.35	-	≈60	Honeywell (Allied Signal)
HOSP	O-I	2.5	6	0.4	-	17	Honeywell
HSQ [c]	I	2.7-3.5	4.9	0.85	0.27-0.44	14	Ref. [11]
TEOS (SiO_2)	I	3.2-4.1	72-100	9.5	0.46	1-2	Ref. [11]
Nanoglass silica (gels) pores <5 nm	I	1.3-2.5	0.5-2.3	.03-0.1	< 0.04 to 0.14	4 up (varies)	Many sources
Parylene AF-4 [e]	O	2.7	2.28	-	-	30-80	Union Carbide
Speedfilm BX [e]	O+5% I	2.1	1.66	-	-	55	W. L. Gore

[a] Trade names are used to describe a material when no other identifier is available. This does not imply any endorsement.

[b] CTEs of organic LoK materials generally increase with temperature. Reported values are average, in the range of 25 °C to 100 °C.

[c] Hydrogen Silsesquioxane (a porous inorganic).

[d] Fracture toughness of "Material" interface with SiO_2, SiN, Ta, or TaN

[e] Discontinued products

Common Si, GaN, & SiC Ohmic Metallizations

Silicon:

Gold Finish: Gold-silicon eutectic, Gold-germanium eutectic
- Chromium-gold, Aluminum-chromium-gold
- Chromium-nickel-gold, Titanium-nickel-silver-gold
- Electroless nickel-gold

Silver Finish: Chromium-silver, Titanium silver, Titanium-nickel-Ag
- Aluminum-titanium-nickel-silver (Ag generally bad for HTE-silver migration??, but Silver glass OK?)

Nickel Finish: Titanium-nickel, Electroless nickel OK for HTE

Gallium Nitride: Al/Ti, Al/Ni/Al/Ti, ZnN/Zr, Pd,/Au

Silicon Carbide: Ni/Ti/$TaSi_2$, Ti/$TaSi_2$/Pt, Ni/Ti/Pt/Au

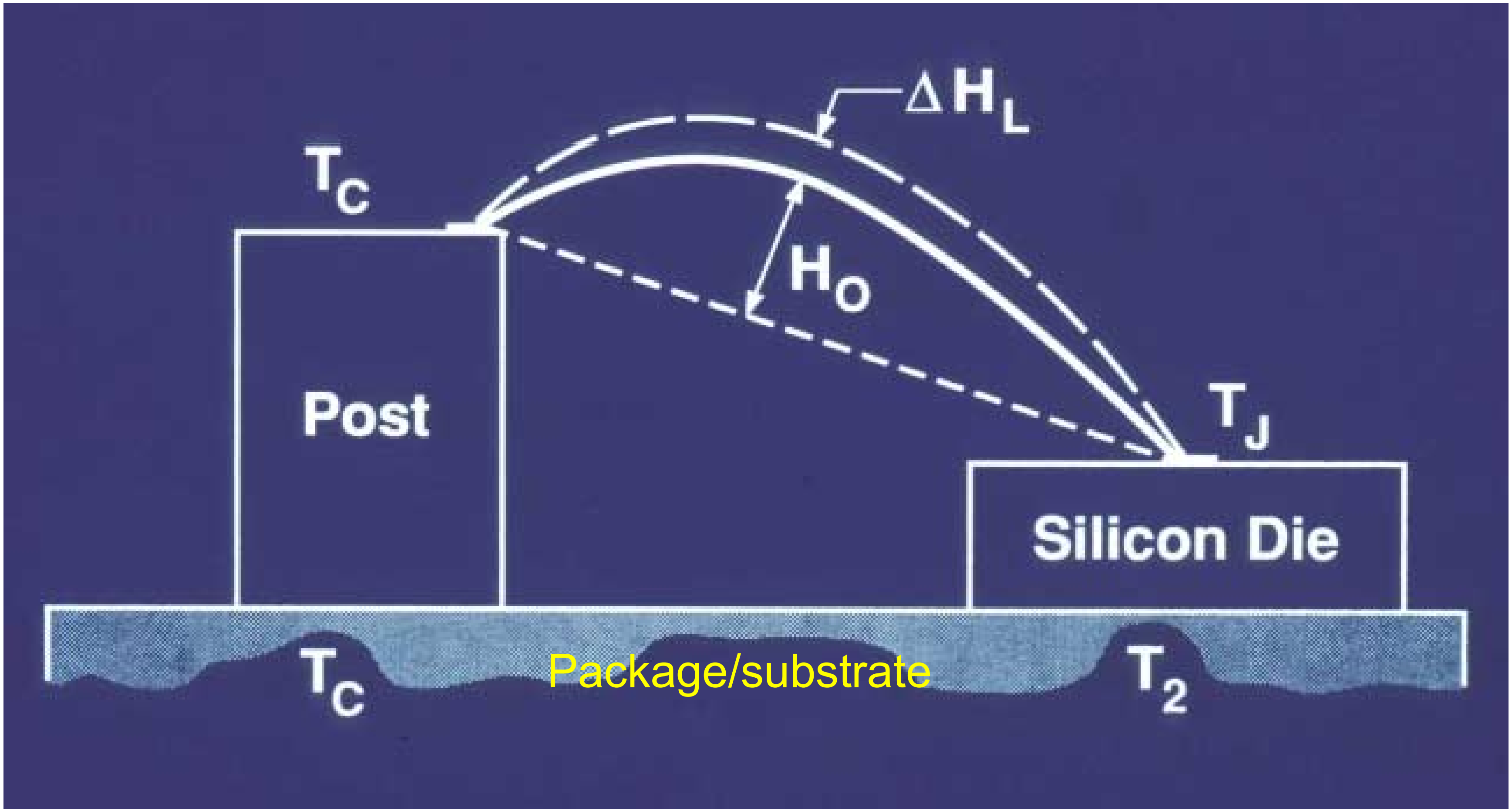
WIRE BOND FATIGUE FAILURES

- **1) THERMAL and or POWER CYCLING**
- a) In Open packages
- b) In Plastic Encapsulation
- 2) **EXTERNAL VIBRATION** (open cavity packages)
- a) Ultrasonic Cleaner Damage
- b) Shock/vibration--Long Wires on 3D Packages (NASA)

Fatigue of Wire Bonds Will Occur During Large ΔT Temperature / power-cycling in both HTE and LTE, which is bad on Mars (-120 to 85 °C), but with low frequency.

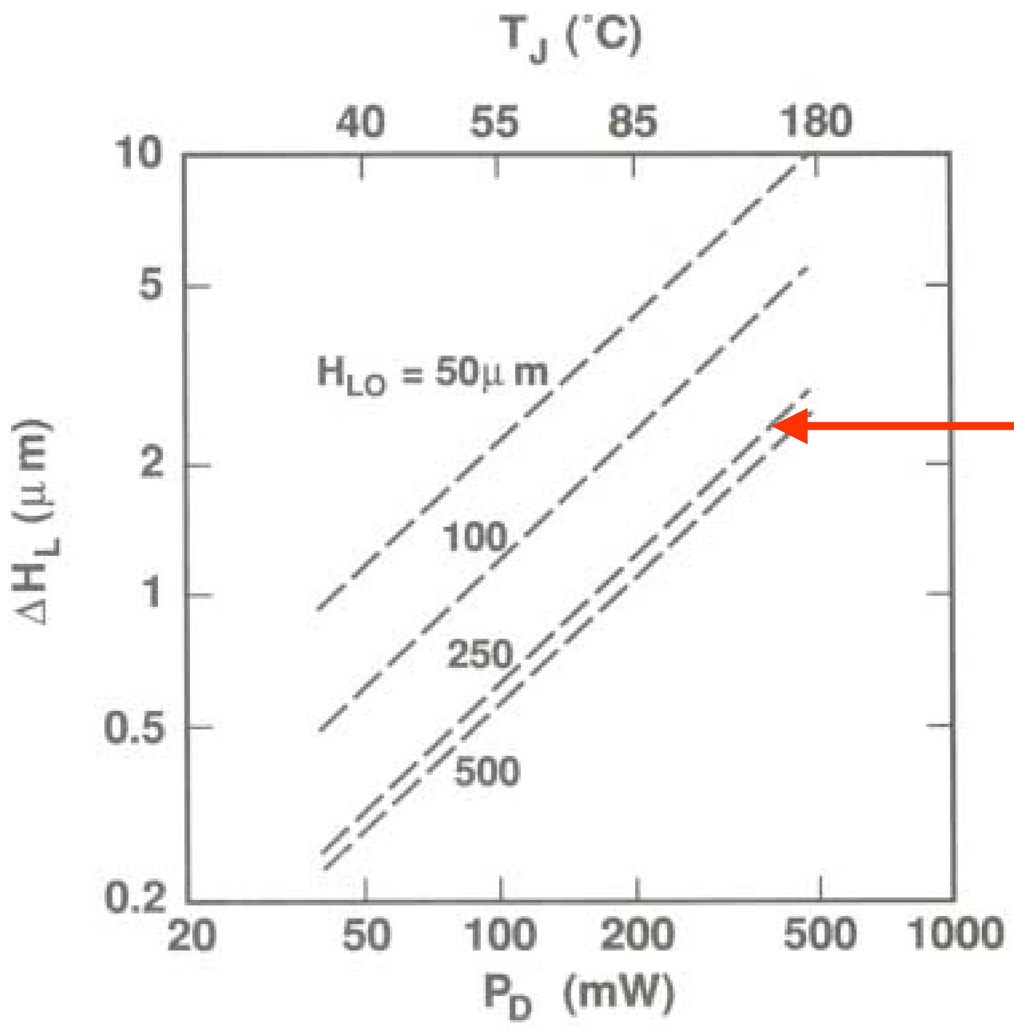
Wire diameter, shape, loop height, and metallurgy determine fatigue susceptibility, and extent.

Schematic of Wire Bond Flexure During Thermal/power Cycling



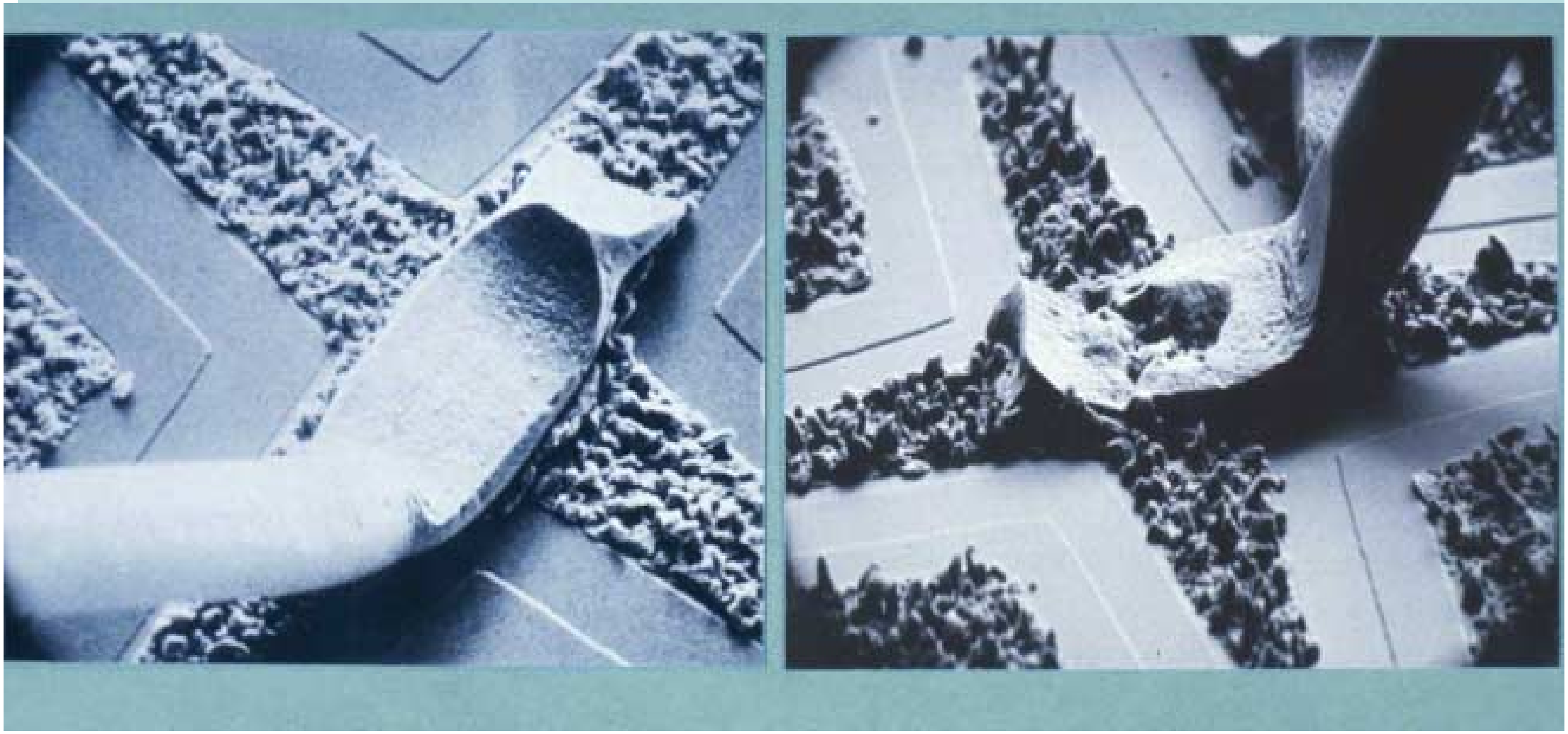
The Effect of Loop Height on Fine Wire (25-50 µm) Flexing During Power Cycling

High loops minimize flexing (ΔH) and increase reliability

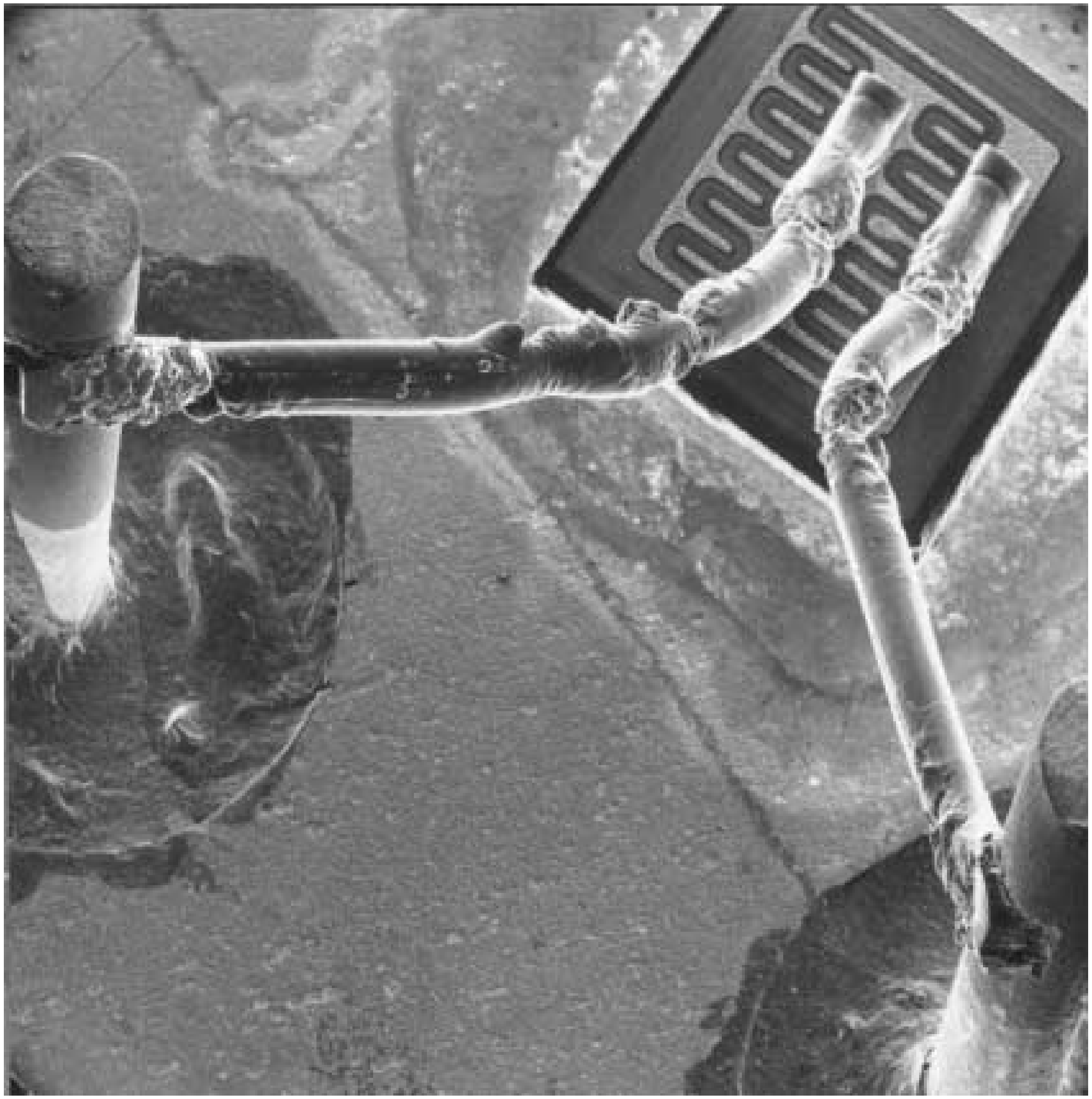


Highest Loops

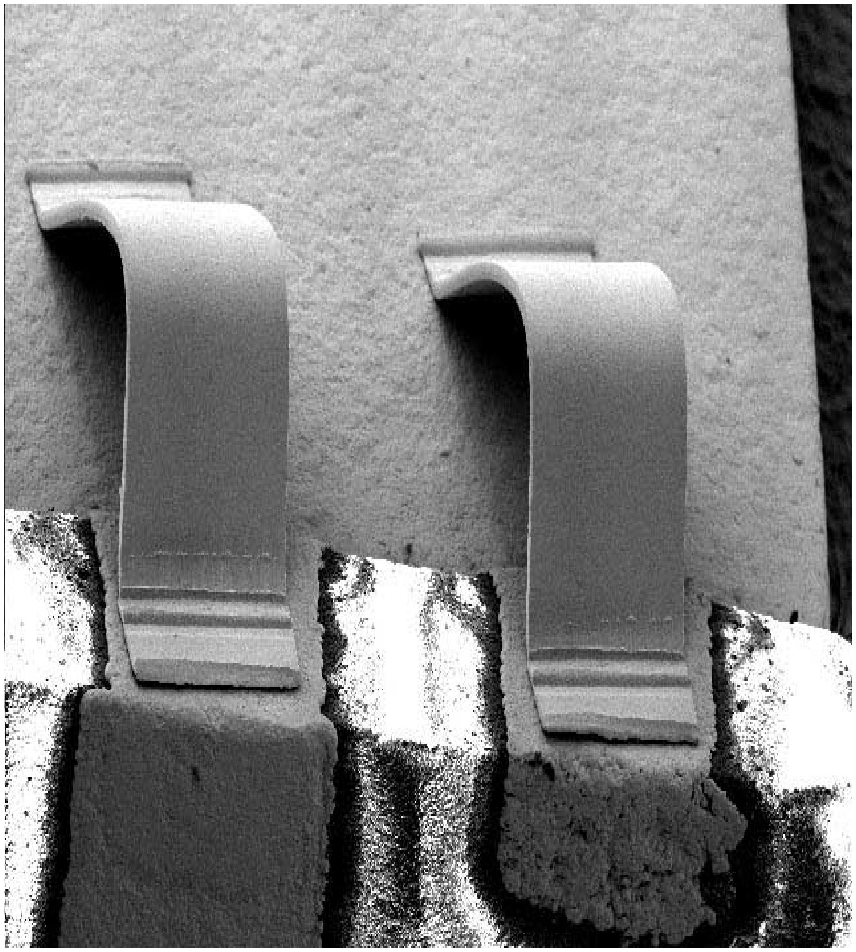
Al Wedge Bonds (made with high loops) that had Undergone 76,000 Power Cycles without Electrical Failure (Surface reconstruction is evident on the device metallization)

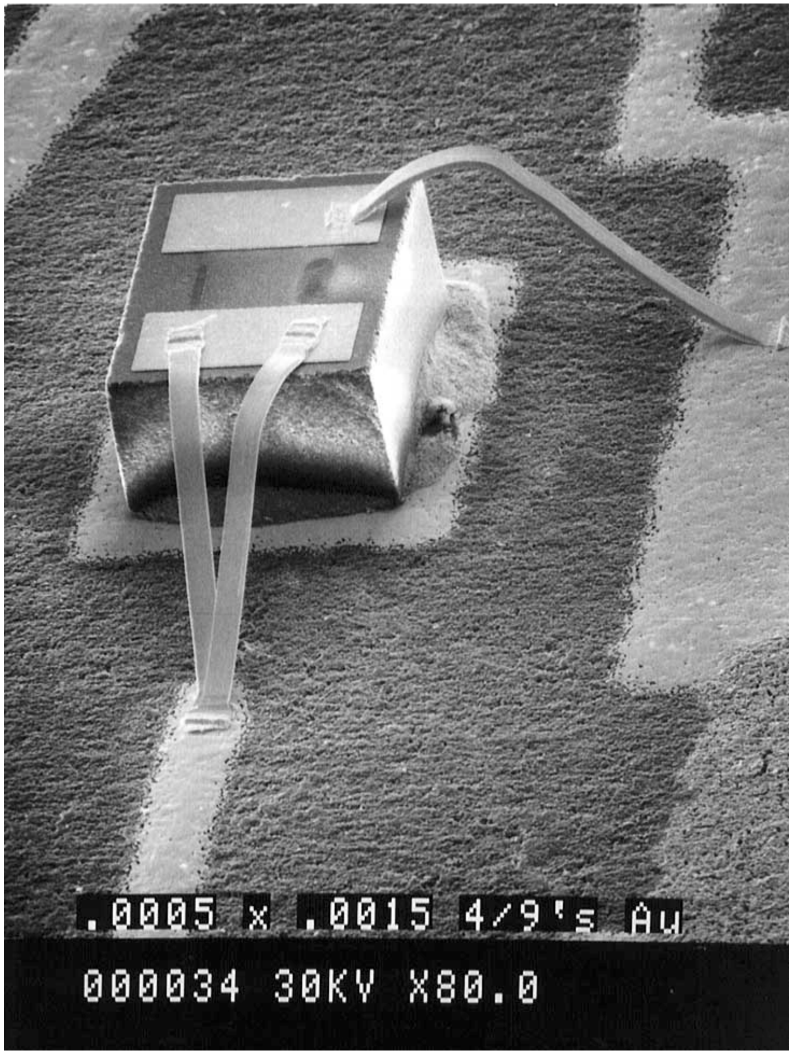


Fatigue of Large (200 µm) Al Wire after Undergoing 18,000 On-off Power Cycles

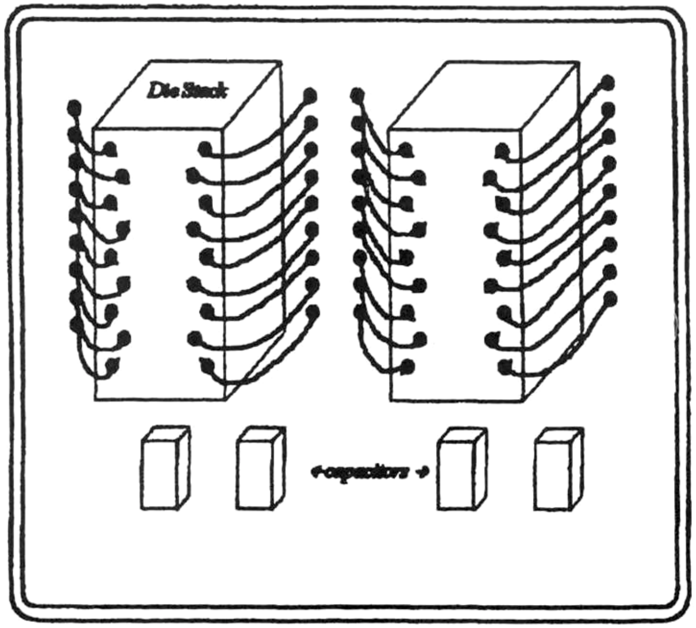


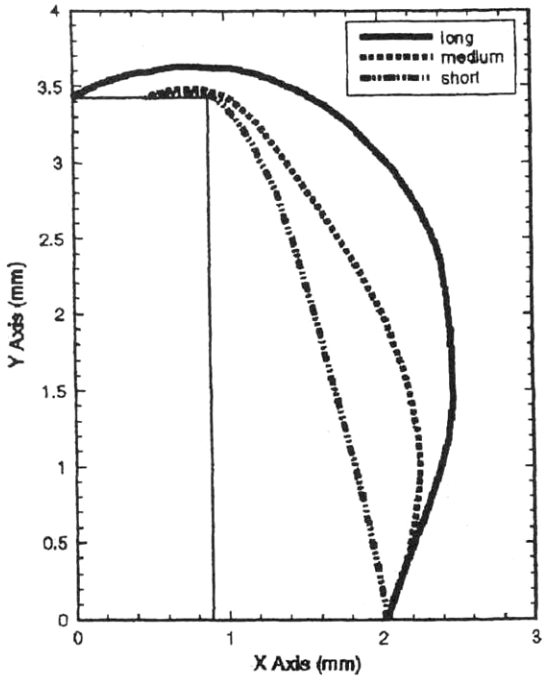
Gold Ribbon Wire Bonds to Interconnect High-Frequency Devices and for best thermal-cycle fatigue resistance





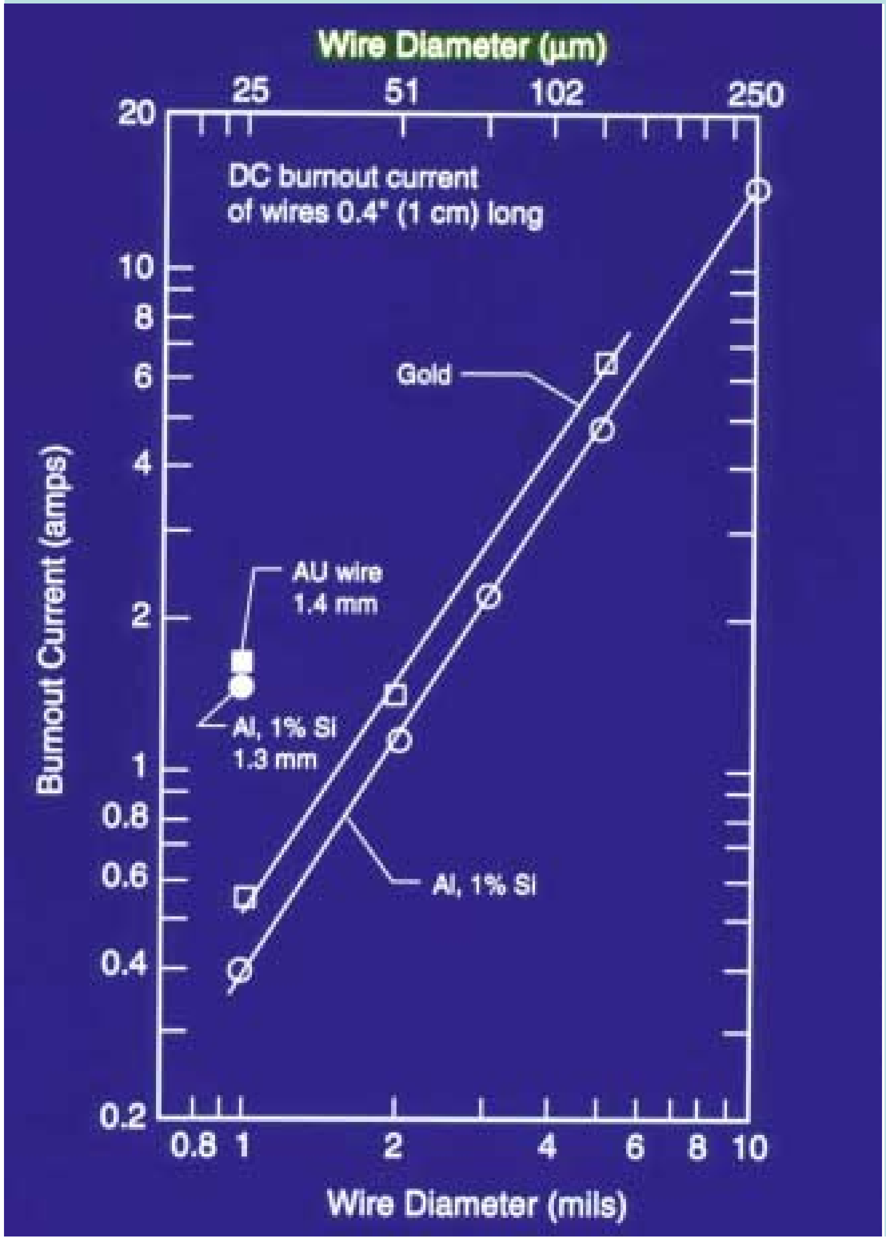
Configuration of Shock/vibration Wire Bond Problem (both in HTE and LTE





NASA Stacked Die, Long-wire, 3.5 mm (140-mil) drop, Au wire bonds (Henning Leidecker)

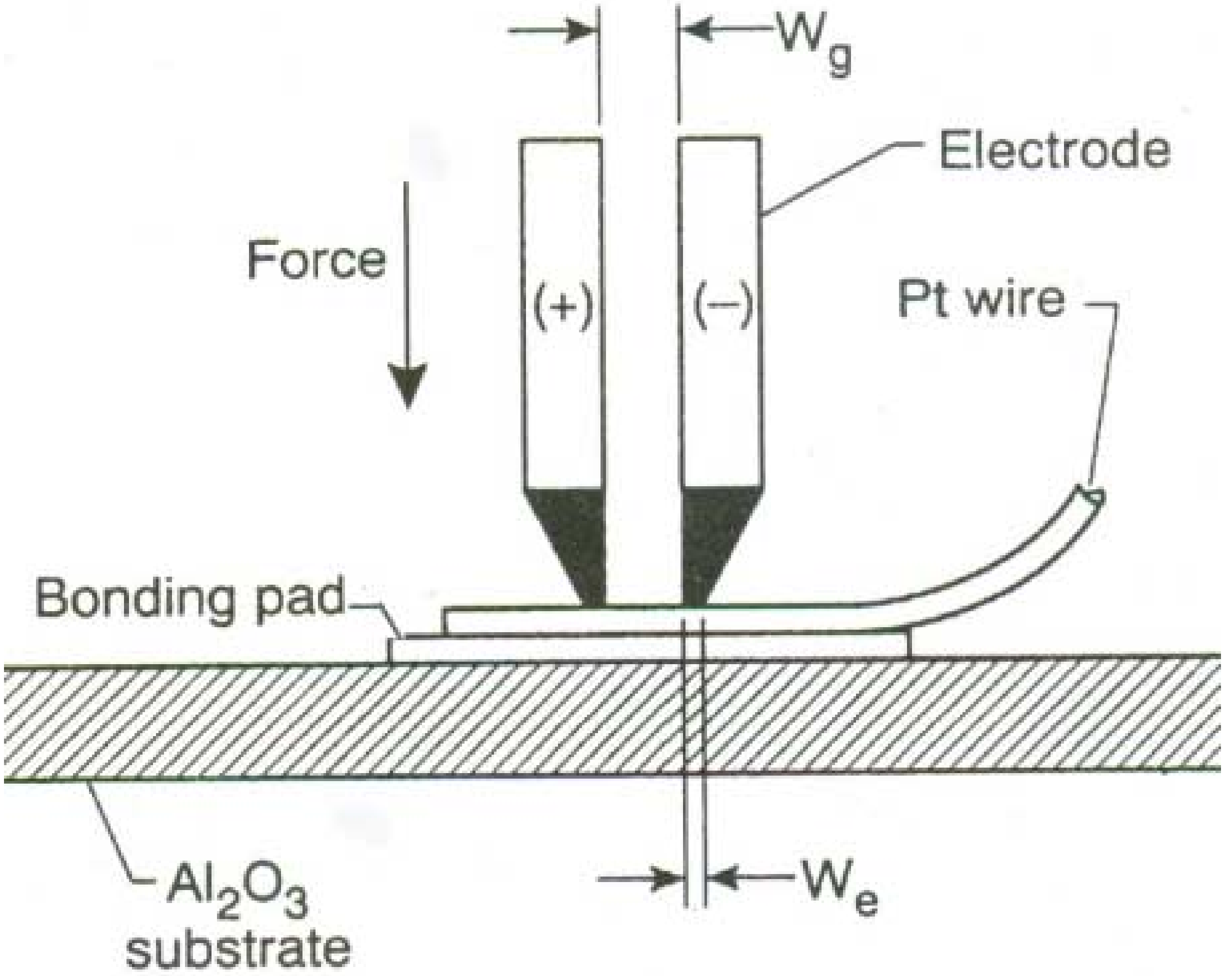
Bonding Wire Burnout Current



Wire Burnout for 1-cm lengths of aluminum, 1% Si, and gold wires.

For HTE, one must Derate the Current Carrying Capacity

Parallel Gap (E-D) Welding for Low Thermal Conductivity Wires, etc.



Flip Chips and other Soft Solder Metallurgy cannot be used in an HTE Environment (OK on Mars??)

- They **Melt,** Creep, and Fatigue
- (Creep is plastic (permanent) deformation of a material at high temperatures (with respect to its melting point) that occurs under load for long periods of time).
- Creep starts when T (K) >~ 0.4 to 0.5 of melting point of the metal (e.g., for soft solder MP ~180 ºC, creep starts about – 70 ºC).
- **Underfill has similar problems-never been developed for LTE**
- **However, can use Gold-ball-bumped flip-chips!**

Stud Bumping for Flip Chips

[Note: this is *not* ball bumping (!!) since the wire-end is bonded back onto the bonded ball]

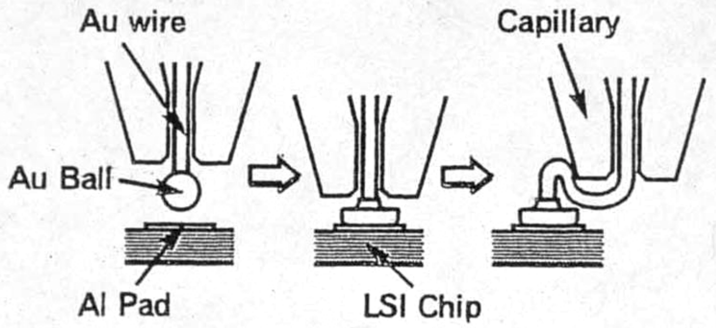


Figure 3 The formation process of Stud-bumps

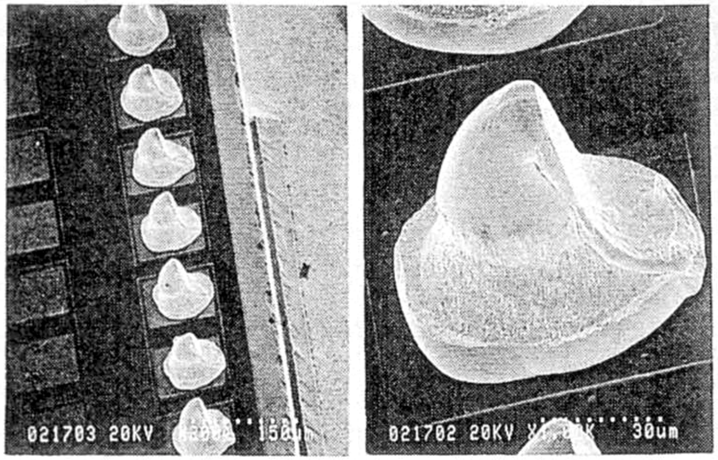
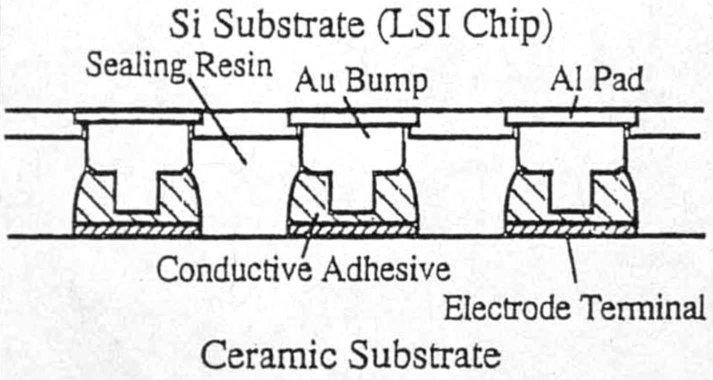
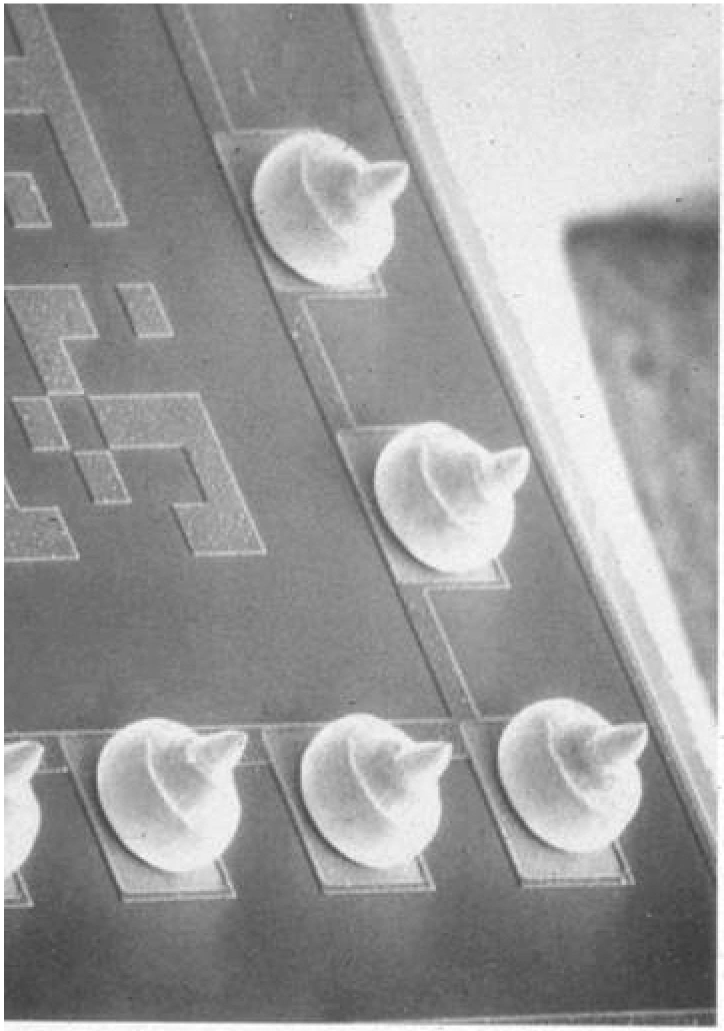


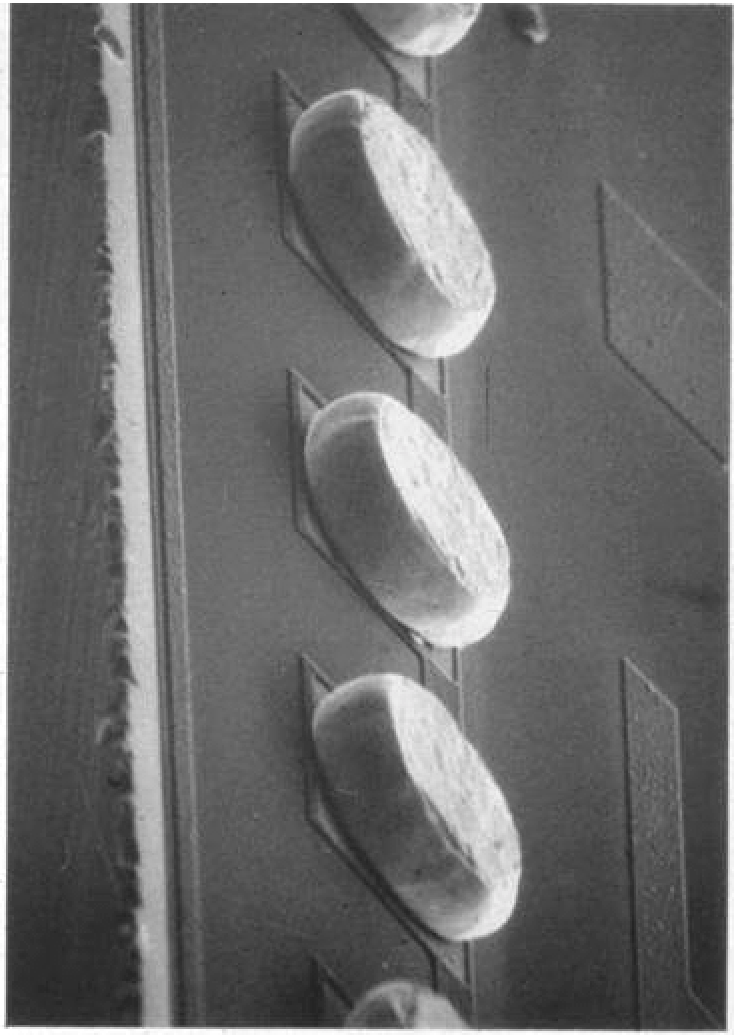
Fig.4 SEM photograph of the Au bumps



Ball Bumped bonds (left) and Same Ones Coined (right) can be used for Flip-chips

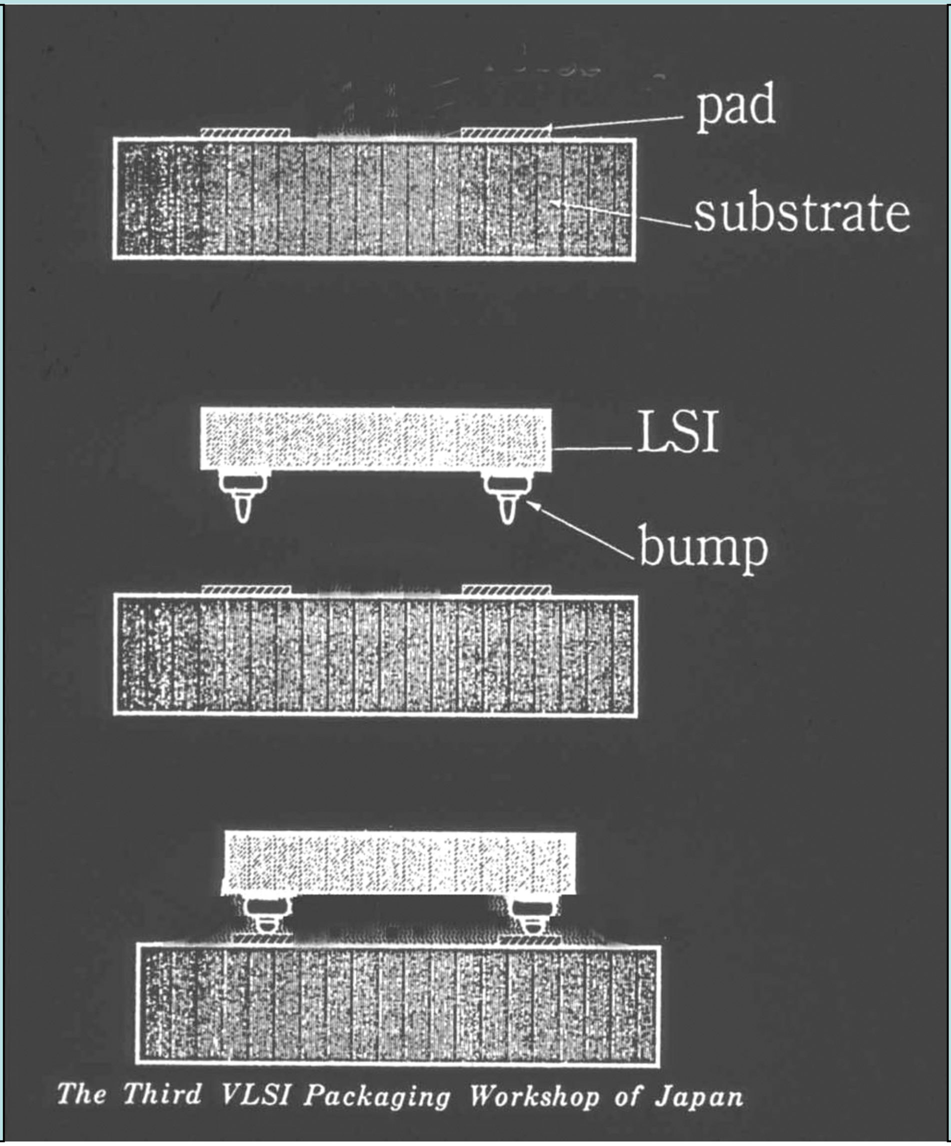


Bumps Before Coining



Bumps After Coining

Flip a ball-bumped-chip over and TC-bond it to Gold Pads on Substrate →*voila!* a high/low-temperature, High-performance, Flip-chip Interconnection!



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Pads on Substrate and Chip are noble metals (i.e., Au, Pt, Pd, etc.) If chip metallization is not noble, then apply a barrier (e.g., Ta) and deposit noble Metal for bondability.

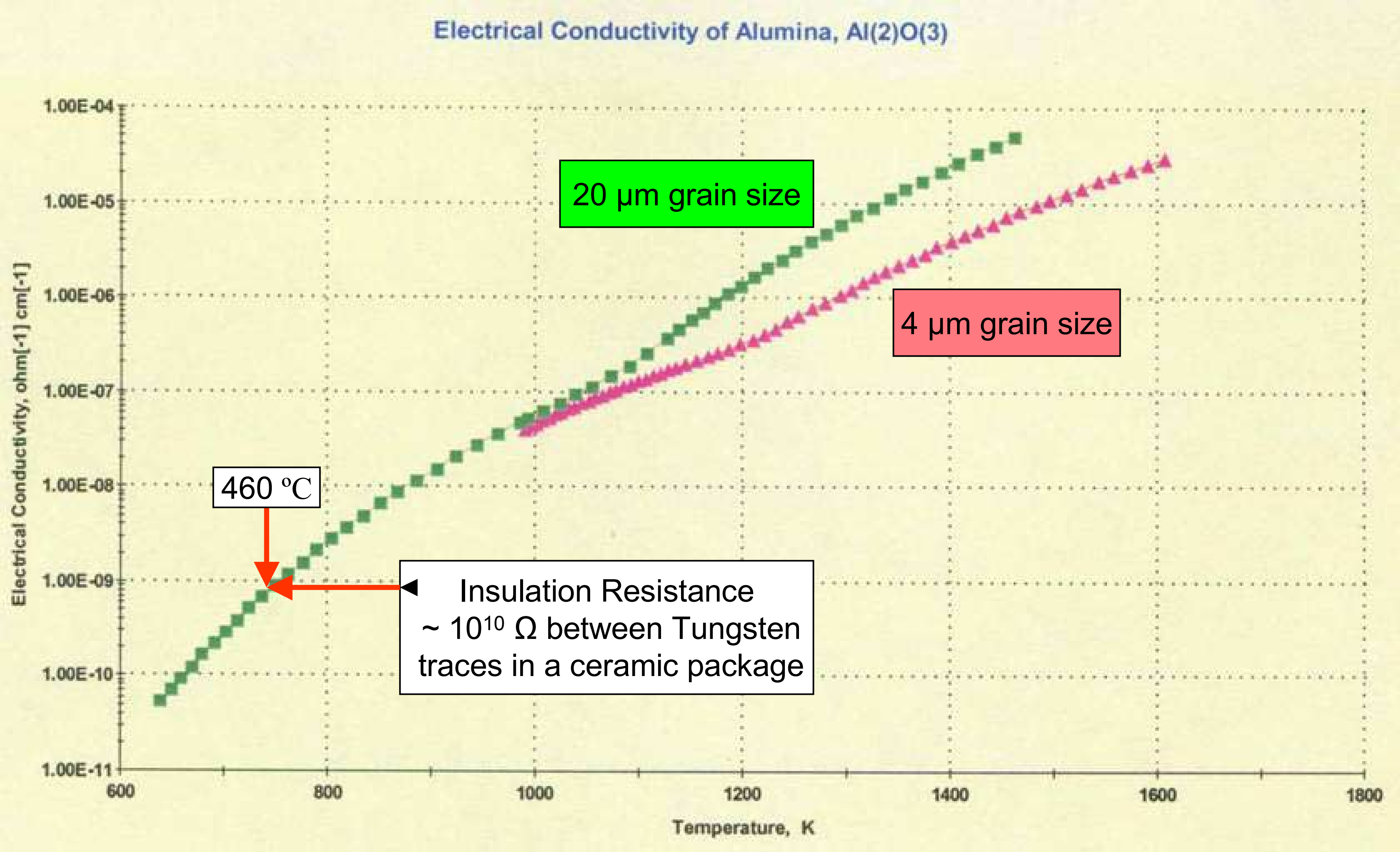
Choose Components to Minimize CTE Differences in No-underfill Flip-chips (*data from SRC-CINDAS*)

(Substrate should have ~ higher CTE than chip)

[***note: these values may go crazy at low temperatures***]

Component	**Material**	**CTE** (ppm/ºC)	**Thermal Cond.** (W/cm-ºC)
Chip	Si	2.6	1.57
	SiC	1-3 (T-dep)	~5 (>T dep)
	GaN	~3	1.3
	GaAs	5.7	0.48
Substrate	SiC	1-3	0.8-2
	AlN	4.6	1.75
	Al_2O_3	~6	0.35
	BeO	~6-7	~3

Low Electrical Leakage of Al_20_3 Ceramic in HTE
(hot pressed-sintered) (SRC-CINDAS)



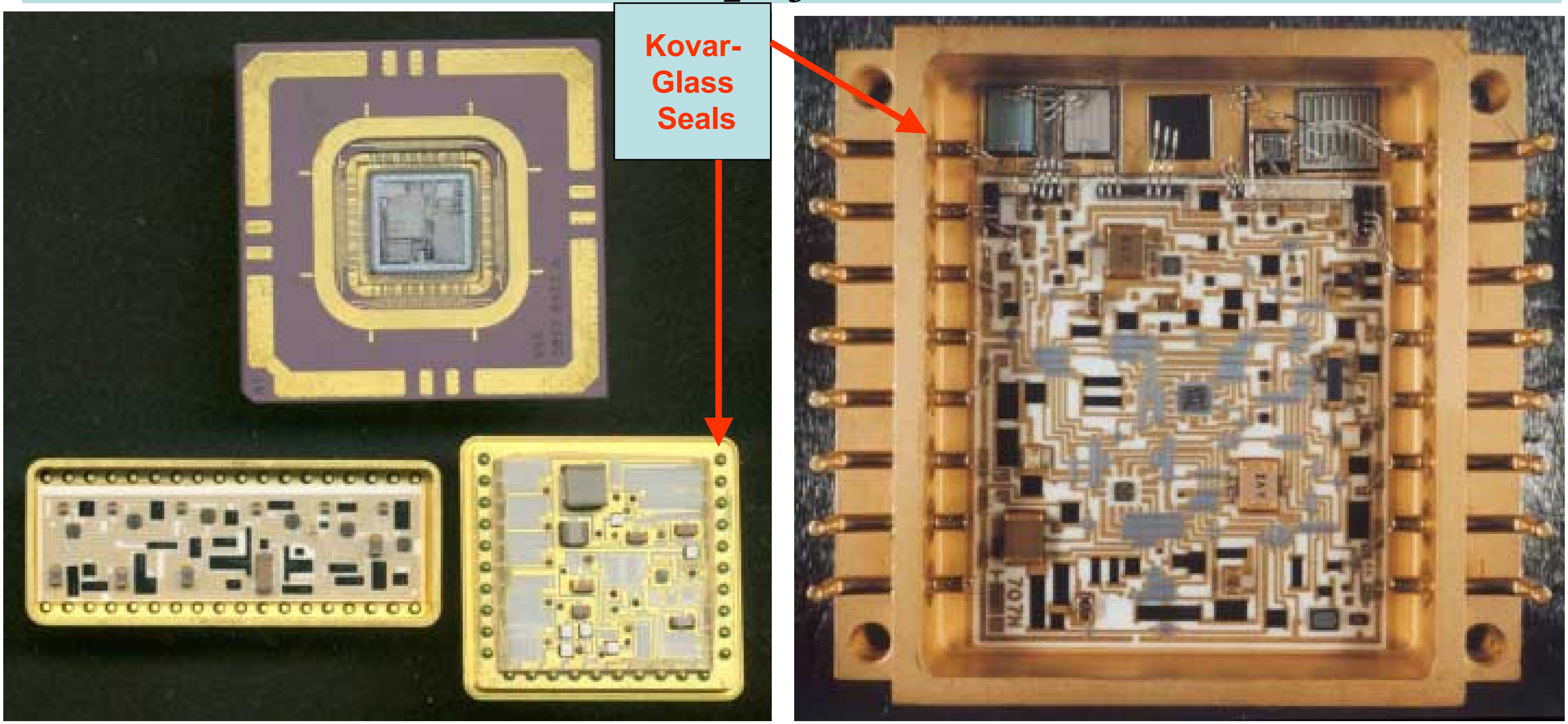
20 µm grain size

4 µm grain size

460 ºC

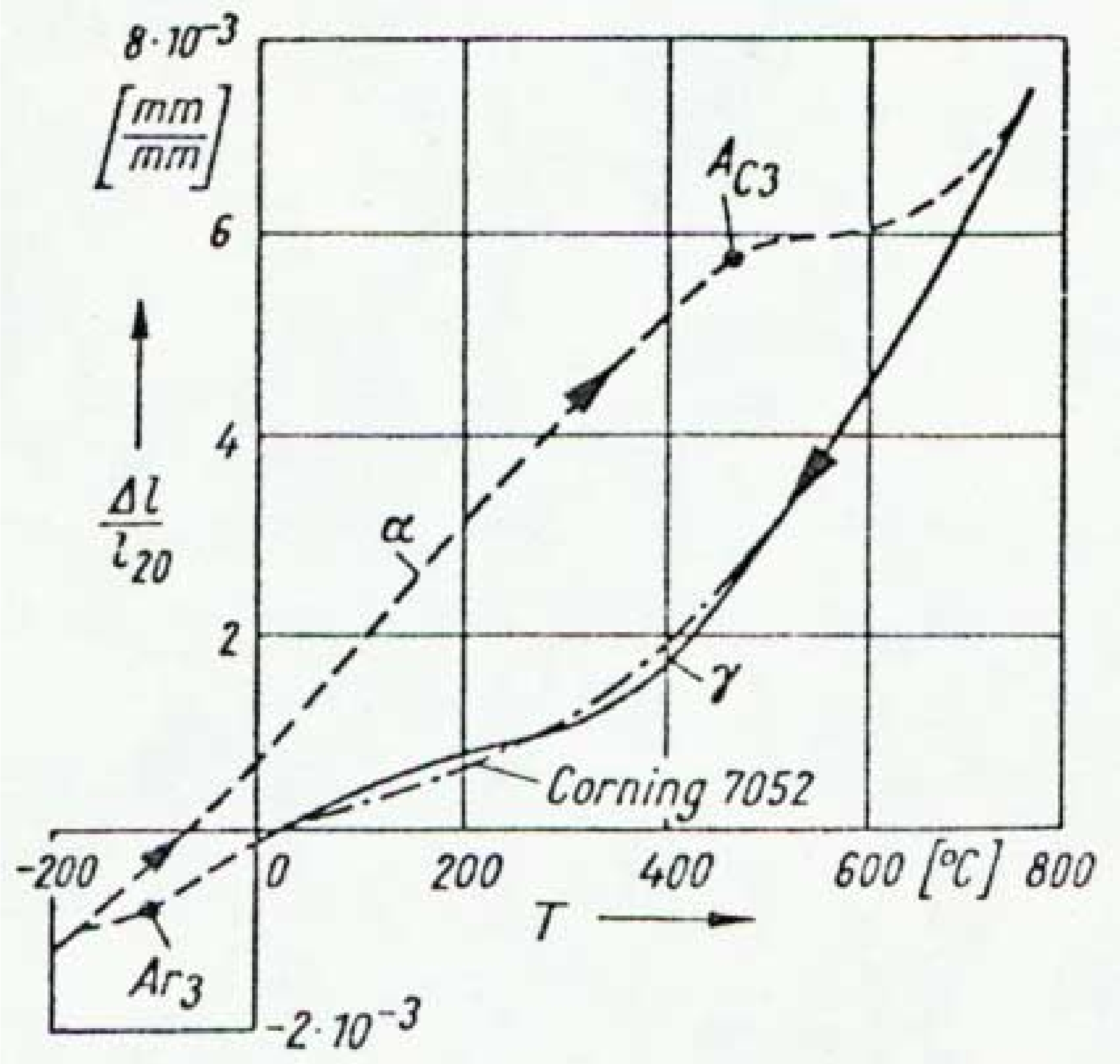
Insulation Resistance
~ 10^{10} Ω between Tungsten
traces in a ceramic package

A Typical Tungsten Trace in a classical Ceramic Package, at 0 ºC ≈ 0.25 Ω, at 460 ºC ≈ 0.8 Ω.
For a thick-film-gold trace it is ≈ 0.1 Ω and ≈ 0.25 Ω.
Thus JPL can use either a **Classical** Al_2O_3/Tungsten Package Seam Welded and **designed for pressure and rad-hard,** or thick-film-Au/Al_2O_3 Hybrid Substrates.



Kovar-Glass Seals

FeNiCo-7052 Hysteresis and Low Temp Phase Change



Flip-Chip Bond Design Considerations for Very Low Temperature Operation

- Match Substrate CTE ≈ to Semiconductor. (Actually Desire Chip to have a Little Lower CTE than Substrate, since Chip heats up).

- Si and SiC chips CTE-match to AlN as a substrate, and **Solder-based flip-chips are possible without underfill!**

- **Avoid Underfill (no data for Low Temp)!**

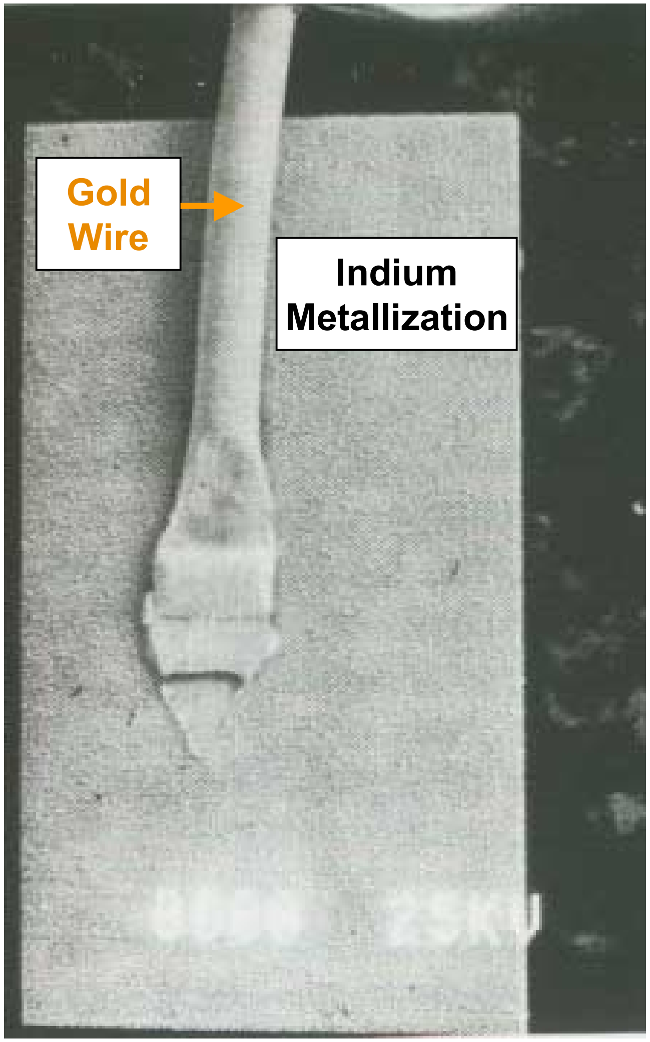
- GaAs is better matched to alumina than is Si.

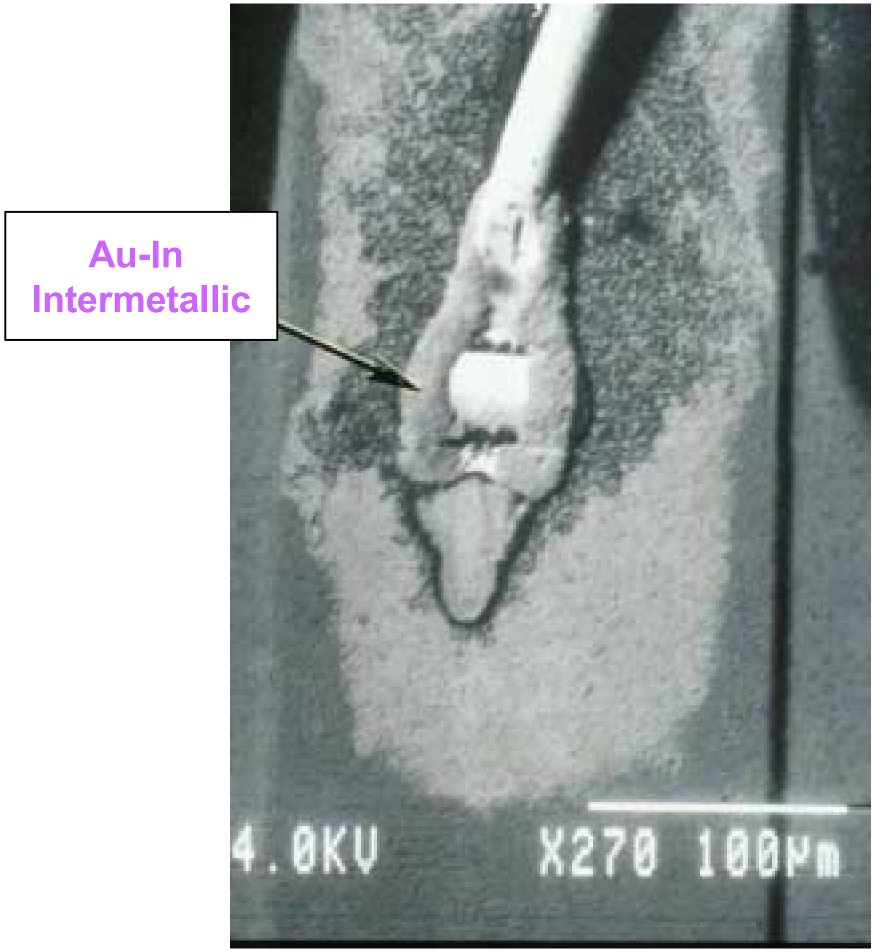
Interconnection Considerations for Very Low Temperature Environments.

- The metallurgy of Bond Pads and Wire/bumps are less Important at Low Temperatures.
- **Au-Al interfaces are reliable for Long Missions**!
- Diffusion is Limited by the Arrhenius Relationship (***$K = Ae^{-E/RT}$***). Intermetallics and Voids do not form. Corrosion is Minimal or Nonexistent.
- Wire/weld/package **Fatigue Problems** may Occur if there is Frequent Temperature Cycling **(also a major Problem for HTE interconnections)**

GOES HgCdTe, 77K, IR detector (Wire is Gold, Pad is Indium: Intermetallics are Obvious!)

Low-Temperature Space Devices may be Damaged during Terrestrial Stress-Testing





Summary and Recommendations Using Metallic Bonding/welding Systems in HTE I

1). Couples for extreme HTE usage:

1000-hrs. at 300 to 500 ºC

- Au-Au, Al-Al, Al-Ni, Pt-Pt, Pd-Pd, Pt-Au and other noble metal/combinations. For ease of use/reliability have all Gold-Gold Interfaces when possible! Also coat all metal surfaces and leads with gold. Spot weld Leads.

2). Couples for moderate HTE usage:

Several hundred hours at <300 ºC

- Al-Au, Au-Cu, Al-Cu, Al-Pd, Ag-Au (additions of diffusion inhibitors or barriers may allow use of some of these couples {e.g., Al wire bonds to thick-film Au containing Pd additives, adding hydrogen to a package containing Au-Al bonds for longer periods or higher Temp. range})

Summary and Recommendations Using Metallic Bonding Systems in HTE II

3). Interconnection Metals to avoid using in HTE

- **Al-Ag**, any form of **soft solder** or its constituents. **NO SOLDER-BASED FLIP CHIPS allowed!**

4) Caveats for making high reliability bonds for HTE.

- To be reliable, most bi-metallic bonds require well-welded, impurity-free interfaces (clean before bonding), and in addition the electronic package should contain no ambient gasses that corrode either metal. (e.g., no halogens in or around welds containing Al.)

- Understand Possible Diffusion into the Semiconductor from the Ohmic Contacts (will it poison the chip?)

Future Work Needed for Metallurgical Reliability in Packaging (1)

1). Establish the long term reliability of the most important bond/weld interfaces at the highest times/temperatures (1000 hr/~500 ºC), Interface ΔR, etc. [Al-Al, Al-Ni, etc] (some measurements must be made insitu at that temperature).

2). How do the bond-pad diffusion barriers on chips hold up against cracking/diffusion in long term HTE? (with damage during bonding?)

Future Work Needed for Metallurgical Reliability in Packaging (2)

- **Wire properties** must be evaluated at temperature/time (there is HTE evidence of grain growth, bamboo structure, fatigue strength decline, etc.)
- Determine the **current-derating of wire** for HTE.
- Evaluate the Die attach materials Integrity for HTE chips—Ag-Glass needs to be developed for 450º C
- Evaluate some new high temp Lo-k polymers inside packages for vibration dampers, die attach, underfill