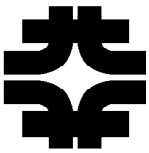

Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

BERT:
Bit Error Rate Tester

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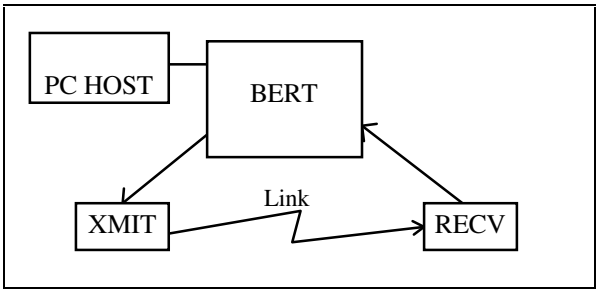
Introduction

The BERT module is a general purpose pattern generator and checker for testing high speed data links. It is designed specifically for testing the DOIM (Dense Optical Interconnect Module) and the G-Link, but it can be easily adapted for other uses.

The BERT is controlled by a host PC and uses adapter cards (XMIT and RCV) that are specific for each type of link.

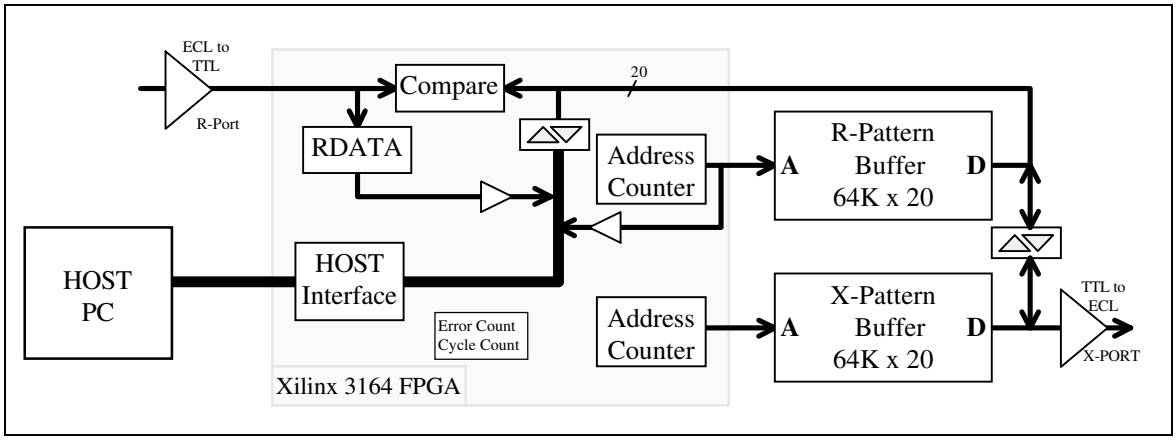


OPERATION

The BERT consists of an independent transmitter and receiver, each with its own pattern buffer. During normal operation, data words from the transmit pattern buffer are sent through the transmit port (X-Port), through the link under test, and received via the R-Port. The receiver compares each word against its own pattern buffer and, if it finds a discrepancy, halts and allows the PC-Host to readout the errant pattern's address and data.

Features:

Data Pattern Word Width	10 or 20 bits
Data Pattern Depth	64K words
Data Rate	20 to 63.5 Mwords/sec in steps of 0.5 Mhz
Host Interface	Standard DOS PC/AT



Other features:

Statistics Mode: In this mode, errors are counted internally and do not require host intervention. Error count and cycle count can be read out by the host.

Remote Mode: In this mode, two BERTs can be used to test links whose ends may not be in the same room. One BERT is used as a transmitter, the other as a receiver. The receiver can control the transmitter via a single twisted-pair cable.

Loopback: A loopback cable will allow the BERT to be tested without a data link present.

Hardware Installation

The BERT comes packaged with a power supply, PC interface card, and cable. The PC interface uses I/O port addresses from 310h to 317h. The software expects the card to be at this location and will not work otherwise.

PC Interface Card Base Address Switch

Default Setting
310h

There is an 8-pin jumper block on the BERT card that configures the handshake signals. Normally, a single BERT will be used in the LOCAL configuration. The Loopback mode is used when a single BERT is used with a cable between X-Port and R-Port.

When two BERTs are used for remote tests, one should be configured as a transmitter, and the other as a receiver. The remote configurations require two BERTs to be connected via the Auxilliary connector.

Handshake Jumper Configuration

LOCAL | Loopback | Remote Transmitter | Remote Receiver

Software

The software requires a minimal MS-DOS system with 512K of memory and a color display. The interface program, BERT.EXE, can be run from a floppy disk or can be copied to the hard disk. The interface program controls, configures, and monitors the BERT. The main display page (right) shows the current status and other useful information:

```
Current Status:                 Error Bits:                 Handshake:
IDLE RUN HALT LOAD START        HALT RCV CLK XFLT RFLT      RUN VALID RFLT XFLT

Number of Errors:          0                  Link type: DOIM  GLINK CABLE
Number of Cycles:      65535                Local/Remote  Xmit/Recv
            Time: 12:12:39          0          On error: Restart/Halt
                                                    Size: 10/20 bits
Last Error: No errors                         Frequency: 33.0 MHz
     Flags: HALT RCV CLK XFLT RFLT           Xilinx File: DOIM.bit
   Address:                                     XPattern: RANDOM.pat
      Data:                                     RPattern: =Xpattern
 Should Be:                                     Log File: =none

Enter a command.  Type F1 for Help.
```

Current Status: The BERT can be in only one of the four states IDLE, RUN, HALT, or LOAD. The state is selected via the function keys F5 through F8.

F5 puts the BERT into the IDLE state.

F6 puts the BERT into the START state and, when all handshakes are valid, (almost immediatly) transitions to the RUN state.

F7 sends a HALT signal to the BERT which will be counted as an error and then transition back to the RUN state.

F8 will stop the BERT and LOAD the currently selected pattern file. Once the pattern file is loaded, BERT is set back to IDLE. If F8 is pressed while the Xilinx File field is hilighted, then the BERT will be completly reset and the xilinx file will be re-loaded.

Error Bits: There are 5 conditions that can cause an error to be counted. The Error Bits panel shows those conditions:

HALT can be a user generated halt (F7 key) or a signal from a remote BERT.

RCV indicates that the received data does not match what is in the pattern buffer.

CLK indicates that the received clock signal missed a pulse.

XFLT and RFLT are signals sent by the link interface to indicate that the link hardware detected an error. In the Error Bits field, these indicate that a fault was detected while a test was running

Handshake: Each of the handshake signals must be on before the BERT starts sending data. If they are not, then the BERT will not enter the RUN state from the START state.

XFLT and RFLT indicate that the link hardware is ready and synchronized.

VALID indicates that a valid, stable clock is being received.

RUN indicates that RSYNC is asserted by the receiver.

Last Error displays information about the most recent error. It displays the time since the error, what the flags were that caused the error, and what the address of the Rpattern buffer was. If the error was a RCV error it also displays the received word and what it expected the word to be.

The configuration panel allows configuration options to be set and viewed. To set a configuration, use up/down arrow keys to select a field, then enter a value or use the space bar to toggle options.

Link type: The software behaves slightly differently for each type of link. Use this to set one of the pre-programmed link types.

Local/Remote The BERT can do tests locally, or it can be a remote transmitter or remote receiver.

On Error: When used as a remote transmitter, the Restart option allows the BERT to run without a host.

Size: Determines how many bits are checked. The DOIM is 10 bits. The G-link is 20 bits.

Frequency: Sets the word transfer rate. This can be from 16mhz to 63.5 in 0.5 Mhz steps.

Xilinx File: This is the bit file that is downloaded when the BERT is reset. The Xilinx gate array can be customized for each type of link. To view available files, press the F2 key. To reset the BERT and download the xilinx file, move the cursor to highlight the Xilinx File field, and then press F8.

Xpattern: is the name of the file to be loaded into the transmit pattern buffer.

Rpattern: is the name of the file to be loaded into the receive pattern buffer. If the name starts with an =, then the name of the Xpattern is used. Normally, RPattern=XPattern. They can be different in order to test the error handling of the BERT.

Log File: Errors will be logged to this file. If the name starts with =, then errors are not logged.

Number of Errors is read directly from the N_ERRS register.

Number of Cycles is the value of the N_CYCLES register. Each cycle is a pass through the 64K word pattern buffer.

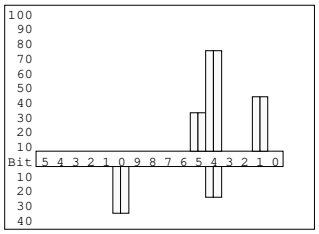
Time is the time of day. When a test is running, the elapsed time, in seconds, is also displayed.

Message: The bottom line of the dislay contains a prompt or error message to explain the current action.

Keys: The following keys have special meaning:

F1	Print a short help message.
F2	List all .BIT and .PAT files in the current directory.
F3	Print a histogram of errors.
F4	Print a histogram of the current Rpattern buffer.
F5-F8	Set the BERT state.
Alt-X	Exit the program.
↑↓	Scroll through configuration options.
SPACE	Toggle configuration options.
ESC	Cancel configuration option.

Histograms are used to summarize error data. Each bar in the histogram represents a bit in the data word. The size of the bar above the center line indicates the percentage of times that the bit was a 1 when it should have been 0. The size below the bar indicates the number of times the bit was a 0 when it should have been 1. Each bar has two halves. The left half indicates the percentage relative to the total number of errors. The right half indicates the bit error percentage relative to the total number of samples. In most cases, they are the same since a sample is only taken when an error occurs.



Running a test:

Start Bert.exe:

Make sure the BERT is connected properly and then run the bert.exe program. The program should load the xilinx chip software, do a simple sanity check, and enter the command mode.

Set the link type:

Use the cursor keys to scroll to the Link type configuration line. Use the space bar to select the desired link type. Use the ENTER key to confirm the selection. A new Xilinx file will be loaded and the data width field will be set appropriately.

Set the clock speed:

Using the up/down arrow keys, scroll till the frequency is highlighted. Enter the desired test frequency. Note that the BERT allows clock frequencies from 16MHz to 63.5MHz. The BERT is design to run at a maximum of 60mhz under worst-case conditions. Higher frequencies may cause errors. Also, some links may not run at slower speeds. The DOIM, for example, is specified by Hitachi to run no slower than 50MHz.

Load a pattern file:

Press the up arrow key until the transmit pattern file name (Xpattern) is highlighted. Enter the name of a pattern file and press ENTER. To view a list of available files, press F2. When the pattern name is entered, press the F8 key to load it.

Run the test:

Press the F6 key to start the test.

Error Messages

Could not allocate pattern buffer: The PC has run out of memory. The program needs at least 400K to run. The pattern memory uses the largest chunk (256K) of this.

Unable to open <file>: Check the local directory by pressing the F2 key. If this happens at startup, set the Xilinx file name to an existing file and press F8 while the file name is highlighted.

Xilinx File format error in <file>: The file is not a proper xilinx bit file.

Error reading pattern file: The file is not exactly 256K bytes.

Hung trying to set BERT to <state>: The BERT is busted. Try resetting by highlighting the xilinx file name and pressing F8. Check cables and power supplies. As a last resort, turn off the power and short the +5V to ground to reset the clock generator.

Histogram of Sanity Check: On startup, the software does a quick sanity check to see that it can read and write a byte on the BERT's data bus. Errors here indicate a hardware problem with the PC interface.

Pattern File Format

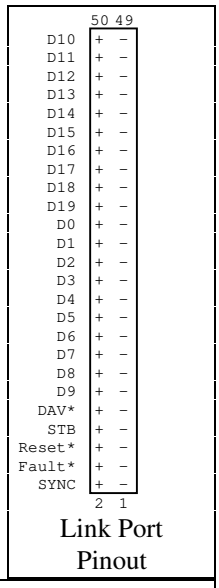
A pattern file must be exactly 65536 longwords (256K bytes). The lower 20 bits of each longword are loaded into the pattern buffers. For the DOIM, only bits 1-9 are used. Bit 0 and bits 10-19 are masked off.

Special consideration must be made for patterns that are loaded for testing the DOIM. Since the DOIM has no DATA-AVAILABLE signal, it uses bit 1 in the data word to signal the start of the test. This means that the word at address 0 must have Bit1=0 and address 1 must have Bit1=1.

INTERFACE SPECIFICATIONS

Link Ports

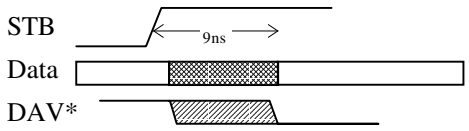
The link to be tested is connected between the X-Port (Transmit port) and R-Port (Receive port). These are general-purpose 20-bit parallel ports as shown in the pinout. Signals are differential 10K ECL. The standard 50-pin connectors are intended to be used with adapter cards that are specific to each link being tested. The ideal adapter card will make it look like there is a solid cable from X-port to R-port. In addition to the 20 data bits, there are 5 control signals:



Link Port Pinout

Signal	X-port	R-Port	Function
STB	Output	Input	Data rate clock. Some links require that this is a constant clock source qualified by DAV. Others prefer that the clock transitions only for valid data words. The Xilinx chip may have to be customized for some links. See **Timing**.
DAV*	Output	Input	This active-low signal indicates that data is valid for the current STB.
Fault*	Input	Input	This active-low signal indicates that the link hardware has detected a fault. It is intended to be connected to the LOCKED pin on the G-link transmitter and the STAT1 pin on the G-link receiver.
SYNC*	Output	Input	This is used for PLL synchronization. For the X-Port, a low on this signal indicates that the transmitter should send sync frames. It is intended to be connected to the FF signal on the G-link transmitter. For the R-port, a low on this signal indicates that the receiver is trying to lock its PLL. It is intended to be connected to the G-link STAT0 pin.
Reset*	Output	Output	The BERT drives this low to reset the transmitter and receiver. For the R-Port, this is connected to the Xfault signal so that the receiver is reset when the transmitter asserts fault.

Timing: transmit strobe and data.

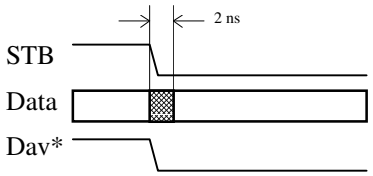


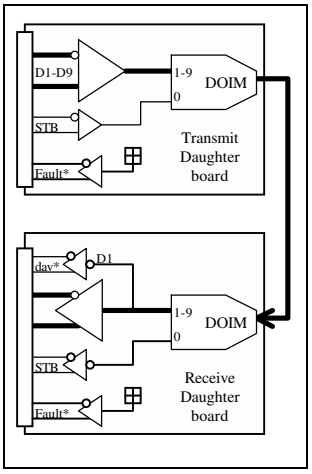
DOIM adapter cards

The DOIM (Dense Optical Interconnect Module) is a simple synchronous 10-bit parallel optical link. Bit 0 is a strobe signal and bits 1-9 are data. Bits D1-D9 and the STB are sent directly from the BERT (through ECL buffers) to the DOIM. On the receiver, bit D0 is inverted before being driven on the STB line (see timing). Note that Fault* is tied high on both cards. On the receiver, data bit D1 is inverted and driven out as DAV*. The first high-to-low transition on DAV is used by the BERT to start its own internal receiver. This means that any data pattern used with the DOIM must have D1=0 (D1=0 => DAV*=1) at address 0 and D1=1 at address 1.

Note from the timing diagram that the skew between STB and the other outputs is about 1ns.

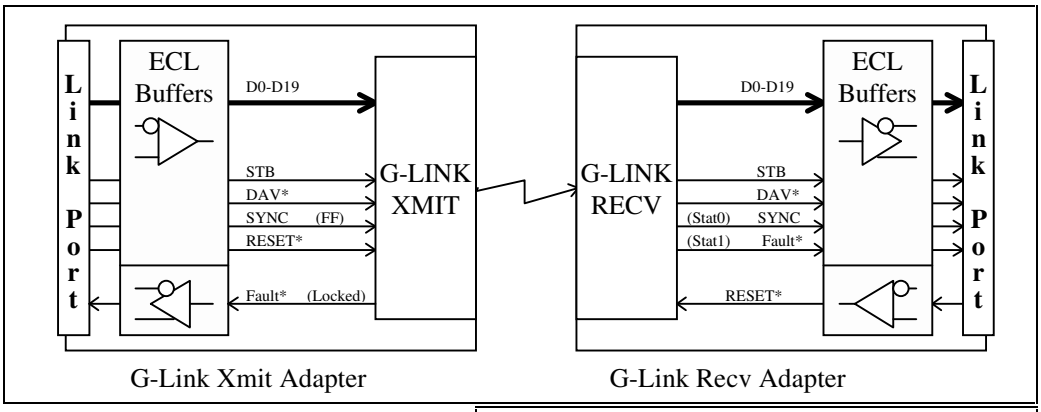
Timing: receive strobe from DOIM board.





G-link adapter card

The G-link is a serial optical link that converts 20-bit words into a serial bit stream. The transmitter requires a constant data-rate clock on the STB input while data words are validated by the DAV* signal.. Several signals are used to establish and maintain synchronization between the transmitter and receiver.

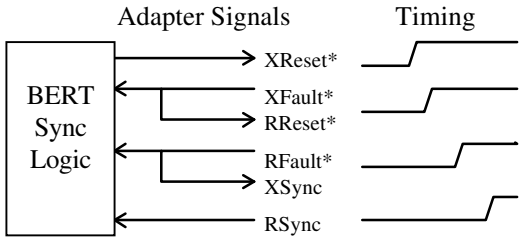


G-Link Xmit Adapter G-Link Recv Adapter

Handshake

When a test starts, the BERT releases XReset and allows the transmitter to run. When the transmitter has locked its PLL on to STB, it releases XFault. XFault is echoed back to release RReset and the receiver begins its synchronization. When the receiver is ready, it releases Rfault which is echoed back as Xsync which tells the transmitter to begin sending FF1 frames. When the receiver receives FF1s, it asserts RSync. When BERT detects RSync, it starts sending test data.

G-Link Handshake Signals



Host Interface

The host PC controls the BERT via a PDMA-16 parallel port interface card (Available from CyberResearch). In addition to 16 data lines, the host interface uses 4 control signals to control the BERT:

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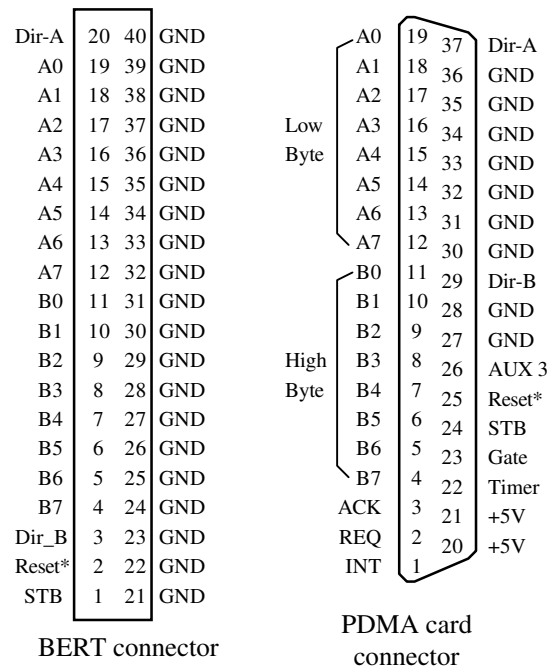
DIR_A	Direction of lower 8 bits (A-Bus)	(1 => Write to BERT)
DIR_B	Direction of upper 8 bits (B-Bus)	(0 => Read from BERT)
STB	Data strobe (Aux-1 on PDMA card).	
Reset*	Reset (Aux-2 on PDMA card)	

In order to minimize noise on the cable between the PC and the BERT, the signals have been re-arranged slightly. An adapter converts the PDMA connector pinout to the BERT connector pinout.

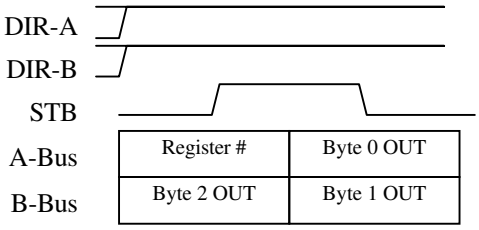
Host port pinout



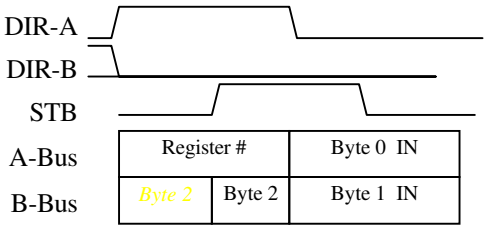
BERT connector PDMA card connector

Access Protocol

Each transfer between the BERT and the Host consists of an 8-bit register number and a 24-bit data word. Each transfer requires a positive and negative transition on the strobe. The register address and upper byte are transferred on the rising STB. The lower two bytes are transferred on the falling edge. State changes inside the BERT do not take place until the falling STB.



Write to BERT



Read from BERT

Registers

There are 9 registers.

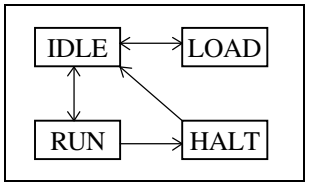
Reg	Dir	Name	Function	[23 Bit Pattern 0]
0	R/W	**XPATTERN**	Access Transmit Pattern buffer.	....DDDD DDDDDDDD DDDDDDDD
1	R/W	**RPATTERN**	Access Receive Pattern buffer.	....DDDD DDDDDDDD DDDDDDDD
6	W	**CONFIG**	Configuration: aux/host/speed	HXRS.... ..FFFFFF F.......
7	W	**CONTROL**	Control: idle/run/halt/load/clear	IRHLC... ....
8	R	**ERRWORD**	Received data that caused error.	....DDDD DDDDDDDD DDDDDDDD
9	R	**ERRADDR**	Address when error occurred.	.... AAAAAAAA AAAAAAAA
10	R	**N_ERRS**	Total number of errors since clear.	.... NNNNNNNN NNNNNNNN
11	R	**N_CYCLES**	Number of cycles through pattern.	.... NNNNNNNN NNNNNNNN
15	R	**STATUS**	Current board status	IRHLS..h DKxr.... RVrx....

The **XPattern** and **RPattern** registers are only available when the BERT is in the LOAD state. Each access to one of these registers transfers a data word to or from the pattern buffer and increments the corresponding address pointer. The address pointers are 16 bits and wrap around after 64K transfers. They get reset when the BERT enters the IDLE state. The pointer to the receive pattern buffer can be read via **Erraddr**.

When an error occurs, the BERT enters the HALT state and increments its error counter. The word that caused the error is available via **Errword** and the receive pattern pointer is available via **Erraddr**. The error counter can be read via **N_Errs**.

Each time the BERT cycles through its pattern buffer, it increments a cycle counter. The value of this counter can be read via **N_Cycles**. Both the cycle counter and error counter are 16 bits wide and wrap to 0. They can be cleared by setting bit 19 of the control word.

The BERT can be set to one of four states via the **Control** register. Only one of bits 23:20 should be set at a time and the BERT must be set to IDLE before it can enter the RUN or LOAD state:



CONFIG Register Bit definitions:

Bits	Name	Function
23	**HOST**	Halt Mode: 0: Halt on error 1: Restart
22	**Remote X**	Become a remote transmitter.
21	**Remote R**	Become a remote receiver.
20	**Size**	Word Size: 0: 10 bits 1: 20 bits.
13:7	**Frequency**	Clock speed = F* 0.5MHz

CONTROL Register bit definitions:

Bits	Name	Function
23	**IDLE**	Put BERT into IDLE state
22	**RUN**	Start test
21	**HALT**	Stop test
20	**LOAD**	Prepeare to load pattern buffers
19	**CLEAR**	Clear statistics counters.

STATUS Register Bit definitions:

Bit	Name	Function
Operational status:		
23	**IDLE**	No activity. Reset address counters.
22	**RUN**	BERT is currently running
21	**HALT**	BERT has been halted
20	**LOAD**	Pattern buffers are being loaded
19	**START**	Trying to RUN: waiting for handshakes
Error status:		
16	**U_HALT**	Bert was halted by the user interface.
15	**DATA**	Data error was detected on compare.
15	**CLOCK**	Receive clock skipped a pulse.
13	**Xfault**	XFAULT became true after test started.
12	**Rfault**	RFAULT became true after test started .
Handshake status:		
7	**RUN**	Transmitter is sending data
6	**VALID**	Received clock is valid and stable.
5	**RFAULT**	Receiver is asserting RFAULT
4	**XFAULT**	Transmitter is asserting XFAULT.

Auxilliary Connector

The auxilliary connector is used for remote operation and triggering. It has 3 signals:

TRIG	Goes low for one clock cycle when an error is detected. This is available as a standard TTL level signal or as a differential RS485 output.
HALT_IN	Stops the transmitter and resets its address pointers. This is an RS485 input.
HALT_OUT	Goes high when an error is detected and remains high until the receiver is re-started. This is an RS485 output.

Auxilliary Connector

GND	1	2	GND
GND	3	4	TRIG (TTL)
TRIG+	5	6	TRIG-
HALT_IN+	7	8	HALT_IN-
HALT_OUT+	9	10	HALT_OUT-

Logic Analyzer Ports

There are three ports for connecting directly to Hewlett Packard logic analyzer pods. Pin 3 is the pod clock and pins 4-19 are the data bits. The RD bus contains data that is coming from the receive port. RSTB is the strobe from the receive port. RCLK is the internal clock signal generated from RSTB. RA is the current address of the receive pattern buffer.

Logic Analyzer Ports

J8

NC	1	2	*NC*
RSTB	3	4	TRIG
/RRESET	5	6	/XRESET
X_SYNC	7	8	R_SYNC
/RDAV	9	10	RD9
RD8	11	12	RD7
RD6	13	14	RD5
RD4	15	16	RD3
RD2	17	18	RD1
RD0	19	20	GND

J9

NC	1	2	*NC*
NC	3	4	*NC*
NC	5	6	*NC*
NC	7	8	*NC*
NC	9	10	RD19
RD18	11	12	RD17
RD16	13	14	RD15
RD14	15	16	RD13
RD12	17	18	RD11
RD10	19	20	GND

J11

NC	1	2	*NC*
RCLK	3	4	RA15
RA14	5	6	RA13
RA12	7	8	RA11
RA10	9	10	RA9
RA8	11	12	RA7
RA6	13	14	RA5
RA4	15	16	RA3
RA2	17	18	RA1
RA0	19	20	GND

Power Connector

Power is supplied to the BERT and its adapter cards via 4-pin molex connectors.

Power Connector

+5V	1
GND	2
GND	3
-5.2V	4