July 19, 2006

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RE: NREL Subcontract # ADJ-1-30630-12
D.5.7

Dear Ken,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of March 16, 2006 to April 16, 2006 under the subject subcontract. The report highlights progress and results obtained under Task 3 (Si-based Solar Cells) and Task 4 (In-Line Diagnostics).

TASK 3: Si-BASED SOLAR CELLS

Aluminum Induced Crystallization (AIC)

In a previous monthly report (January 2006), two possible approaches to achieve large-grain silicon films on glass by the AIC process were suggested: normal structure (glass/Al/a-Si) annealed below eutectic temperature (resulting in 20~30μm grains); and reverse structure (glass/a-Si/Al) annealed above eutectic temperature (which forms a continuous silicon top layer). The crystallized Si obtained through both methods may be used as seed layer in a polycrystalline thin film solar cell.

Design structure of AIC-based solar cell

We plan to investigate both methods mentioned above to produce a heavily doped p+ large grain seed layer. Incorporation of AIC seed layers will be evaluated using different structures. Two different kinds of absorber layers (i-type μc-Si & p-type μc-Si) and two different emitter layers (n-type a-Si & n-type μc-Si) are planned. Both the absorber layer and emitter layer will be deposited by HWCVD.

Altogether, we plan to investigate the following 4 cell structures as shown in Figure 1, using the two different AIC approaches with different absorber layer and emitter layers:

(1) AIC seed layer using normal structure with 450 ^{o}C heat treatment to get AIC (p+) seed layer. Here, Al etching is needed. Device structures as shown in Figure 1.
(2) AIC seed layer using reverse structure, 600 ^{o}C heat treatment to get AIC seed layer, and no Al etching is needed. The device structures would be the same as in Figure 1 except they would have a layer of Al between the AIC Si layer and the glass substrate.

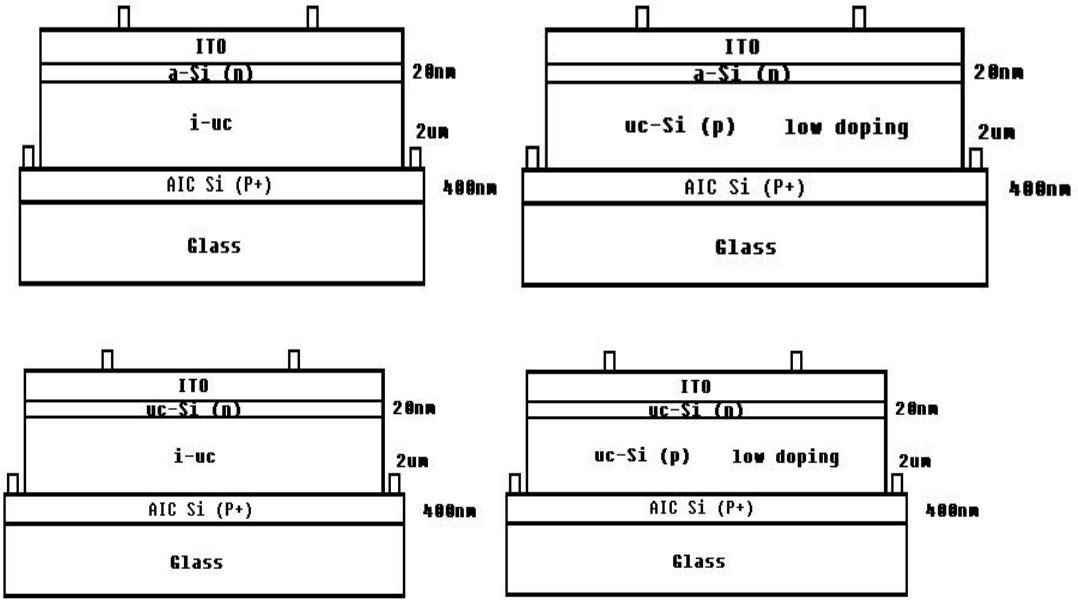


Figure 1. Four possible devices incorporating AIC p+ seed layer after Al etching. Differences are the absorber (intrinsic or p-type) and emitter (a-Si or µc-Si). The AIC seed layer would be produced by two methods as described above.

Seed layer by AIC using normal structure

Efforts so far have focused on making the seed layer using normal structure (glass/Al/a-Si) annealed below the eutectic temperature.

According to previous experience, e-beam was used to deposit both a-Si and Al, and two batches of samples a-Si/Al/7059 and a-Si/Al/1737 were deposited using different types of glass substrates. However, a new problem arose. After the deposition of a-Si, almost all the samples exhibited strain or stress cracks on the film, and the Al and Si films are easily peeled from the glass. This occurred for both 7059 and 1737 glass substrates. Optical microscopy pictures in Figure 2.a shows the strain lines. The deposited amorphous silicon and Al films had normal XRD spectra as expected. Annealing was performed at 450°C to promote the AIC process. Figure 3 shows optical microscopy (OM) for the sample

after annealing. It can be seen that crystallized Si is formed with ~30 µm grains, but the strain fractures make the layer discontinuous, which would cause problems for making a solar cell.

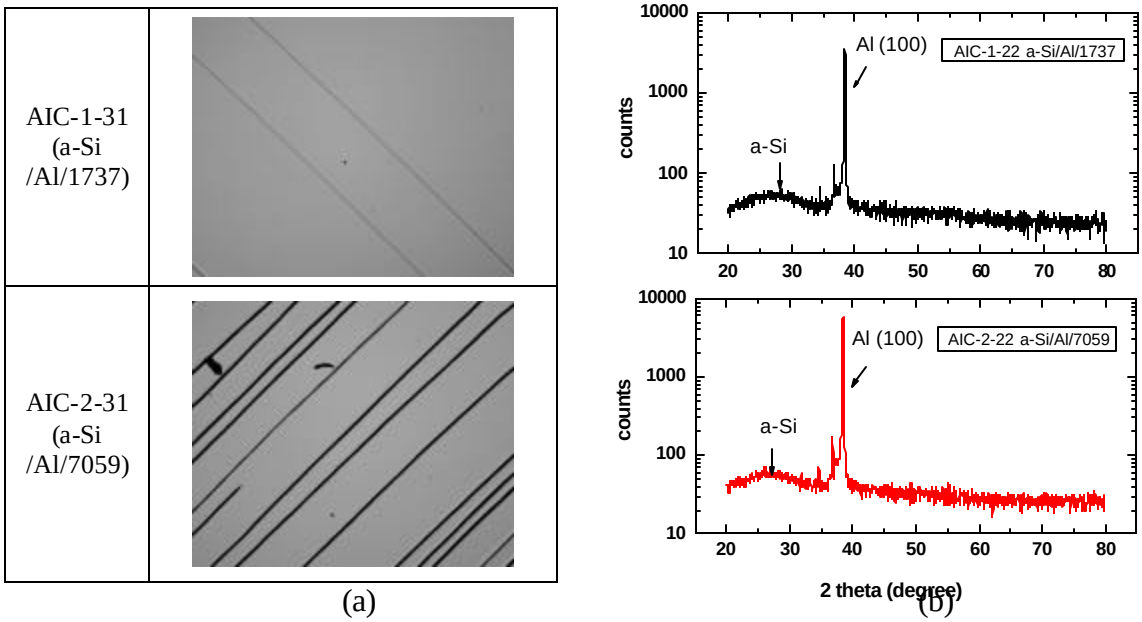


Figure 2. Samples on 1737 (top) and 7059 (bottom) before heat treatment. (a)OM images. (b) XRD pattern. (b) is not clear above

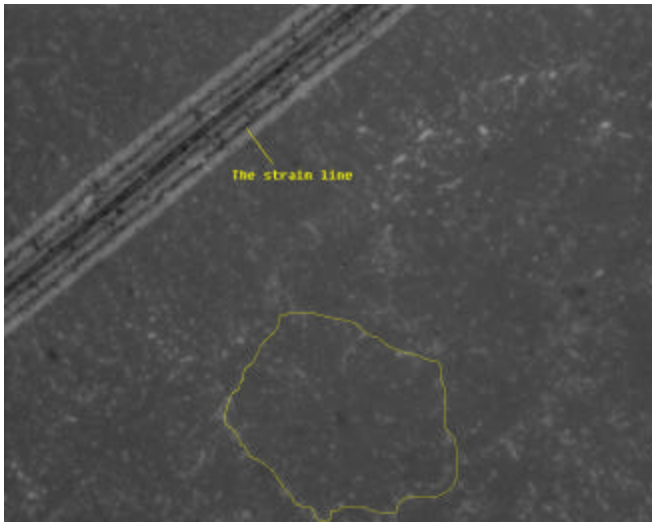
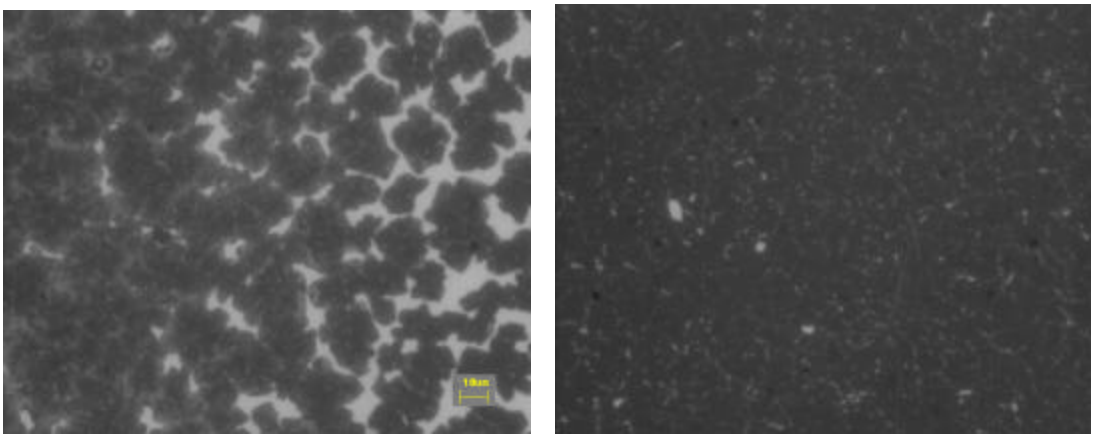


Figure 3. Optical microscope image for sample with strain fracture after annealing. Crystallized Si was formed, but the layer was discontinuous due to the fracture. Here, the yellow circle highlights a grain.

Several more depositions were tried, but same problem occurred. The reason is still unknown. In order to isolate the source of the problem, and to make progess, we deposited a-Si by HWCVD.

Samples were deposited (Al by e-beam, a-Si by HWCVD) and the AIC annealing was performed. No fracture or peeling was observed. OM image of the resulting sample is shown in Figure 4. Due to the nonuniform a-Si deposition at sample's edge, crystallized Si is not connected at edge (Fig. 4.a), but a nearly continuous Si layer is formed across the main part of the substrate (Fig. 4.b). From Figure 4.a, it is easy to tell the grain size of the crystallized Si. We can see, the grain size is about 10~20μm, smaller than the ones using e-beam deposited a-Si. This is due to the high H content in HWCVD deposited a-Si film. XRD (Fig. 5) confirmed the crystallinity of the Si film, but 10-20 μm is more than sufficient for the seed layer. These HWCVD Al/Si seed layers will be used for subsequent device fabrication.



(a) (b)

Figure 4. Optical microscopy of sample after annealing. (a) edge area, showing the grain size but non-uniform with 10-30 μm grains. (b) typical of most area of the sample showing almost continuous large grain Si layer.

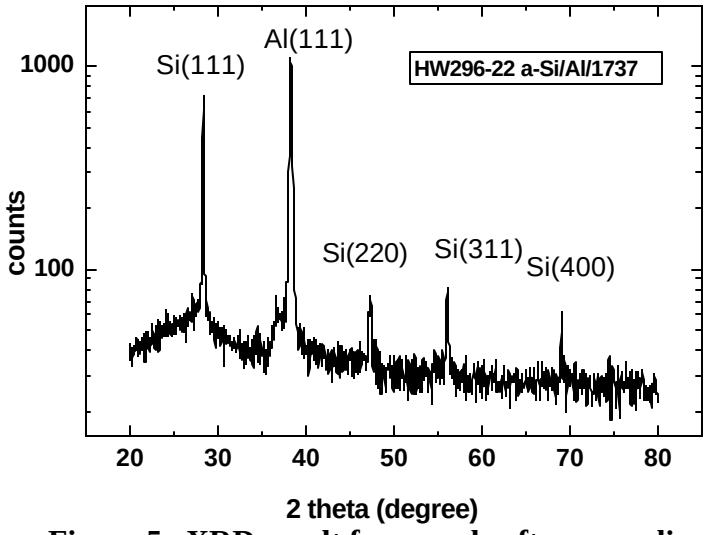


Figure 5. XRD result for sample after annealing.

Formation of seed layers using the second condition, i.e. the reverse structure (glass/a-Si/Al) annealed above eutectic temperature, is in progress. HWCVD will also be used for the Si layer.

When both types of seed layer are ready, electrical properties of the seed layer will be studied, and then used to make a complete solar cell, e.g. poly-Si deposition by HWCVD will be performed.

Solid Phase Crystallization (SPC)

Our previous monthly report (January 2006) described plans for fabricating nc-Si devices from a-Si via SPC or rapid thermal processing (RTP) without the aid of AIC. Table I lists device structures that were deposited by HWCVD for further SPC and RTP study. HW281 (n+/i) and HW283 (p+/i) are partially completed devices lacking a second doped contact or emitter while HW282 (n+/i/p+) and HW284 (p+/i/n+) are completed devices. Conditions for the doped layers were the same except for the dopant gas. The i-layers were 1.5 µm and deposited under conditions known to give amorphous Si not nc-Si. There were 4 types of substrates in each deposition: 1-7059 glass; 2-ZnO on 1737; 3-ZnO on 7059; and 3- Tec 15 SnO_2 on soda-lime glass (SLG). Raman measurements verified that there is no nc-Si in these devices as deposited.

Table I. Device structures deposited by HWCVD for SPC.

Run #	Structure
HW281	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 um)
HW282	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 um) / a-Si:H.p+ (20nm)
HW283	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 um)
HW284	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 um) / a-Si:H.n+ (20nm)

Our previous report (January 2006) described studies to evaluate the effect of dehydrogenation for 4 hours at 400 or 500°C followed by SPC at 0, 24 or 48 hours at 600°C. It was unclear whether dehydrogenation had an effect.

It is reported that SPC Si grain growth is enhanced by a heavily doped n+ (P atoms) layer, and by using glass not glass/TCO substrates. UNSW claims in patents that SPC is enhanced by use of low softening point glass like SLG, not high softening point like 1737. We used the above substrates to investigate these variables. SPC was performed at 600°C for 64 or 100 hours in H_2/Ar. Fraction crystallinity was evaluated by Raman spectroscopy and grain size was determined from the (111) peak obtained from XRD.

Table II shows the crystalline fraction and grain (particle) size for the above device structures annealed at 600°C for 64 or 100 hours. There is a clear difference between 7059 and 1737 glass. All 4 types of samples on 7059/ZnO had higher crystalline fraction

and larger grain size compared to the same 4 samples on 1737/ZnO. Since they both had ZnO, it is not due to a surface nucleation effect. The three samples on bare 7059 had larger grain size than those on 7059/ZnO. This is consistent with reports in the literature that SnO_2 suppresses the grain growth. Samples on SLG/Tec15 substrates deformed due to melting, the Si films were severely cracked, and were generally unmeasurable. Films on SLG/Tec15 survived SPC at 575 or RTP at 750°C and had 100% crystallinity, as reported last year. There is a slight but consistent enhancement of grain size in samples containing a P-doped n+ layer, consistent with reports in the literature, but they generally report much greater enhancement, perhaps because the entire 1-3 μm Si film is heavily P-doped, not just a 10 nm contact layer.

However, the grain size on all samples was disappointingly small. It is surprising that crystallinity was not ~100% even after 100 hours. Our previous work applying RTP to films or devices found ~100% crystallinity but with grains of 20-30 nm, about half the size of those on 7059.

Table II. Crystalline fraction and grain (particle) size for device structures annealed at 600°C for 64 or 100 hours, having different substrates.

Sample	Structure	Time (hrs)	Crystalline Fraction (%)	grain size (nm)
HW281-13	7059/ZnO/n-i	64	77	54
HW282-13	7059/ZnO/n-i-p	"	83	56
HW283-13	7059/ZnO/p-i	"	78	46
HW284-13	7059/ZnO/p-i-n	"	82	47
HW281-23	1737/ZnO/n-i	"	67	39
HW282-23	1737/ZnO/n-i-p	"	72	38
HW283-23	1737/ZnO/p-i	"	70	33
HW284-23	1737/ZnO/p-i-n	"	73	37
HW281-11	7059/n-i	100	n/a	70
HW283-11	7059/p-i	"	"	63
HW284-11	7059/p-i-n	"	"	58

Some of these films will be selected for RTP treatment to see if it increases the crystallinity or grain size. All films will receive a hydrogenation in the HW system, followed by top n+ (283 pieces) or p+ (281 pieces) if needed. The HW system has been unavailable for almost two months due to pump failure. Repair has been hindered by the pump's age and by difficulty of finding replacement parts. A used pump has been purchased and will be installed. Devices will be completed with ITO/Ni grids. Bifacial characterization will be performed since they are transparent on both sides and a priori we don't know where the junction will be.

TASK 4: IN-LINE PROCESS DIAGNOSTICS

Attached is a paper presented at the WCPEC-4 which is a good summary of recent work under this task.

Thin Film Partnership Team Activity

Researcher Ujjwal Das and graduate student Meijun Lu attended the Thin Si Team meeting in San Francisco in April. They made a presentation on our AIC work and participated in other discussions.

Best regards,

Robert W. Birkmire
Director

RWB/eak

Cc: Brian McCandless, IEC
Kevin Dobson, IEC
Steven Hegedus, IEC
Paula Newton, IEC
Susan Tompkins, OVPR UD
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