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INSTITUTE OF ENERGY CONVERSION

UNITED STATES DEPARTMENT OF ENERGY
UNIVERSITY CENTER OF EXCELLENCE
FOR PHOTOVOLTAIC RESEARCH AND EDUCATION

October 3, 2006

Bolko von Roedern
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

RE: NREL Subcontract # ADJ-1-30630-12 D5.5

Dear Bolko,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of 6/16/2006 to 7/15/2006 under the subject subcontract. The report highlights progress and results obtained under Task 3 (Si-based Solar Cells).

TASK 3: Si-BASED SOLAR CELLS

Aluminum Induced Crystallization (AIC)

In the previous monthly report (April 2006), we presented initial results from new AIC experiments above and below the eutectic temperature and proposed device structures to use these layers to create highly conductive "seed" layers for subsequent HW Si growth. Incorporation of heavily doped p+ large grain seed layers by AIC will be evaluated using different structures. Two different kinds of absorber layers (i-type µc-Si & p-type µc-Si) and two different emitter layers (n-type a-Si & n-type µc-Si) are planned. Both absorber layers and emitter layers will be deposited by HWCVD. Here, we report the status of that work and also other experiments.

AIC seed layers for thin Si film solar cell

Seed layers made from the normal structure—glass/Al/a-Si— annealed below eutectic temperature. Samples have been deposited (0.5 µm Al by e-beam, 0.4 µm a-Si by HWCVD) and annealed (450^{o}C, 6 hr). The Al was etched away, leaving Al-doped Si seed layers for the further µc-Si deposition by HWCVD. XRD measurements and OM pictures prove that a-Si was crystallized with grains of 10-20 µm, which were partly shown in previous monthly report.

Electrical conductivity of the seed layer was measured with a 4-point probe and results are in Table I.

Table I. Resistivity of AIC layers on glass.

Sample ID	Sample description	Resistivity (Ohm.cm)
HW296-13	7059,HWCVD	0.0673
HW296-23	1737,HWCVD	0.0658

These are close to values from other groups (e.g. Nast's group reported 0.041 Ω•cm). This may not be low enough for a good contact layer, but we will still continue to process these layers with further HWCVD deposition to grow large grain p-i-n solar cells. However, Si layer deposition in the HWCVD system was delayed due to a failed backing pump. Due to its age, it could not be repaired and had to be replaced. Then the HW filament had to be replaced. Deposition of Si devices on seed layers is planned for the next reporting period.

Seed layers of the reverse structure—glass/a-Si/Al— annealed above eutectic temperature were also made. Deposition (0.5 μm Al by e-beam, 0.4μm a-Si by HWCVD) and annealing (600°C, 6 hr) are completed. XRD confirmed that the a-Si was crystallized from the XRD measurement (Fig.1). No Al etching was needed for this type of seed layer as described before. Seed layers are ready for the further absorption layer (μc-Si) deposition by HWCVD. Electrical properties are still under investigation.

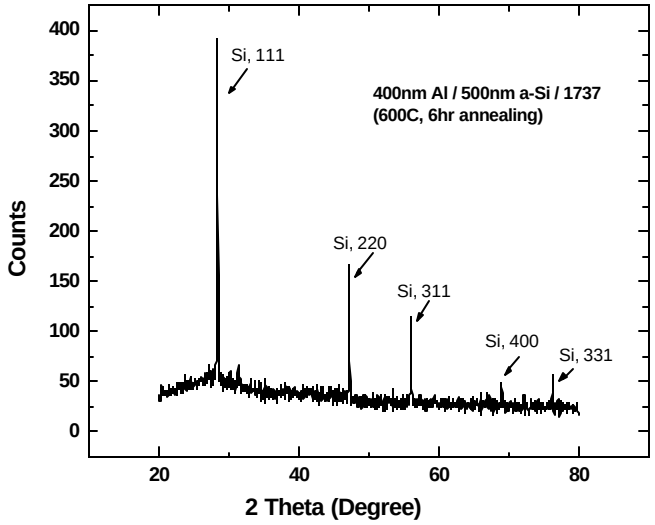

Figure 1. XRD for reverse structure sample annealed at 600°C, 6 hr.

More AIC Experiments

For the case of AIC with reverse structure annealed above the eutectic temperature, the normal layer exchange mechanism is not sufficient to explain the experimental results, since annealing is done above-eutectic temperature, and the critical oxide layer between Al and a-Si could have been destroyed by the liquid interface. To find out if the oxide layer also plays an important role

in the above- eutectic temperature annealing, and also if the crystallization was happening during liquid phase or during the cooling process, some more experiments are being performed:

Two sets of AIC experiments are being investigated:

1. Reverse structure, above-eutectic but with different cooling down: fast, normal and slow.
2. Reverse structure, above-eutectic, with and without oxide layer between Al and a-Si.

For each set, two types of glasses (1737 & 7059) are used as substrates. Hence, samples can be described by the following table:

Table II. Sample matrix for new AIC experiments above eutectic.

	Normal cooling down (~10min)	Quick cooling down ("quench"~1min)	Slow cooling down (~hours)
Reverse, with oxide layer (a-Si deposited by HWCVD, Al by e-beam)	7059, 1737 (6hr, 600°C)	7059, 1737 (6hr, 600°C)	7059, 1737 (6hr, 600°C)
Reverse, no oxide layer (both a-Si and Al are deposited by e-beam)	7059, 1737 (6hr, 600°C)	7059, 1737 (6hr, 600°C)	7059, 1737 (6hr, 600°C)

Presently, all samples have been deposited and annealed. XRD, Raman and OM measurements are in progress. The measured samples are all crystallized. Results will be reported when available.

Solid Phase Crystallization (SPC)

This section reports on results of fabricating nc-Si devices from a-Si via SPC or rapid thermal processing (RTP) without the aid of AIC. Table III lists device structures that were deposited by HWCVD for further SPC and RTP study. HW281 (n+/i) and HW283 (p+/i) are partially completed devices lacking a second doped contact or emitter, while HW282 (n+/i/p+) and HW284 (p+/i/n+) are completed devices. Conditions for the doped layers were the same except for the dopant gas. The i-layers were 1.5 μm and deposited under conditions known to give amorphous Si not nc-Si. There were 4 types of substrates in each deposition: 1) 7059 glass; 2) ZnO on 1737; 3) ZnO on 7059; and 4) Tec 15 SnO_2 on soda-lime glass (SLG). After SPC, samples on SLG/Tec15 substrates deformed due to melting, the Si films were severely cracked, and are not included further. Raman measurements verified that there is no nc-Si in these devices as deposited.

Table III. Device structures deposited by HWCVD for SPC.

Run #	***Structure***
HW281	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 um)
HW282	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 um) / a-Si:H.p+ (20nm)
HW283	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 um)
HW284	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 um) / a-Si:H.n+ (20nm)

The sequence for processing was deposition of the above structures by HWCVD; dehydrogenation at 400 or 500°C; SPC at 600°C; some samples received RTP at 750°C; hydrogen repassivation by HWCVD at 400°C followed by deposition of doped emitter or contact on some incomplete structures; finally ITO and Ni/Al grids. We previously reported (January and April 2006) evaluating the effect of dehydrogenation for 4 hours at 400 or 500°C followed by SPC at 600°C for 64 or 100 hours in H_2/Ar. Select samples received RTP consisting of 5 thermal spikes of ~1sec each from a bias point of 600°C up to 750°C under moderate vacuum (150 mT). The fraction crystallinity was evaluated by Raman spectroscopy, and grain size was determined from the (111) peak obtained from XRD. All 4 types of device structures on 7059/ZnO had larger grain size compared to the same 4 structures on 1737/ZnO. However, the grain size on all samples was only in the range of 40-70 nm as shown in Table IV.

Table IV. Crystalline fraction, grain (particle) size for device structures annealed at 600°C for 64 or 100 hours, having different substrates, and type of deposited doped layer to complete the device after SPC and hydrogenation. HW284-13 had an as-deposited n-layer top contact followed by a nc-Si n-layer after SPC and hydrogenation. HW282-12 and -22 and HW284-12 and -22 pieces were deposited as nip or pin and did not receive post-SPC doped layers. X means grain size was not measured on that particular piece.

Sample	Structure	Grain Size (nm)	Post SPC deposited layer	V_{oc} (V)
HW281-12	1737/ZnO/n-i	39	p a-Si	0.06
HW281-13	7059/ZnO/n-i	54	p a-Si	0.01
HW281-22	7059/ZnO/n-i	X	p nc-Si	0.13
HW283-12	1737/ZnO/p-i	33	n a-Si	0.08
HW283-13	7059/ZnO/p-i	46	n a-Si	0.00
HW283-22	7059/ZnO/p-i	X	n nc-Si	0.00
HW284-13	7059/ZnO/p-i-n	47	n nc-Si	0.06
HW282-12	1737/ZnO/n-i-p	38	none	0.01
HW282-22	7059/ZnO/n-i-p	56	"	0.00
HW284-12	1737/ZnO/p-i-n	37	"	0.08
HW284-22	7059/ZnO/p-i-n	47	"	0.08

All pieces receiving the RTP warped, and either the glass cracked or the Si film had visual cracks. They were not processed into devices. All surviving films received a hydrogenation in the HW system. Structures from HW282 (n-i-p) and HW284 (p-i-n) did not need an additional doped layer so they received ITO/Ni grids after hydrogenation. Structures from HW281 (n-i) and HW283 (p-i) received a p or n doped layer, respectively, after hydrogenation to complete the device then ITO/Ni grids. Each type received an a-Si and nc-Si p or n layer. We have previously

seen large differences between a-Si and nc-Si used as deposited emitters or contacts for c-Si . One device , HW284-13 which was already a complete p-i-n cell received a second nc-Si doped n-layer after hydrogenation to see if this additional doped layer gave a better junction or contact.

Typically, a-Si devices which are crystallized by SPC or RTP receive a post-crystallization hydrogenation step to passivate grain boundary defects since all H has evolved during the high temperature annealing. Hydrogenation was performed here in the HWCVD system with the following conditions: filament T=1750°C; substrate T=400°C; P=25 mT; and H_2=20 sccm. Following the hydrogenation step, devices from HW281 and HW283 received their final doped layer (both amorphous and nanocrystalline were used). Devices were completed with ITO/Ni grids.

Table IV lists the V_{oc} for the different device structures. They are all very low. The JV curves for several devices are shown in Figure 2 (the n-i-p devices) and Figure 3 (the p-i-n devices). Only HW283-33 is clearly shunted. The others all indicate some diode behavior along with high resistance. Devices with the nc-Si deposited layer had higher currents at forward bias indicating better emitter injection or lower resistance, but there was negligible photocurrent or photovoltage in all cells.

Since all devices had poor performance, problems which would be common to all are being considered. One obvious one is the hydrogenation step. We did not attempt to optimize or explore other conditions. Further, we have since determined that our H_2 gas is contaminated with C and O since a low purity grade was purchased by mistake. This contaminated H_2 was used to perform hydrogenation. A higher purity cylinder had been installed and lower C and O in the films confirmed by FTIR. Samples with and without hydrogenation will be sent to NREL for SIMS to see if contaminants are present as-deposited or after hydrogenation.

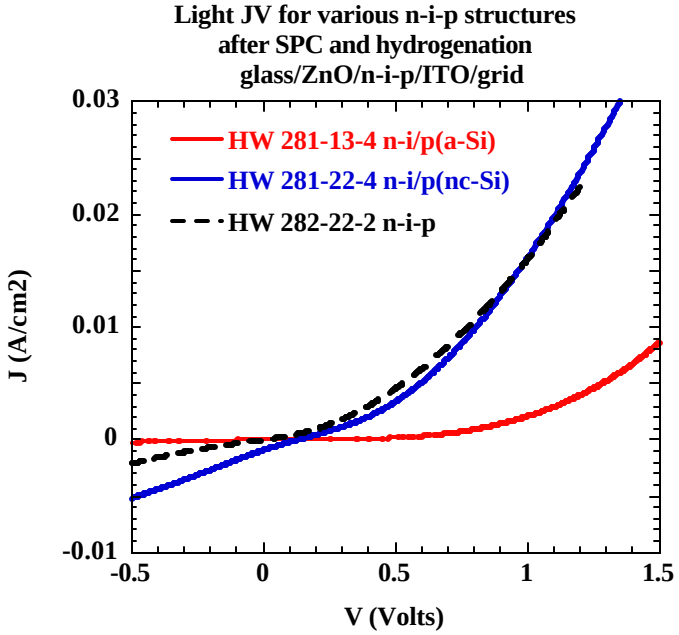

Figure 2. JV curves for n-i-p devices with 3 different p-layers: a-Si and nc-Si deposited after SPC and hyrodgenation, and as-deposited p.

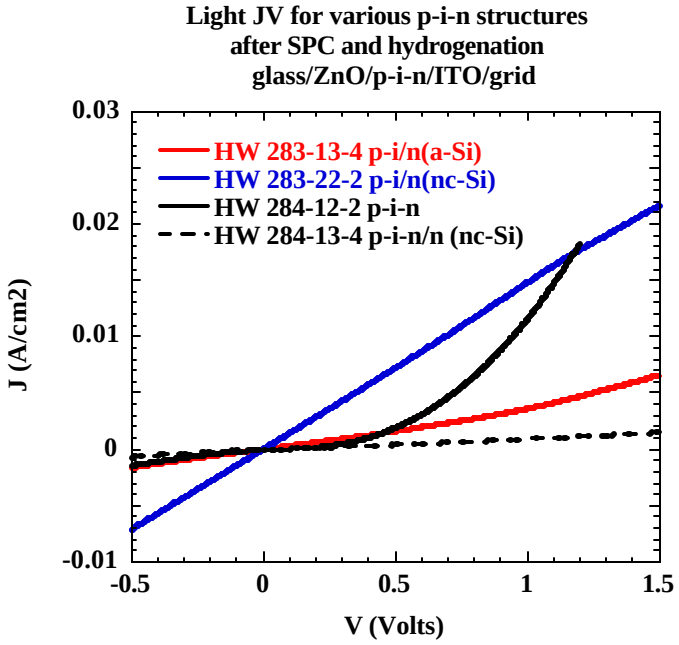

Figure 3. JV curves for p-i-n devices with 4 different n-layers: a-Si and nc-Si deposited after SPC and hydrogenation, as-deposited n, and as-deposited with nc-Si deposited after SPC and hydrogenation.

Best regards,

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