CPT Week
Trigger Session
April 15, 2002

Status and Schedule of HCAL Trigger and Readout

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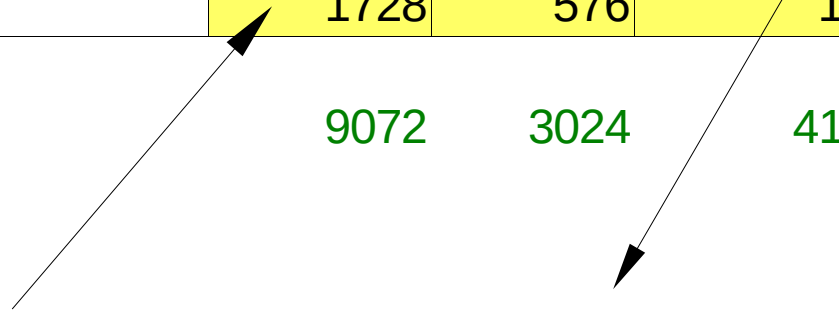
HCAL readout group:
Boston, Fermilab, Illinois Chicago, Maryland, Princeton

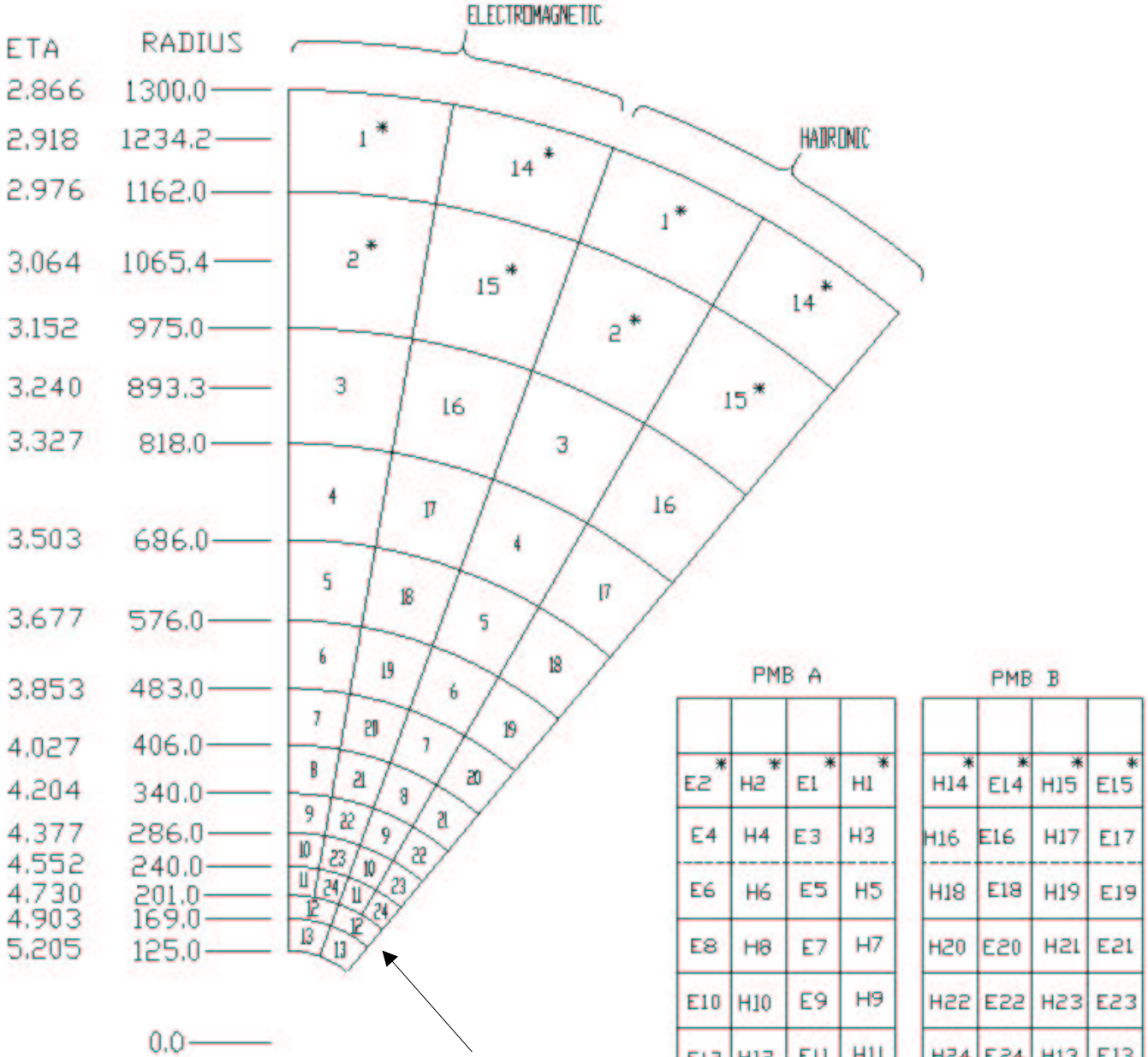
HCAL Channel Count

	channels	fibers	trig towers	SLB	HTR	crates	HTR/crate
HB (pure)	1728	576	1728	216	36	3	12
HB/HE overlap	1728	576	864	108	36	3	12
HE (pure)	1728	576	1440	180	36	3	12
HO	2160	720	*		48	4	12
HF	1728	576	144	18	36	3	12
TOTAL	9072	3024	4176	522	192	16	



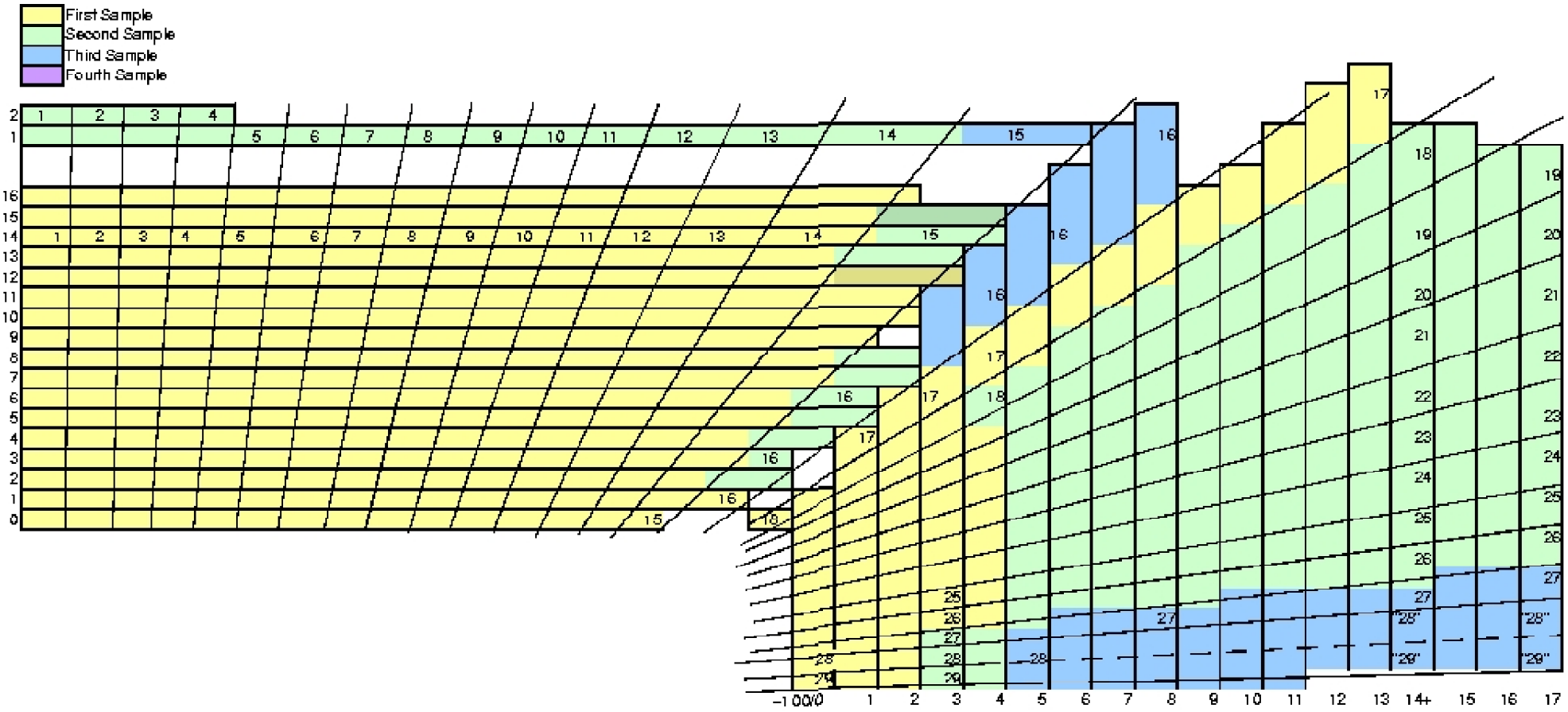
New

96 trigger bit streams (working proposal)

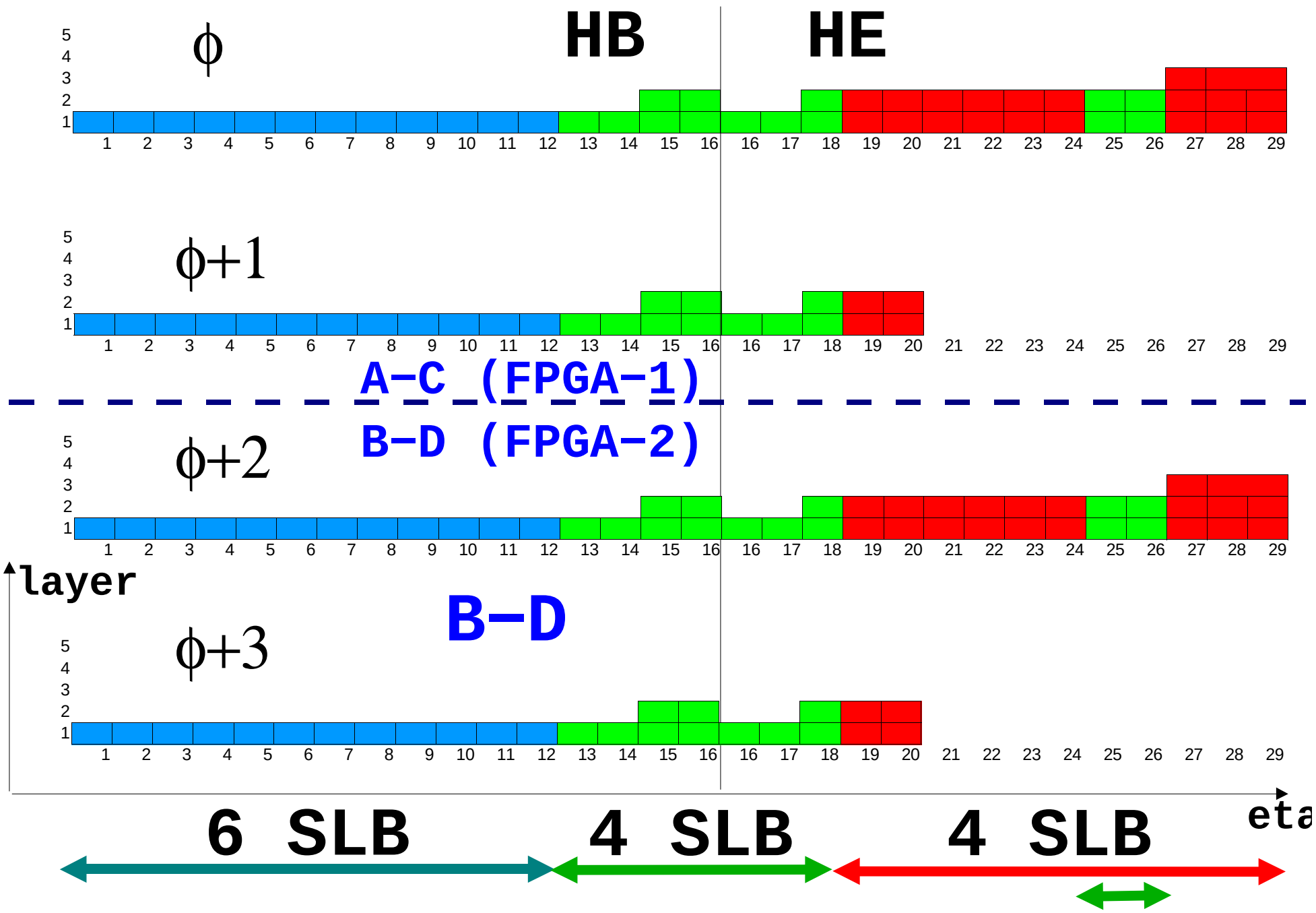


New
(20 phi seg.)

HCAL Segmentation



20° slice: 144 ch. (3 HTR)



HO Trigger Bit Mapping: $8 \times 12 = 96$ links

bit stream 1

bit stream 2

bit stream 3

bit stream 4

bit stream 5

bit stream 6

bit stream 7

bit stream 8

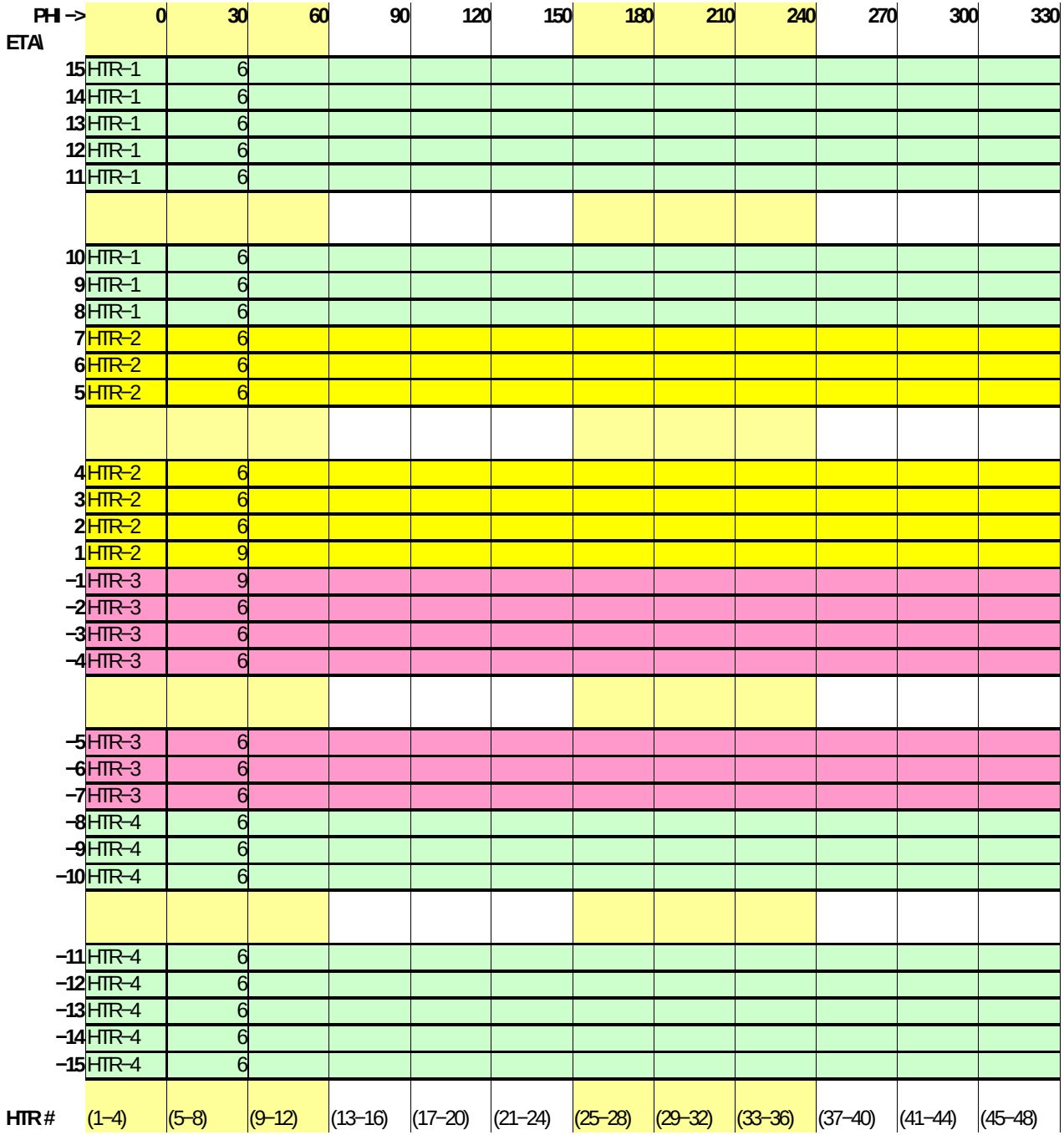
Ring 2

Ring 1

Ring 0

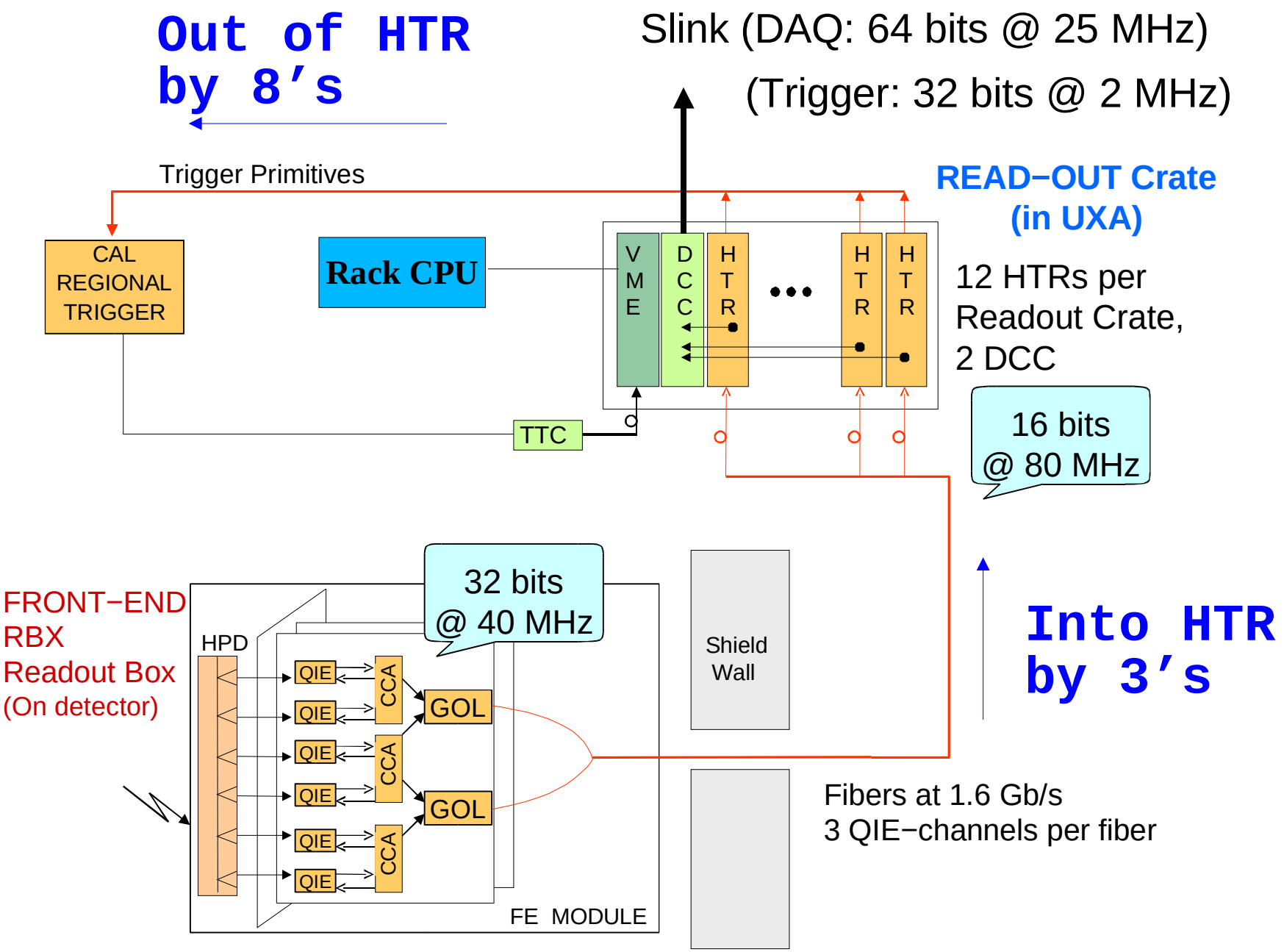
Ring −1

Ring −2

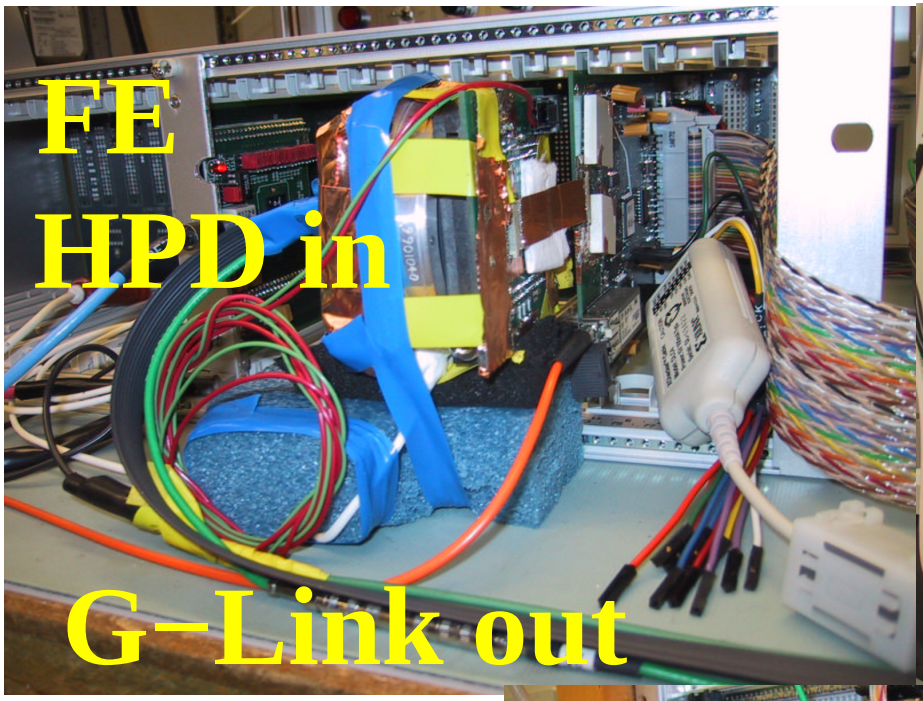


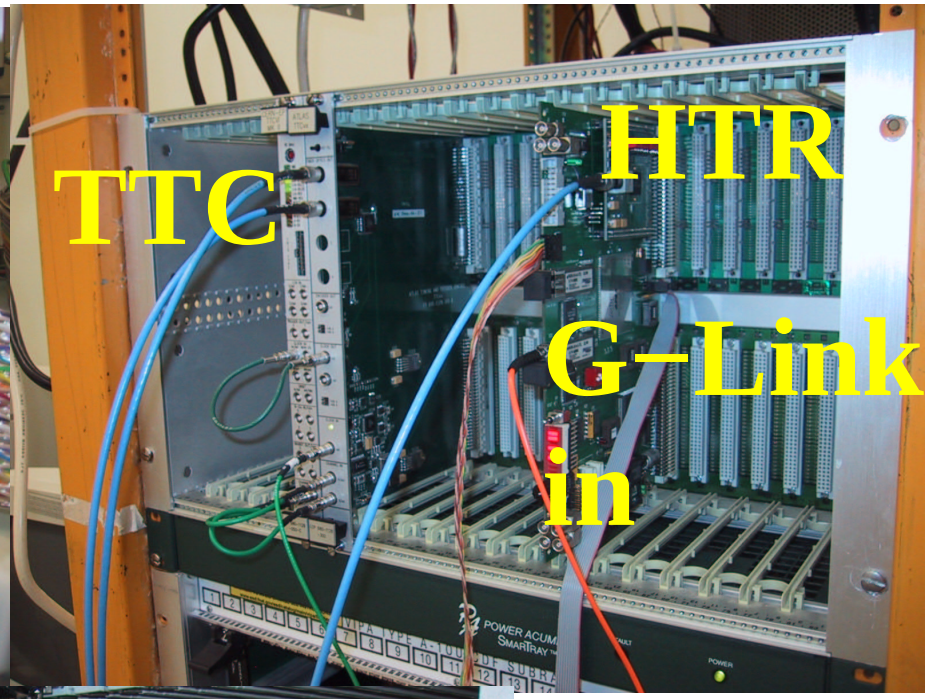
PHI ->	0	30	60	90	120	150	180	210	240	270	300	330
ETA\												
15	HTR-1	6										
14	HTR-1	6										
13	HTR-1	6										
12	HTR-1	6										
11	HTR-1	6										
10	HTR-1	6										
9	HTR-1	6										
8	HTR-1	6										
7	HTR-2	6										
6	HTR-2	6										
5	HTR-2	6										
4	HTR-2	6										
3	HTR-2	6										
2	HTR-2	6										
1	HTR-2	9										
−1	HTR-3	9										
−2	HTR-3	6										
−3	HTR-3	6										
−4	HTR-3	6										
−5	HTR-3	6										
−6	HTR-3	6										
−7	HTR-3	6										
−8	HTR-4	6										
−9	HTR-4	6										
−10	HTR-4	6										
−11	HTR-4	6										
−12	HTR-4	6										
−13	HTR-4	6										
−14	HTR-4	6										
−15	HTR-4	6										
HTR #	(1–4)	(5–8)	(9–12)	(13–16)	(17–20)	(21–24)	(25–28)	(29–32)	(33–36)	(37–40)	(41–44)	(45–48)

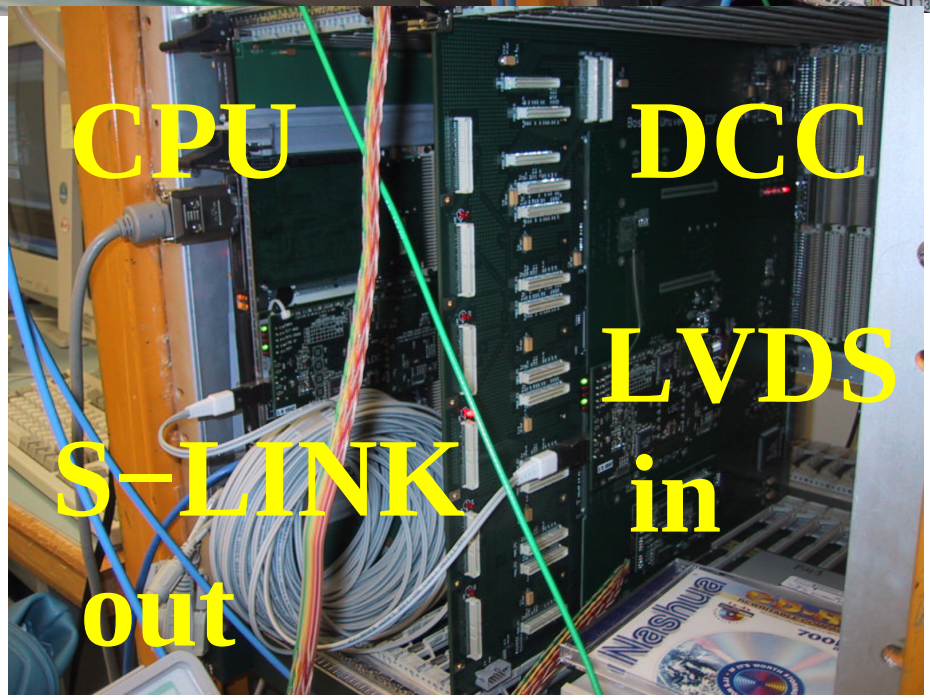
HCAL FE/DAQ Overview



HCAL Demonstrator

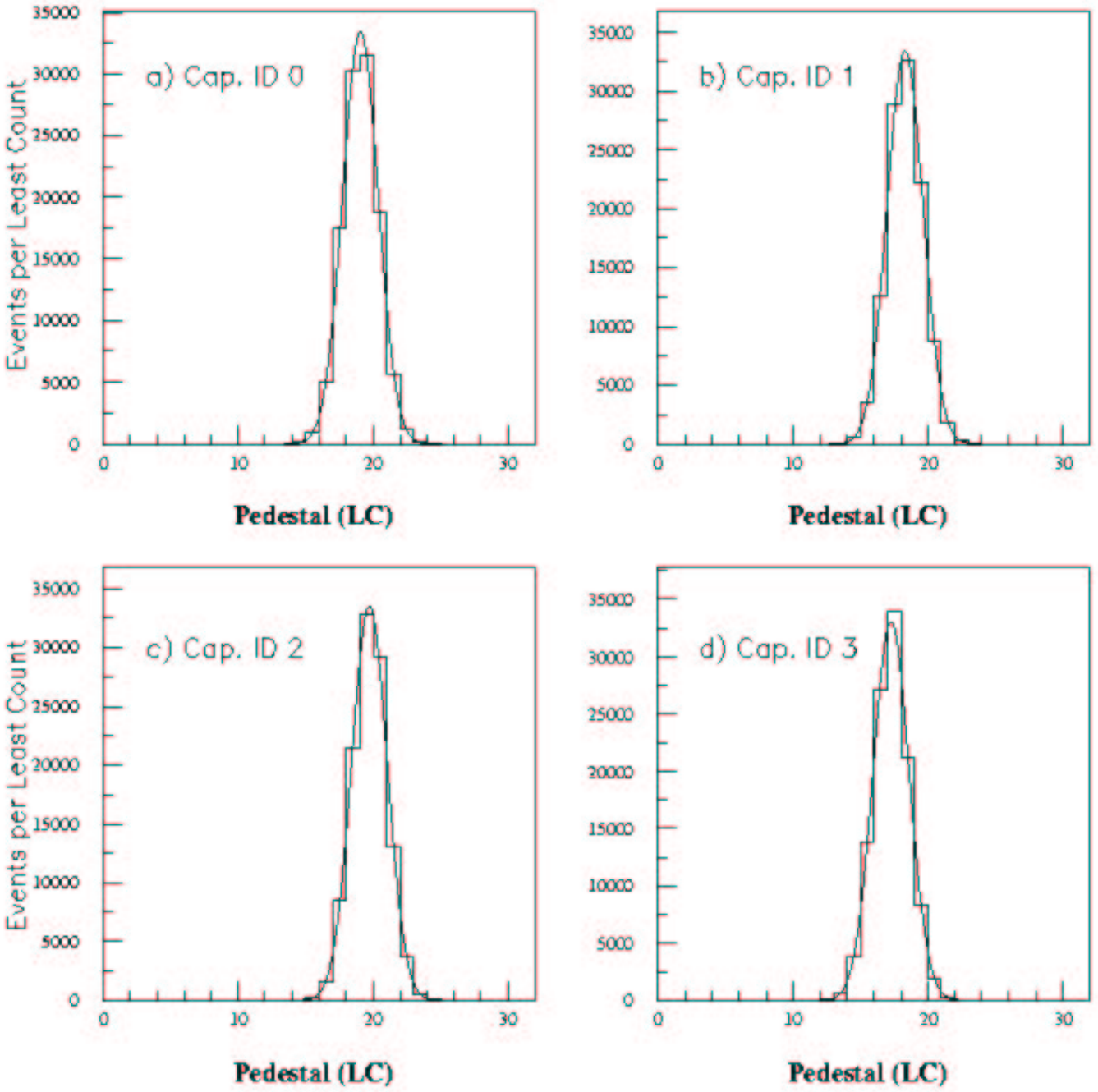




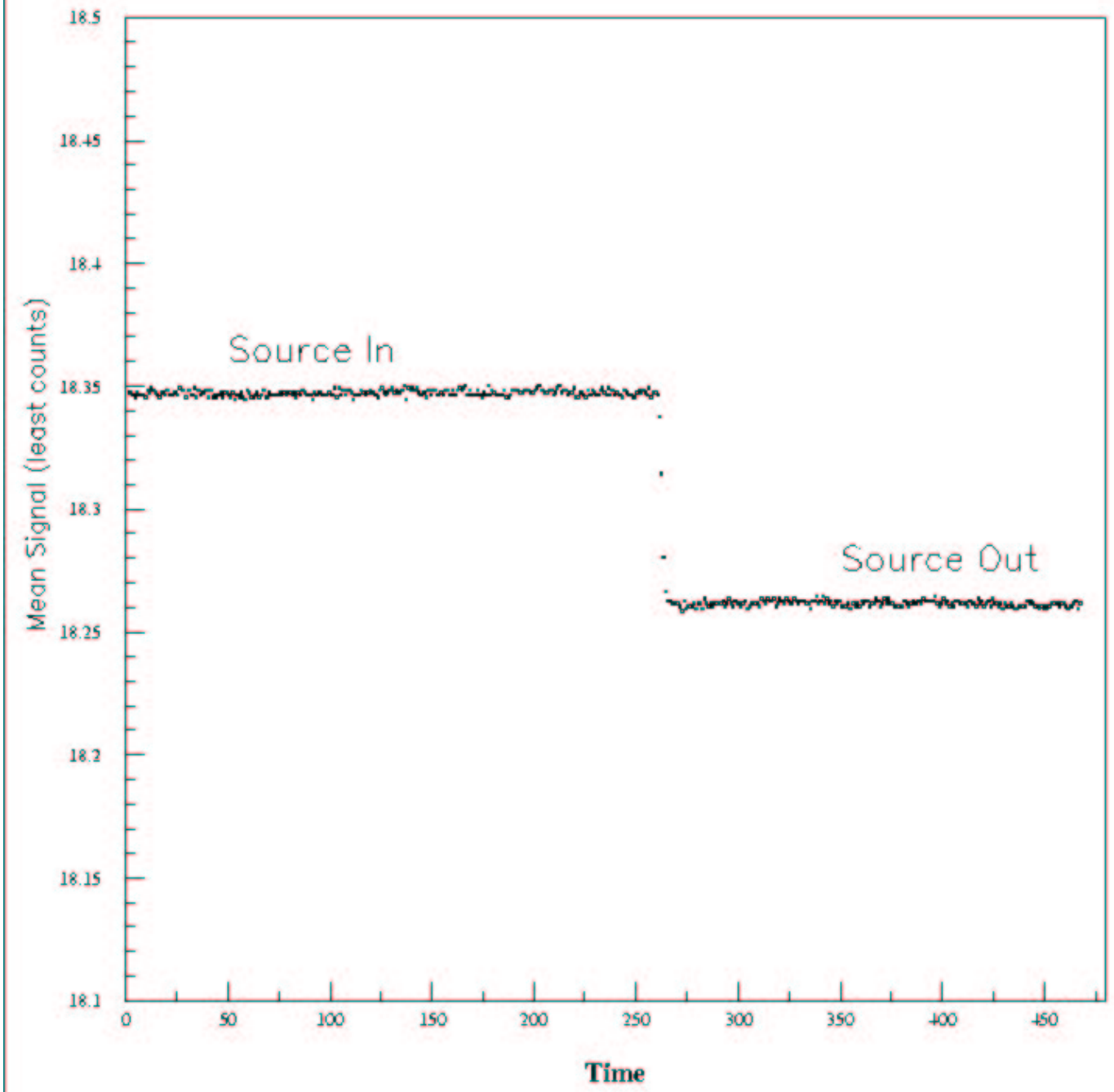


Pedestals: 2800 *e* noise

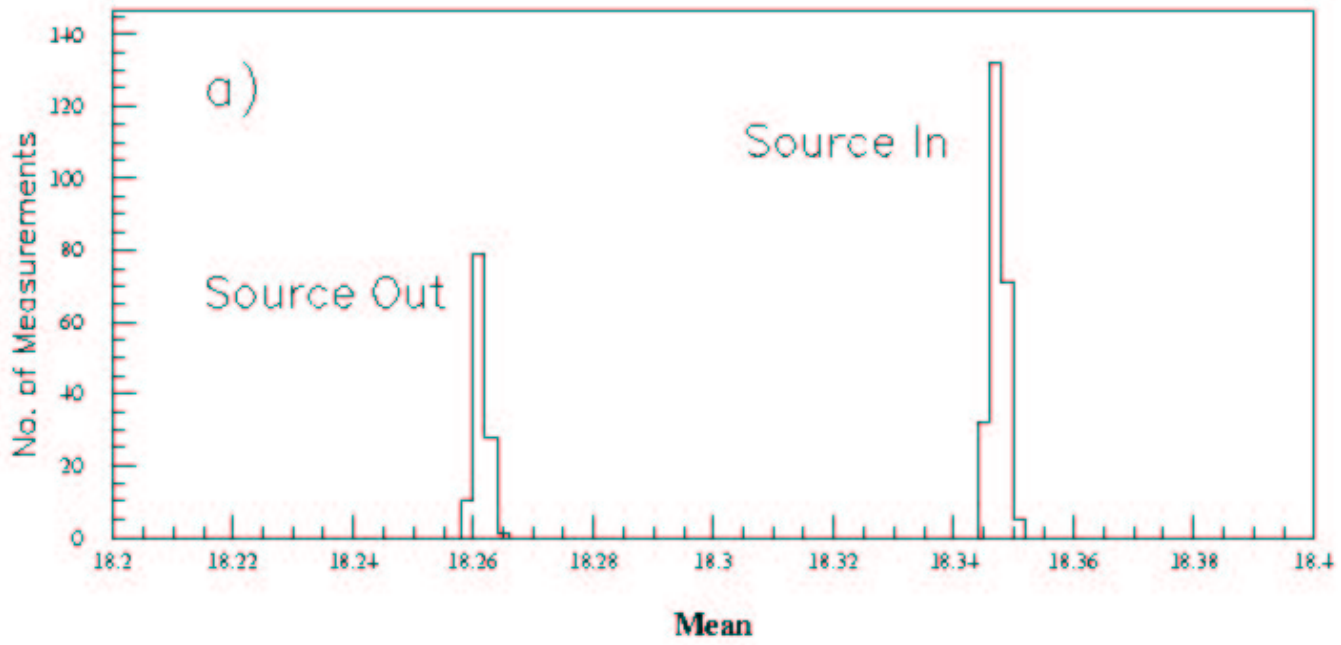
2002/03/15 12.35

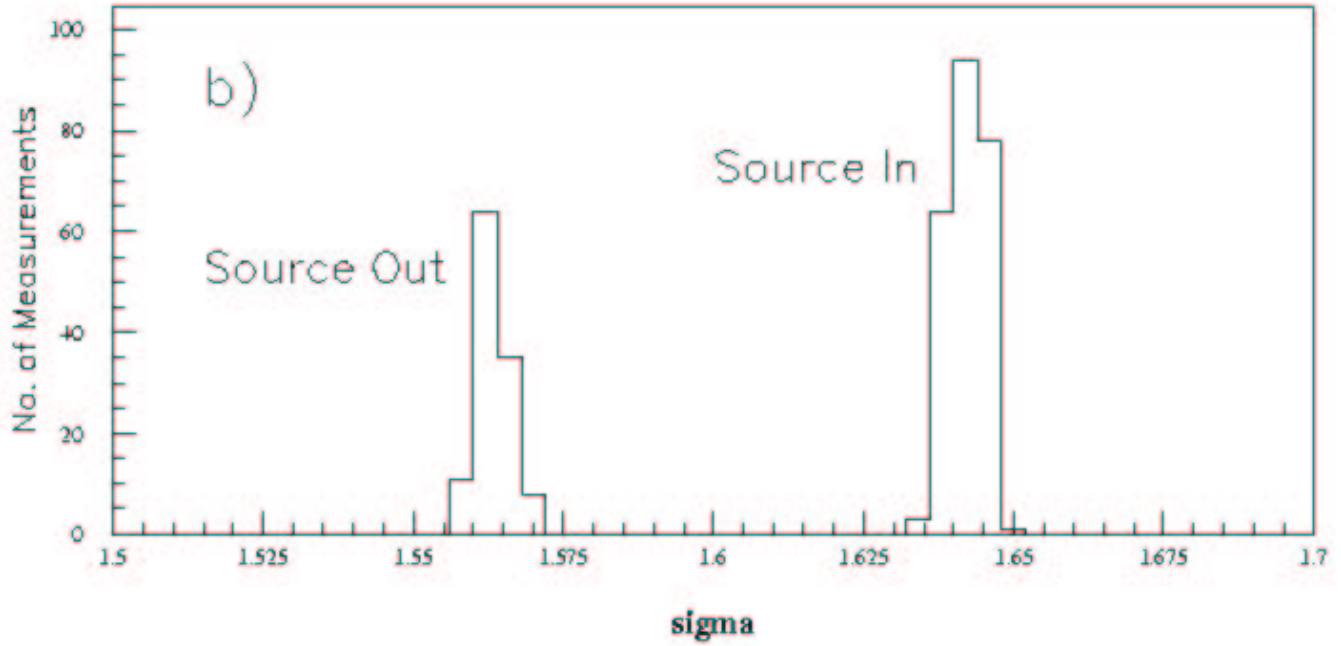


2002/03/28 14.06

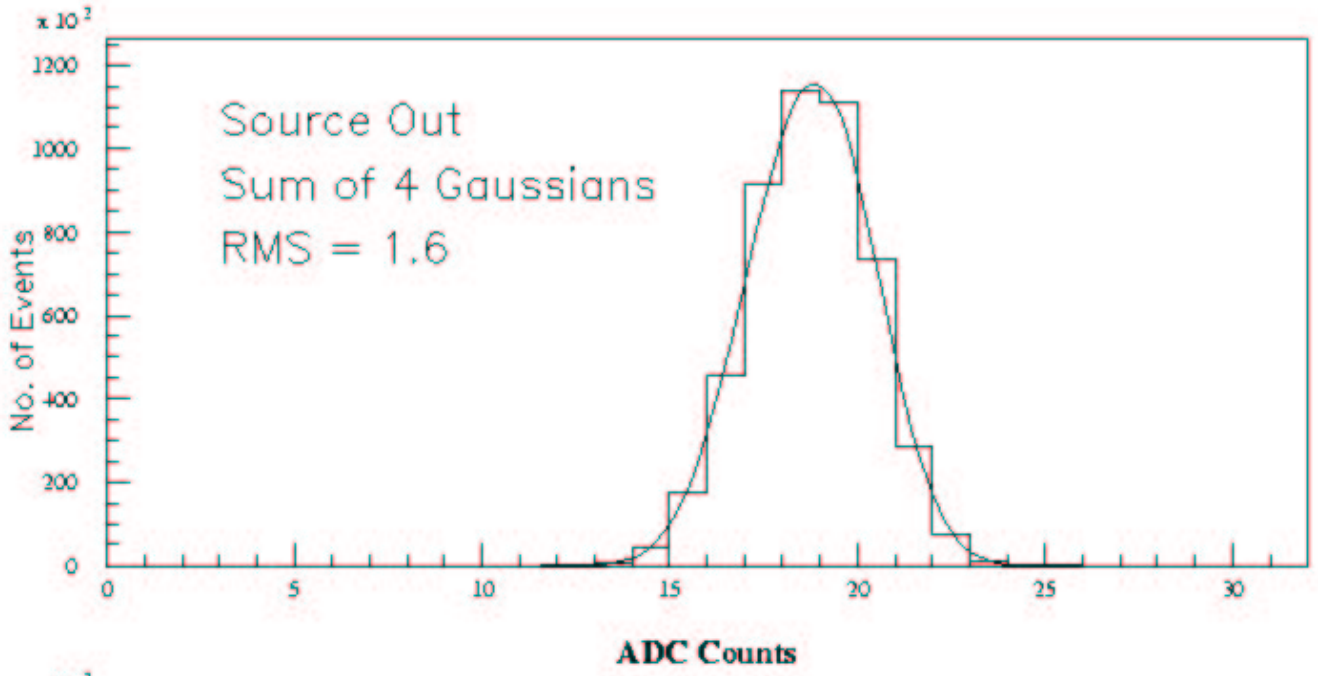


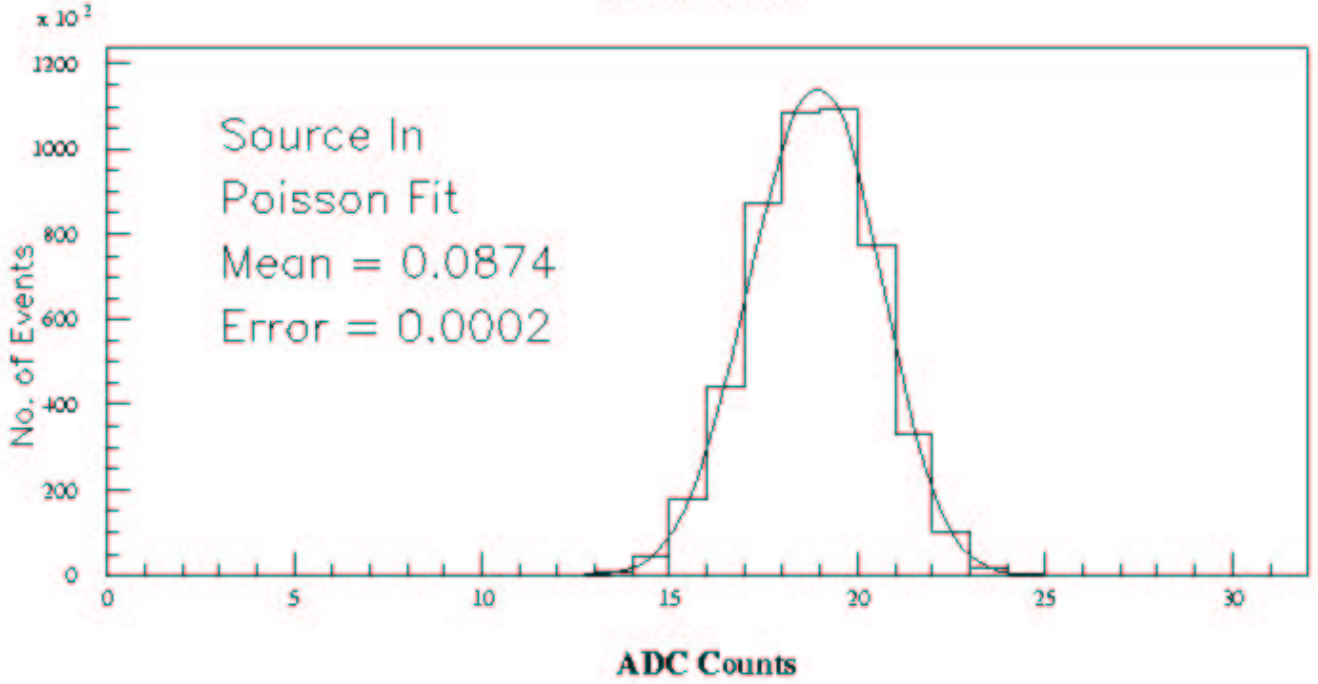
2002/03/15 12.13



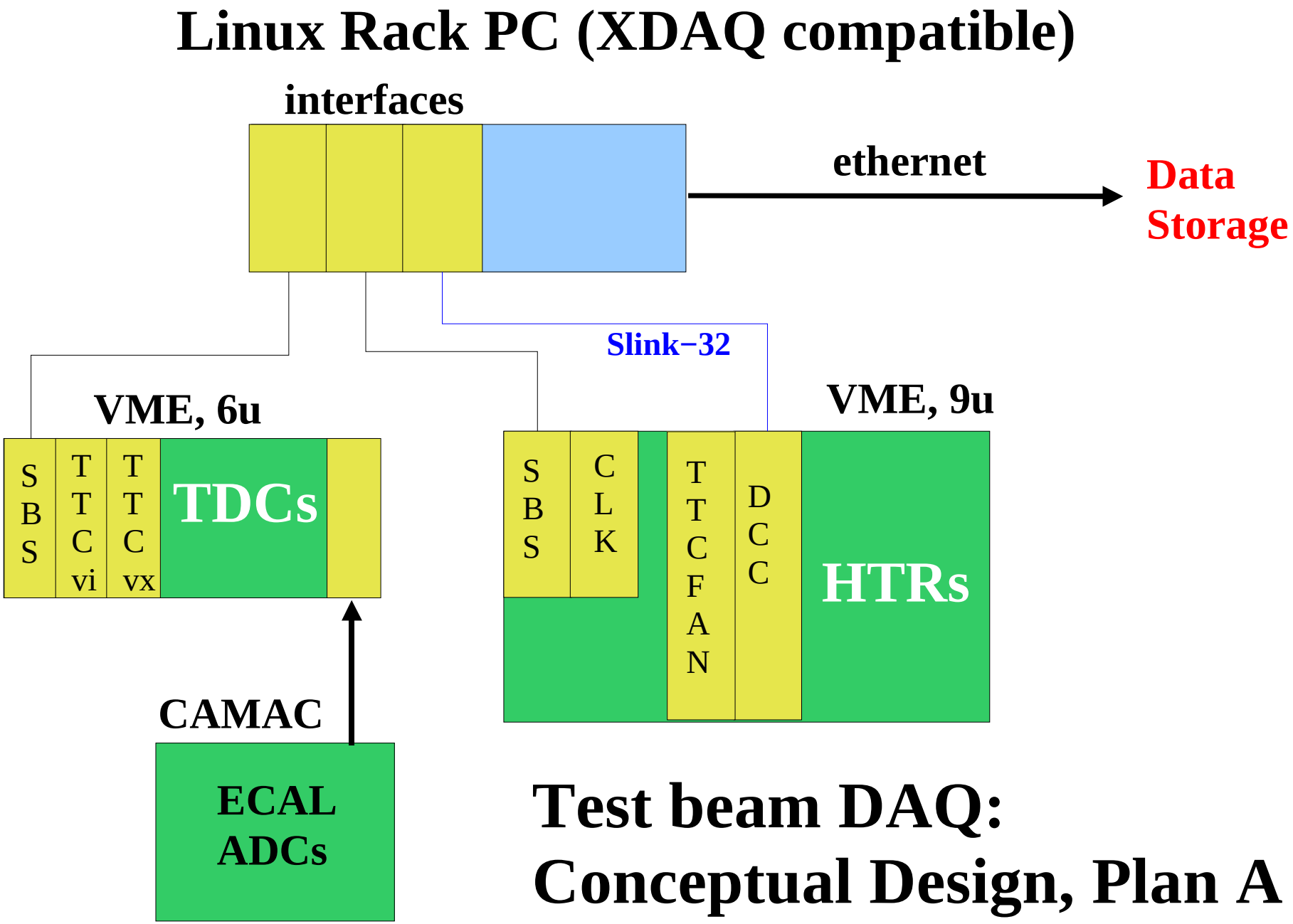


2002/04/03 14.35





Prototype Hardware: Test Beam 2002



Front End Status

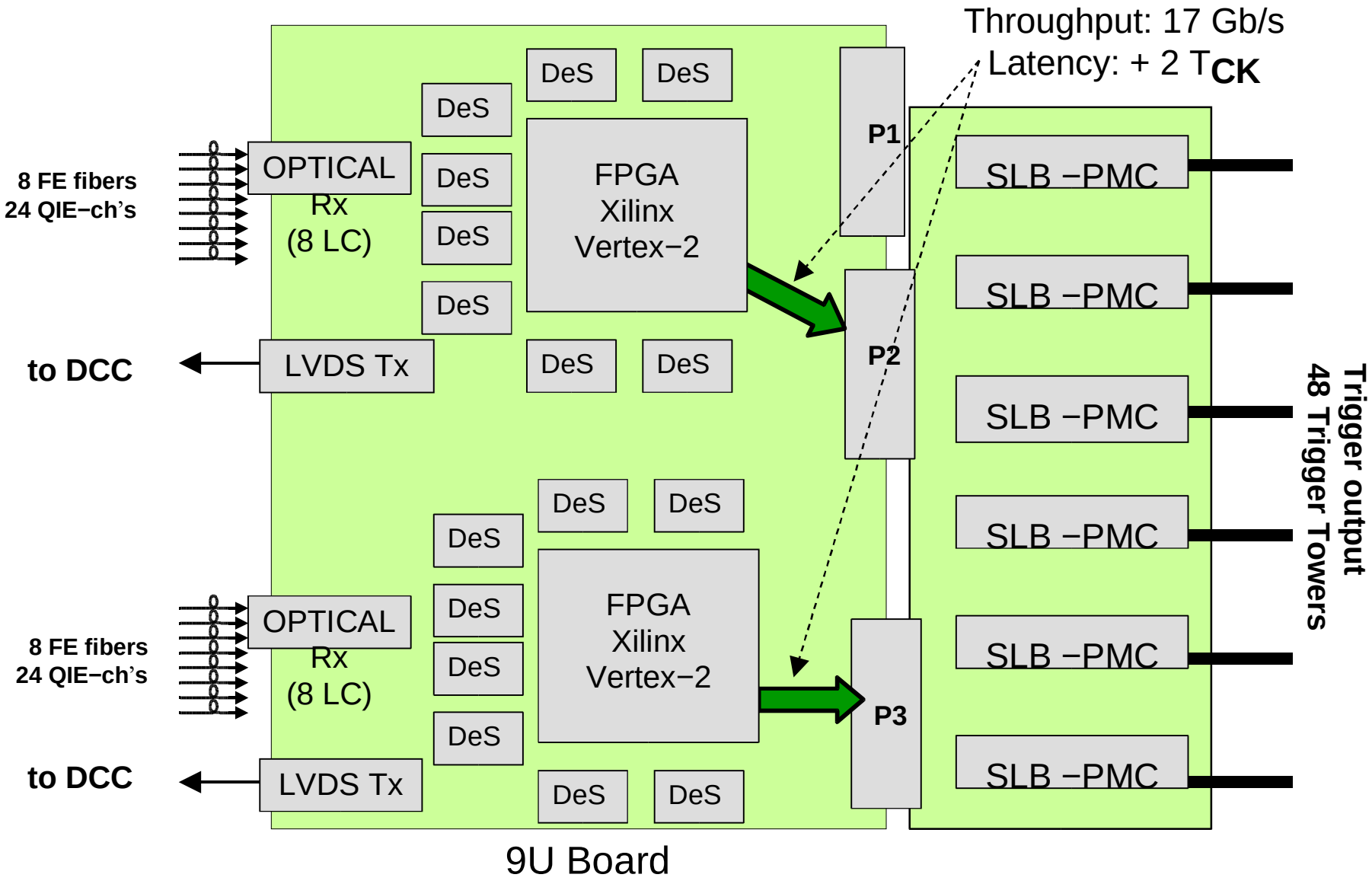
35 MHz production for test beam delivered;
to be tested starting this week

HF prototype tests (non−inverted input) starting now

Final production scheduled to start in Aug. 02

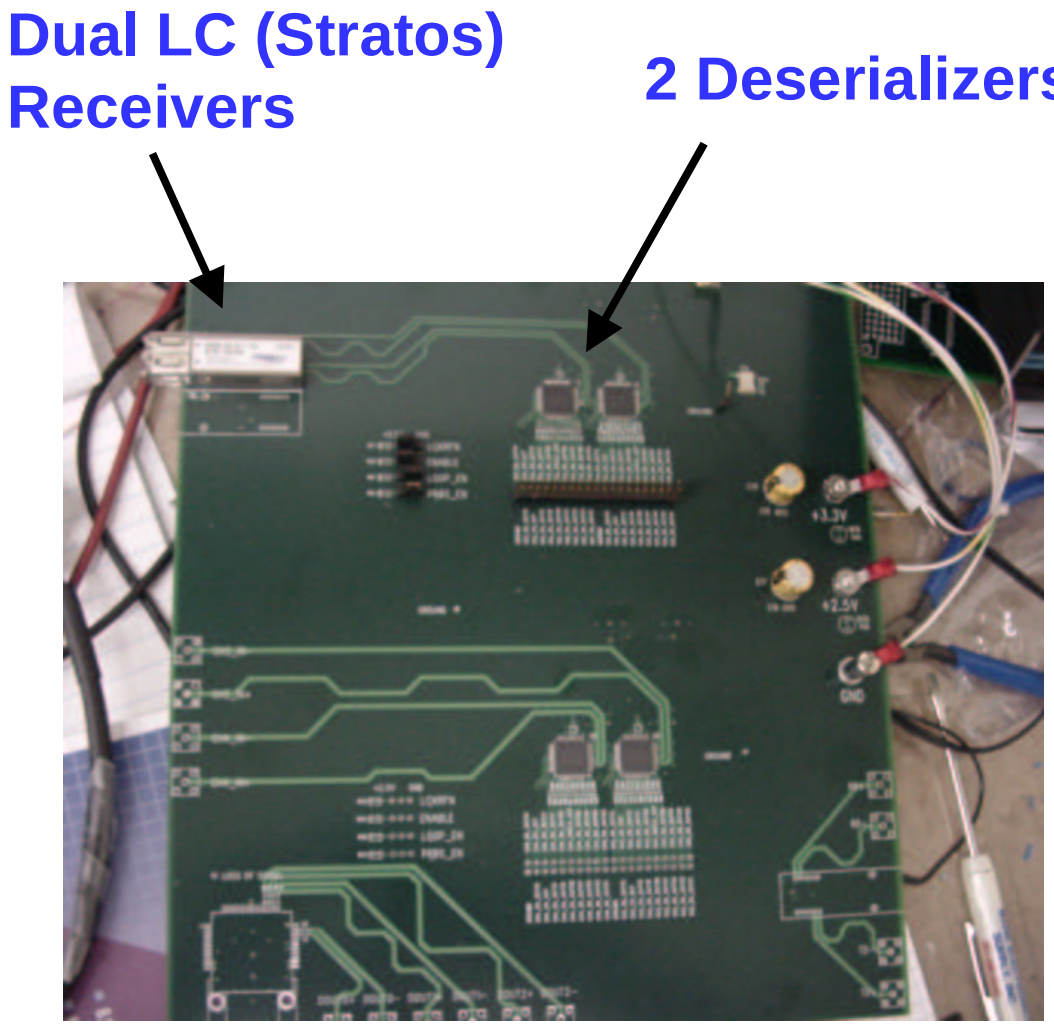
RBX installation in HB+ and HB− begins Nov. 02

HTR Prototype



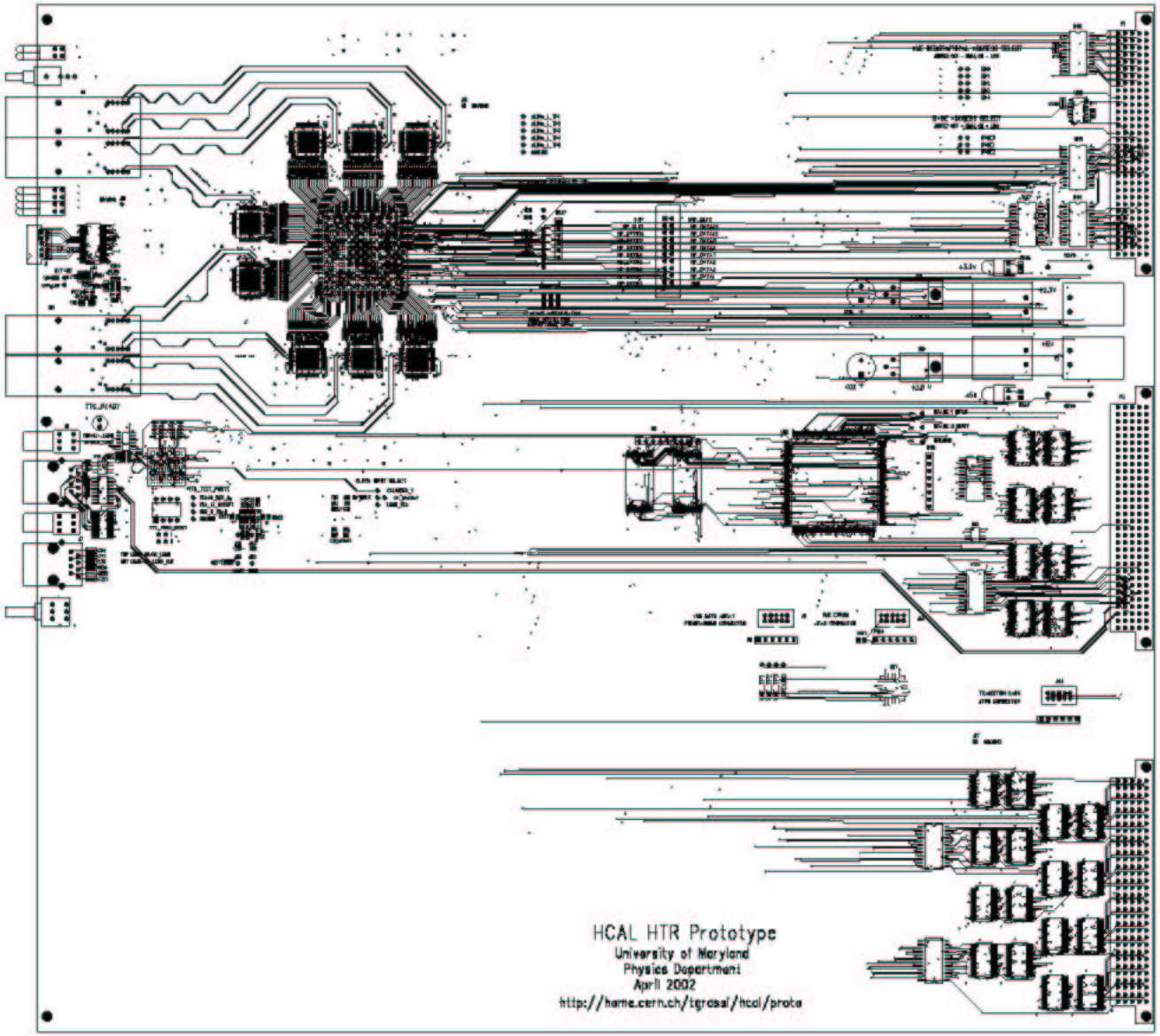
The links are better treated as major components rather than simple module interconnects.

"Link Only" Board, 1.6 GHz (GOL)

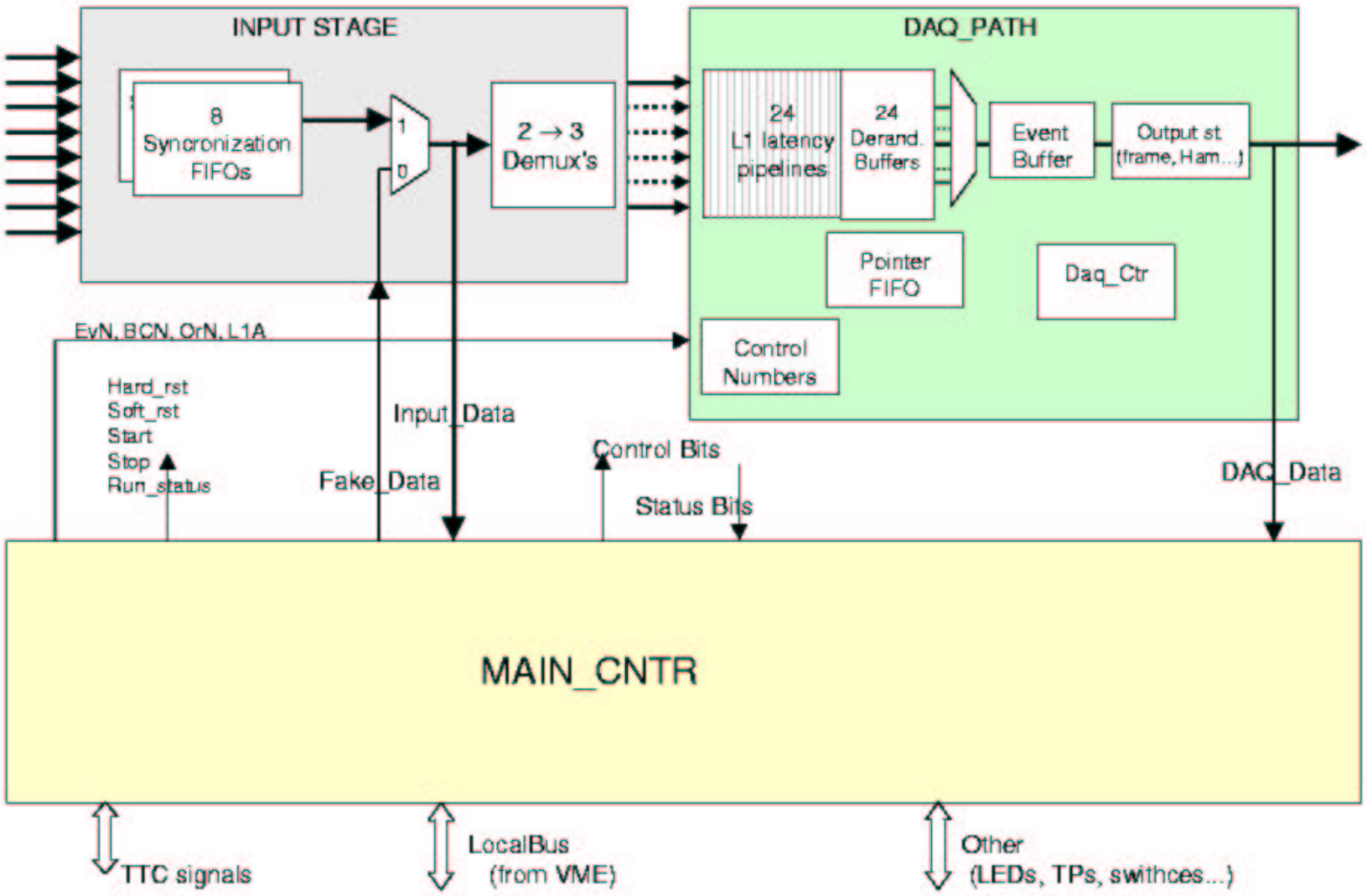


HTR Prototype, Stage I (24 ch.)

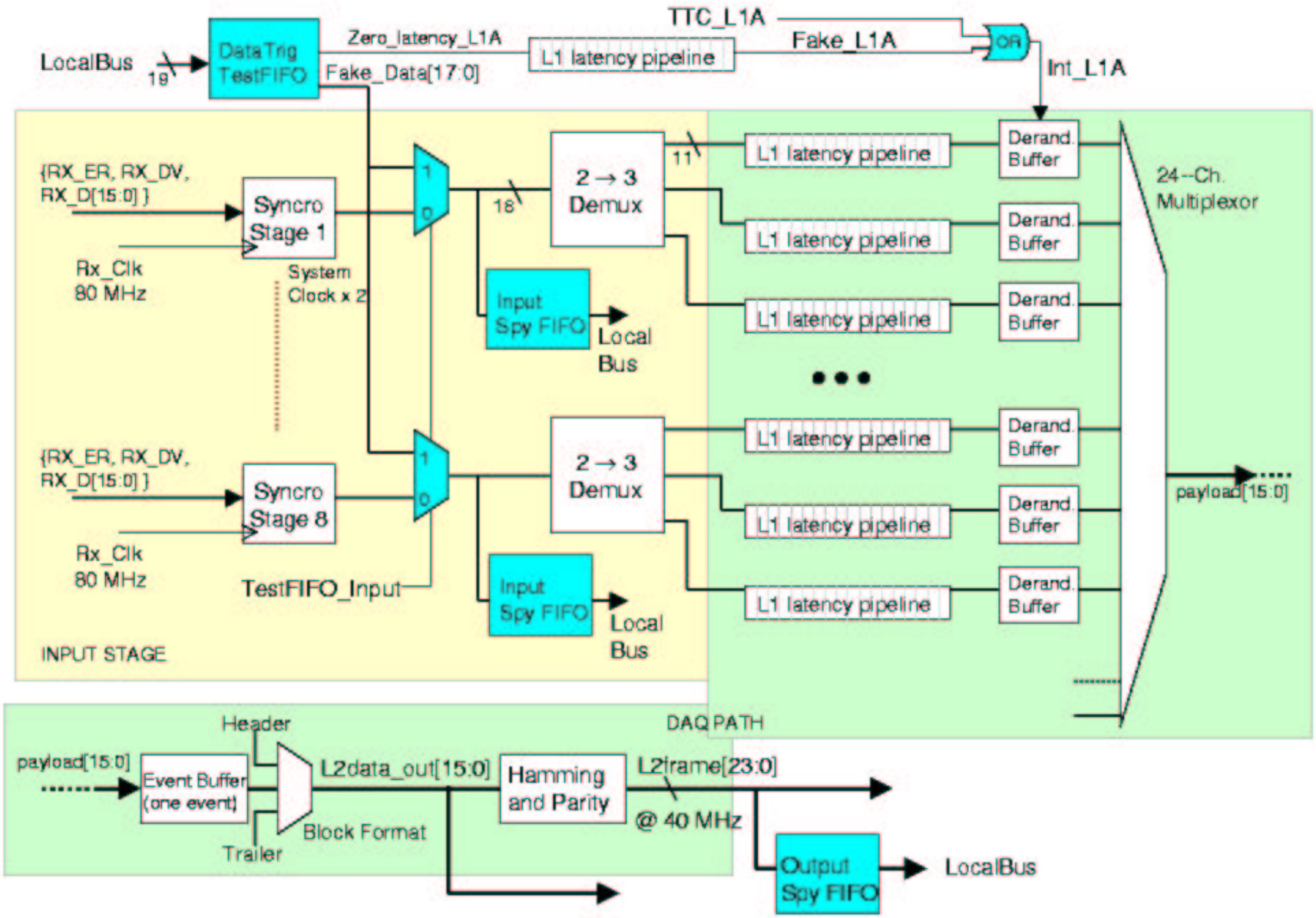
stuffed boards due this week



Main FPGA for Test Beam 2002 - Overview - version 1.0



Main FPGA for Test Beam 2002 - Data path



Summary of Recent HTR Progress

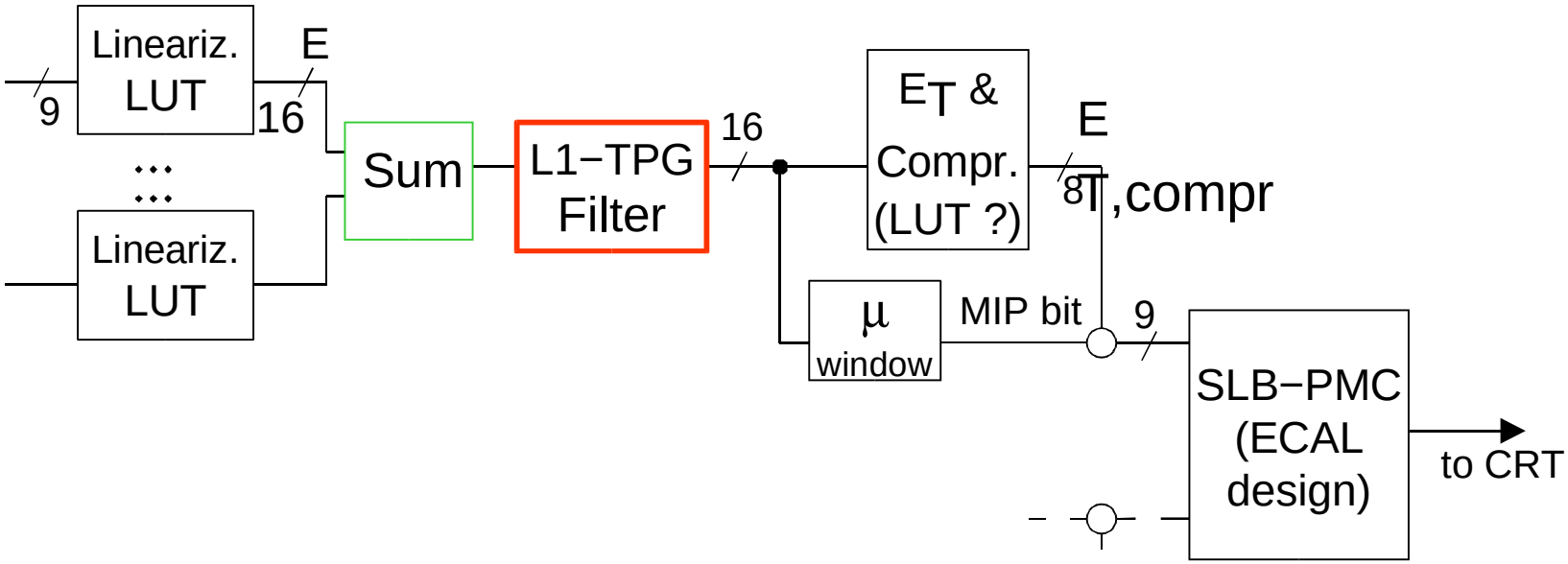
Drew Baden *et al.*

Jan: Designed Link−Only board.
Feb: Link−Only board tested OK in lab conditions.
March: Definition of clock scheme for TB readout create.
April: 24−ch, HTR being manufactured and stuffed.
We use clock and receiver parts targeted at 35 MHz.
If this board works, it will be used for TB2002.

NB: For schedule reasons the present HTR has only 24 channels and connections to one SLB board. Upgrading to a full 48−channel HTR occurs second half of 2002

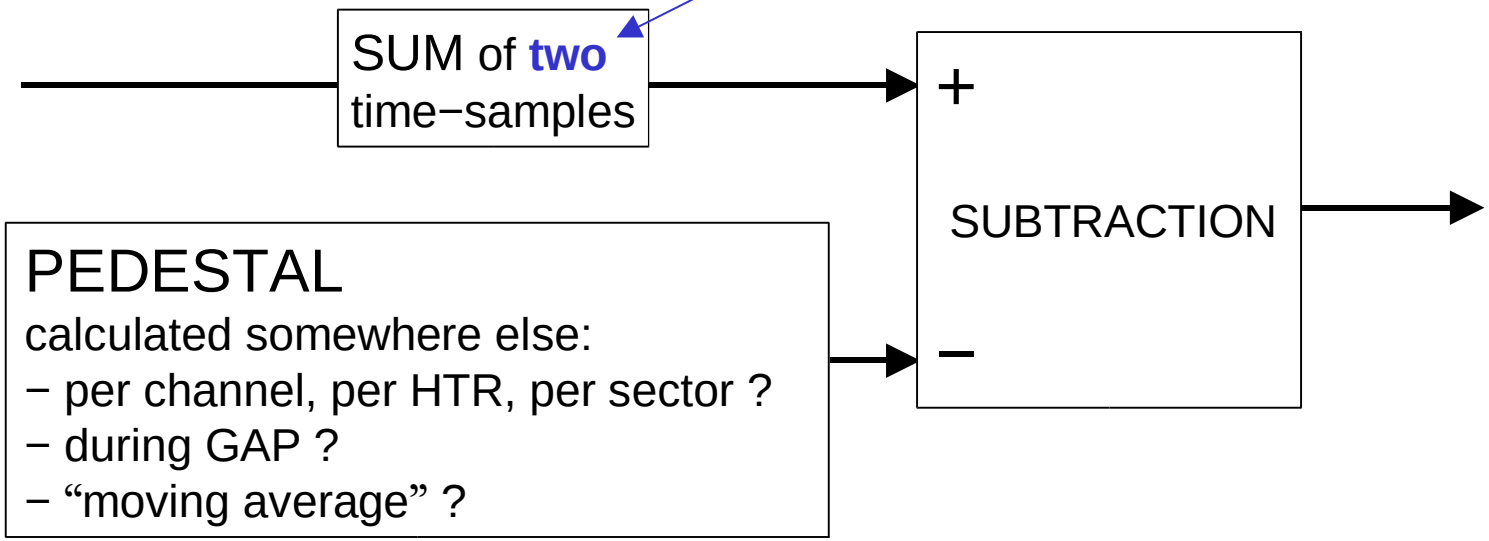
HTR VME interface: designed by G. Antchev (Boston)
HTR Main FPGA: under design by T. Grassi (Maryland)
on the critical path for TB2002
HTR Source calib. FPGA: to be done by S. X. Wu (Boston)

Energy Filter on the Trigger path



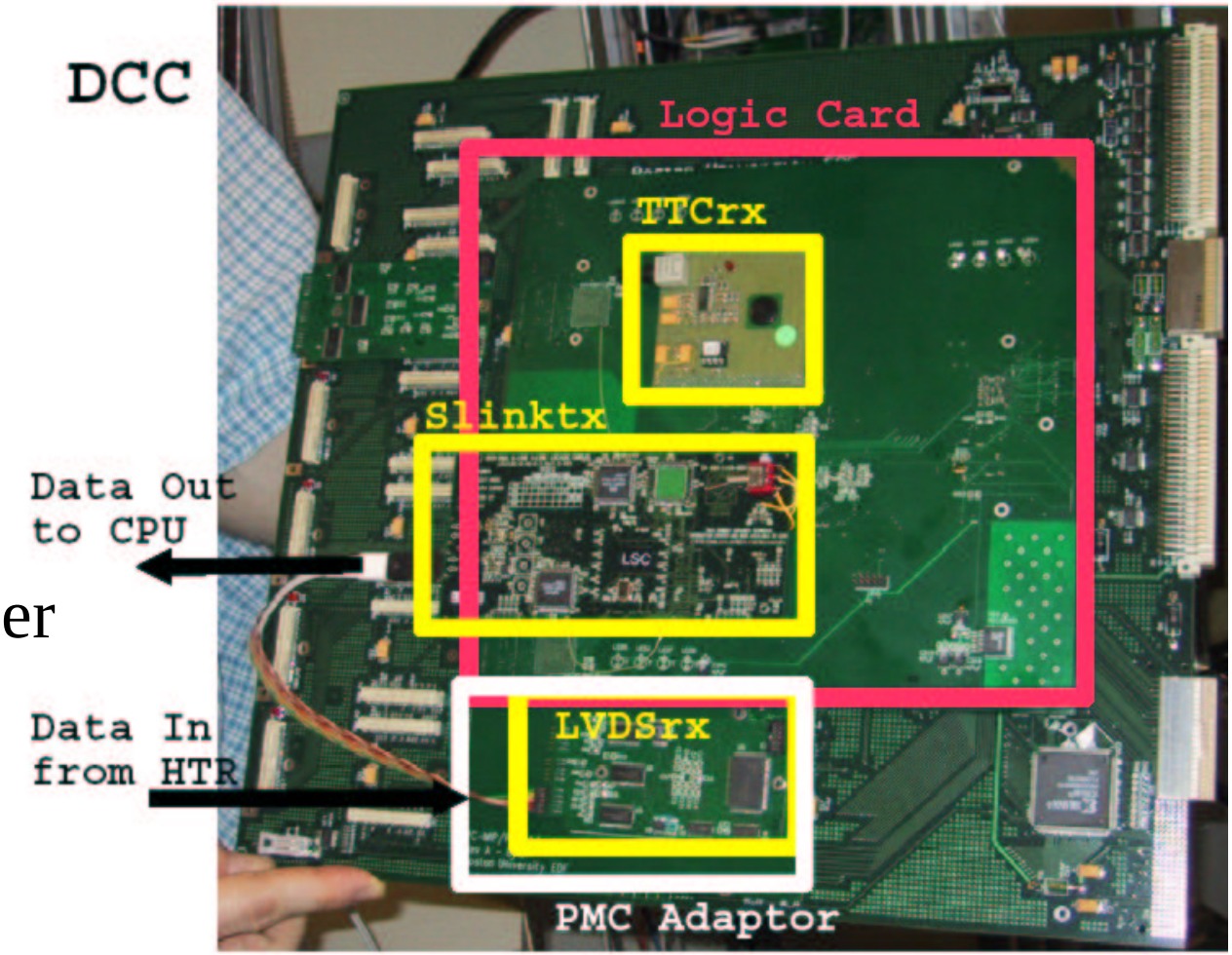
Energy Filter − Candidate

Good for latency constraints on trigger path



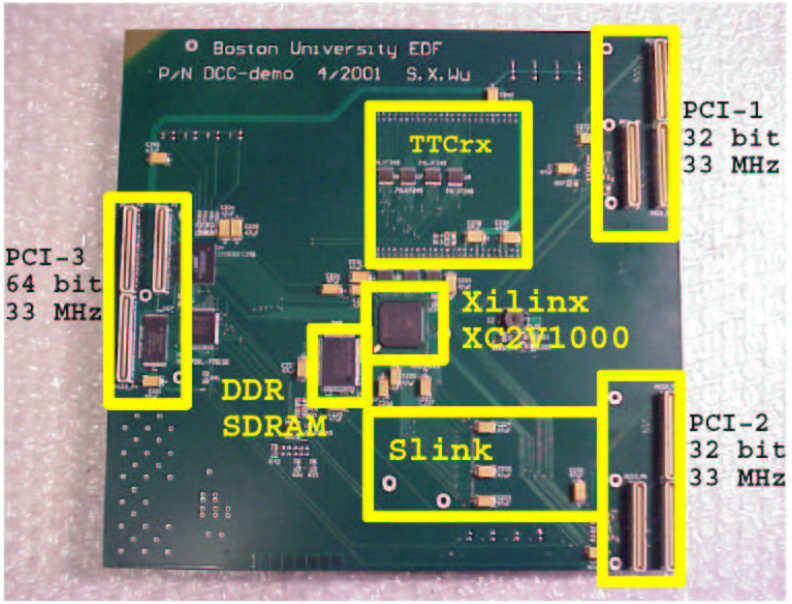
Current Status DCC Motherboard

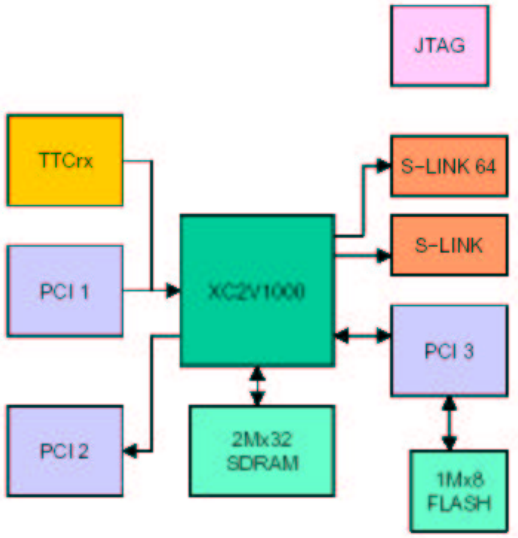
- VME Motherboard
  - Production started
  - 5 prototypes in hand for CMS.
  - All production parts bought
  - PCB / Assembly order ~ May ‘02



Status of DCC Logic Board and LRBs

- PC−MIP Link Receiver
  - Design approved except for change to RJ−45 connector for links
  - Final prototype PCBs on order Production parts on order
  - Production to start ~ June ‘02
- Logic Board – final prototype
  - Decisions about S−Link Data Width / Card location
  - Expect final PCB design late CY 2002
  - Production in early 2003; driven by final decisions about functionality



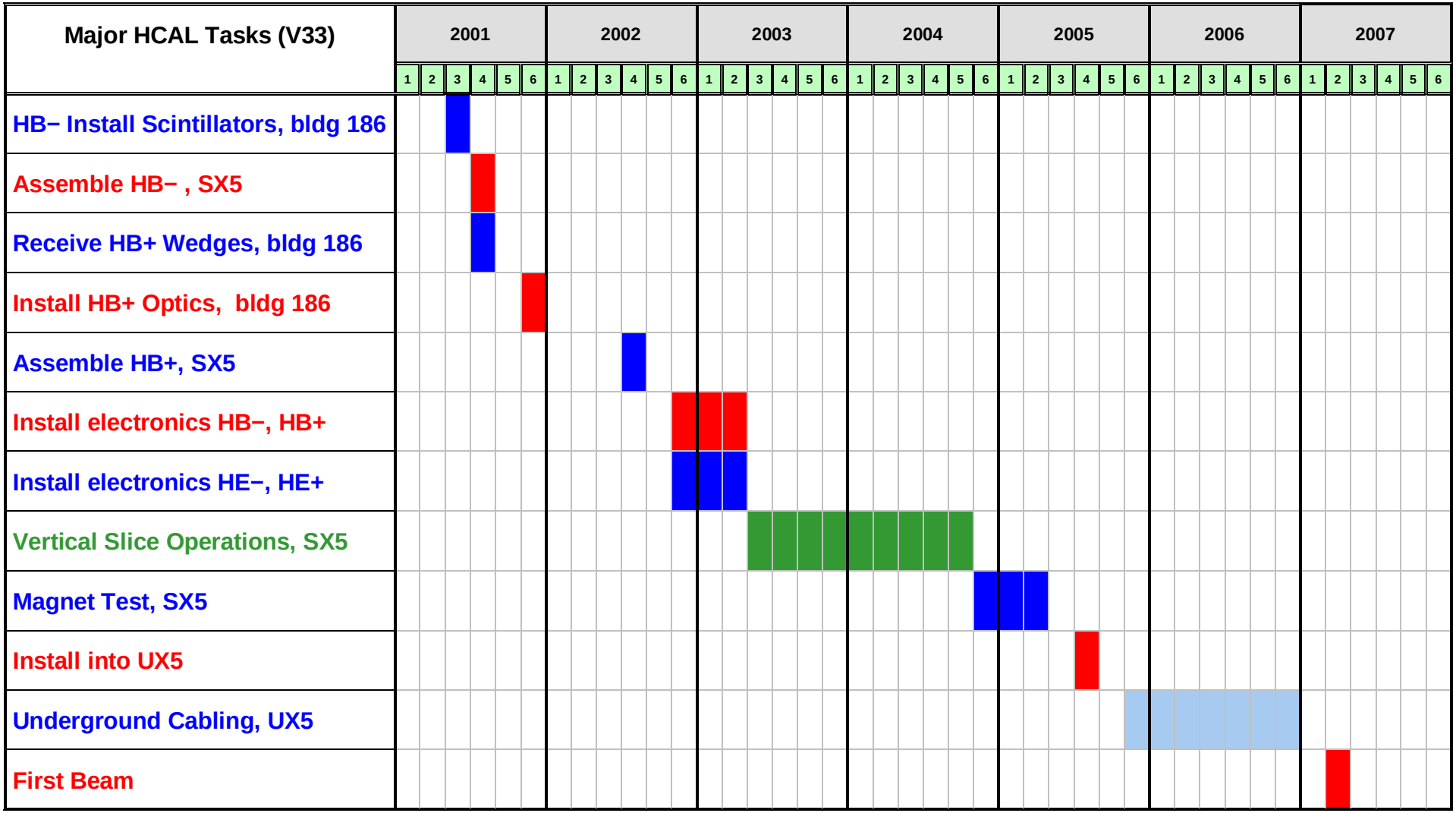


Summary of Recent DCC Progress (since CMS week March 02)

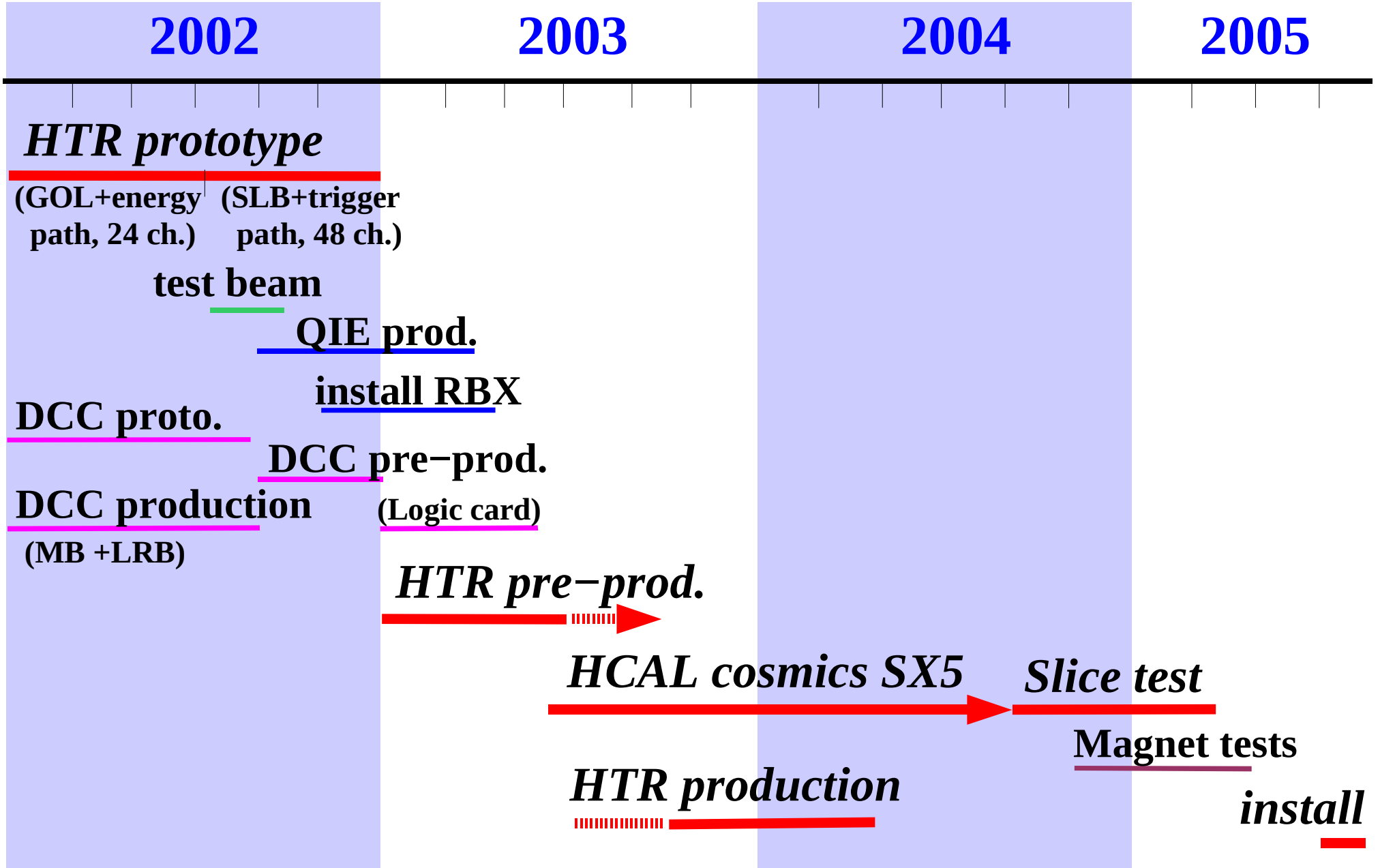
Reading from multiple HTR inputs on both PCI−1 & 2 busses working

Input Bandwidth measured to be 200 MBytes/s

HCAL Schedule: Overview



HCAL TPG Schedule* (Rev. April 2002)



Notes*

1) Test beam July −Sept. 2002 is a test of the prototype electronics
2) QIE production contingent on delivery of voltage regulators and GOL ASIC
3) HTR prototype has 2 phases: 24 ch. GOL + energy path and 48 ch. transition board + trigger path
4) Production of DCC logic cards is contingent upon final specification of the data link
5) HTR preproduction has time contingency
6) HCAL cosmic tests begin with preproduction units.
7) Much firmware is involved!