DWG NO	SN	REV

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

RESET
TSI(8:0)
TSI_DSTRB
VIOLATION
RES_TAXI_ERROR
WR_DONE
D24
en_TSI_CGI(8

CLK
CLR
CZB0
CZB1
DRIVE
CRSVD0
CRSVD1
CALEN
CAL0
CAL1
CAL2
CAL3
CAL4
CAL5
CAL6
CZA
CZA
CZB0
CZB1
CZA_EN
EVID0
EVID1
EVID2
EVID3

STOP
RECOVER
TEST
RUN
RC0
RC1
RC2
HALT
DONE
START_SCAN
TSI_SESBA0
TSI_SESBA1
TSI_EVID0
TSI_EVID1
TSI_EVID2
TSI_EVID3
TSI_RL0
TSI_RL1
TSI_RL2
TSI_TAXI_ERROR

XRESET
PROG
U64
74F38N
VCC
R10
4700
R11
4700
XINT
GND
RC2
TP20
TP25
U4
XC3130A-1PQ100C
U3
XC17256-PD8C
CE
OE/RESET
CLK
CEO
DATA

C
B
A
D

CDF UPGRADE ELECTRONICS	Fermi National Accelerator Lab
	TRACER - Xilinx FPGA
	TSI Interface Decoding
Theresa M. Shaw	SIZE D; FSMC NO; DWG NO TMS-TRAC-071197-P9A; REV B
RD/EED/EES	SCALE; SHEET 1 of 1

8 7 6 5 4 3 2 1