Modifications to the ABCD3T Wafer-Level Testing Procedure

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January 15, 2002

Hardware Revision:	**None**
Online Software Revision:	**7.5**
Offline Software Revision:	**7.5**
Operating Procedure Revision:	**None, except to update software release**

The changes to the test procedures are enumerated in Table 1. Most of them are related to the plans to speed up the testing (from 9 hours per wafer to under 5 hours) and to introduce additional tests. The details are explained below.

Table 1. Changes to the test sequence.

Tests	***Modifications***	***Need Qualification ?***
Strobe Delay Scan	Added two extra histograms (1)	No
Pipeline Scans	No change	No
Power Consumption	No change	No
Analog Scans	No change	No
Trim DACs Scans	No change	No
Internal DACs Scans	No change	No
Digital Tests	Modifications described below (2)	Yes
New Additions	I/O tests described below (3)	No
GUI embellishments	Temperature readout displayed (4). Software version is available from the Help part of the GUI menu.	No

(1) Originally, there was one strobe delay scan histogram, obtained for each channel of a chip under test in order to verify the strobe delay settings. The scan was done at 4.0 fC injected charge. That histogram is preserved, and two others are introduced. They are done at 1.0 fC and 10.0 fC, with the purpose to evaluate the timewalk. These scans are not used in the selection of good chips.

(2) The digital tests sequence had several modifications with the goal of reducing the testing time:

- reduction of the number of iterations from 100 to 10 per a test vector run,
- merging of the "test vector 4 family" into a single test vector, thereby saving on the long trim dacs initialization sequences,
- running the test vectors at one Vdd value for frequencies above 50 MHz, instead of the usual Vdd loop,
- addition of a test vector checking for chip non-response to commands sent to different addresses.

The first two and the last one of the changes affect the data considered in the chip selection, and therefore require the test performance validation.

SCIPP crew [1] has tested two wafers with both the currently used version of the software and the new updated version, listed in Table 2. We have compared the value of the minVdd[1] for both screenings for all test vectors for all chips. The comparison is straightforward for most test vectors. For the "test vector 4 family" we compare minVdd value for the new (single) test vector with the minimal value from the four test vectors in the family. For the test vector 4 types of vectors, we lowered the efficiency threshold from 95% to 85%, due to the low number of iterations in the new software. The threshold is 100% for all other test vectors. The results are shown in Table 3. The number of chips having different minVdd is typically 2% or lower. In most cases, the difference is 0.1 V (i.e. the minimal step size in the Vdd loop), with both values being below the required threshold for the digitally good chip. We conclude that the results with current and the new tests are consistent.

Table 2. Wafers used in the updated test sequence qualification.

Lot/Wafer number	***Initial screening date***	***Development software screening date***
z40602/w06	04/01/2001	12/01/2001
z40602/w03	10/02/2001	11/17/2001

[1] The minimum Vdd value for which a test vector works, i.e. it has efficiency above the agreed-upon threshold. This is the parameter which goes into selection of digitally good chips.

Table 3. Comparison of the screening results with new and old versions of the Digital Tests. Shown are the number of chips with different values of minVdd for each test vector (# diff.), the average non-zero absolute value of the differences (<|diff|>), and the average value of minVdd for chips with difference from the first screening (<minVdd>).

<table>
<tr><th rowspan="3">Test Vector</th><th colspan="6">Number of chips with different minVdd</th></tr>
<tr><th colspan="3">wafer z40602/w06</th><th colspan="3">wafer z40602/w03</th></tr>
<tr><th># diff.</th><th><|diff|>, [V]</th><th><minVdd>, [V]</th><th># diff.</th><th><|diff|>, [V]</th><th><minVdd>, [V]</th></tr>
<tr><td>TV1</td><td>0</td><td>0.00</td><td>N/A</td><td>7</td><td>0.20</td><td>3.34</td></tr>
<tr><td>TV2</td><td>0</td><td>0.00</td><td>N/A</td><td>2</td><td>0.35</td><td>3.65</td></tr>
<tr><td>TV3</td><td>7</td><td>0.17</td><td>3.55</td><td>4</td><td>0.20</td><td>3.53</td></tr>
<tr><td>TV4</td><td>6</td><td>0.15</td><td>3.32</td><td>2</td><td>0.35</td><td>3.30</td></tr>
<tr><td>TV4com1</td><td>8</td><td>0.11</td><td>3.45</td><td>0</td><td>0.00</td><td>N/A</td></tr>
<tr><td>TV5</td><td>4</td><td>0.20</td><td>3.53</td><td>5</td><td>0.10</td><td>3.32</td></tr>
<tr><td>TV6</td><td>0</td><td>0.00</td><td>N/A</td><td>1</td><td>0.10</td><td>3.40</td></tr>
</table>

The additional test vector is designed to find a relatively rare problem [2]. The TV was included in the screening of wafer z40602/w06. The chips passing the other test vectors passed this one as well, which is consistent with the expected low frequency of the problem occurence. We will follow the performance of this test vector in the future screenings. Based on the evidence we have, the impact of the additional selection on the yields is negligible.

(3) The I/O tests are added. We measure the voltage swings and phases (relative to the input clocks) of the input *clk, com, datain, tokenin* and output *LED/datalink, dataout, tokenout* signals. We also measure the duty cycles of the clocks. More details can be found in the Ref. [3].

The performance of these tests was looked at, but they do not require the qualification as their results do not add to the selection criteria with this revision. The selection, based on the results of these tests will be established as we start to collect more data.

(4) The temperature inside the blue box is being read out now and displayed on the GUI panel. The measurement is taken on the pin driver board, the hottest place in the box, due to the high current consumption by the pin driver chips. The readout and the display update happen before testing a chip. The test is aborted if the temperature is higher than a pre-set threshold.

This is a safety feature, designed to prevent possible damage to the chip under test due to a fan failure, and to alarm an operator about inappropriate testing conditions.

Appendix A. List of new keywords in the configuration file.

The extra keywords, which can appear in the configuration files for the new software, are listed in Table 4. Of them, only *nPDB* and *nCB* need to be specified (they have no defaults). The other parameters have sensible default values.

Table 4 Additional configuration file keywords for the new software.

Keyword	***Default***	***Description***
DoSignalLevel	yes (1)	Enables I/O signals levels measurements
DoSignalPhase	yes (1)	Enables I/O signals phases measurements
SkipHiFreq	yes (1)	Enables running TVs at only one Vdd value (no loop) at frequencies above 50 MHz
VddHiFreq	3.7	Vdd value [V] to run TVs at above 50 MHz if *SkipHiFreq* value is 1.
alarmTemperature	80.0	Blue box temperature threshold [C] for alarm
nPDB	N/A	# of the pin driver board (to invoke the calibration constants used in I/O tests)
nCB	N/A	# of the connector board (to invoke the calibration constants used in I/O tests)
nEvtPerIOPoint	10	# of times to run TVs used in I/O tests

References:

[1] Many thanks to the SCIPP testing crew (Max Wilder *et al.*)
[2] Discovered by KEK SCT group, private communications with Nobu Unno. The findings were reported at December 2001 SCT meeting.
[3] http://www-physics.lbl.gov/~fadeyev/io_tests.pdf