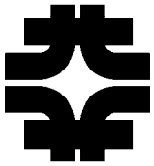

Fermi National Accelerator Laboratory

D0 Silicon Strip Detector Upgrade Project

SVX SEQUENCER BOARD

D0 Engineering Note Number 3823.110-EN-480

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1 INTRODUCTION

The SVX Sequencer boards are 9U by 280mm circuit boards that reside in slots 2 through 21 of each of eight Eurocard crates in the D0 Detector Platform. The basic purpose is to control the SVX chips for data acquisition and when a trigger occurs, to gather the SVX data and relay the data to the VRB boards in the Movable Counting House. Functions and features are as follows:

- Initialization of eight SVX chip strings using the MIL-STD-1553 data bus.
- Real time manipulation of the SVX control lines to effect data acquisition, digitization, and readout based on the NRZ/Clock signals from the VRB Controller.
- Conversion of 8-bit electrical SVX readout data to an optical signal operating at 1.062 Gbit/sec, sent to the VRB. Eight HDIs will be serviced per board.
- Built-in logic analyzer which can record the most important control and data lines during a data acquisition cycle and put this recorded information onto the 1553 bus.
- Identification header and end of data trailer tacked onto data stream.
- 1553 register which can read the current values of the control and data lines.
- 1553 register which can test the optical link.
- 1553 registers for independent phasing of the SVX DVALID signals, crossing pulse width, calibration pulse voltage, and calibration pipeline select.
- Abundant front panel displays and LEDs show the board status at a glance.
- In-system programmable EPLDs are programmed via 1553 or Altera's "Bitblaster".

2 I/O CONFIGURATION

2.1 General Crate Configuration

The boards will reside in eight centrally-located crates in the detector platform. These are 9U by 280mm Eurocard crates with a board separation of 0.8". There are 21 slots. Maximum Sequencer cards per crate is projected to be eighteen. Slot one in each crate will house a card that receives several NRZ/Clock control links from the VRB Controllers in the MCH. This card buffers and distributes these links across the Sequencer J1 backplane to each of the Sequencer Boards. The old Shaper-to-FADC cables carry the NRZ/Clock signals from the Controller to the Sequencer.

The J2/J3 backplanes provide the connection to 3M cables that go to the SVX chips. The cables carry control and bus signals and connect to a "Transition board," where the SVX power also connects. From there a flex-circuit cable will carry the control, bus and power to the HDIs on which three to nine chips are mounted.

Two 1553 cables will connect to the J1 backplane, as will the crate power. Four fibers are routed out the front panel of each Sequencer.

Each of slots 2 through 21 will have five bits of geographic addressing labeled 1 through 20 respectively.

2.2 Control Signals from the VRB Controller

Two “Shaper-to-FADC” coaxial ribbon cables connect to the back of the fanout board in slot 1 and carry a maximum of sixteen NRZ/Clock signal pairs from the VRB Controller (each ribbon has sixteen coaxes). These signals are buffered and then fanned out onto the backplane. Each slot will get its own NRZ/Clock pair of traces on the backplane. The NRZ/Clock pair to slots 1 and 2 will be derived from the same pair of coaxes. The NRZ/Clock pair to slots 3 and 4 will be derived from the same pair of coaxes, and so on.

NRZ stands for Non-Return to Zero and is a basic data transmission protocol whereby a high represents a logic 1 and a low represents a logic 0. The Clock line simply acts as a strobe for NRZ. In our control link, NRZ consists of a continuous stream of seven-bit packets, each bit being the same duration as one Tevatron RF cycle. The packets are synchronized with the accelerator. The bits in each packet consist of one framing bit which is always high, a bit which is high if a beam crossing is imminent, four bits representing the command desired, and one parity bit (odd parity). If the controller detects that a framing bit is zero, a NoSynch indication will occur, readable via 1553 or front panel LED. Synch is automatically re-established by sending only the framing bit for three cycles. This also happens to be the Idle command. The four command bits are defined in Table 1.

Idle	0 0 0 0
Acquire	0 0 0 1
Trigger	0 0 1 1
Ramp	1 0 1 0
Digitize	0 0 1 0
Readout	0 1 1 0
Reset_Preamp	0 1 0 1
Cal_Inject	0 1 1 1
TF_Event_OK	1 0 1 1
Reserved_9	1 0 0 1
Read_Status	0 1 0 0
Pwr_Up	1 1 0 0
Reset	1 0 0 0
G_Link_Lock_Toggle	1 1 1 1
Reserved_D	1 1 0 1
Reserved_E	1 1 1 0

Table 1. Command codes encoded in NRZ

2.3 Interface to the SVX Chips

The J2/J3 backplane accepts the Futurebus-style connectors from the Sequencer. Four such 4 by 18 connectors exist on each Sequencer; each connector carries the signals for two HDIs. The backplane routes these signals to connectors on the rear of the backplane that accept the 3M cables that go to the Transition boards. Four such cables are associated with each Sequencer board. The bidirectional bus signals use TI 74ABT162500 transceiver chips to drive the 82Ω

cable. Other control signals use TTL drivers. A direction line is routed to the Transition board to control the transceivers on that board. Another signal called HDI-EN is sent to the Transition board to tell it to turn power on to the SVX chips.

2.4 Data Readout to the VRB

During readout of the SVX chips, the eight data bits from each of two HDIs is strobed into FIFO memories, and almost immediately read out into a Hewlett-Packard G-Link transmitter chip. These sixteen bits, each changing at 53Mb/s, are serialized by the G-Link and the resultant 1.062Gb/s serial signal is fed into a Finisar Laser optical driver. A 160 ft. fiber carries this signal out the front panel and to the VRBs in the MCH. Four such links emerge from each sequencer; each VRB accepts four fiber links. The data stream recovered by the VRB consists of eight bit words in succession. The data for each HDI is as follows:

Sequencer ID
HDI # & Status
Chip ID
Byte of zeroes
Channel ID
Data
Channel ID
Data
…and so on

2.4.1 Header in Data Readout to the VRB

The Sequencer ID is a number from 0 to 255; there will be about 150 total sequencers in the detector. The next byte is defined, starting with the MSB, as follows:

Downloaded status bit 2
Downloaded status bit 1
Downloaded status bit 0
Control Link No_Synch
Control Link Parity Error
HDI # bit 2
HDI # bit1
HDI # bit0

The Downloaded status bits are provided for general use and are set via 1553.

The No_Synch and Par_Err bits are reset to zero shortly after the data header is sent to the VRB. If a constant or momentary fault condition occurs after this time, the appropriate bit will be set to one and latched for readout during the next event readout.

The three HDI # bits are numbered 0 - 7 and are associated with the cables connecting to the HDI Interface Modules as follows:

0	**A half of top cable (wrt Sequencer backplane)**
1	**B half of top cable**
2	**A half of second cable**
3	**B half of second cable**
4	**A half of third cable**
5	**B half of third cable**
6	**A half of bottom cable**
7	**B half of bottom cable**

2.4.2 Trailer in Data Readout to the VRB

The Trailer for each HDI data stream will be hex C0 and will be appended to the data immediately following the last data byte of the last chip on its HDI. The forced readout of channel 127 of the last chip on each HDI (a feature of the SVX2E chip) will not be used; the option to use this feature, however, still exists.

2.5 1553

The J1 backplane has two triaxial bulkheads, each connected to a separate 1553 Controller output. One bulkhead connects to slots 2 through 11; the other connects to slots 12 through 21. Each Sequencer has two identical “Port-Card Equivalents” operated as its own Remote Terminal (RT). Thus there are 20 RTs connected to each 1553 Controller. The various registers in the Sequencer are accessed by reading/writing to a different subaddress. Subaddressing of each RT is defined in the table in Section 5.

3 GENERAL CONTROL CIRCUITRY

3.1 Main Control

The NRZ Control Link is the main input to the Control EPLD (Altera 7128S). The EPLD manipulates the SVX bus lines, Mode lines, and TNBR in the appropriate fashion based on the commands received over the Control link.

The SVX chips can be initialized when the VRB Controller is sending the Idle command. Data taking commences when the Acquire code is sent. Occasional Preamp Reset codes, most likely once every Tevatron revolution, will keep the preamps from saturating. When a trigger occurs, the Trigger code is sent which causes the Sequencer to effect digitization in the SVX chips. After a predetermined delay, the VRB Controller sends the Readout code, and the chips are instructed to read out the data.

3.2 Utility

Two identical EPLDs perform some general utility functions, one for each half of the sequencer. The utility pal operates the Sequencer's Status Register (subaddress 15). The bits are defined in Table 2 and Table 3.

Bit	Function
0	High if a Parity Error has occurred in the Control Link
1	High if the Control Link had lost synch.
2	High if the G-Link has lost lock (reads the Control link)
3	HDI select for diagnostics LSB
4	HDI select for diagnostics MSB
5	Reserved
6	Logic Analyzer FIFO Trigger LSB
7	Logic Analyzer FIFO Trigger
8	Logic Analyzer FIFO Trigger MSB
9	Bit appears in Status Word at beginning of readout LSB
10	Bit appears in Status Word at beginning of readout
11	Bit appears in Status Word at beginning of readout MSB
12	Reserved
13	Reserved
14	Reserved
15	Software reset

Table 2. Status Word bits

Bit 8	Bit 7	Bit 6	Logic Analyzer Trigger
0	0	0	Cal or Trig Codes
0	0	1	Cal
0	1	0	Trig
0	1	1	Readout
1	0	0	Nosynch
1	0	1	Parity Error
1	1	0	Acquire
1	1	1	Reserved

Table 3. Logic Analyzer Trigger encoding in the Status Word.

4 DIAGNOSTICS

Since the Sequencer boards will be in the platform and therefore in an interlocked enclosure, remote diagnostics are necessary to isolate the cause and location of a malfunction. If the board freezes and no control is possible, reading subaddress 10 will give the current status of the bus lines, Mode 0 and Mode 1, TNBR, Nosynch, and the four BNBR lines. This is called the

"Snapshot" register. Bits 3 and 4 of the Status Register choose which of the four HDIs will appear for the Bus lines. Table 4 shows the bit arrangement.

Bit	Signal
0-7	Bus 0-7
8	TNBR
9	Mode 1
10	Mode 0
11	NoSynch
12	BNBR1
13	BNBR2
14	BNBR3
15	BNBR4

Table 4. Bit assignment for diagnostic registers.

Another feature is a built-in logic analyzer which records the same bits (except Parity Error replaces TNBR) as the Snapshot register, except that a 4096-deep record of a previous event is stored, strobed at the main clock frequency of 53MHz. Triggering of this logic analyzer is selectable by writing to the Status register. See Tables 2 and 3. The trigger selects which event starts the recording of the signals in the logic analyzer FIFO. Selecting ACQ would show most of the data acquisition cycle. The FIFO overwrites upon receiving the next trigger. Codes must be inhibited in the Controller in order to view a specific event. Selecting NoSynch or ParErr as a trigger, in contrast, causes continual writing to the FIFO until a loss of NRZ synch or parity error occur. The FIFO will record the last 4096 clocks before the error has occurred, and will not retrigger until either the FIFO has been read or a software reset is given. The logic analyzer is read out by reading Subaddress 11 4096 times.

Front panel displays include hex displays of the eight bus lines; again, the HDI desired is selectable in the Status register. LEDs for each half of the Sequencer indicate Idle, Cal_Inj cycle, and normal Trigger. Board-wide indicators are Parity error, No Synch, G-Link unlock, and 1553 strobe.

5 1553 REGISTERS

The following table defines the 1553 registers used by the SVX Sequencer.

Subaddress	Function
0	N/A 1553 spec defines as Mode Code
1	Init HDI A
2	Init HDI B
3	Init HDI C
4	Init HDI D
5	Pulse shadow register after download
6	Crossing pulse width (RT 1 controls both)
7	Calibration voltage (RT 1 controls both)
8	Calibration pipeline (RT 1 controls both)
9	Sequencer ID (appears in readout data stream)
10	Read current state of bus and control lines
11	Read logic analyzer FIFO (4096 words deep)
12	Fiber Test path AB
13	Fiber Test path CD
14	EPLD Programming Register
15	EPLD Programming Key
16	Power command to HDI (RT 1 controls both)

Table 5. Definitions of the 1553 registers.

6 Operation

6.1 Initialization

The following is a list of a general initial setup of the SVX Sequencer. Set the crossing pulse width to h10, Cal voltage to h80, Cal pipeline to match what is downloaded into the SVX chips. Load the Sequencer ID with a value corresponding to some meaningful relationship with the detector configuration. After turning on power to the chips, set bits 0 through 7 of subaddress 16 to enable the bus and control lines to the HDIs.

To initialize the chips, each bit of the serial 1553 signal is used for the serial download to the chips. Therefore, bits go to the chips in multiples of sixteen. Since each chip has 190 bits in its initialization shift register, twelve words are sent for each chip in a string. Twelve times sixteen is 192, resulting in two “dummy bits” per SVX that must be sent in the beginning of the first word.

A three-chip HDI will require 36 1553 data words. The first data word will have six dummy bits. An eight chip HDI will require exactly 95 data words with no dummy bits. A nine chip HDI will require 107 data words with two dummy bits in the first word.

7 JTAG

The JTAG interface of the in-system-programmable EPLDs is used for burning the program into the EPLDs. There are four lines: TDI, TDO, TCLK, and TMS. TDI and TDO are the data lines and are daisy chained from one pal to the next. TMS is a control line and TCLK is the clock. The procedure will be to convert the Altera output file into the bitstream necessary to program the EPLDs, then ship the bitstream via 1553 to subaddresses 14. Table 6 shows the bit assignment. Subaddress 15 is a "key" into which a code must be written prior to programming the EPLDs. This code is h10. Unlike downloading the SVX chips where every 1553 data word loads sixteen bits, each 1553 data word sends only one bit to the JTAG port (One bit every 20μs, plus the overhead of Control and Status words in the 1553 protocol.). This is slower but will be exercised only when reprogramming of the EPLDs is necessary; nevertheless, the complete programming of all four EPLDs is projected to take less than one minute per card.

1553 Bit	JTAG function
4	TDO
3	JTAG_ENA
2	NA
1	TMS
0	TDI

Table 6. 1553 bits for programming the ISPLDs via the JTAG port.

APPENDIX A

The Schematic Diagram for this board is number 3823-110-EC-330169 can be found in the D0 flat files at the northeast corner of the third floor of DAB. The backplanes are described in Engineering Notes 3823-110-EN-478 and 3823-110-EN-479.

APPENDIX B

The EPLD files are included on the following pages, but the most up-to-date versions can be found in D0server1\users\utes\SVX Sequencer. Use Max+plus II to view them.