Study of Bulk and Elementary Screw Dislocation Assisted Reverse Breakdown in Low-Voltage (<250 V) 4H–SiC p^+n Junction Diodes—Part II: Dynamic Breakdown Properties

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***Abstract*— This paper outlines the dynamic reverse-breakdown characteristics of low-voltage (<250 V) small-area ($<5 \times 10^{-4}$ cm^2) 4H–SiC p^+n diodes subjected to nonadiabatic breakdown-bias pulsewidths ranging from 0.1 to 20 μs. 4H–SiC diodes with and without elementary screw dislocations exhibited positive temperature coefficient of breakdown voltage and high junction failure power densities approximately five times larger than the average failure power density of reliable silicon pn rectifiers. This result indicates that highly reliable low-voltage SiC rectifiers may be attainable despite the presence of elementary screw dislocations. However, the impact of elementary screw dislocations on other more useful 4H–SiC power device structures, such as high-voltage (>1 kV) pn junction and Schottky rectifiers, and bipolar gain devices (thyristors, IGBT's, etc.) remains to be investigated.**

***Index Terms*— P–N junctions, power semiconductor diodes, semiconductor defects, semiconductor device breakdown, silicon carbide.**

I. Introduction

As discussed in the introduction of Part I [1], it is important that SiC power devices exhibit good reliability that is comparable to the reliability of present-day silicon-based power electronics. SiC power devices must demonstrate superior safe operating area (SOA) and immunity to switching and overvoltage stresses as silicon power devices before they can be considered reliable for applications in high-power systems. Large SOA is achieved primarily in silicon that is totally free of dislocation defects and has a minimum of undesired electrically active impurities. However, SiC electrical material quality is arguably decades behind the excellent quality of silicon used to manufacture present-day high-power solid-state electronics. As discussed in Part I [1], almost all large current (>1 A) SiC power devices manufactured on commercial SiC wafers are virtually guaranteed to contain elementary screw dislocations for the foreseeable future. Furthermore, there is much less control of impurities, both intentional (shallow dopants) and unintentional, in SiC crystals than is routinely attainable in silicon wafers. If SiC high-power electronics are to be incorporated in many high-power applications in the near-future, SiC power devices will have to achieve reliable operation and large SOA despite the presence of crystal dislocation defects and residual impurities in concentrations that are generally not acceptable for silicon solid-state power devices.

Many years of silicon power device experience has shown that the operational reliability of a semiconductor high-power rectifier is closely related to its reverse-breakdown characteristics. Silicon power devices that uniformly distribute breakdown current over the entire junction area exhibit greater reliability than silicon devices that manifest localized breakdown behavior [2]–[5]. This is because silicon devices that avoid localized junction breakdown exhibit larger safe operating areas and can much better withstand repeated fast-switching stresses and transient overvoltage glitches that arise in high-power systems. Positive temperature coefficient of breakdown voltage (PTCBV), a standard behavior in silicon power devices free of crystal dislocation defects, helps insure that current flow is distributed uniformly throughout a device, instead of concentrated at high-current-density filaments. When subjected to transient breakdown or switching bias conditions in which voltage and current are simultaneously large, PTCBV enables silicon power rectifiers to uniformly dissipate high-power densities for short periods of time without any point in the device reaching a critical temperature that results in permanent junction damage or failure. It is generally accepted that power rectifier SOA and reliability increases with increasing semiconductor junction energy to fail.

If a semiconductor diode has a negative temperature coefficient of breakdown voltage (NTCBV), any localized temperature increase that occurs within the breakdown-biased junction will cause a localized current increase or hot spot. The current increase feeds back and causes even more localized and intensified heating leading to an unstable load line operation. This escalating process can quickly focus high power into a very small area that quickly overheats leading to second breakdown and permanent junction damage as well as contact metallization damage. Therefore, silicon junctions that suffer

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localized breakdown, often due to the presence of crystal dislocation defects, do not generally exhibit sufficient energy to fail characteristics to be considered reliable for use in many high-power systems.

Similar to silicon, reverse breakdown properties greatly influence the operational reliability of SiC high-power devices. The stabilizing properties of PTCBV and uniform breakdown may, as was the case with silicon, prove particularly important for high-power switching applications in which SiC is a candidate semiconductor for operating at much higher voltages and power densities than employed in present-day silicon-based power devices. There have been a number of interesting investigations of dc properties of SiC breakdown, including Part I of this work [1]. However, because most solid-state power devices are employed in switching circuits, transient measurements of device switching and breakdown generally yield better insight into device physics that will be encountered in many real-world power system circuits. This paper details transient breakdown and junction energy to fail measurements conducted on the low-voltage 4H–SiC p^+n junction diodes whose dc characteristics were described in Part I [1].

II. Background

One method of measuring important rectifier junction reliability properties is to subject a diode to high-voltage pulses that momentarily bias the device beyond its reverse breakdown voltage. Reverse bias is usually more susceptable to electrical failure than forward bias. As high breakdown current is drawn at high applied voltage, a large breakdown power is dissipated at the junction which quickly heats up the device. By monitoring the transient device voltage $V(t)$ and current $I(t)$ as the device heats during the pulse, the sign of the temperature coefficient of breakdown voltage can be determined as positive or negative. Pulses of increasing energy (i.e., increasing amplitude and/or duration) are applied on a single-shot basis until a pulse causes the device to heat beyond a critical failure temperature T_m. Beyond the critical failure temperature, the device suffers permanent physical damage that compromises the diode electrical behavior.

For short pulse durations between 0.1 and 20 μs in length, heat flow occurs almost exclusively from the junction into the bulk semiconductor wafer; heat flow from the substrate to the package is essentially negligible on this timescale. Wunsch and Bell [6] derived a general first-order approximation for the junction power density P_D (kW/cm^2) applied over time t (μs) necessary for a device to reach a critical failure temperature T_m from an initial starting temperature of T_i

$$P_D = \sqrt{\pi\kappa\rho C_p}[T_m - T_i]t^{-1/2} \text{ kW/cm}^2 \tag{1}$$

where κ is the thermal conductivity (W/cm-K), ρ is the density (g/cm^3), and C_p is the specific heat of the semiconductor (J/gm-K). One choice for T_m is the temperature at which intrinsic carriers exceed the junction doping leading to second breakdown [2]. Metal–semiconductor contact degradation can also limit the peak temperature a device can withstand without damage. For more general first-order calculations that are independent of the junction doping and contact metallization, T_m is often set to the semiconductor Debye temperature T_D. The theoretical P_D versus t curve calculated by Wunsch and Bell [6] for silicon using $\rho = 2.33$ g/cm^3, $C_p = 0.7566$ J/gm-K, $\kappa = 0.526$ W/cm-K, $T_i = 298$ K, $T_m = T_D = 948$ K is

$$P_D = 1109[t(\mu\text{s})]^{-1/2} \text{ kW/cm}^2 \quad \{\text{Silicon Theoretical}\}. \tag{2}$$

Wunsch and Bell found that (1) reasonably approximates the general junction failure behavior of a wide variety of experimental silicon rectifiers. However, the experimentally observed best fit to the P_D versus t curve they observed for silicon rectifier diodes actually followed the equation [6]:

$$P_D = 560[t(\mu\text{s})]^{-1/2} \text{ kW/cm}^2 \quad \{\text{Silicon Experimental}\} \tag{3}$$

which lies somewhat below the theoretical calculation (2). Silicon experimental studies also indicate that pulse shape does not significantly change experimental device failure power densities, so that average power density may be used as a good approximation when diode voltage and/or current waveforms are nonconstant over the pulse duration [5].

If current flow is focused through junction hotspots or defects, the effective power density, which is normalized to the total junction area instead of the hotspot junction area, will decrease accordingly. For example, if current flow is focused through hotspots so that most of the current flows through only 10% of the total junction area, the theoretical silicon P_D versus t approximation (2) shifts downward to [6]

$$P_D = 110.9[t(\mu\text{s})]^{-1/2} \text{ kW/cm}^2 \quad \{\text{Silicon } 10\% \text{ Hotspot Theoretical}\}. \tag{4}$$

Thus, localized breakdown can seriously reduce the failure energy of a device with a specified voltage and current rating, which in turn can adversely affect the operational reliability and SOA.

Similar to the above first-order calculations for silicon rectifiers, theoretical P_D versus t failure characteristics of 4H–SiC rectifiers can be estimated using basic SiC material properties. While specific heat and thermal conductivity are both functions of temperature, their temperature dependence has not been taken into account in these first-order calculations. Furthermore, there is inconsistency between the few SiC thermal properties that have been reported in the scientific literature. Nevertheless, basic "best-case" and "worst-case" combinations of thermal conductivity and specific heat can be calculated to roughly estimate upper and lower theoretical limits on the junction failure power densities that might be observed in defect-free 4H–SiC junctions. For both calculations, $\rho = 3.2$ gm/cm^3, $T_i = 298$ K, and $T_m = T_D = 1120$ K [7] were used. The worst-case specific heat $C_p = 0.3$ J/gm-K at 300 K is calculated using the simple Debye model described by Kittel [8]. A worst-case 4H–SiC thermal conductivity $\kappa = 2$ W/cm-K is chosen based on measurements recently reported in [9]. Combined into relation (1) these worst-case material constants yield a P_D versus t relationship for 4H–SiC of

$$P_D = 2014[t(\mu\text{s})]^{-1/2} \text{ kW/cm}^2 \{\text{SiC Worst Case Theoretical}\}. \tag{5}$$

Even using worst-case material constants, the theoretical failure power density level of SiC diodes is more than twice the silicon experimental rectifier failure power density (3).

The best-case thermal conductivity $\kappa = 4.9$ W/cm-K was chosen from Slack's measurements of 6H–SiC at 300 K [10]. The work of Zywietz *et al.* [7] suggests that the specific heat of 4H–SiC does not increase much beyond $C_p = 1.0$ J/gm-K at temperatures above 600 K. Using these thermal parameters, the best-case first-order estimation of P_D versus t becomes

$$P_D = 5755[t(\mu\text{s})]^{-1/2}\ \text{kW/cm}^2 \quad \{\text{SiC Best Case Theoretical}\}. \tag{6}$$

which is more than ten times the experimentally observed silicon failure power density.

In Part I [1] it was noted that localized 4H–SiC breakdown microplasmas arising at elementary screw dislocations accounted for less than 1% of the total junction area. If all breakdown current flowed through elementary screw dislocation defects (i.e., no bulk breakdown current), the effective power density normalized to the total junction area could correspondingly plummet by more than a factor of 100. This would shift even the best-case SiC theoretical failure power density (6) to low levels considered unacceptable for silicon power devices

$$P_D = 57.5[t(\mu\text{s})]^{-1/2}\ \text{kW/cm}^2 \quad \{\text{SiC 1\% Hotspot Theoretical}\}. \tag{7}$$

Because bulk breakdown current becomes dominant over microplasma current at larger reverse biases (Part I [1 Fig. 5]), (7) is strictly a worst-case hypothetical analysis that doesn't seem to apply to the experimental devices of this study which contained elementary screw dislocations. However, the low failure power level of (7) may well apply to any 4H–SiC devices where highly localized breakdown does cause physical device failure prior to the onset of bulk breakdown, as is likely to be the case with diodes containing micropipe defects.

Theoretical relations (2)–(7) are plotted later in Fig. 4 for reference to experimental data presented in the following section.

III. Experiment

Prior to breakdown-bias pulse-testing, ohmic contacts were deposited onto the epitaxial mesa-isolated 4H–SiC p^+n junction diodes (n-doping between 2.5×10^{17}–1.5×10^{18} cm^{-3}) described in Part I [1]. Nickel annealed at 1000 °C for 5 min in an argon tube furnace served as a backside contact, while an unannealed 300 Å Al/1000 Å Ti/2000 Å Al sandwich patterned by liftoff provided good ohmic contact to the degenerately doped p^+ cap epilayer.

The presence or absence of screw dislocations in individual devices was conclusively determined by examination of reverse current–voltage (I–V) properties as demonstrated in [11]. A total of 17 circular diodes varying in size from 100 to 250 μm in diameter were pulse-tested into failure, 6 of which contained no elementary screw dislocations. Devices were pulse tested on-wafer in near-dark conditions on a probing station equipped with coaxial probes. For pulse durations of less than 0.5 μs, the charge-line circuit described in [12] was employed to apply pulses and measure device voltage $V_D(t)$ and current $I_D(t)$ transient response. Longer bias pulses were supplied by a Velonex Model 350 pulse generator. Devices were subjected to manually triggered single-shot pulses of increasing pulse amplitudes and/or widths until device failure occurred. Between pulses, device I–V was checked for degradation using a standard 60 Hz curve-tracer. Device failure was observed by sudden changes in the $I_D(t)$ and $V_D(t)$ response (decreased surge impedance), degradation in the curve-tracer measured I–V, and physical changes in device appearance observed with the probe station microscope. Devices were sometimes tested immersed in Fluorinert FC-77 [13] to reduce the possibility of edge-related surface flashover [14], while others were tested in air.

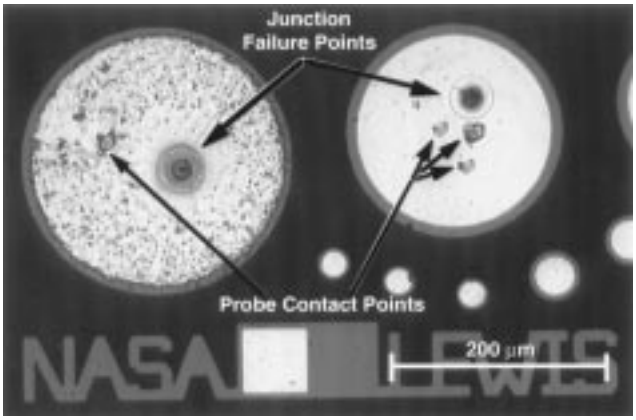

Fig. 1. Optical micrograph of two 4H–SiC mesa p^+n diodes following device failure during pulse-breakdown testing carried out on unpackaged devices on a probing station. In both diodes, junction failure points are clearly visible in the central mesa regions. Probe contact splotches in the metal mark where probe tips contacted each device. The multiple splotches on the left-hand device are a result of multiple re-positioning of the probe tip during pulse-testing. The left-hand device contact shows evidence of contact metal melting.

Post-failure optical microscopic examination was carefully conducted on each damaged device. A few devices exhibited clear evidence of surface flashover failure near the mesa periphery. A few other devices were totally obliterated similar to what is depicted in [15]. However, strong evidence of bulk junction failure was seen in the majority of diodes tested, as physical contact and mesa damage was confined to near-central regions of the device mesa away from the mesa edge and often away from where the probe tip contacted the diode. Two examples of such diode damage are shown in Fig. 1. While evidence of contact melting, such as the left-hand device in Fig. 1, was observed on some failed devices, there was no obvious trend to indicate that observed diode failure energy was limited by contacts. For contacts to cause initial failure in the near-central regions of devices, molten metal would need to migrate through nearly 1 μm of p^+ SiC [1, Fig. 1] in microsecond timespans to reach the high-field junction, which is seemingly unlikely given the notoriously low reactivity and slow impurity diffusion rates of SiC below 2000 K.

Figs. 2 and 3 show four selected transients of $V_D(t)$ and $I_D(t)$ data observed on two 200-μm diameter devices as bias-

pulse amplitude was increased. While both of these devices contained elementary screw dislocations and both were pulse-tested while immersed in Fluorinert, the important behaviors shown in Figs. 2 and 3 are consistent with test results of screw-dislocation free diodes as well as diodes tested in air ambient without Fluorinert immersion.

The Fig. 2 single-shot bias pulses were applied using the transmission line pulse-generation circuit [12] to a device that exhibited microplasmic breakdown at 80 V and bulk breakdown at 93 V. While the 90 V amplitude of bias Pulse 1 in Fig. 2 should have been sufficient to draw many milliamps of microplasmic breakdown current, the microplasmic breakdown currents nevertheless were below the 50 mA resolution of the transformer used to measure current in the pulse-testing setup. Thus for all diodes tested (regardless of screw-dislocation content), pulse-breakdown current was only observed when the bias pulse amplitude exceeded the dc-measured bulk breakdown voltage. NTCBV behavior is exhibited over the entire duration of Pulse 2, in that device voltage decreases while current increases as the device self-heats. The NTCBV trend is apparent for the initial stages of Pulses 3 and 4, but this trend changes to PTCBV behavior as the device self heats beyond 0.2 μs. At $t = 0.44$ μs into Pulse 4, the device fails as evidenced by the onset of a sharp current increase coupled with voltage collapse prior to the falling edge of the 0.5 μs bias pulse. Curve-tracer characterization immediately following the pulse confirmed the device failed to a resistive short-circuit during Pulse 4. An average device power density P_D was calculated by averaging $P(t) = V_D(t)I_D(t)$ over the pulse prior to failure and dividing by the total junction area. Thus the device withstood an average power density P_D of 4.17 MW/cm^2 over a period of 0.44 μs in Fig. 2, which is one of the experimental data points plotted later in Fig. 4. Post-failure analysis of this device indicated physical damage in the near-central device region, with no evidence of edge-related breakdown failure.

Very similar results from longer bias pulses generated by the Velonex pulser are displayed in Fig. 3, as the same trend of initial NTCBV followed by PTCBV is observed prior to device failure. The device of Fig. 3, which exhibited bulk breakdown at 132 V, failed 5 μs into Pulse 4 under an average power density PD of 1.26 MW/cm^2.

Fig. 4 shows all experimentally P_D versus t failure data points collected in this study on devices whose dc-measured bulk breakdown voltages ranged from 70–220 V due to n-layer doping variation across the wafer. Previously discussed relations (2)–(8) are also plotted in Fig. 4 for reference to experimental data. Diamond symbols on the plot represent devices that clearly exhibited bulk failure where exact failure times and power densities could be directly inferred from the $V_D(t)$ and $I_D(t)$ traces. Triangles represent data points that were collected from pulses in which a diode did not fail (failure occurred during a subsequent pulse), or from pulses where the diode failure occurred at the edge of a device mesa presumably due to surface flashover. Devices that contained no screw dislocations are denoted by open symbols, while filled symbols represent data collected from devices that contained at least one screw dislocation.

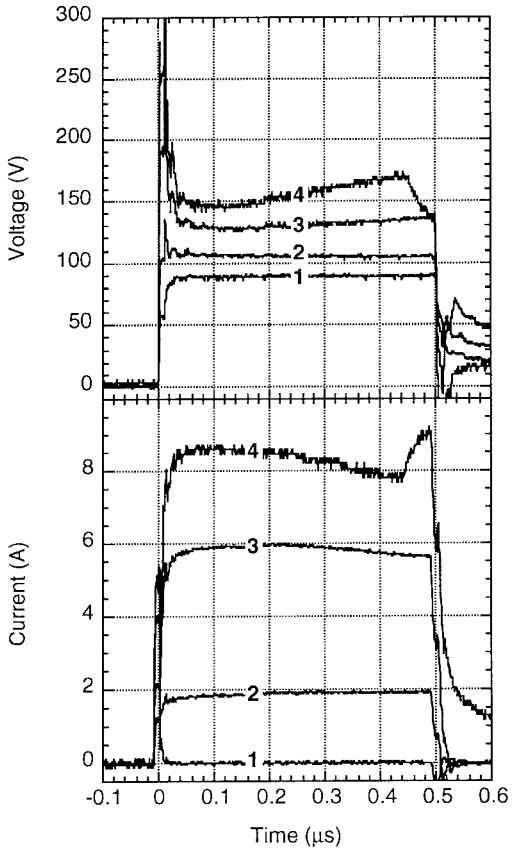

Fig. 2. Four selected voltage $V_D(t)$ and current $I_D(t)$ pulse-breakdown transients observed on a 200-μm diameter diode as a function increasing 0.5-μs bias-pulse amplitude. The diode fails 0.44 μs into Pulse 4.

The experimentally observed failure data points plotted in Fig. 4 are consistent with the $t^{-1/2}$ behavior predicted by (1). The fit to the experimental data

$$P_D = 2800[t(\mu\text{s})]^{-1/2}\ \text{kW/cm}^2 \quad \{\text{4H-SiC Experimental}\} \tag{8}$$

falls between the theoretical 4H–SiC limits approximated in (5) and (6). Thus, these 4H–SiC parts can withstand pulse breakdown power densities approximately five times the power density that silicon diodes typically withstand before junction failure is reached. The power density (8) is also about 50% greater than pulse breakdown power densities observed for 6H–SiC pn diodes in [16], [17]. It is important to note that the 4H–SiC data of Fig. 4 indicates that the presence or absence of elementary screw dislocations from a diode had no significant impact on the reverse failure energy of these low-voltage 4H–SiC diodes. Devices with and without screw dislocations exhibited comparable failure power densities to within the range of experimental scatter shown in Fig. 4.

An initial repetitive breakdown stress test was conducted on a 120 V (bulk breakdown) 100 μm diode with elementary screw dislocations. The device was subjected to 1 μs, 740 kW/cm^2 breakdown-bias pulses at a 2 Hz repetition rate for 16 h. While this resulted in significant changes to the physical appearance of the top ohmic contact metallization, there was no measurable change in junction reverse leakage and breakdown properties following this test. Further stress tests

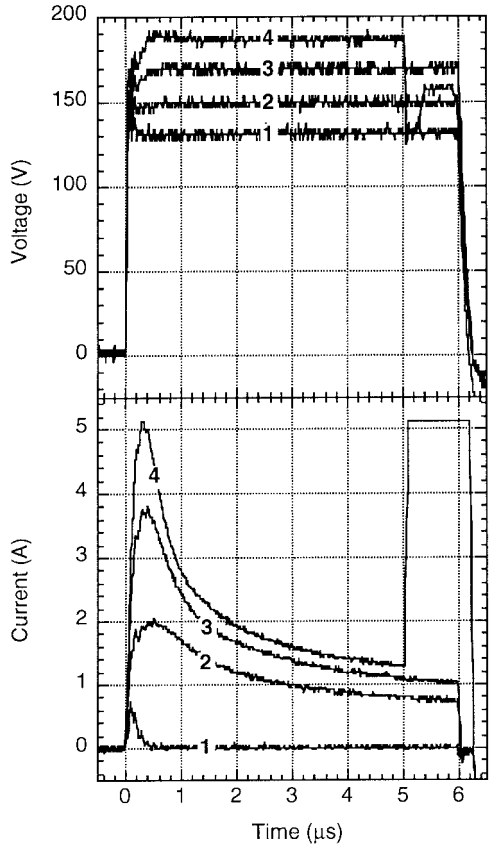

Fig. 3. Four selected voltage $V_D(t)$ and current $I_D(t)$ pulse-breakdown transients observed on a 200-μm diameter diode as a function increasing 6-μs bias-pulse amplitude. The diode fails 5 μs into Pulse 4.

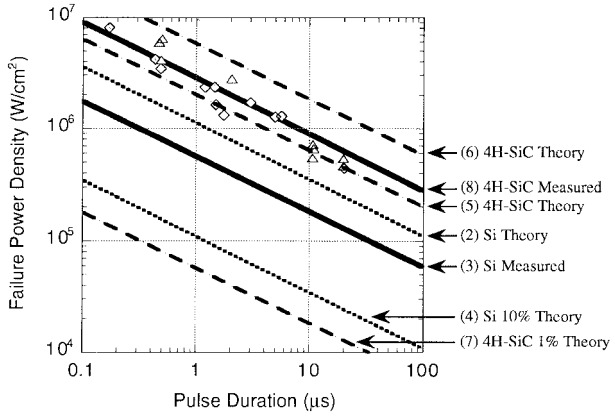

Fig. 4. Average failure power density P_D versus bias-pulse duration t for device reverse breakdown failure. Experimental data points for NASA 4H–SiC diode sample 1905-4 are plotted along with Wunsch–Bell experimental and theoretical approximations for silicon and 4H–SiC. The parenthetical number labels at the right of the graph correspond to equation numbers cited and discussed in the text.

are planned to more fully ascertain the functional limitations of these diodes under repetitive breakdown-bias stress.

IV. Analysis and Discussion

Extrapolations of dc breakdown properties presented in Part I [1] suggest that the pulse-failure power density of these low-voltage diodes should be largely independent of the elementary

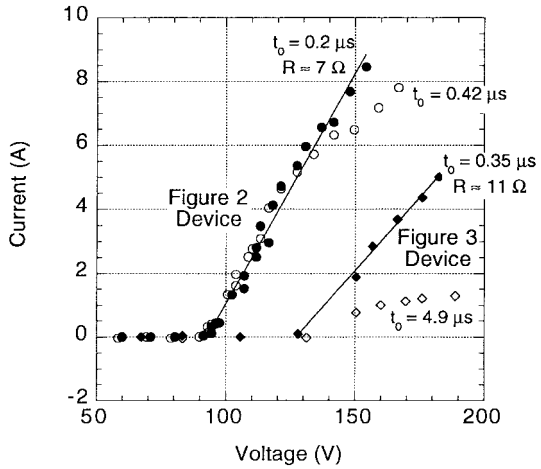

Fig. 5. Current–voltage characteristics constructed from series of pulse-measured voltage and current data at fixed time t_0 into each transient. Data taken from same devices as Fig. 2 ($t_0 = 0.2$ μs and $t_0 = 0.42$ μs) and Fig. 3 ($t_0 = 0.35$ μs and $t_0 = 4.9$ μs).

screw dislocation content, as was observed. At the maximum nonadiabatic pulsewidth of 20 μs, relation (5) yields a worst-case breakdown failure power density of 450 kW/cm^2. This power density is well above the 150 kW/cm^2 local power density (estimated in Part I [1]) of a typical microplasma (3 μm radius) just prior to the onset of bulk junction breakdown. As voltage is further increased, dc measurements ([1], Figs. 3 and 5]) indicate that bulk breakdown current initially increases at a much faster rate than the space-charge limited microplasma current. From Relation (3) derived in Part I [1], one can approximate a 3 μm radius breakdown microplasma power density $P_{D\mu}$ (normalized to microplasma area) as a function of applied reverse-bias V_R by

$$P_{D\mu} = J_N V_R = 2.83(V_{RN} - 3)^2 V_R \cong 2.83(V_R - V_\mu)^2 V_R \ \mathrm{W/cm^2} \tag{9}$$

where V_μ is the microplasma turn-on voltage. At appreciable breakdown currents, the calculated microplasma power density (9) is significantly smaller than the average power density (normalized to the entire device area) dissipated during pulse measurements. For example, the 200-μm diameter device tested in Fig. 2 roughly withstands 130 V at 6 A during Pulse 3, corresponding to an instantaneous power density of 2.48 MW/cm^2. Using the $V_\mu = 80$ V microplasma turn on voltage observed for the device, Relation (9) at $V_R = 130$ V evaluates to 0.92 MW/cm^2. Thus, dc-measured properties suggest that bulk breakdown current should dominate the power density and local junction temperature of these devices during pulse-breakdown testing. Furthermore, the apparent dominance of bulk breakdown current over space-charge limited microplasma current predicts that PTCBV would be measured in transient pulse-breakdown experiments, even if elementary screw dislocation defects exhibited localized NTCBV behavior as recent measurements of ionization coefficients at 4H–SiC crystal defect sites seem to indicate [18].

To what degree the experimental results of this paper apply to other SiC device structures remains to be ascertained. While screw dislocations were not explicitly considered in

pulse breakdown testing of 400 V pn diodes in [16], [17], the 6H–SiC devices tested were sufficiently large (area = 5.19×10^{-3} cm^2) that elementary screw dislocations were almost certainly present. The existence and properties of localized breakdown microplasmas in high-voltage (>1 kV) SiC devices has not been reported to date. Previous silicon experience suggests that microplasma current is relatively insensitive to junction width and doping [19]. Therefore, it is conceivable that the power density of localized 4H–SiC current filaments may greatly increase as SiC device blocking voltage is increased to 1 kV or 10 kV envisioned for many high-power applications. As a hypothetical example, if a 5 kV 4H–SiC pn diode exhibited 3-μm radius microplasma turn-on behavior according to (9) at 98% of the bulk breakdown voltage (i.e., $V_\mu = 4.9$ kV), a screw dislocation would have to dissipate 142 MW/cm^2 prior the onset of bulk breakdown. This power level is over an order of magnitude in excess of even the most optimistic 4H–SiC failure power density predicted by (6) for appreciable pulsewidths greater than 0.1 μs. This prediction is based on unproven assumptions, which future data could either verify or refute. Nevertheless, it emphasizes the strong need to study localized breakdown related to elementary screw dislocations in higher-voltage 4H–SiC pn junctions. These studies should also be extended to other silicon carbide device topologies, which in silicon experience have proven more susceptible to failure than pn junctions [5], such as SiC Schottky barrier rectifiers and SiC bipolar amplification devices like BJT's, thyristors and IGBT's. Localized breakdown and damaging failure at non-micropipe crystal defects in lightly-doped 4H– and 6H–SiC Schottky junctions has very recently been observed in [18]. While this work suggests the possibility that these crystal defects might be elementary screw dislocations, the crystallographic structure of the defects responsible for failure was not ascertained.

Domeij *et al.* [20] recently studied dynamic avalanche during reverse recovery turn-off in high-voltage (>1 kV) 4H–SiC pin diodes. They observed a maximum power density of 1.7 MW/cm^2 dissipated over ~0.2 μs prior to device failure, well below the 6.3 MW/cm^2 measured for 0.2 μs pulsewidths in our low-voltage 4H–SiC diodes. While the high-voltage 4H–SiC pin devices in [20] appear to have been compromised by nonideal perimeter edge termination, no information was given as to the presence or absence of elementary screw dislocations. The device size was large enough that elementary screw dislocations were probably present. In order to refute or confirm the theoretical discussion presented in the previous paragraph, it is very important that future experimental studies of energy to fail and SOA in high-voltage SiC devices conclusively ascertain the presence or absence of elementary screw dislocations.

It is informative to construct a device's I–V characteristic from measured pulse data. This can be done by choosing a constant time t_0, and plotting $I_D(t_0)$ versus $V_D(t_0)$ for a series of increasing-amplitude pulses recorded on a particular device. I–V's constructed from all pulses recorded on the 200 μm diameter devices of Figs. 2 and 3 are shown in Fig. 5. Solid symbols represent I–V's constructed by choosing t_0 close to the time where maximum pulse current was measured in the highest-current pulses ($t_0 = 0.2$ μs for Fig. 2 and 0.35 μs for Fig. 3), while open symbols use to chosen near the end of the pulses when device temperatures were as large as possible ($t_0 = 0.42$ μs for Fig. 2 and $t_0 = 4.9$ μs for Fig. 3). The apparent knee voltages in Fig. 5 are consistent with the onset of dc-measured bulk breakdown for these devices. The minimum effective series resistances calculated from the smaller t_0 I–V's in Fig. 5 are around 7 and 11 Ω. Based on 8.5 and 5 A maximum currents, the average I^2R resistive power losses for the largest pulses calculate to no more than 60 W for the largest pulses of Figs. 2 and 3. Normalized to device area (3.14×10^{-4} cm^2), the resistive power dissipation estimates to less than 200 kW/cm^2, well below the average power density of the largest pulses of Figs. 2 and 3 (4.17 and 1.26 MW/cm^2). This indicates that the vast majority of power is dissipated at the metallurgical pn junction during the initial stages of the bias pulse, not at resistive losses elsewhere in the device.

The Fig. 5 I–V's constructed with t_0 chosen near the end of the Figs. 2 and 3 pulsewidths (unfilled symbols) show very pronounced self-heating effects. The decreased current and increased voltage near the end of the pulses arise from some unknown combination of increased breakdown knee voltage and increased diode series resistance at high internal device temperature. The relatively small temperature coefficient of breakdown voltage observed at dc in [1, Fig. 5] (less than 3 V from 298 to 673 K) suggests that increased device series resistance with increasing device temperature may be controlling pulse breakdown $I(t)$ and $V(t)$ characteristics to a greater degree than actual increase in breakdown voltage of the junction with temperature. Under the Wunsch–Bell failure model, the junction temperatures of both the Figs. 2 and 3 devices should be comparable (i.e., both close to T_m) near the ends of pulses whose amplitudes are close to the failure pulse amplitude. Therefore, differences in breakdown voltage with temperature do not appear to explain the significantly larger percentage decreases in current typical for longer duration pulses. However, experimental observations are perhaps consistent with a basic physical argument that more of the semiconductor regions outside the junction that contribute to device series resistance will be hotter, and therefore more resistive, for the longer duration pulses.

Complete physical understanding of the 4H–SiC pn junction breakdown process will require further more-detailed measurements and analysis coupled with thermal and electrical modeling beyond the scope of the present study. The difficulty of decoupling device series resistance from breakdown voltage knee over the duration of a bias pulse makes precise estimation of temperature coefficient of breakdown voltage somewhat problematic. Likewise, estimation of junction temperatures at various times during a pulse is also dependent upon one's choice of reported 4H–SiC thermal properties [6]. For instance, the maximum junction temperature estimated from (1) using failure data of the best experimental diode ($P_D = 6.28$ MW/cm^2, $t = 0.5$ μs) is either 2110 K or 930 K, depending upon whether "worst-case" or "best-case"

4H–SiC thermal properties [see previous discussion relating to (5) and (6)] are employed in the calculation. Given that carrier mobility in 4H–SiC decreases as $T^{-1.8}$ due to phonon scattering [21], large (perhaps on the order of $10\times$) increases in device series resistance are plausible for this temperature range, more than adequate to explain experimentally observed voltage increases and current decreases recorded during pulse testing. The experimental results reported here will hopefully serve as an initial guide for the development of general two-dimensional and three-dimensional computer models capable of accurately predicting breakdown behavior and SOA of various 4H–SiC device topologies.

It is important to note that most transients in Figs. 2 and 3 exhibit initial NTCBV, followed by subsequent PTCBV as the pulse progresses. Furthermore, the time into the pulse at which the device transitions from NTCBV to PTCBV decreases as pulse power is increased. This general trend was observed in devices with and without elementary screw dislocation defects, and is consistent with pulse-breakdown results previously obtained in low-voltage 6H–SiC pn junction diodes [22], [23]. Such behavior is consistent with previously proposed models which suggest that stable pulse-breakdown behavior with PTCBV will not be observed until the vast majority frozen-out dopants and deep levels ionize some finite time following the rising edge of the breakdown-bias pulse [12], [24]. In contrast to the unstable 4H–SiC devices described in [12], [24], [25], these devices seem to be "conditionally stable" [24] in that they appear to self-heat to stability before a destructive current density is reached anywhere in a device. We speculate that increased self-heating arising from increased power density accelerates the emission of carriers from frozen-out dopants and/or deep levels, enabling stable breakdown (i.e., PTCBV) to be reached at shorter intervals following bias application. The timescales at which PTCBV is reached are of the same order of magnitude as theoretically predicted in [26].

Finally, it is worth pointing out that the highly unstable breakdown reported in [12], [24], [25] may well have arisen due to unusually high incorporation of unintentional impurities (revealed by subsequent SIMS analysis) during junction epilayer growth. The excess impurities, which are speculated to have been a source of excess carriers that destabilized fast-risetime pulse-breakdown, appear to have arisen from a nonoptimal two-step epilayer growth process, in which the respective p-type and n-type 4H–SiC epilayers were grown during totally separate CVD growth runs. The pn junction diodes discussed in this paper were produced during one continuous epilayer growth run, and exhibit far fewer unintentional impurities when examined by SIMS. While many more experiments are required to establish definitive trends, the experimental results of this paper and [27] are probably more representative of the pulse-breakdown behavior intrinsic to high-quality 4H–SiC p^+n diodes than highly unstable pulse-breakdown behavior reported in [12], [24], [25].

Nevertheless, the ability of fast-risetime pulse measurements to reveal undesirable switching instabilities indicates that pulse-testing should play an important role in the development, testing, and reliability qualification of high-power SiC electronic components.

V. Conclusion

While not necessary for all applications, excellent breakdown reliability and large SOA are key requirements of many operational high-power solid-state devices. For the first time, this work has quantified the pulse-breakdown failure characteristics of low-voltage 4H–SiC p^+n junction diodes. Positive temperature coefficient of breakdown was observed on devices with and without elementary screw dislocations as large as 250 μm in diameter. Good agreement with classic Wunsch–Bell thermal junction failure theory was experimentally observed. The 4H–SiC diodes exhibited pulse-breakdown failure power densities approximately five times greater than typical failure power densities of silicon rectifiers. The presence or absence of elementary screw dislocation defects did not significantly impact the failure power densities of these devices, a result consistent with extrapolations of dc-measured bulk and microplasmic breakdown properties. However, this result may not hold for other 4H–SiC device structures that contain elementary screw dislocations, as there is some indirect evidence to suggest that higher-voltage 4H–SiC devices may be more susceptible to damage arising from localized breakdown at elementary screw dislocation defects. There is strong motivation to definitively investigate the impact of elementary screw dislocations on various high-voltage 4H–SiC device topologies being developed for use in solid state power conversion and control electronics.

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