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ATLAS Pixel Detector Electronics and Sensors

G. Aad[10], M. Ackers[2], F.A. Alberti[11a], M. Aleppo[11a,11b], G. Alimonti[11a], J. Alonso[1], E.C. Anderssen[1], A. Andreani[11a,11b], A. Andreazza[11a,11b], J-F. Arguin[1], K.E. Arms[13], D. Barberis[7a,7b], M.B. Barbero[2], M. Bazalova[15], R.B. Beccherle[7a], K.H. Becks[21], P.K. Behera[8], F. Bellina[21], J. Beringer[1], K. Bernardet[10], J.B. Biesiada[1], L. Blanquart[1], J. Boek[21], G.R. Boyd[14], P. Breugnon[10], P. Buchholz[17], B. Butler[16], M. Caccia[11a,11b], A.C. Capsoni[11a], C. Caso[7a,7b,*], D. Cauz[19a,19b], M. Cepeda[1], R. Cereseto[7a], M. Cervetto[7a,7b], M.L. Chu[18], M. Citterio[11a], J.C. Clemens[10], Y.C. Coadou[3], M. Cobal[19a,19b], A. Coccaro[7a,7b], S. Coelli[11a], S. Correard[10], M. Cristinziani[2], S. Cuneo[7a], S. D'Auria[19a,19b], M. Dameri[7a], G. Darbo[7a], S. Dardin[1], B. De Lotto[19a,19b], U. De Sanctis[11a,11b], J.B. De Vivie De Regie[10], C. Del Papa[19a,19b], P. Delpierre[10], B. Di Girolamo[3], W. Dietsche[2], F. Djama[10], D. Dobos[6], M. Donega[3], J. Dopke[21], K. Einsweiler[1], A. Eyring[2], D. Fasching[20], L. Feligioni[10], D. Ferguson[20], W. Fernando[13], P. Fischer[2], M.J. Fisher[13], T. Flick[21], G. Gagliardi[7a,7b], E. Galyaev[5], K.K. Gan[13], M. Garcia-Sciveres[1], N. Garelli[7a,7b], G.G. Gariano[7a], G.G. Gaycken[2], C. Gemme[7a], P. Gerlach[21], M. Gilchriese[1], M.P. Giordani[19a,19b], D. Giugni[11a], K.W. Glitza[21], C. Gössling[6], T. Golling[1], F. Goozen[1], I. Gorelov[12], G. Gorfine[21], C. Grah[21], H.M. Gray[4], I.M. Gregor[21], J. Grosse-Knetter[2], K. Grybel[17], P. Gutierrez[14], G.D. Hallewell[10], N. Hartman[1], M. Havranek[15], B. Heinemann[1], T. Henß[21], M.R. Hoeferkamp[12], D. Hoffmann[10], M. Holder[17], W. Honerbach[2], C. Horn[16], S. Hou[18], G.S. Huang[14], F. Huegging[2], E. Hughes[4], I. Ibragimov[17], I. Ilyashenko[3], M. Imhaeuser[21], J.M. Izen[5], J. Jackson[13], D. Jana[14], R.C. Jared[20], P. Jez[15], T. Johnson[1], J. Joseph[20], H. Kagan[13], M. Karagounis[2], R.D. Kass[13], M. Keil[2], S. Kersten[21], P. Kind[21], J. Klaiber-Lodewigs[6], L. Klingbeil[2], R. Klingenberg[6], A. Korn[1], V.V. Kostyukhin[7a], I. Kostyukhina[7a], O. Krasel[6], H. Krüger[2], K. Krueger[1], J. Kudlaty[6], T. Kuhl[2], O. Kvasnicka[15], K. Lantzsch[21], T. Lari[11a], S.L. Latorre[11a], S.C. Lee[18], T. Lenz[21], G. Lenzen[21], J. Lepidis[21], J. Levêque[10], M. Leyton[1], D. Lopez Mateos[4], K. F. Loureiro[13], D. Lüke[6], L. Luisa[19a,19b], J. Lys[1], R. J. Madaras[1], P. Mättig[21], F.M. Manca[11a], E. Mandelli[1], M. Marcisovsky[15], Z. Marshall[4], G. Martinez[2], L. Masetti[2], M. Maß[6], M. Mathes[2], R. McKay[9], G. Meddeler[1], R. Meera-Lebbai[14], C. Meroni[11a], J. Metcalfe[12], W.T. Meyer[9], D.W. Miller[16], W. Miller[1], S. Montesano[11a,11b], M.M. Monti[11a], P. Morettini[7a], J.M. Moss[13], T. Mouthuy[10], P. Nechaeva[7a], W. Ockenfels[2], G.A. Odino[7a,7b], M. Olcese[7a], B. Osculati[7a,7b], F. Parodi[7a,7b], A. Pekedis[1], K. Perez[4], I. Peric[2], C. Pizzorno[7a], J. Popule[15], R. Post[1], F. Ragusa[11a,11b], A.M. Rahimi[13], B. Raith[2], S. Rajek[6], K. Reeves[21], I. Reisinger[6], J.D. Richardson[1], E. I. Rosenberg[9], L. P. Rossi[7a], I. Rottländer[2], A.R. Rovani[7a], A. Rozanov[10], O. Runolfsson[2], E.R. Ruscino[7a], A.F. Saavedra[1], F.S. Sabatini[11a], M. Saleem[14], S. Sandvoss[21], B. Sanny[21], L. Santi[19a,19b], M.I. Scherzer[1], C. Schiavi[7a,7b], A. Schreiner[8], J. Schultes[21], A. Schwartzman[16], R. Seibert[17], S.C. Seidel[12], H. Severini[14], S. Shanava[3], P. Sicho[15], P. Skubic[14], A.C. Smith[1], D.S. Smith[13], J. Snow[14], T. Stahl[17], T. Stockmanns[2], S. Strandberg[1], M. Strauss[14], D. Ta[2], F. Tegenfeldt[9], P.K. Teng[18], R. Ter-Antonyan[13], J. Thadome[21], T. Tic[15], L. Tomasek[15], M. Tomasek[15], F. Tomasi[11a], K. Toms[12], C. Tran[1], J. Treis[2], N. Triplett[9], C. Troncon[11a], L. Vacavant[10], S. Vahsen[1], J. Valenta[15], G. Vegni[11a,11b], F. Vernocchi[7a], E. Vigeolas[10], J. Virzi[1], E. Viscione[11a], V. Vrba[15], J. Walbersloh[6], W. Walkowiak[17], J. Weber[6], T.F. Weber[1], J. Weingarten[6], C. Weldon[1], N. Wermes[2], U. Werthenbach[17], J.S. Wirth[1], R. Witharm[1], B. Witt[21], M. Wittgen[16], J. Wuestenfeld[6], R. Wunstorf[6], J. Wyckoff[1], W-M. Yao[1], C. Young[16], R. Zaidan[10], M. Zdrazil[1], F. Zetti[1], J. Zhong[18], M. Ziolkowski[17], G. Zizka[1] and M.M. Zoeller[13]

[1]*Lawrence Berkeley National Laboratory and University of California, Physics Division MS50B-6227, 1 Cyclotron Road, Berkeley, CA 94720, United States of America*
[2]*Physikalisches Institut der Universität Bonn Nussallee 12, D - 53115 Bonn, Germany*
[3]*CERN CH - 1211 Geneva 23, Switzerland*
[4]*Columbia University, Nevis Laboratory 136 So. Broadway, Irvington, NY 10533, United States of America*
[5]*800 West Campbell Road Richardson, TX 75080-3021, United States of America*
[6]*Universität Dortmund, Experimentelle Physik IV DE - 44221 Dortmund, Germany*
[7]*INFN Genova ([a]), Università di Genova, Dipartimento di Fisica ([b]) via Dodecaneso 33, IT - 16146 Genova, Italy*
[8]*203 VAN ALLEN HALL IOWA CITY IA 52242-1479, United States of America*
[9]*Iowa State University, Dept of Physics and Astronomy,Ames High Energy Physics Group Ames, IA 50011-3160, United States of America*
[10]*CPPM, Aix-Marseille Université CNRS/IN2P3, Marseille, France*
[11]*INFN Milano ([a]), Università di Milano, Dipartimento di Fisica ([b]) via Celoria 16, IT - 20133 Milano, Italy*
[12]*Department of Physics and Astronomy, University of New Mexico Albuquerque, NM 87131, United States of America*
[13]*Ohio State University 191 West Woodruff Ave, Columbus, OH 43210-1117, United States of America*
[14]*University of Oklahoma, Homer L. Dodge Department of Physics 440 West Brooks, Room 100, Norman, OK 73019-0225, United States of America*
[15]*Institute of Physics, Academy of Sciences of the Czech Republic Na Slovance 2, CZ - 18221 Praha 8, Czech Republic*
[16]*Stanford Linear Accelerator Center Stanford, California 94309, United States of America*
[17]*Universität Siegen, Fachbereich Physik DE - 57068 Siegen, Germany*
[18]*Insitute of Physics, Academia Sinica TW - Taipei 11529, Taiwan*
[19]*INFN Gruppo Collegato di Udine ([a]), Università di Udine, Dipartimento di Fisica ([b]) via delle Scienze 208, IT - 33100 Udine, Italy*
[20]*University of Wisconsin, Department of Physics Madison, WI 53706, United States of America*
[21]*Bergische Universität, Fachbereich C, Physik Postfach 100127, Gauss-Strasse 20, D- 42097 Wuppertal, Germany*
[*]*Deceased*
Corresponding author: M. Gilchriese: `MGGilchriese@lbl.gov`

ABSTRACT: The silicon pixel tracking system for the ATLAS experiment at the Large Hadron Collider is described and the performance requirements are summarized. Detailed descriptions of the pixel detector electronics and the silicon sensors are given. The design, fabrication, assembly and performance of the pixel detector modules are presented. Data obtained from test beams as well as studies using cosmic rays are also discussed.

KEYWORDS: Particle tracking detectors;ATLAS;LHC.

Contents

1. Introduction

This paper describes the pixel detector system for the ATLAS experiment at the Large Hadron Collider (LHC). ATLAS [1] is a general purpose detector for the study of primarily proton-proton collisions at the LHC. The pixel detector system is a critical component of the inner tracking detector of ATLAS. The ATLAS Inner Detector [2] provides charged-particle tracking with high efficiency over the pseudorapidity range $|\eta| < 2.5$. The pixel detector system is the innermost element of the Inner Detector [3]. The pixel detector contains approximately 80 million channels and provides pattern recognition capability in order to meet the track reconstruction requirements of ATLAS at the full luminosity of the LHC of $\mathscr{L} = 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$. It is the most important detector used in the identification and reconstruction of secondary vertices from the decay of, for example, particles containing a b-quark or for b-tagging of jets. In addition, it provides excellent spatial resolution for reconstructing primary vertices coming from the proton-proton interaction region within ATLAS even in the presence of the multiple interactions at the LHC design luminosity.

In the sections below we first present the performance requirements for the pixel detector. This is followed by an overview of the system and its relationship to the Inner Detector. We then describe the principal components of the pixel detector systems, namely the electronics, sensors and modules. Results from test beam studies of the pixel detector components are then given. Results from studies of cosmic ray tracks passing through a sub-assembly of the pixel detector, corresponding to about 10% of the pixel system, are also presented. Mechanical systems and services are described in a separate publication [4].

2. Performance Requirements and Design Choices

The performance requirements for the ATLAS Inner Detector (ID) were formulated in the Inner Detector Technical Design Report (TDR) [2]. The pixel system is an important part of the ID and plays a major role in fulfilling these requirements.

The general performance requirements for the pixel system are:

- coverage of the pseudorapidity range $|\eta| < 2.5$;
- transverse impact parameter resolution of better than about 15 microns;
- good resolution in the longitudinal z-coordinate, allowing primary vertex reconstruction of charged tracks with $\sigma(z) < 1$ mm;
- three-dimensional-vertexing capabilities;
- very good b-jet tagging capabilities both in the high-level trigger and in the offline reconstruction;
- minimal material for all elements in the system, in order to reduce multiple scattering and secondary interactions;
- excellent efficiency for all pixel layers; and
- radiation hardness of the pixel detectors elements to operate after a total dose of 500 kGy or about $10^{15}\ \mathrm{n_{eq}cm^{-2}}$(lifetime dose).

These performance requirements lead to the following major design choices:

- three pixel hits over the full rapidity range. The requirement to have three pixel layers is based on a detailed study comparing a layout with two-pixel-hits versus a layout with three-pixel-hits [5];
- minimal radius of the innermost layer (b-layer), set at 5 cm due to the practical limitations of clearances around the interaction region beam pipe vacuum system;
- the smallest pixel size achievable, which is set to 50 μm $\times$ 400 μm by electronics design limitations.

The expected dose for the innermost layer is expected to reach 500 kGy after approximately five years of LHC operation. The other layers are expected to reach a 500 kGy dose, the lifetime dose, after 10 or more years of LHC operation (at a maximum luminosity of 10^{34} cm^{-2}s^{-1}).

The expected tracking performance of the pixel system is described elsewhere [2]. For example, the effective two-track resolution and the number of merged clusters of pixel hits (where a single cluster can have contributions from two or more charged tracks) depends on the local track density and other event properties and thus is not easily characterized except through measurements of tracking performance.

3. System Overview

In this section we present a brief overview of the pixel system and its relationship to the Inner Detector. The basic parameters of the pixel system are also summarized in this section. The pixel detector is the innermost element of the Inner Detector as shown in Fig. 1. The pixel tracker is designed to provide at least three points on a charged track emanating from the collision region in ATLAS. The pixel detector and the other elements of the Inner Detector span a pseudorapidity range $|\eta| < 2.5$.

The principal components of the pixel tracking system are the following:

- the active region of the pixel detector, which is composed of three barrel layers and a total of six disk layers, three at each end of the barrel region;
- internal services (power, monitoring, optical input/output and cooling) and their associated mechanical support structures (also supporting the interaction region beam pipe) on both ends of the active detector region;
- a Pixel Support Tube into which the active part of the pixel detector and the services and related support structures are inserted and located; and
- external services that are connected to the internal services at the end of the Pixel Support Tube.

The active region of the pixel detector is shown in a schematic view in Fig. 2. The active part of the pixel system consists of three barrel layers–Layer 0 (so-called b-layer), Layer 1 and Layer 2–and two identical endcap regions, each with three disk layers.

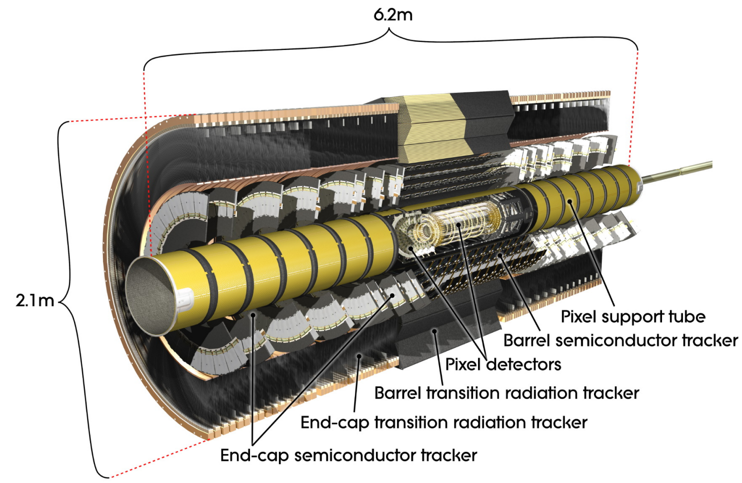


Figure 1. The ATLAS Inner Detector.

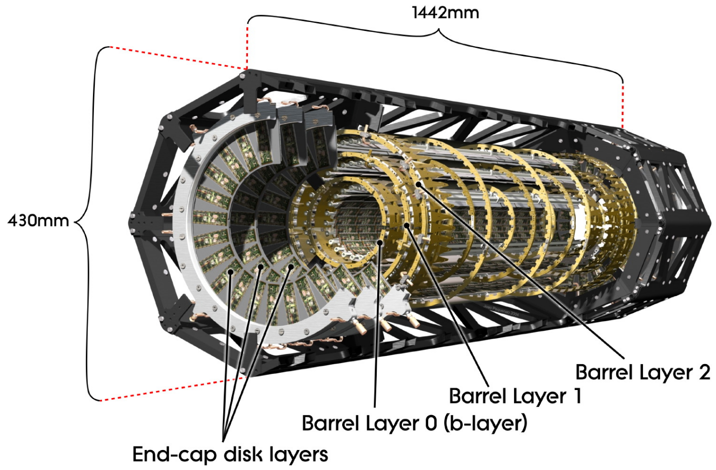


Figure 2. A schematic view of the active region of the pixel detector consisting of barrel and endcap layers.

The basic building block of the active part of the pixel detector is a module (section 6) that is composed of silicon sensors (section 5), front-end electronics and flex-hybrids with control circuits (section 4). All modules are functionally identical at the sensor/integrated circuit level, but differ somewhat in the interconnection schemes for barrel modules and disk modules. The nominal pixel size is 50 microns in the ϕ direction and 400 microns in z (barrel region, along the beam axis) or r (disk region). A few special pixels in the region between integrated circuits on a module have larger dimensions–see sections 5 and 6. There are 46,080 pixel electronics channels in a module.

The essential parameters for the barrel region of the pixel detector system are summarized in Table 1. Modules are mounted on mechanical/cooling supports, called staves, in the barrel region.

Thirteen modules are mounted on a stave and the stave layout is identical for all layers. The active length of each barrel stave is about 801 mm. The staves are mounted in half-shells manufactured from a carbon-fiber composite material. Two half-shells are joined to form each barrel layer.

Layer Number	Mean Radius [mm]	Number of Staves	Number of Modules	Number of Channels	Active Area [m^2]
0	50.5	22	286	13,178,880	0.28
1	88.5	38	494	22,763,520	0.49
2	122.5	52	676	31,150,080	0.67
Total		112	1456	67,092,480	1.45

Table 1. Basic parameters for the barrel region of the ATLAS pixel detector system.

The two endcap regions are identical. Each is composed of three disk layers, and each disk layer is identical. The basic parameters of the endcap region are given in Table 2. Modules are mounted on mechanical/cooling supports, called disk sectors. There are eight identical sectors in each disk.

Disk Number	Mean z [mm]	Number of Sectors	Number of Modules	Number of Channels	Active Area [m^2]
0	495	8	48	2,211,840	0.0475
1	580	8	48	2,211,840	0.0475
2	650	8	48	2,211,840	0.0475
Total one endcap		24	144	6,635,520	0.14
Total both endcaps		48	288	13,271,040	0.28

Table 2. Basic parameters of the endcap region of the ATLAS pixel detector system.

The total number of pixels in the system is approximately 67 million in the barrel and 13 million in the endcaps, covering a total active area of about 1.7 m^2.

The barrel shells and the endcap disks are supported by a spaceframe also manufactured from a carbon-fiber composite material (see Fig. 2). Electrical, optical and cooling services are connected and routed within service panels (four on each end of the pixel detector) from patch panels (Patch Panel 0–PP0) at the ends of the supporting spaceframe to the end of the Pixel Support Tube. These services are supported by carbon fiber structures that also hold the beryllium vacuum pipe within the Pixel Support Tube. Electrical, optical and cooling connections are made at the end of the Pixel Support Tube at Patch Panel 1 (PP1). Connections and control of external services are made at additional patch panels (PP2, PP3 and PP4) located within the ATLAS detector or near the ATLAS control room complex. The principal sub–elements of the pixel detector — barrels, endcaps, service supports and eight service panels — were assembled in a surface building near the ATLAS underground cavern. The complete pixel detector along with its services was tested in part and then installed as a unit in the Inner Detector. The mechanics, services and assembly of the pixel detector are described in detail in Ref. [4].

The contribution of the pixel detector to the total Inner Detector material budget as a function of pseudorapidity is given in Fig. 3 (radiation lengths) and Fig. 4 (interaction lengths). The beam pipe contribution is also presented.

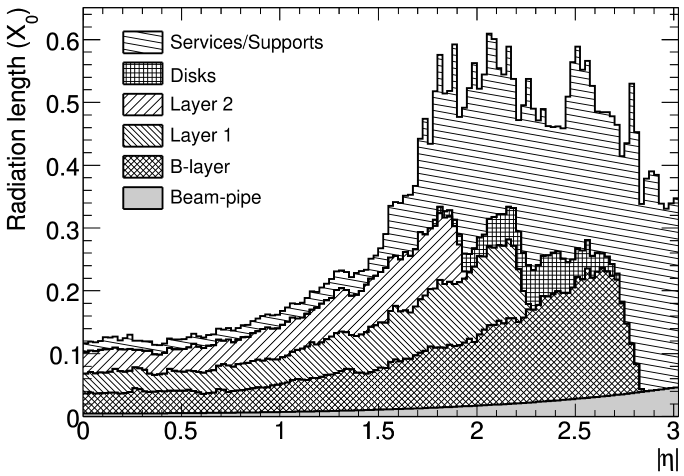


Figure 3. Radiation length of the pixel detector versus pseudorapidity showing the contribution from each layer and from all disks. Layer and disk contributions include services and supports directly in front of and behind the layer/disk. All remaining services and supports, including services in the region between the barrel and endcap are included in the "Services/Supports" category.

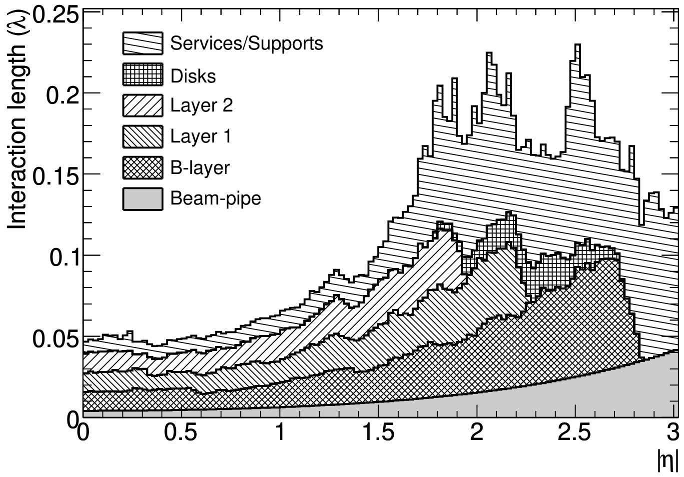


Figure 4. Interaction length of the pixel detector versus pseudorapidity showing the contribution from each layer and from all disks. Layer and disk contributions include services and supports directly in front of and behind the layer/disk. All remaining services and supports, including services in the region between the barrel and endcap are included in the "Services/Supports" category.

4. Electronics Systems

4.1 Overview

The first comprehensive proposal of the pixel electronic system was described in 1997-98 in the ATLAS Inner Detector and Pixel Detector Technical Design Reports [2, 3]. The complete system underwent several revisions in subsequent years. The total number of instrumented channels is about 80 million, each containing approximately 1,000 transistors and each consuming a maximum power of 100 μW (power for on-detector circuitry only).

4.1.1 System Architecture

A block diagram that illustrates the principal elements of the system architecture is shown in Fig. 5. There are 16 front-end chips (FE) in each pixel module and these are arranged in two rows of eight

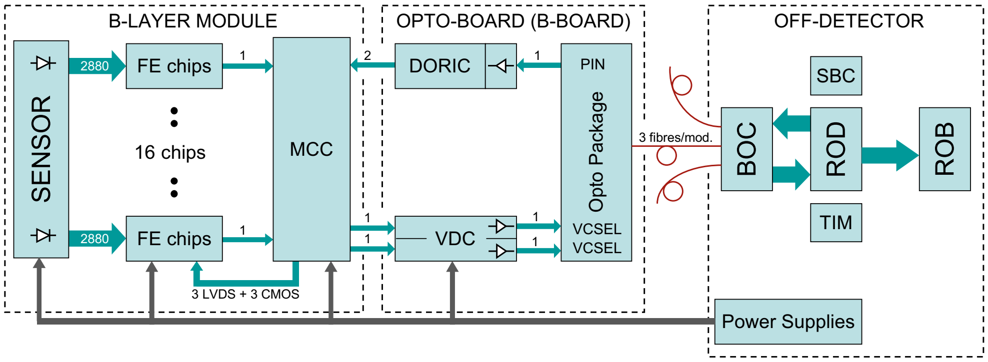


Figure 5. Block diagram of the pixel detector system architecture.

chips. The 16 FEs are read out by a Module Control Chip (MCC). Data are transmitted from the FE to the MCC using Low Voltage Differential Signalling (LVDS) serial links, configured in a star topology. The serial protocol minimises the number of lines to be routed, while the star topology maximizes bandwidth and reliability. Each module is then connected to the off-detector Read-out Drivers (RODs) through optical-fiber links (opto-links). One down link is used to transmit clock, trigger, commands and configuration data, while one or two up-links are used for event readout. The b-layer uses two up-links to increase the aggregate bandwidth needed for the higher average hit occupancy that occurs at the minimum radius. The readout (R/O) architecture is "data-push". This means that each component in the chain (FE, MCC) always transmits at the maximum rate, and there is no busy mechanism to stop transmission when buffers are full. Each upstream component in the R/O chain (MCC, ROD) constantly monitors the number of events received and compares the results with the number of triggers sent. If the difference of the two is bigger than a predefined value, triggers downstream are blocked and empty events are generated.

The power supply system uses a combination of customized-commercial components and fully-custom components for the low (electronics) and high (sensor bias) voltages. The use of deep sub-micron electronics and long resistive cables with significant voltage drops, required the use of low-voltage regulator boards, approximately 10 meters from the pixel detector. The absolute maximum voltage rating for the pixel electronics is 4 V. The optical-links are custom made using commercial diode and laser array bare die with custom integrated circuits (DORIC and VDC) and packaging. An optical-interface card (Back of Crate or BOC) is also used for each ROD.

4.2 Front-end Chip

4.2.1 Front-end Chip History

Small scale, front-end chips that demonstrated the required analog and digital architecture were first developed in the second half of the 1990s [6–9]. The first radiation-soft functional prototypes of full-size chips were submitted for production in 1998: FE-B and FE-A/C (Pirate). The FE-B chip was designed using 0.8 μm CMOS technology and had the same basic readout architecture used for the final chips. The FE-B charge amplifier used a direct cascode[1] and source follower, with a feedback capacitance of 4 fF. The DC feedback was based on a previous design [7, 8]. The discriminator used a dual threshold, with a low threshold for precise timing and a high threshold to flag a hit pixel.

FE-A was made using 0.8 μm BiCMOS technology, whereas FE-C was a full CMOS version. The charge amplifier used a folded cascode input stage with feedback capacitance of 3 fF and a new, improved DC feedback. The discriminator was AC coupled, with an input, fully-differential, bipolar pair in the A-version and CMOS in the C-version. The FE-A column readout architecture used a shift register to transport the hit address to the bottom of the chip. Hits were associated with the level 1 trigger (L1) by counting the number of clock cycles needed for the hit to reach the bottom of the column. FE-A/B/C demonstrated all the basic ATLAS pixel performance goals in the laboratory and in beam.

The subsequent chip was developed merging the basic concept of the amplifier/discriminator from FE-A/C and the column readout architecture from FE-C into a common layout for the DMILL [2]- Durci Mixte sur Isolant Logico-Lineaire - technology (known as FE-D). FE-D1 was submitted in July 1999 together with the DORIC and VDC chips (see section 4.4) and a prototype MCC-D0 (see section 4.3). A new production run was submitted in Aug 2000 with two versions of FE-D2: one with dynamic and the other with static memory cells. This run included the full MCC-D2 and new DORIC and VDC chips as well. Yields of both FE and MCC were unacceptable and work with this vendor was terminated. Work in an alternative radiation-hard technology, FE-H, began in Dec 1999. The chip was almost ready but was never submitted because of large cost increases. The failure of both traditional radiation-hard vendors pushed the collaboration towards the Deep Sub-micron (DSM) approach, based upon a commercial 0.25 μm CMOS process and a radiation-tolerant layout. A major design effort was initiated in September 2000. Three versions (FE-I1, FE-I2 and FE-I3) were eventually produced. The final chip (FE-I3) became available in late 2003. Table 3 gives a summary of the front-end designs developed for the ATLAS pixel detector.

4.2.2 Design

Chip Architecture The readout chip for the ATLAS pixel detector [15, 16], shown in Fig. 6, contains 2880 pixel cells of 50 $\times$ 400 μm^2 size arranged in an 18 $\times$ 160 matrix. Each pixel cell

[1]The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer.

[2]DMILL technology was developed by CEA, France, and then produced under license by TEMIC Matra MHS.

Chip	Year	Cell size [μm^2]	Col $\times$ Row	Transis-tors	Technology	References
Beer & Pastis	1996	50×436	12×63	–	AMS 0.8μm BiCMOS, 2M	[6, 9]
M72b	1997	50×536	12×64	–	HP 0.8μm CMOS, 2M	[6]
Marebo	1997	50×397	12×63	0.1 M	DMILL 0.8μm BiCMOS, 2M	[7, 8]
FE-B	1998	50×400	18×160	0.8 M	HP 0.8μm CMOS, 3M	[10–12]
FE-A/C	1998	50×400	18×160	0.8 M	AMS 0.8μm BiCMOS, 2M	[9, 12]
FE-D1	1999	50×400	18×160	0.8 M	DMILL 0.8μm BiCMOS, 2M	[12]
FE-D2	2000	50×400	18×160	0.8 M	DMILL 0.8μm BiCMOS, 2M	–
FE-I1	2002	50×400	18×160	2.5 M	DSM 0.25μm CMOS, 6M	[13]
FE-I2/I2.1	2003	50×400	18×160	3.5 M	DSM 0.25μm CMOS, 6M	[14]
FE-I3	2003	50×400	18×160	3.5 M	DSM 0.25μm CMOS, 6M	[15–18]

Table 3. Summary of the ATLAS pixel front-end chips designed and fabricated as described in the text. The chips contain two (2M), three (3M) or six (6M) metal layers as indicated.

contains an analogue block where the sensor charge signal is amplified and compared to a programmable threshold using a comparator. The digital readout part transfers the hit pixel address, a hit leading edge (LE) timestamp, and a trailing edge (TE) timestamp to the buffers at the chip periphery. In these buffers a Time-over-Threshold (ToT) is calculated by subtracting the TE from the LE timestamp. These hit-buffers monitor the time of each stored hit by inspecting the LE time stamp. When a hit time becomes longer than the latency of the L1 trigger (approximately 3.2 μs) and no trigger signal is recorded, the hit information is deleted. Hits marked by trigger signals are selected for readout. Triggered hit data are then transmitted serially out of the chip in the same order as the trigger arrival.

Charge Sensitive Preamplifier The charge-sensitive amplifier uses a single-ended, folded-cascode topology, which is a common choice for low-voltage and high gain amplifiers. The amplifier is optimised for a nominal capacitive load of 400 fF and designed for the negative signals expected from n$^+$–on–n-bulk detectors. The design of the charge amplifier was particularly influenced by requirements pertaining to sensor irradiation, which can produce leakage currents up to 100 nA. The preamplifier has a 5 fF feedback capacitor with a current-source-continuous reset, a 15 ns rise-time and operates at about 8 μA bias. Since the input is DC-coupled, a compensation circuit is implemented that drains the leakage current and prevents it from influencing the continuous reset circuit. The implementation, shown in Fig. 7, uses two PMOS devices, one (M2) providing leakage current compensation and the other (M1) continuously resetting the feedback capacitor.

An important property of this feedback circuit is that the discharge current provided by the reset device saturates for high-output-signal amplitudes. The return to baseline is, therefore, nearly linear and a discriminator pulse width proportional to the input charge is obtained. The width of the discriminator output, Time-over-Threshold (ToT), can therefore be used to measure the signal amplitude. The duration of the ToT is measured by counting the cycles of the 40 MHz master chip clock. The feedback current is 4 nA for a 1 μs return to baseline for a 20,000 electron-equivalent input. The feedback circuit has an additional diode-connected transistor M3, which acts as a level shifter so that the DC-levels of input and output nodes are nearly equal. It also simplifies the

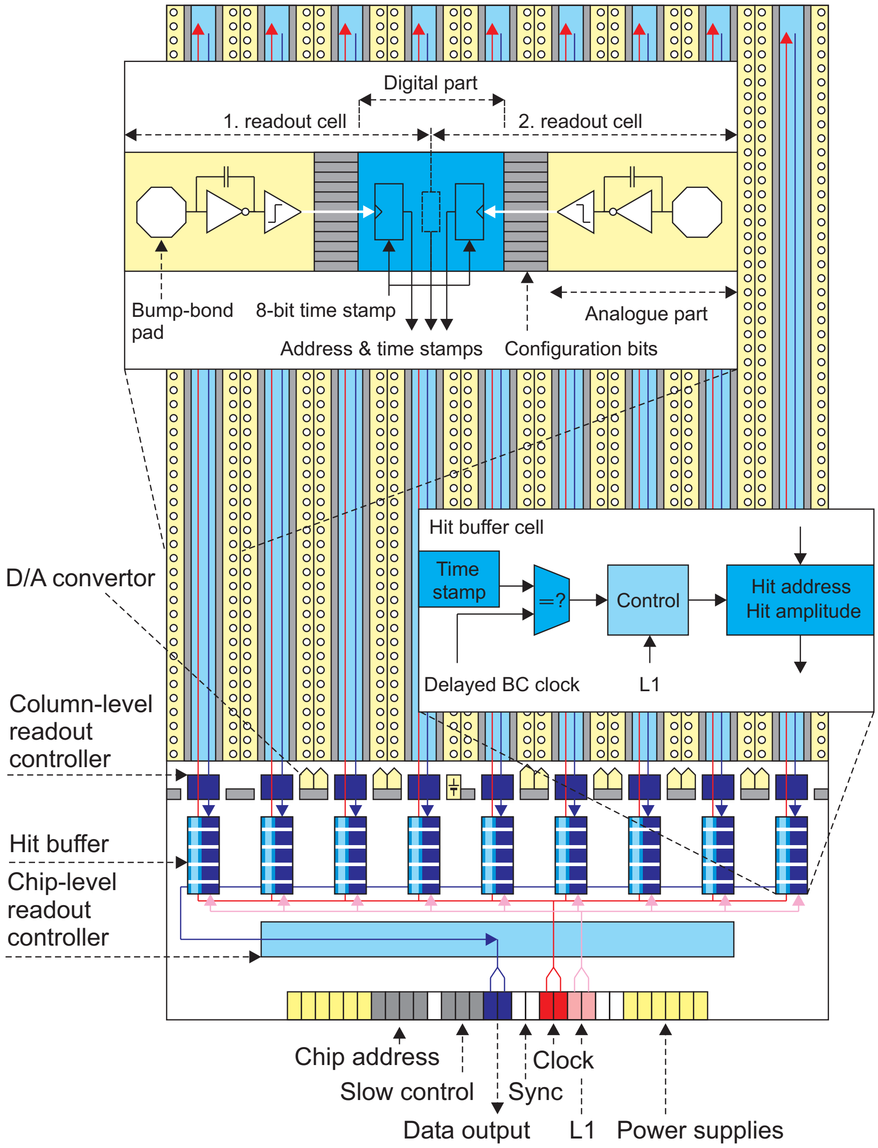


Figure 6. Schematic plan of the front-end chip (FE-I3) with main functional elements. Not to scale.

DC-coupling between the amplifier and the discriminator, as described below.

Discriminator Signal discrimination is made by a two-stage circuit: a fully differential, low-gain amplifier, where the threshold control operates by modifying the input offset, and a DC-coupled, differential comparator. The first stage has a bias of about 4 μA, whereas the second uses a current of about 5 μA. A local threshold generator is integrated in every pixel in order to make the threshold independent of the local digital supply voltage for each pixel and on the amplifier bias current I_f. Seven-bits are used for each pixel to adjust the discriminator threshold.

Pixel Cell Control Logic A complete block diagram of the analogue part with several additional circuit blocks is shown in Fig. 8. Each pixel has several parameters that can be tuned through a

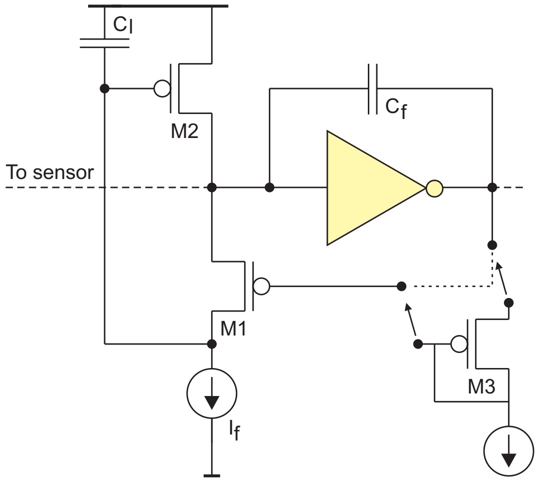


Figure 7. Charge preamplifier feedback circuit.

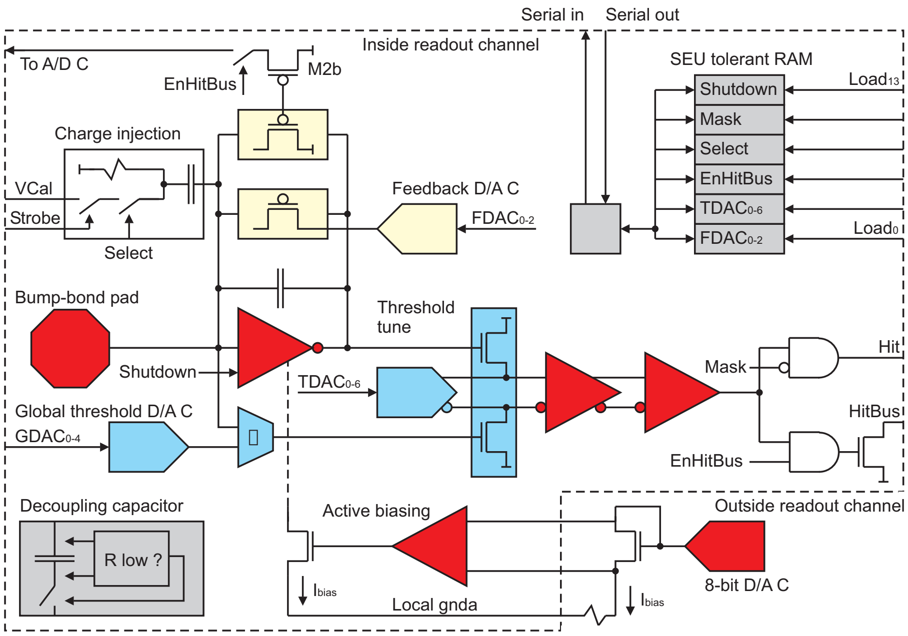


Figure 8. Pixel cell block diagram.

14-bit control register. These bits are:

- *FDAC 0-2:* 3-bits to trim the feedback (I_f) current for tuning the ToT response.
- *TDAC 0-6:* 7-bits to trim the threshold in each pixel.
- *MASK:* the digital output of the analogue part can be switched off locally by setting this bit.
- *EnHitBus:* the digital outputs of all readout channels can be directly observed using a wired OR which is locally enabled with this bit. This bit also controls, through transistor M2b, the

summing of a current proportional to the feedback plus leakage current in the preamplifier, allowing for monitoring of the feedback current and of the leakage current from the sensor.

- *Select:* enables the pixel for test charge injection. The amplitude is generated from V_{Cal} (voltage proportional to the injected calibration charge), whereas the timing comes from an external *Strobe* signal.
- *Shutdown:* disables the charge amplifier so that no output is generated from the pixel.

Pixel Cell Readout Logic A block diagram of the column-pair readout is shown in Fig. 9. LE and

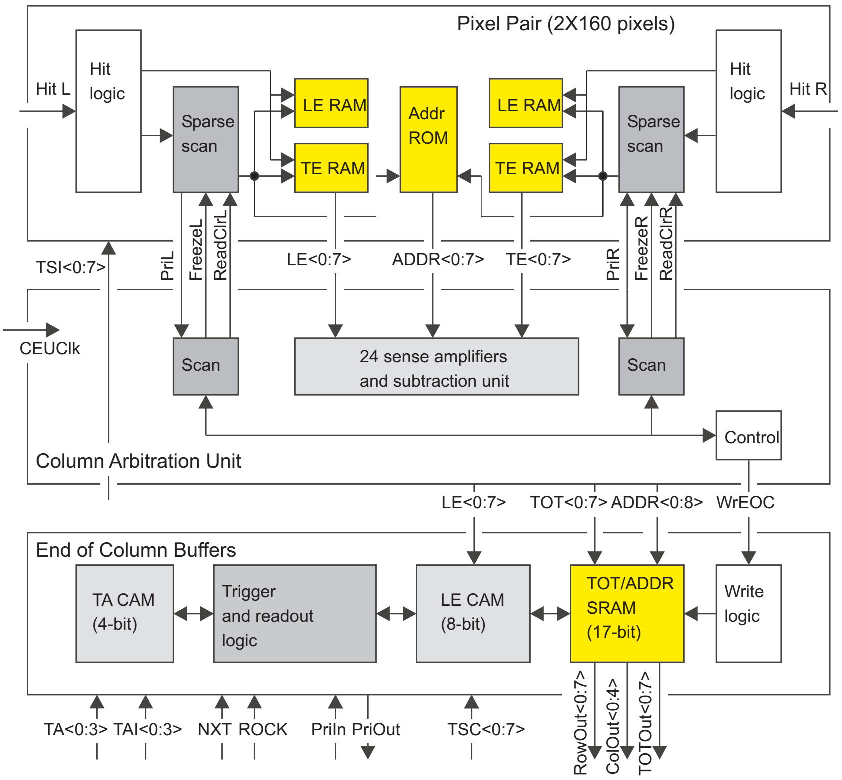


Figure 9. Block diagram of the column-pair readout.

TE timestamps are temporarily stored in local memories before being transferred to the hit-buffers at the chip periphery. A digital circuit generates two short (1 *ns*) strobes at the LE and TE comparator edges. These signals are used to store the 8-bit Gray-coded time stamp in two memories. The time stamps, generated at the chip periphery, running at 40 MHz, are distributed differentially in order to decrease the digital crosstalk to the analogue circuits and the sensor electrodes. The complete hit information is available after the TE of the comparator signal and data transfer starts. The time stamp of the LE (8-bits), of the TE (8-bits) and the row number (8-bits) are transferred to the end-of-column (EoC) buffers. Transfer happens by a priority mechanism that selects cells with data starting from the top row. The topmost cell with a hit transfers its data to the bus and all the cells below it are inhibited. When the cell is read out, it releases the priority encoder bus and subsequent hits are selected and put on the readout bus. The readout speed is limited by the time the priority logic needs to ripple down. Hits can ripple through at a programmable speed that is obtained from the 40 MHz clock division. The maximum speed at which bytes can be transferred to the EoC is 20 MHz.

Column Readout Controller The readout is column based, and two columns are read out from the same controller. The first task of the controller is the generation of the readout sequence to transfer hit information: LE and TE timestamps, and the pixel-row address into an EoC buffer. This operation begins when data is complete, which is after the TE discriminator is activated. The transfer of hits from a column pair is synchronized by the Controller end-of-Column Unit (CEU), which operates at a selectable speed of 5, 10, or 20 MHz. A total of 64 hit buffers are available for each double-column. The second task involves digital processing of the hit data. Hit information is formatted by the CEU. Formatting includes the ToT calculation: subtraction of a TE time stamp from a LE timestamp. Optionally, a digital threshold may be applied to the ToT, and a timewalk (time slewing for small charges with respect to high charge) correction may be applied (write a hit twice if below correction threshold, once with LE and once with LE − 1, or both. These operations are pipelined to minimize deadtime, but the EoC writes cannot occur faster than 20 MHz. Hit information is written to the EoC buffer, where it waits for a corresponding L1 trigger. If a trigger arrives at a time corresponding to the LE time stamp plus a programmable trigger latency, the hit is flagged as belonging to a particular 4-bit trigger number. Otherwise, it is reset and the buffer is cleared. Once the chip has received one or more L1 triggers, the trigger FIFO will no longer be empty. This initiates a readout sequence in which the EoC buffers are scanned for the presence of hits belonging to a particular trigger number. If hits are found, they are sent to the output serializer block, which encodes and transmits them to the MCC. After all hits for a given trigger number have been sent, an End-of-Event (EoE) word is appended to the data stream. All of these operations occur concurrently and without deadtime, with all column pairs operating independently and in parallel.

Event readout from the EoC buffers happens concurrently with the column readout. When the chip-level readout controller starts processing a particular L1 event, it first broadcasts the corresponding L1 readout address to all buffers. All cells with hits waiting for readout compare their stored L1 address with a request value. The readout of the selected L1 hits is controlled by a priority network, which sorts them in column and row order.

Chip Level Readout Controller The chip-level readout controller collects hit data from the EoC buffers and transmits the results off the chip serially. All hits belonging to the same L1 are grouped together into a single event, and events are transmitted out of the chip in consecutive trigger order. When a L1 trigger arrives, the current bunch-crossing time and a buffer-overflow bit are stored in a FIFO memory, which has a depth of 16 locations. This allows the chip to keep track of 16 pending L1 signals. The write-pointer of the FIFO is used as the L1 identification, which is sent to the hit buffers. The readout sequence is started as soon as the FIFO receives an L1 trigger. If the L1 priority scan in the hit buffers flags cells with matching trigger numbers, the data of the first cell in the hierarchy is sent to a global data bus, where the information is copied to a shift register. The content of the shift register is then transmitted serially. This is repeated until the priority scan shows no more hits. An End-of-Event data word, which includes error flags, is then added to the event.

Chip Configuration FE-I3 has 231 global configuration bits plus 14 local bits for each of the 2880 readout channels. The global bits are the settings for eleven 8-bit bias-current DACs, for one 10-bit calibration voltage DAC, for the global threshold bits, for the L1 latency, for the ToT filter thresholds, for column-enable bits, as well as for others. The configuration is loaded into the chip using a serial protocol running at 5 MHz. This protocol uses three chip input pads: a data input, a clock and a load. Each write operation begins with a 4-bit address, which permits the 16 chips in a module to receive independent configurations. The address of each chip is encoded with wire bonds during module assembly.

4.2.3 Requirements, Performance and Production

The design requirements for the pixel front-end electronics come from operation at high radiation doses, from the time resolution of 25 ns to separate two contiguous bunch crossings, from noise, from the minimum operation threshold and dispersion and from the overall power budget. The calibration relies on a 7-bit adjustment of individual pixel thresholds (tuning). The untuned (tuned) threshold dispersion σ is 800 (70) electrons equivalent-input charge (e). The noise with the sensor attached is 160 e (for a pixel size of 50 μm $\times$ 400 μm) and the typical operating threshold is 4000 e, which results in hits with signals $> 5500\,e$ appearing in the correct 25 ns time bucket (described as in-time threshold) [17, 18]. Neither the dispersion nor the noise depend on the choice of threshold. The tuned thresholds have been observed to re-disperse with moderate radiation dose in prototypes, and it is expected that periodic threshold re-tuning will be needed. However, the actual dispersion rate in the real operating environment will need to be measured. A selectable option internally duplicates near-threshold hits in two adjacent time buckets in order to allow for recovery of in-time threshold inefficiencies. Measurements made on a few modules irradiated to 600 kGy show a negligible tuned threshold dispersion and a 20% increase in the noise, despite the very high induced sensor leakage current (60 nA for normal pixels at $-7\,^{\circ}$C). For a configured chip, the typical digital current is 45 mA at 2 V and the analogue current is 75 mA at 1.6 V for a total power of 220 mW.

Chip production was made in batches of 48 wafers. There are 288 chips on each 8-inch wafer. Six production batches were purchased along with the six wafers from an engineering production run. The average wafer-probing yield was about 80%. The ATLAS pixel detector contains a total of 27904 front-end chips. The wafers were probed using semi-automatic probe stations. Each chip was fully characterized including measurement of a reference calibration capacitor value using a dedicated circuit only available during probing. This removed process variations from the charge and threshold calibration scale. The test time was approximately 30 hours per wafer. Chip selections was based on the evaluation of 30 analog and digital parameters. Every chip was also probed after dicing the bumped wafers (section 6) using custom vacuum chucks to hold up to 60 chips. About 2% of the chips failed after dicing. In addition, the indium-bumped chips were photographed during probing and 160 images-per-chip archived for future reference.

4.3 Module Control Chip (MCC)

4.3.1 MCC History

The prototype sequence leading up to the Module Controller Chip (MCC) is shown in Table 4. The very first version of the chip, submitted in 1998, was fabricated in a radiation-soft process

Chip	Year	Std.Cells	Transistors	Chip size [mm^2]	Technology
MCC-AMS	Apr 1998	17 922	363 000	10.3×6.3	AMS 0.8μm CMOS, 2M
MCC-D0	Aug 1999	–	–	6.1×3.5	DMILL 0.8μm BiCMOS 2M
MCC-D2	Aug 2000	13 446	328 000	11.9×8.4	DMILL 0.8μm BiCMOS, 2M
MCC-I1	Nov 2001	33 210	650 000	6.38×3.98	DSM 0.25μm CMOS, 5M
MCC-I2	Feb 2003	67 919	880 000	6.84×5.14	DSM 0.25μm CMOS, 5M
MCC-I2.1	2003	67 919	880 000	6.84×5.14	DSM 0.25μm CMOS, 5M

Table 4. Summary of the ATLAS pixel MCC chips. The number of metal layers in a chip is designated by 2M (two metal layers) or 5M (five metal layers).

using 0.8 μm CMOS technology [19]. This chip was extensively used when building radiation-soft modules. The technology was chosen as it was very close to the 0.8 μm BiCMOS DMILL technology which, at the time, was the chosen radiation-hard technology for the ATLAS pixel detector.

A first prototype of the rad-hard chip (MCC-D0) was built in 1999. It contained only one Receiver, but all the remaining circuitry was implemented thereby providing a good test of the DMILL technology. The final version of the chip (MCC-D2) was submitted in August 2000. The chip worked fine but had an unacceptably low yield, for both MCC-D2 and FE-D2. Consequently, this technology was abandoned.

At this time, the MCC was ported to the DSM 0.25 μm CMOS technology, and the MCC-I1 chip was submitted in November 2001. A new version of the chip, MCC-I2, was made in 2003 in order to provide better Single Event Upset (SEU) hardening to the chip. It turned out that this chip had a small error that could be corrected by modifying only one metal line. Six additional wafers, containing the correction in the layout, were produced in 2003 leading to the final MCC-I2.1 chip.

4.3.2 Design

This section briefly describes the actual implemetation of the production MCC chip, labeled MCC-I2.1. A simplified block diagram of the MCC internal architecture is shown in Fig. 10. The MCC has three main system tasks: (1) loading parameter and configuration data into the FEs and into the MCC itself; (2) distributing timing signals such as bunch-crossing, L1 trigger and resets; and (3) reading out the FE chip and event building.

System Configuration The FE chips and the MCC must be configured after power-up or before starting a data-taking run. It is possible to write and read to all the MCC registers and FIFOs. This is used to configure, to read status information or to test the functionality of the chip. For this last function we provide a special set of commands that allows one to write simulated events into the FIFOs and to run the Event Builder with the stored values in order to check the complete functionality of the chip. Once the MCC is embedded in the pixel detector, it will be important to

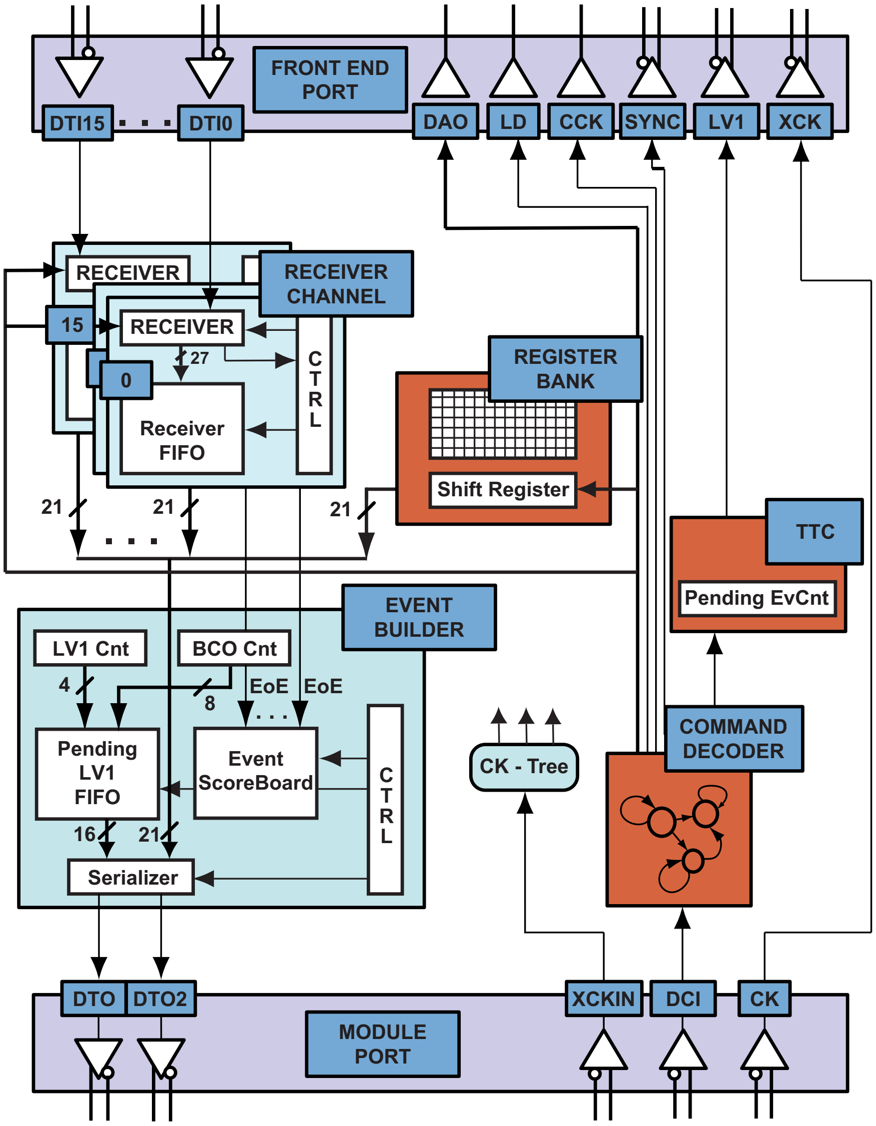


Figure 10. Module Control Chip block diagram.

test whether the event building works with known simulated events. Global FE chip registers and parameters in each of the pixel cells are written and read back through the MCC.

Trigger, Reset and Timing The second task of the MCC is the distribution of L1 triggers, resets and calibration/timing signals for the FE chips. In *Data Taking* mode, each time a L1 trigger command is received by the MCC, the Trigger, Timing & Control (TTC) logic issues a trigger to the FEs, as long as there are less than 16 events still to be processed. In case of an overflow, the L1 trigger is not generated by the MCC and the corresponding event is lost. The information is sent to the ROD together with the number of missing events in order to keep up with event synchronisation. In addition to the triggers, the TTC logic generates a hierarchy of reset signals that can be applied either to the MCC or to one or more FE's. The last function of the TTC logic is the ability to issue calibration strobes to the FEs.This is used to calibrate the FE analogue cells on a pixel-by-pixel basis.

Event building The read-out logic that was chosen for the pixel detector is a data-push architecture with two levels of buffering: EoC buffers in the FE chips and 16 individual 128×27-bit deep FIFOs (ReceiverFIFO) at the MCC inputs.

Event readout and building is by far the most complicated task, and it occupies most of the chip area. Data received from the FEs, in response to a L1 trigger, are deserialised and buffered in 16 FIFOs, one FIFO for each receiving FE line. These FIFOs are used to derandomise the 16 data flows from the FEs and are used by the event builder to extract ordered hits and to prepare them for transmission out of the pixel module. Event building is performed by two concurrent processes running in the MCC. The first (Receiver) deals with filling the 16 input FIFOs with data received from the corresponding FE chip, while the second (Event Builder) extracts data from the FIFOs and builds up the event. Each FE sends data as soon as they are available with two constraints. Event hits must be ordered by event number and for each event an end-of-event (EoE) word is generated. The EoE is also sent for the case of an empty event to maintain the event synchronisation.

The event transmitted to the ROD is organized by the Event Builder process on an event-by-event basis, instead of a hit-by-hit basis. If the FIFO becomes full while storing incoming hits, all subsequent hits are discarded and only the EoE word is written into the FIFO. In this case, a truncated event flag will be stored in the ReceiverFIFO and then recorded to the MCC output data stream. The mechanism ensures that reconstructed events are not corrupted by FIFO overflows.

As soon as the Event Builder finds that an event is completely received from all of the 16 FEs, it starts building up and transmitting the event. The Event Builder learns from the Scoreboard when the events are complete. The first information written to the output data stream is the bunch crossing identifier (BCID) and the L1 identifier (L1ID). At this point the Event Builder starts fetching data from the ReceiverFIFOs, until it finds an EoE in the data. Once the Event is finished, a Trailer word is sent out to inform the ROD that the Event has ended.

I/O Protocols Several serial protocols were defined for communication to/from the ROD/MCC and the MCC/FE. All protocols that are active during data taking use only LVDS-type signals (low-voltage differential, but not necessarily conforming to the LVDS standards), whereas signals occuring during configuration use single-ended CMOS to reduce the number of interconnection lines. Communications from the ROD to the MCC use a 40 Mb/s data line (Data Command Input - DCI) validated by the rising edge of the 40 MHz clock (CK).

The MCC to ROD link may use 40, 80 or 160 Mb/s data rates. For the case of 40 Mb/s, a new bit is transmitted at every rising edge of the CK. For the 80 Mb/s, bits are sent at both clock transitions. Finally for 160 Mb/s, both lines and clock edges are used. This can be considered as a 2-bit parallel link. Only the event readout uses the two higher bit rates. Readout of configuration data is always at 40 Mb/s. The robustness of data passing from the MCC to the ROD is improved by providing a bit-flip-safe Header and by adding synchronisation bits after a known numbers of clock cycles.

Communications from the MCC to the FE chips are accomplished using a serial CMOS data bus (Data Address Output - DAO), a CMOS control line (Load - LD) and a 5 MHz validation

CMOS clock (Control Clock - CCK). Both configuration and event data from the FE to the MCC are transmitted using 16 individual LVDS serial links (Data Input - DTI). The MCC and the FE use the 40 MHz (XCK) system clock fanned out by the MCC, which is obtained from the beam crossing clock. The clock is distributed to the 16 FEs in a module using a multi-drop LVDS connections from a single MCC output.

Special care is needed in the implementation of the Data–Taking protocols in order to minimize the effect of possible Single Event Upset events. In particular, while in data taking mode, there are only two possible 5-bit commands: 'trigger' and 'exit data-taking modes'. All permutations of the trigger command, obtained by flipping one single bit, are also interpreted as a trigger command with the correct timing.

4.3.3 Requirements, Performance and Production

The design requirements include operation at high radiation dose, time resolution of 25 ns separating two contiguous bunch crossings, the expected bandwidths at the highest luminosity, the L1 trigger rate of 100 kHz and the number of FE chips that are controlled in a module.

The 16 FIFO's in the MCC were designed to handle the expected data rate of the FE chips operating at full luminosity with a L1 trigger rate of 100 kHz. In addition, the circuits were designed to be robust against a Single Event Upset (SEU). This problem was addressed using either triple redundancy majority logic or error detection and correction schemes. Several modules were irradiated up to (and in some cases beyond) the full LHC-lifetime dose, continuously reading out the data during irradiation. From these SEU studies, we expect stable operation at the LHC without a significant loss in the configuration data coming from bit-flips in the memory elements.

For a configured chip, the typical digital current is 145 mA at 2.0 V. All MCC-I2.1 chips were produced in a single batch of six wafers. The number of potentially good chips per wafer is 536. The measured yield was 83%, providing a total of 2666 good chips. A total of 1744 chips are used in the ATLAS pixel detector. The wafers were probed at a commercial vendor using supplied test vectors. Test vectors were produced using Automatic Test Pattern Generation (ATPG) design methodology together with additional hand generated vectors. The combined test vectors provided almost 100% fault coverage of the chip.

4.4 Optical Communication

4.4.1 Optical Link Architecture

The communication between the detector modules and the off-detector electronics occurs via optical links. The opto-links were selected to implement electrical decoupling and to minimize the material budget. The architecture was inherited from the ATLAS SCT [20]. Modifications were made to adapt to the data-rates, modularities and radiation hardness needs of the pixel detector.

A block diagram of the optical-link system architecture is shown in Fig. 11. The two main components in the optical-link system are the opto-board, on the detector side, and the Back of Crate Card (BOC), on the off-detector end. In order to keep the material budget low, accommodate fiber routing requirements, control radiation exposure, and permit the use of optical arrays, the opto-components and the related receiver/driver IC's were not implemented on the detector modules. The optical components were put on the opto-boards at Patch Panel 0 (PP0), at a distance of

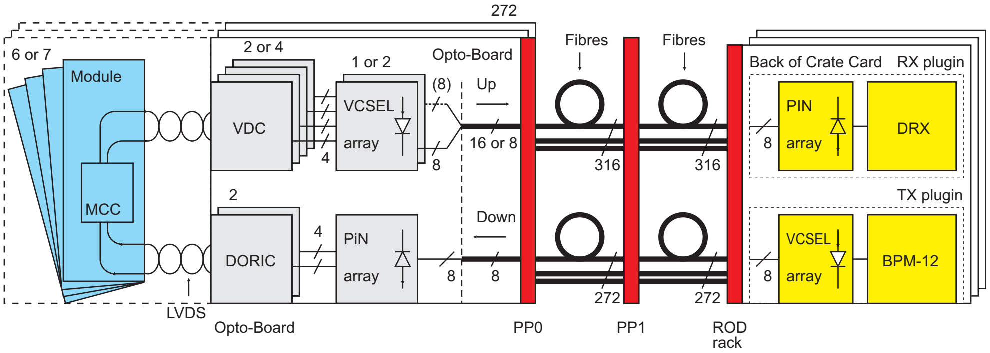


Figure 11. Optical-link system architecture.

up to about one meter from the modules and at relatively large radius, namely about 200 mm inside the Pixel Support Tube.

The transmission of the signals from the detector modules to the opto-boards uses LVDS electrical connections. These serial connections link the MCC with the VCSEL Driver Chip (VDC) and the Digital Optical Receiver IC (DORIC) sited on the opto-boards. The DORIC and VDC designs were also derived from the SCT project, but have been adapted to survive the higher radiation dose expected in the pixel detector. These chips have been fabricated on the same silicon wafers used to produce the MCC chips.

The communication with each detector module uses individual fibres: one for down-link and one or two for up-links. Trigger, clock, commands and configuration data travel on the down-link, while event data and configuration read-back data travel on the up-link(s). On the down-link, a bi-phase mark (BPM) encoding is used to send a 40 Mb/s control stream on the same channel as the 40 MHz Bunch Crossing (BC) clock. Decoding of the BPM channel within the DORIC recovers both the data stream and the clock signal. The use of individual links for every module permits the adjustment of the timing used to associate the hit to the bunch crossing. The timing adjustment is accomplished by changing the delay of the transmitted signal with respect to the phase of the LHC machine reference clock received in the BOC.

The readout bandwidth required to extract the hits from the detector modules depends on the LHC instantaneous luminosity, on the L1 rate and on the distance between the module and the interaction point. Simulation of the readout architecture using generated physics events [19] shows that a rate of 40 Mb/s for the Layer-2 modules, 80 Mb/s for the Layer-1 or Disk modules and 160 Mb/s for the b-layer modules are needed to keep the number of lost hits due to bandwidth saturation sufficiently low. The data transmitted in the up-links are encoded in non-return-to-zero (NRZ) format. Electrical-to-optical conversion occurs in the opto-boards on the detector side and in the optical-receiver (RX) and optical-transmitter (TX) plug-ins in the BOC.

There are two flavours of opto-boards: Disk/L1/L2-boards (D-board) with eight down-link and eight up-link channels and b-layer-boards (B-board) with seven down-links and 14 up-links. The B-boards use two 80 Mb/s channels to obtain the aggregate bandwidth of 160 Mb/s. Because of the modularity of staves (13 modules) and of sectors (six modules) D-boards use either six channels for the disk-sectors or six or seven channels for the half-staves in Layer-1 and Layer-2.

In the off-detector part of the links, one BOC exists serves each ROD. BOCs have a a variety of hardware options that are implemented by equipping the card with a variable number of optical-receiver or optical-transmitter plug-ins. Each plug-in, in principle, can serve up to eight modules, but, in practice, only six or seven are used due to the modularity of the detector. BOCs come with four TX plug-ins and four RX plug-ins, where the maximum bandwidth requirement is 40 Mb/s, with two TX and two RX for 80 Mb/s and with one TX and two RX for 160 Mb/s. Two custom chips have been designed by the SCT collaboration and used in the optical plug-ins: the DRX (12-channels Data Receiver ASIC in the RX) and the BPM-12 (12-channels Bi-Phase Mark encoder ASIC in the TX). In the BOC there is also the optical S-Link interface used to send the ROD output to the ATLAS Readout Buffer (ROB) units, which are the next level up in the event readout chain.

4.4.2 Opto-Board

The opto-board is the optical-electrical interface on the detector side. It consists of a beryllium-oxide (BeO) printed circuit board measuring 2×6.5 cm^2. As discussed in Section 4.4.1, two types of opto-boards (D-boards and B-boards) exist and six or seven detector modules are connected to them. The D-boards are equipped with one PiN diode array and one VCSEL (Vertical-Cavity Surface-Emitting Laser) array, while the B-boards have a second VCSEL array. Each opto-board has two 4-channel DORIC chips, whereas two and four 4-channel VDC chips are loaded onto the D-board and B-boards, respectively. The opto-package (opto-pack), which holds the PiN/VCSEL arrays and the connector for the optical fibres, is custom designed to fulfill requirements of low mass, and be non-magnetic and radiation tolerant. The total number of opto-boards in the detector is 288. This is more than the minimum 272 (44 B-boards and 228 D-boards) needed to read out the detector so that spares are available to recover from problems during integration. Ultimately, only one spare board was used. The remaining spares are mounted on the Patch Panel 0 elements, but not connected.

PiN Diode Array Arrays of silicon PiN diodes are used to receive the data sent by the VCSELs. Epitaxial silicon PiN diodes are used because their intrinsic layer provides a thin active layer allowing for fast operation at low PiN bias voltage. The active area of each individual PiN diode is circular with a diameter of 130 μm, and the depth of the intrinsic region is 35 μm [20]. A PiN current amplitude of 100 μA ensures a Bit Error Rate (BER) less than 10^{-9}.

DORIC The Digital Optical Receiver Integrated Circuit (DORIC) amplifies the signal detected in the PiN diode and extracts the clock and data from the BPM encoded signal. Data and clock are transmitted in LVDS format to the MCC. Each DORIC chip contains four identical channels. The specification for the current from the PiN diode is in the range of 40 μA to 1 mA. The requirements for the clock are a duty cycle of (50 ± 4) % and a time jitter better than 1 ns.

The DORIC has been designed to have a bit error rate of less than 10^{-11} after a lifetime-radiation dose, for a PiN-diode bias current amplitude of 40 μA. The PiN diode current amplifiers use a single-ended scheme [21], avoiding the direct application of the diode bias voltage (10 V), which is much higher than the rating of the DSM technology. The DORIC must withstand up to 170 kGy over the expected 10 years of ATLAS operation. It is, therefore, implemented in the same (0.25 μm) CMOS technology as used for FE, MCC and VDC.

VDC The VDC converts the LVDS input signal, received from the MCC, into a suitable single-ended signal to drive the VCSELs in a common cathode array configuration. The VDC chips have four channels and drive one half of the VCSEL arrays. An external current used to drive the VCSEL operates up to 20 mA. The nominal current to operate the VCSEL is 10 mA. A standing (dim) current of $\sim$1 mA is provided to improve the switching speed in the VCSEL. The dim current is remotely controlled by an external voltage. The requirement for the rise/fall time (20 to 80 %) is in the range of 0.5 to 2.0 ns, where 1.0 ns is nominal. A voltage ($V_{I_{set}}$), remotely controlled, determines the current I_{set} that sets the amplitude of the VCSEL current (bright minus dim current). The chip is designed to have constant current consumption, independent of the VCSEL being bright (on) or dim (off), to avoid generating ripple (noise) on the power supply which is being shared with the two DORICs on an opto-board.

VCSEL Array Vertical-Cavity Surface-Emitting Laser (VCSEL) arrays are used to transmit the data optically. The main advantages of VCSELs are that they provide large optical signals at very low currents and have fast rise and fall times. In order to maintain a low laser threshold current, VCSELs use ion-implants to selectively produce a buried current-blocking layer to funnel current through a small area of the active layer. The VCSELs [20] used in the pixel and SCT systems have an oxide implant to achieve the current confinement, which is becoming the standard VCSEL technology since it produces lower current thresholds at higher bandwidth. VCSELs are produced in arrays of eight diodes. The typical fibre-coupled-power per channel is greater than 1 mW at a drive current of 10 mA. The optical power at 10 mA is sufficient to give a noise immunity of 6.2 dB. Using a slightly higher current, it is possible to add another 1.8 dB of noise immunity [20]. The down-link, where the current is not a critical issue, can profit from this improved margin corresponding to a higher immunity to SEU and to a lower Bit Error Rate.

4.4.3 Back of Crate Card (BOC)

Each BOC [20, 22] is connected to one ROD through the crate back-plane. The BOC has two functions: it interfaces between the ROD and opto-links and it controls the distribution of the timing to the on- and off-detector electronics. Each BOC receives a system clock signal and redistributes it to the pixel detector modules and ROD. Each detector module needs a precise phase adjustment of its 40 MHz clock relative to the bunch-crossing time reference. The adjustment of this phase can be done for each module independently using the BPM-12 ASIC. [20] The phase of the data from the modules relative to the global BOC clock can be adjusted using the PHOS4 ASICs [23]. The adjustment range is 0–25 ns in steps of 1 ns. The clock phase can also be adjusted using the same ASIC to ensure stable data transmission to the ROD. The opto-electrical conversion and the connection to the fibres are located in two plug-in cards: TX-plug-in and RX-plug-in, respectively, for transmission and reception of optical data. The TX-plug-in has an 8-channel VCSEL array and a BPM-12 ASIC. The RX-plug-in has an 8-channel PiN diode array and a DRX ASIC. [20]

DRX The DRX ASIC amplifies, discriminates and converts the signal from the PiN diode into an LVDS signal. The comparator is DC coupled and the threshold can be controlled over a current range up to 255 μA by an external voltage reference generated by a DAC. The DRX chip was originally designed for the ATLAS SCT detector and contains 12 channels. Only eight channels per chip are used in the pixel BOC.

BPM-12 The Bi-Phase Mark (BPM-12) ASIC encodes clock and data in the Bi-Phase Mark format for the fibre optic transmission. This chip was originally designed for the SCT detector and only 8 of the 12 channels are used for the pixels. A critical specification for this component is to have a short delay between the input signals and the encoded outputs to minimize the overall L1 trigger delay. The measured delay value is 60 ns. In addition, the BPM-12 has the capability to delay data transmitted to the detector by up to 63 full clock cycles to adjust for the trigger latency. This is implemented as a coarse delay (step-size 25 ns) covering the 63 clock cylces and a fine delay (step-size of about 300 ps) to cover the full range of one clock cycle with a fine-grained phase adjustment for each module.

4.4.4 Opto-fibres

The connection between the BOC and the opto-boards uses optical fibres. Two different kinds of fibres are used, Stepped Index Multi-Mode fibres (SIMM) and GRaded INdex multi-mode fibres (GRIN). SIMM fibres have been tested to be radiation tolerant but have lower bandwidth per unit length than GRIN fibres [24]. To optimise the bandwidth and radiation tolerance, splicing of 8.1 m SIMM and 71.1 m GRIN fibres have been used. The fibres are ribbonised into 8-way ribbons, and eight ribbons are bundled together to form an optical cable. The 8.1 m length of the SIMM fibre is terminated by an MT16 connector at $\sim$ 2.5 m from PP0 (at PP1). A total of 84 cables were installed outside the Pixel Support Tube. SIMM fiber ribbons were used within the Pixel Support Tube to connect the opto-boards mounted at Patch Panel 0 with the multi-ribbon connector at PP1.

4.4.5 Production and Testing of Opto-Link Components.

The opto-boards were required to pass a stringent quality assurance (QA) procedure, including burn-in and thermal cycling, at the two production sites. In addition, the boards were required to pass a reception test at CERN before installation on the service panels. Subsequent tests were also then performed. Each opto-board was required to produce good optical power, similar to those observed during the production testing of each board, and over a reasonable DAC operating range in the DRX. Three major problems were encountered during the test and are discussed below [25].

- *Common Serial Resistance (CSR).* During the reception test it was discovered that some of the VCSELs on the opto-boards produced very little or no optical power on all channels. Moreover the optical power on one channel was found to also depend on the current from other channels. This could be understood as the development of a common resistance in the array. The voltage drop on the CSR results in an inadequate voltage to drive the VCSELs. The only fault that could be identified in the production process of the opto-pack was that the thickness of the conductive epoxy under each VCSEL array was $\sim 5\ \mu$m, as opposed to $\sim 15\ \mu$m as recommended by the manufacturer. A procedure was formulated to estimate the CSR by measuring the current-vs-voltage (IV) characteristics of one VCSEL channel with and without current in the other channels. Opto-boards with $> 2.25\ \Omega$ of CSR in the VCSELs were rejected, corresponding to $\sim 7\%$ of the total production.

- *Slow Turn On (STO).* The SCT group discovered that, following a few microseconds of inactivity, some of their VCSEL arrays took a few microseconds to produce full optical power. A random sample of opto-boards was tested for STO at the production sites, and it was found that there was no indication of the problem until the test was performed on a prototype service panel with the production readout chain, including the fibres. It turned out that this subtle STO behaviour depended on the distance between the VCSEL surface and the fiber in a polished, mechanical-transfer (MT) ferrule. The production fiber with the bevelled edges on the MT ferrule allowed the fiber to be pushed closer to the VCSEL, picking up transverse modes that might have been time dependent. The exact cause of the slow turn-on behaviour is still under investigation. A new testing procedure was introduced, resulting in rejection of $\sim 7\%$ of the opto-boards with severe STO VCSELs.

- *Fluctuations in the optical power (noise).* It was discovered that the optical signals had more noise than was observed during production testing, because of the long electrical cables. These cables allowed noise to enter into the VCSEL bias voltage via the VCSEL current control circuitry in the VDC. Consequently, a bypass capacitor on the bias voltage was not mounted due to the concern that the capacitor might leak after exposure to radiation, rendering the opto-board inoperable. There was no data to support the above concern but the decision was taken because the opto-boards on the production test system had low noise when no bypass capacitor was mounted. Fortunately, the capacitors could be readily retrofitted and this greatly reduced the fluctuations in the optical power.

Another problem was discovered when the prototype service panel was operated with the cooling system. The temperature of the opto-boards at a certain region on the service panel was much lower than anticipated. We required the opto-packs on the opto-boards to produce good power at 10°C as part of the QA requirements. However, a significant fraction of the opto-packs did not produce sufficient optical power at -25°C, another temperature where data was collected as part of the QA procedure. The optical power of these opto-packs was below the specification of 350μW on the prototype service panel. To overcome the problem, it was decided to add a remotely-controllable heating element to the opto-boards, so that the opto-boards could operate at up to 20°C.

One VCSEL and one PIN channel failed during the detector integration. It is believed that the former was due to electrostatic discharge damage and the latter due to detached solder (cold solder) on a lead of the opto-pack. The affected modules were recovered by switching to a spare opto-board, in one case, and by moving one module to an unused (seventh channel of a board serving only six modules) channel, in the other.

Optical fibres, fabricated and assembled by external companies, have been tested during production by measuring light coupling and attenuation. Two 8-way ribbons in the external optical cables (eight ribbons each) showed failures. Fibres were also tested after installation using a Optical Time Domain Reflectometer (OTDR) and then replaced by spares, if they failed the test. Similar tests were performed on the ribbons inside the Pixel Support Tube as they were installed on service panels.

4.4.6 Opto-link Performance

The selection and qualification of the components for use in the opto-link system was done by extensive laboratory tests and irradiation campaigns. From measurements made on single components or parts of the system, a stable performance for the opto-links over 10 year of operation at LHC is expected [21, 24, 26–28]. The measurement of the BER in opto-link ring-loops running at 40 Mb/s (80 Mb/s) gives an upper limit $BER < 1.45 \times 10^{-14}$ ($BER < 3.62 \times 10^{-14}$). In fact no single errors were found during the tests [29]. The method to adjust the timing in the BOC to time the pixel detector with a bunch crossing is reported in [30]. Automatic tuning of the opto-link parameters for the entire detector (the system laser forward currents, PiN-diode photo-current thresholds, etc.) should be achievable in under 10 minutes.

4.5 Data Acquisition System

The pixel detector Data Acquisition System (DAQ) has been designed following the specifications of the ATLAS global DAQ architecture [31].

4.5.1 Architecture Overview

The off-detector readout architecture of ATLAS consists of two parts: a sub–detector specific part, where the Readout Drivers (ROD) are the main building blocks, and an ATLAS common design that is referred to as the Read Out System (ROS) [32].

The pixel ROD [33] is a 9U-VME module. The ROD handles the data transfer from the on-detector electronics to the ROS system. Data from the detector arrive at the RODs through the BOCs. Data pass through the RODs and are then received at the ROS by custom designed interface modules. The ROS is a PC-based system. These PCs temporarily store readout events in their memory and transfer only those accepted by the L2 trigger to the next level up in the readout chain.

ROD modules are plugged into ROD crates. There are nine crates with up to 16 ROD modules per crate. In total, there are 44 modules (three crates) for the b-layer, 38 modules for Layer-1 plus 28 modules for Layer-2 (four crates) and 24 modules (two crates) for the disks. A Trigger, Timing & Control Interface Module (TIM) [34–36] and a Single Board Computer (SBC) [37] complete the ROD crate. The TIM is the interface to the trigger system. The DAQ software running in the SBCs controls the modules in the ROD crate. There is no event traffic on the ROD VME–bus during normal data–taking. Data are routed directly from the ROD to the ROS PCs [32] via custom-designed optical links (S-Links). The VME-bus is, however, heavily used during calibration of the pixel detector. RODs are controlled, via the VME-bus, by the SBC, which also acts as interface to the global DAQ system.

Calibration data are treated differently from collision data. The procedure to calibrate the pixel detector consists of a sequence of injections of a known charge into the pixel's front-end amplifiers. The response of each pixel is measured as a function of the injected charge and of other parameters (thresholds, preamplifier feedback currents, trigger delay) that can be varied during the calibration procedure. The typical result of a calibration scan consists of a set of occupancy histograms corresponding to different values for the scanned parameters. In order to achieve maximum precision, it is important to extract data from the FEs at the maximum speed supported by the detector links. This makes it difficult to extract calibration data using the normal data path, as the read-out chain from the ROS to the Event Builder is designed to transfer only L2-trigger accepted events, while the detector links are designed to support the full L1 trigger rate. For this reason, during calibration runs, the ROD decodes the data stream sent by the front-end electronics, fills occupancy histograms and stores them in memory. The histograms are then extracted via the VME-bus by the SBC and sent to an analysis farm for further manipulation and archiving.

Single Board Computer (SBC) The Single Board Computer is a commercial VP-315[3] 6U VME card with a Pentium-M[4], having 1.6 GHz clock and 1 GB memory. The card uses a Universe II[5] PCI-VME bridge. It has three gigabit-ethernet interfaces, of which two are used, one to connect to the ATLAS control network and the second to the analysis farm, where histograms generated in the ROD are collected. Up to 40 MB of internal RAM memory is used to cache the configuration data needed in the pixel detector modules for a complete crate of RODs. The configuration data, cached in the SBC memory, are stored offline in a database server. The memory is also used as a transfer buffer for the histograms moved from the RODs to the analysis farm.

Trigger, Timing & Control Module (TIM) The TIM is the interface between a ROD crate and the ATLAS trigger system. It receives a TTC fibre-link from a Local Trigger Processor (LTP), carrying LHC bunch crossing (BC) and orbit signals, trigger signals such as the Level 1 Accept (L1A) and the trigger type, and control/synchronisation signals such as the event counter reset (ECR) and the synchronisation (SYN). These signals are distributed to the RODs via a custom backplane installed in the lower part of the VME crate. On the same backplane, the busy signals generated by the RODs pass to the TIM. The TIM can create a collective ROD Busy signal and send this signal to the LTP. The LPT on reception of the Busy signal stops the L1A to the detector electronics, thus allowing the front-end and ROD buffers to be emptied. Several features are implemented in the TIM to operate on the trigger signal. These include programmable delays on distributed triggers, generation of trigger bursts and strobe signals having a fixed delay from a L1A. Moreover, the TIM can be used as a local trigger generator with a programmable rate. This has been very useful for studying ROD and DAQ behaviour for simulated event rates.

Read Out Driver (ROD) The structure of the ROD is outlined in Fig. 12. Three main sections of the design are the control path, data flow path, and the Digital Signal Processing (DSP) Farm. The control path section consists of two Xilinx Field Programmable Gate Arrays (FPGA) and a Texas Instruments Fixed Point Digital Processor (TI 320C6201) operating at 160 MHz with a 32 MB SDRAM module. The Program Reset Manager (PRM) FPGA functions as a VME slave controller, allowing read and write access to all ROD and BOC registers and a configuration controller for the data path FPGAs. In order to allow the users to easily upgrade the firmware on the ROD, the PRM FPGA allows VME access to an on-board flash memory chip that stores the FPGA configuration data. The Master DSP receives commands and transmits replies to the VME host and coordinates the configuration, calibration and data-taking modes of the ROD. The ROD Controller FPGA is used in the control path as an interface for the Master DSP to the DSP farm, the BOC, and all

[3]From Concurrent Technologies Corporation, http://www.ctc.com
[4]From Intel Corporation, http://www.intel.com
[5]From Tundra Semiconductor Corporation, http://www.tundra.com

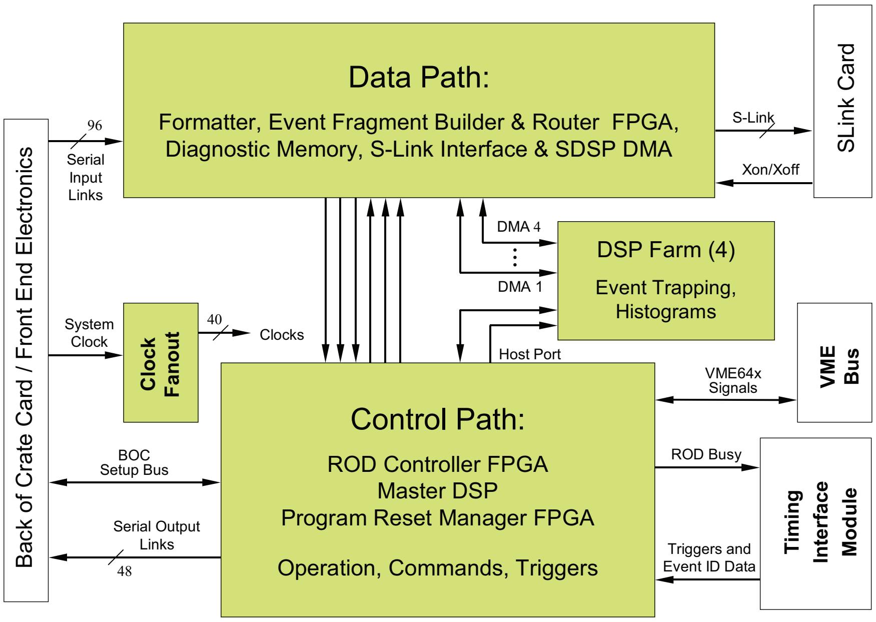


Figure 12. Block diagram of the ROD.

of the internal ROD registers in the data flow FPGAs. It also controls all of the required, data-flow-path specific, real-time functions on the ROD, including serial transmission of commands to the FE modules (two independent command streams can be sent to two modules or group of modules), calibration mode trigger generation, and transmission of TIM generated triggers and fast commands. In summary, these are the main actions performed by the control path block:

- full control of ROD reset and FPGA configuration;
- receives and executes commands from the SBC via VME;
- receives module configurations via VME and stores them in Master DSP memory;
- transmits configuration data to the modules;
- control of calibration procedures, transmitting triggers and configuration data to FE modules;
- control of FE module data histograms;
- propagation of trigger commands from the TIM to the FE modules.

The structure of the ROD Data Flow Section is outlined in the block diagram of Fig. 13. The data flow section receives serial data from the FE modules, packs the individual module fragments into a single ROD fragment and sends it to the ROS via the S-Link. Normal event data flows through the ROD via the Input Link Interface, which leaves the data unchanged. It can, however, trap the serial data stream in FIFOs (used in module configuration or to trap an event for diagnostics). The FIFOs can also be loaded with events for analysis by the ROD for diagnostics. After the Input Link Interface, the event data enters the Formatters. The Formatters convert the serial data

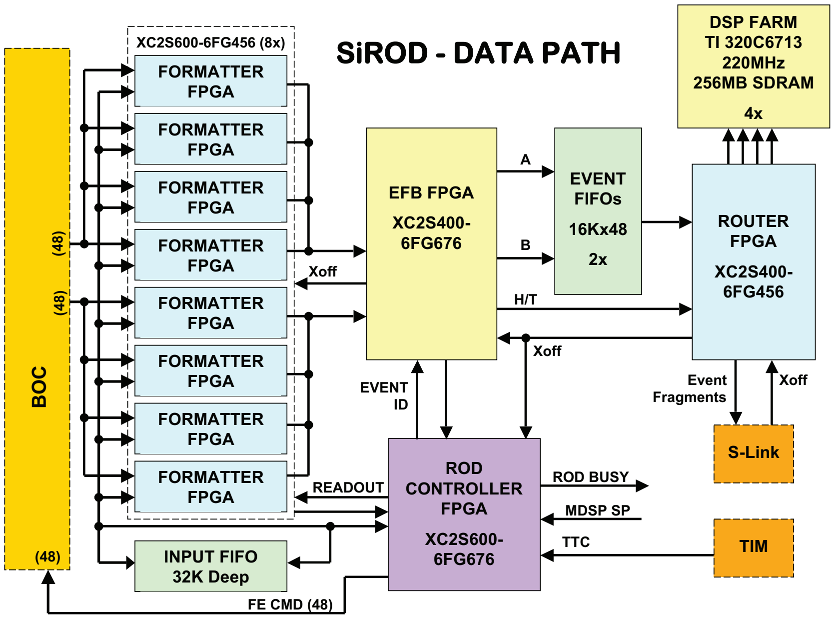


Figure 13. Block diagram of the ROD data flow section.

streams to parallel format, and fill the derandomising buffers used to queue events for transmission to the Event Fragment Builder (EFB) FPGA. An event is transmitted from the Formatters to the EFB after the Controller FPGA sends a command notifying that a Level 1 Accept has been sent to the modules. The ROD Event Fragment is constructed in the EFB using the ATLAS Event ID data that was transmitted from the controller FPGA. In normal data taking, the primary source of the ATLAS Event ID data is the TIM with the ROD providing some additional information. After the header and mode information is sent to the EFB, the ROD Controller FPGA issues one token to the Formatters, and event data is pushed to the EFB. The EFB checks L1ID and BCID values and records errors. It also records any errors that were decoded or flagged by the Formatters. The event data are then stored in two derandomising FIFOs. There are two identical engines in the EFB each capable of transferring 32-bit words at 40 MHz yielding a maximum rate of 320 MB/s. When an event is ready (header, data body and trailer in the FIFOs), it is transmitted to the Router. The Router has two main functions. The first one, which is for the main physics data path, is to transmit 32-bit data words to the S-Link at 40 MHz. If the S-Link is receiving data faster than it can transfer to the ROS, the S-Link can assert Xoff to apply back pressure to the ROD data path. When back pressure is applied, read out of data from the EFB FIFO is stopped. When the EFB memories are almost full, back pressure is applied to the Formatters. This will stop event data transmission from the formatter link FIFOs. The second function of the Router is to trap data for the DSPs. This is performed with no effect on the S-Link data during normal running. When the ROD is in calibration mode, the DSPs can assert back pressure to pause the ROD data flow.

Finally, the ROD is equipped with four ’Slave’ DSP processors (TMS320C6713)) with 256 MB memory each. They are connected to the Router FPGA from which they can sample the produced ROD fragments. Different tasks can run on the DSP processors to analyze captured events: monitoring task, used during normal data taking to compute average occupancy and detect noisy pixels or data transmission errors. Calibration tasks accumulate histograms during the multi-dimensional scan procedure and perform an analysis to reduce the data volume to be transferred to the SBC. During data taking, the DSPs spy on the data-flow at the maximum possible rate without introducing dead time or applying back pressure on the data flow path. During calibration, on the other hand, the slave DSPs analyse fragments, so they actually become the most important limiting factor on the data rate. For this reason the code of the calibration task must be optimised to maximum efficiency using the 128 KB internal DSP fast memory to fill the occupancy histograms.

4.5.2 ROD Crate Software and Calibration Analysis Farm

The ROD Crate software is the interface between the ATLAS Run Control and the pixel detector DAQ.

For each ROD in the crate, a ROD Interface thread is created. This gives access to the basic functionalities that an external application can perform on the modules using the ROD. The implemented functions range from very basic commands (like ROD module reset and configuration) to complicated scan procedures. The ROD software interfaces are based on Remote Procedure Calls (RPC). They use a Common Object Request Broker Architecture (COBRA) layer called Interprocessor Communication (IPC) which is used in most ATLAS DAQ applications. These interfaces can be accessed either locally in the ROD, from another process running in the SBC, or from a process running on a remote CPU. Only one application at a time can be allowed access to a given ROD; for this reason, each SBC runs a Crate Broker. Each process accessing a ROD must first ask the Crate Broker, verify if the requested resource is free and allocate it. Only at this point is access to the ROD Interface granted. The last element of the ROD Crate software is the Run Controller. This process is a local receiver of the commands issued by the central ATLAS Run Control.

During normal data taking, the ROD Crate Run Control allocates all the ROD Interfaces and executes the transitions (INITIALISE, CONFIGURE, START, STOP) as indicated by the global Run Control. During calibrations, the Run Control disconnects the RODs, which are then controlled by a Calibration Console, controlling the calibration procedure. The interface/broker mechanism gives the possibility to run a calibration or a debugging session on a ROD while the others are taking data. Occasionally the amount of data produced during a calibration may be too large to fit into the SBC memory. The histograms are then immediately moved (again using IPC) from the SBC to a remote analysis farm, which takes care of the final data analysis, including generating new configuration sets based on the tuning/calibration procedures, and archiving the results. Consequently, the memory of the SBC is not saturated, and a new scanning procedure is immediately started, while the analysis farm is analysing the previous data set.

4.6 Detector Control System (DCS), Power Supplies, and Interlock System

The operation of the pixel detector modules and the on-detector opto-components requires a complex power supply [38, 39] and control system [40, 41]. The following supplies are required at the module and opto-board level:

- V_{DDA}: analog low-voltage supply for the FE chips;

- V_{DD}: digital low-voltage supply for the FE chips and the MCC;
- V_{DET}: high-voltage supply to bias the sensor;
- V_{VDC}: low-voltage supply for the VDC and DORIC chips;
- V_{PIN}: PiN diode bias voltage;
- V_{ISET}: digital voltage to adjust the VCSEL bias;

Power supply requirements for pixel modules and opto-boards are summarised in Table 5. The adjustment of the operating conditions of the system requires a large modularity. Robust software packages are used to monitor and control the hardware. There is, in addition, an independent interlock system that focuses on safety for the equipment and human operators.

Supply Type	Supply Voltage [V]	Supply Current [mA]	Nominal Voltage [V]	Nominal Current [mA]	Nominal Power [mW]	Worst Voltage [V]	Worst Current [mA]	Worst Power [mW]
Module								
V_{DDA}	10	1500	1.6	1100	1760	2.1	1300	2730
V_{DD}	10	1200	2.0	750	1500	2.5	1000	2500
V_{DET}	600	2	600	1	600	600	2	1200
Total					3860			6430
D-board								
V_{VDC}	10	800	2.5	280	700	2.5	490	1225
V_{PIN}	20	20	10.0	–	–	20	20	400
V_{ISET}	5	20	1.0	–	–	2	20	40
Total								1665
B-board								
V_{VDC}	10	800	2.5	420	1050	2.5	770	1925
V_{PIN}	20	20	10.0	–	–	20	20	400
V_{ISET}	5	20	1.0	–	–	2	20	40
Total								2365

Table 5. Specifications for module and opto-board power supplies. D-boards serve disk and layers 1 and 2, B-boards serve B layer.

4.6.1 The Hardware of the DCS

The scheme for the powering, control and interlock system is shown in Fig. 14. The main components of the pixel DCS are:

- the power supplies to operate the sensors, front end chips and opto-boards;
- the Regulator Stations;
- temperature and humidity sensors plus monitoring devices for their readout;

- multi-channel current measurement units;
- the Interlock System;
- the DCS computers to control the hardware.

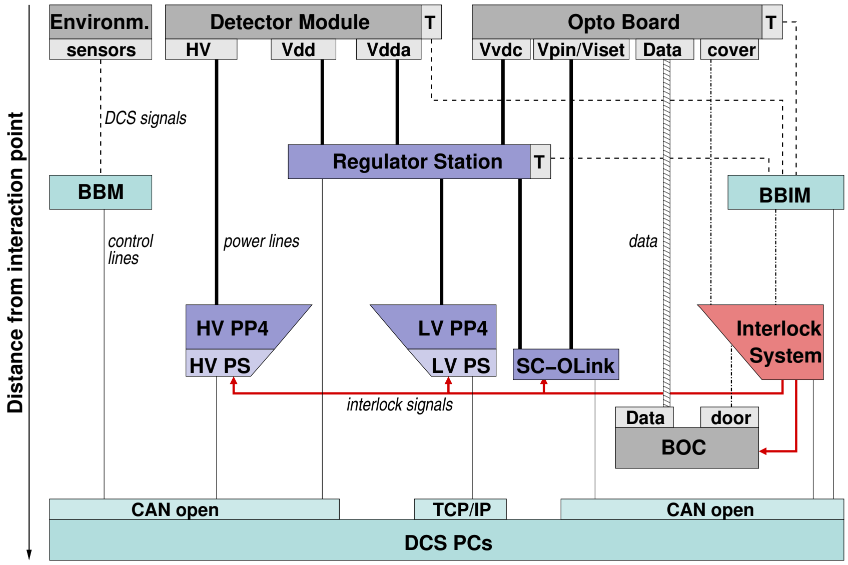


Figure 14. Overview of the hardware of the pixel detector control system.

To comply with the ATLAS grounding scheme, all power supplies and monitoring systems must be floating. Radiation damage requirements during operation of the sensors and the on-detector electronics imply that all power supplies have adjustable voltage outputs. For operational safety, over-current protection and interlock input signals are available for all the power supplies. The pixel power supply system has five main components: low voltage power supply (LV-PS), high voltage power supply (HV-PS), Regulator Station, Supply and Control for the Opto Link (SC-OLink), and the opto-board heater power supplies. Two low voltages supply the analog (V_{DDA}) and digital part (V_{DD}) of the front-end read out electronics. Both are delivered by the LV-PS, which is a commercial component – the PL512M from WIENER [6].

To protect the sensitive front end electronics against transients, remotely-programmable Regulator Stations are installed as close as possible (approximately 10 m) from the detector [42]. The Regulator Stations provide individual low-voltage power outputs with low ripple and protect the integrated circuits against transients up to 4 V. A Regulator Station consists of 12 circuit boards and a controller housed in a custom crate. One station can provide power for up to 84 detector modules and can also provide power to the opto-boards.

The pixel sensors are biased by the high voltage V_{DET} from the HV-PS. The HV-PS is assembled with EHQ-F607n_405-F modules provided by Iseg [7]. The LV-PS and HV-PS are, respectively,

[6]WIENER, Plein & Baus GmbH, Burscheid, Germany
[7]Iseg Spezialelektronik GmbH, Rossendorf, Germany

connected to the low voltage Patch-Panel-4 (LV-PP4) and to the high voltage Patch-Panel-4 (HV-PP4) that are used to distribute the power and monitor the currents of the individual lines.

The SC-OLink, a complex channel consisting of three voltage sources and a control signal, delivers adequate levels for the operation of the on-detector part of the optical link. Monitoring of temperatures and of humidity is performed by the Building Block Monitoring (BBM) and the Building Block Interlock and Monitoring (BBIM) crates. While the BBM provides a reading of values, the BBIM additionally creates logical signals, which are fed into the Interlock System. All components of the LV-PS, HV-PS, SC-OLink as well as the BOC boards are connected to the hardware based Interlock System that acts as a completely independent system. Several units guarantee safety for human operators as well as protect detector parts. The Interlock System has high modularity; more than a thousand individual interlock signals are distributed. The high modularity has been chosen to minimize the number of detector modules out-of-service, resulting from failure in a single module or system component. The Regulator System and some parts of the Interlock System (those installed inside the ATLAS detector) had to pass requirements pertaining to radiation tolerance.

Besides the LV-PS and HV-PS, all other components in the system are custom designed, adapted to the specific needs of the pixel detector and use the Embedded Local Monitoring Board (ELMB) [43] for monitoring through the DCS. ELMB is the ATLAS standard front end I/O unit for the slow control signals. The Control Area Network (CAN) interface of the ELMB and its CAN-open protocol ensure that the communication is reliable and robust. Different Openness, Productivity, Collaboration (OPC) servers are used to integrate the hardware into the higher level of the software. All together 630 CAN nodes on 43 CAN busses and 48 TCP/IP nodes for the LV power supplies are used to build the pixel control network. In total, more than 44000 variables need to be monitored.

4.6.2 The Software of the DCS

The DCS software establishes the communication to the hardware, to support the operator required monitoring and control tools, and provides automatic safety procedures as well as easier operation of the detector for non-DCS experts. Additionally, detector operation requires good coordination between the DAQ and DCS actions. Data relevant to the offline analysis must be recorded and stored in the conditions database. The core of the DCS software is the Prozess- Visualisierungs- und SteuerungsSoftware (PVSS). [8] These projects run as a distributed system on eight control stations. Since each part of a distributed system has its own control and data managers (processes inside PVSS), an independent development and operation of the different projects is possible. The core of the control software is the Front-end Integration Tools (FIT), which establish the communication with various hardware components. For each hardware component, like the HV-PS, the LV-PS and the different devices using the ELMBs, dedicated FIT exist. Each FIT consists of an integration and a control part. The integration part initialises each given hardware component and creates the data structures required to control it. The control part of the FIT supervises the operation of the same component. The FITs are mainly used by a DCS expert who needs to check the behaviour of the hardware. For persons who run shifts, a detector-oriented view of the hardware is provided

[8] PVSS is made by ETM, Eisenstadt, Austria.

by the System Integration Tool (SIT). The mapping of read-out channels to the detector devices is done by the SIT. The SIT creates a virtual image of the detector inside the DCS. It combines all information which is relevant to the operation of the detector unit such as a half stave, a disk or even the full detector. Furthermore, the SIT is responsible for storing the data in the conditions database.

The control software used to operate on the detector is the Finite State Machine (FSM). This software was developed, in common, for the four largest LHC experiments [44]. The FSM uses geographical, organised data structures, created by the SIT, and provides the user with a set of commands to act on small or large fractions of the detector simultaneously. The detector status is returned by the FSM. Furthermore, proper settings and special power-on sequences are performed automatically by the FSM. The FSM also provides the link to the ATLAS-wide control system. As part of the overall ATLAS control system, the pixel FSM will receive commands from the ATLAS FSM during normal data taking. The communication between DAQ and DCS is provided by DAQ-DCS Communication (DDC), which provides command transfer from the DAQ system to DCS, publishes DCS values to the DAQ and vice versa. For the tuning of the optical links, the DDC is critical.

The DCS hardware and software system has been fully exercised in various configurations during the prototype and construction phases of the pixel detector, namely in test beams, with cosmic ray tests and during the integration of the pixel detector into ATLAS [45, 46].

5. Sensors

Sensors are the sensitive part of the pixel detector used for charged particle detection and function as a solid-state ionization chamber. The sensor must meet exacting geometrical constraints concerning thickness and granularity as well as have a high charge collection efficiency, while sustaining a massive amount of ionizing and non-ionizing particle radiation damage. On one hand, this is reflected in the selection of the bulk material and, on the other hand, it impacts the design of the pixel structure itself.

5.1 Design

The ATLAS pixel sensor is an array of bipolar diodes placed on a high resistivity n-type bulk close to the intrinsic charge concentration. The sensor is made by implanting high positive (p^+) and negative (n^+) dose regions on each side of a wafer. An asymmetric depletion region at the p^+-n junction operates in reverse bias and extends over the whole sensor bulk volume. Here, one is able to collect and detect charge carriers generated by ionizing particles passing through the active volume. The sensor design guarantees single pixel isolation, minimizes leakage current and makes the sensor testable as well as tolerant to radiation damage.

The pixel sensor consists of a $256 \pm 3\,\mu$m thick n-bulk. The bulk contains n^+ implants on the read-out side and the p-n junction on the back side. For each sensor tile, the 47232 pixel implants are arranged in 144 columns and 328 rows. In 128 columns (41984 or 88.9 %) pixels have implant sizes of $382.5 \times 30\,\mu\mathrm{m}^2$ with a pitch corresponding to $400 \times 50\,\mu\mathrm{m}^2$, and in 16 columns (5248 or 11.1 %) pixels have implant sizes of $582.5 \times 30\,\mu\mathrm{m}^2$ corresponding to a pitch of $600 \times 50\,\mu\mathrm{m}^2$. In each column eight pairs of pixel implants, located near the center lines, are ganged to a common read-out, resulting in 320 independent read-out rows or 46080 pixel read-out channels. This arrangement was chosen to allow for the connection of the sensor tile to 16 electronic front-end chips. Aside from increased leakage current, radiation damage will invert the sensor bulk and then gradually increase the depletion voltage. For unirradiated sensors, the depletion starts at the back (p) side, where the pixels are not isolated from each other until full depletion of the bulk. Irradiation of the bulk leads to a change in the effective doping concentration N_{eff}. First N_{eff} drops off and then runs through type inversion, after which N_{eff} increases [47]. At type inversion, the junction moves to the front (n) side, isolating the pixels and enabling operation even if the bulk cannot be fully depleted. Maximum achievable depletion is desirable to maximize the signal. The advantage of the depletion zone for the n^+-in-n design is shown in Fig. 15.

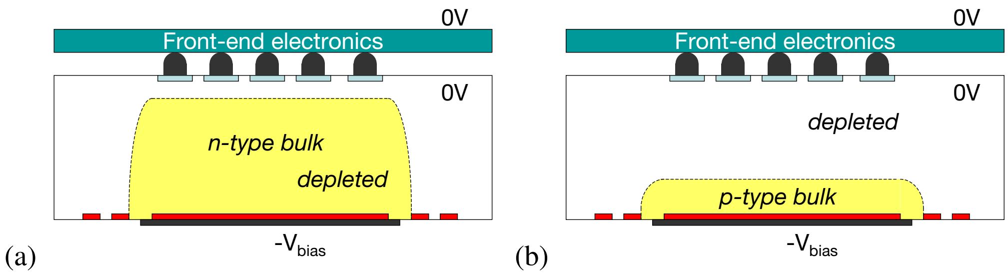
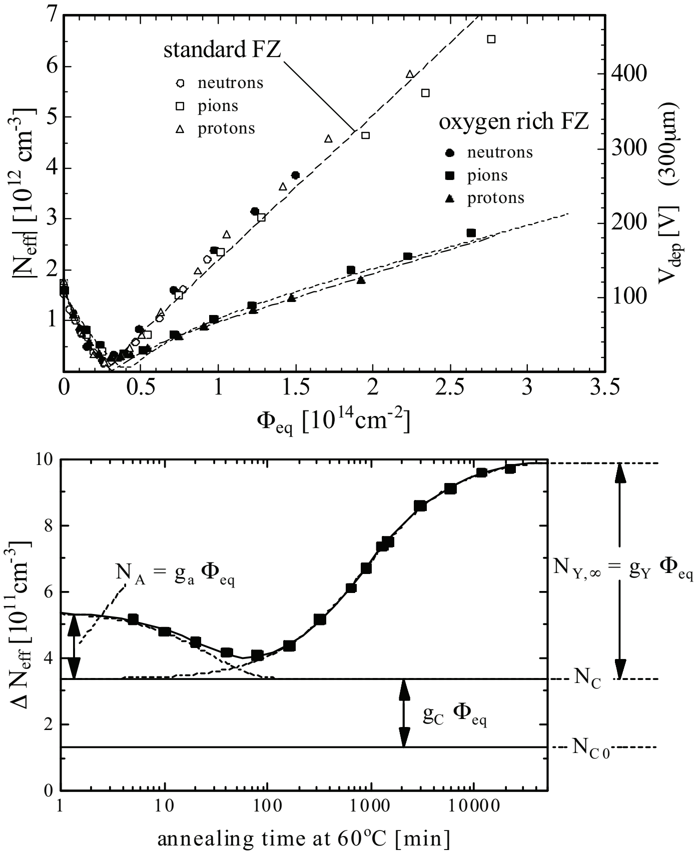


Figure 15. Comparison of depletion zones in n^+-in-n pixel sensors before (a) and after (b) type inversion. Before type inversion the electrical field grows from the backside and reaches the pixel implants (full depletion). After type inversion the depletion zone grows from the pixel side and allows operation even if the bulk is not fully depleted.

Oxygen impurities have been introduced in the bulk to increase tolerance of the silicon against bulk damage caused by charged hadrons [48,49]. A comparison of the evolution of charge densities in standard and oxygenated silicon during irradiation with hadrons is shown in Fig. 16a. In addition to the continuous irradiation of the sensors affecting the induced doping concentration, N_{eff} also evolves due to thermal effects. On short time scales, N_{eff} drops off (beneficial annealing), runs then through a minimum of constant damage and finally increases again on longer time scales (reverse annealing). See Fig. 16b.

While the beneficial annealing is not altered in oxygenated silicon, the constant radiation damage (N_{C}) is reduced, and the reverse annealing (N_{Y}, see Fig. 16b) is significantly slowed down [48, 49], producing a lower overall effective charge density in similarly irradiated samples undergoing identical annealing scenarios. Sensors built from such material exhibit deeper depletion zones at the same bias voltage and full depletion at a lower bias voltage.

By choosing an appropriate temperature profile (i.e. operation at 0°C, short periods of +20°C during detector access, and cooling down to −20°C during longer operational breaks in the experiment), one tries to keep sensors near the lowest possible N_{eff} and avoid reverse annealing, so as to derive benefit from the lowest possible depletion voltage. Model calculations (Fig. 17) of the combined effects of bulk irradiation and annealing have been performed [50]. The increase of the intrinsic charge carrier concentration due to radiation exposure leads to higher leakage currents and also contributes to noise. Cooling of the sensors to values well below room temperature helps reduce these effects.



(a)

(b)

Figure 16. (a) Evolution of effective charge densities and full depletion voltage in standard and oxygenated silicon during irradiation with various hadrons. In oxygenated silicon the increase after type inversion induced by charged particles (pions, protons) is significantly lower. (b) Evolution of the effective doping concentration due to annealing and reverse annealing effects. The parameterization of this evolution is the so-called "Hamburg model" and represents an important input to the ATLAS pixel sensors, which will operate near the point of minimal depletion voltages. In oxygenated silicon, both N_C and N_Y are reduced [48,49].

The positive and the negative implanted sensor wafer sides are both structured by mask processes for implantation, metalisation and deposition of silicon-oxide and silicon-nitride. This double-sided processing demands precise mask steps and incorporates front-to-back mask alignment of a few microns, which makes the manufacturing process demanding. However, this allows for a segmented n^+ implantation used for the definition of pixel cells and a guard ring structure on the p^+ implanted wafer side, locating the main voltage drop on the sensor surface opposite to the bump connections [51, 52]. The sensors can be fully depleted before type inversion with bias voltages below 100 V. After type inversion the depletion zone grows primarily from the segmented n^+ implant when the region of highest electric field in the bulk now converts to p-type.

On the sensor front side, pixel structures are arranged and isolated by moderated p-spray [52, 53] implants, which have proven to be radiation tolerant with respect to surface damages induced by ionising charged particles for doses up to 500 kGy in silicon. The principal layout is shown in

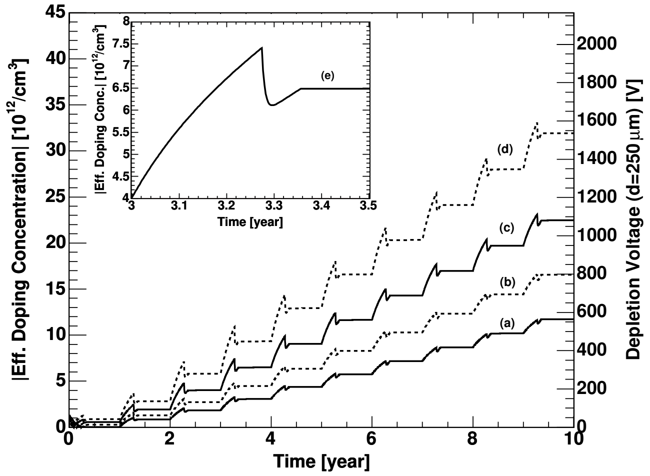


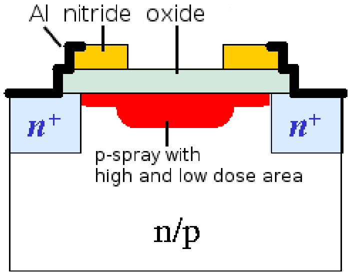
Figure 17. Change of the effective doping concentration (left scale) and the voltage necessary for full depletion (right scale) of oxygenated sensors according to irradiation and annealing effects under the Hamburg model for the two inner pixel detector layers in a standard (solid) and elevated (dashed) radiation scenario. (a) Layer 1 at 8.85 cm radial distance from interaction point with a standard fluence of $0.9 \times 10^{14}\,\mathrm{cm}^{-2}\mathrm{year}^{-1}$ (after the 3rd year of operation), (b) the same as (a) with a 50 % elevated fluence, (c) b-layer at 5.05 cm radial distance from the interaction point with a standard fluence of $2.4 \times 10^{14}\,\mathrm{cm}^{-2}\mathrm{year}^{-1}$, (d) the same as (c) with a 50 % elevated fluence. The enlarged detail (e) shows the evolution of the sensor characteristics during one year of assumed detector operation: 100 days of beam operation with irradiation at an operation temperature of 0°C, a period of about 30 days at +20°C during detector access, and cooling down to −20°C during the rest of the year.

Fig. 18a. The dose of implant ions leading to the moderated p-spray isolation is regulated with a help of a nitride layer, which is opened during an additional mask step, creating a deeper high dose p-spray region in the center of the inter-pixel gap and a shallower low dose layer everywhere else. This isolation technique avoids high field regions in the interface between the pixel isolation and the bulk and ensures radiation tolerance of the design [54, 55]

All 46080 read-out channels of a sensor tile are connected to a common bias grid structure [52] (Fig. 18b) by employing a punch-through connection technique to each channel. The method biases the entire sensor without requiring individual connections, but still ensures isolation between pixels. This bias grid has been used for quality assurance measurements before the read-out electronics are connected to the sensors. An opening for each pixel in the passivation layer of the sensor allows for a connection to each channel using a bump-bond technique (see section 6) to front-end electronics (see section 4), which is DC-coupled and provides biasing for each individual pixel.

5.2 Prototyping and Tests

Bulk and surface design features of the sensors have been extensively tested during the prototype phase [55] and a dedicated pixel sensor quality assurance plan was developed [57]. The sensor layout has been designed on four-inch-diameter, double-sided wafers, which include three sensor tiles of about 18 mm×62 mm each. During the prototype phase, dedicated test structures were

(a) 

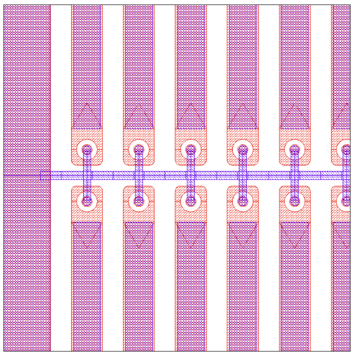
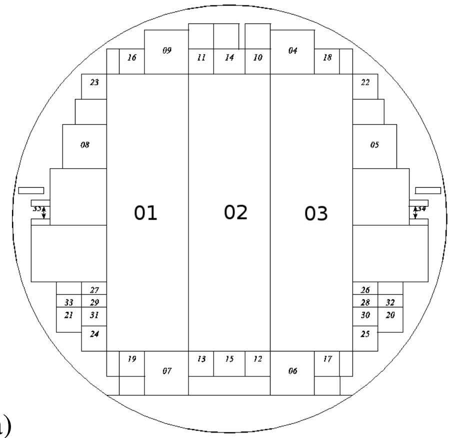
(b) 

Figure 18. (a) Principal layout of the moderated p-spray isolation which consist of high and low dose areas between the n^+ pixel implantations in the n bulk. Compared to other isolation profiles like p-stop [56] and p-spray [53] high field regions are avoided in the transition regions between pixel and bulk. (b) Layout detail of the bias grid [52] visible in the production mask for a pixel double row.

(a) 

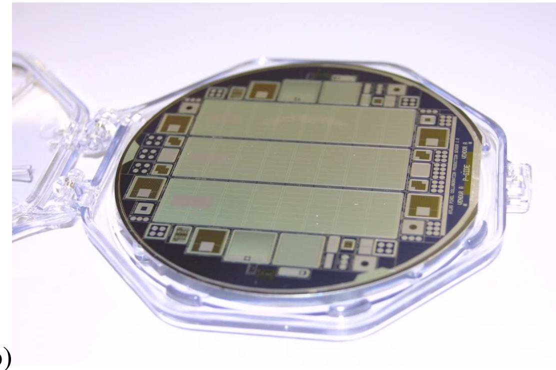
(b) 

Figure 19. (a) Geometrical layout of the sensor wafer. Central large structures 01, 02 and 03 are the sensor tiles carrying 46080 read-out channels employed in the ATLAS pixel sensor modules; structures 04 to 35 are dedicated test structures to monitor the quality of prototyping and production. (b) A photograph of a 4-inch diameter ATLAS pixel sensor wafer (p-side view).

developed. The test structures were placed on the ATLAS pixel sensor wafer surrounding the sensor tiles to allow for dedicated electrical tests of various design features for the sensor (Fig. 19).

The sensor quality control included mechanical as well as electrical inspections and tests. Examples of visual and mechanics tests include unique wafer identification with the help of scratched serial numbers, visual inspection of the surface quality, a check of the mask alignments, and planarity as well as thickness measurements of wafers. Electrical tests included measurement of the leakage current and the capacitance of diodes using the guard ring structure. Leakage currents were monitored on sensor tiles, and on test structures. Current and capacitance measurements were performed on oxide structures.

As an example of the bulk characteristics, the dark current on sensor tiles was monitored. The break down voltage was required to be well above 150 V. Fig. 20 shows an example of measure-

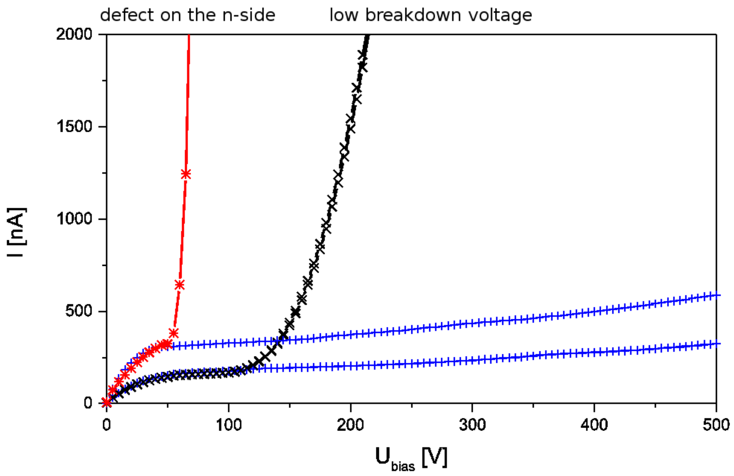
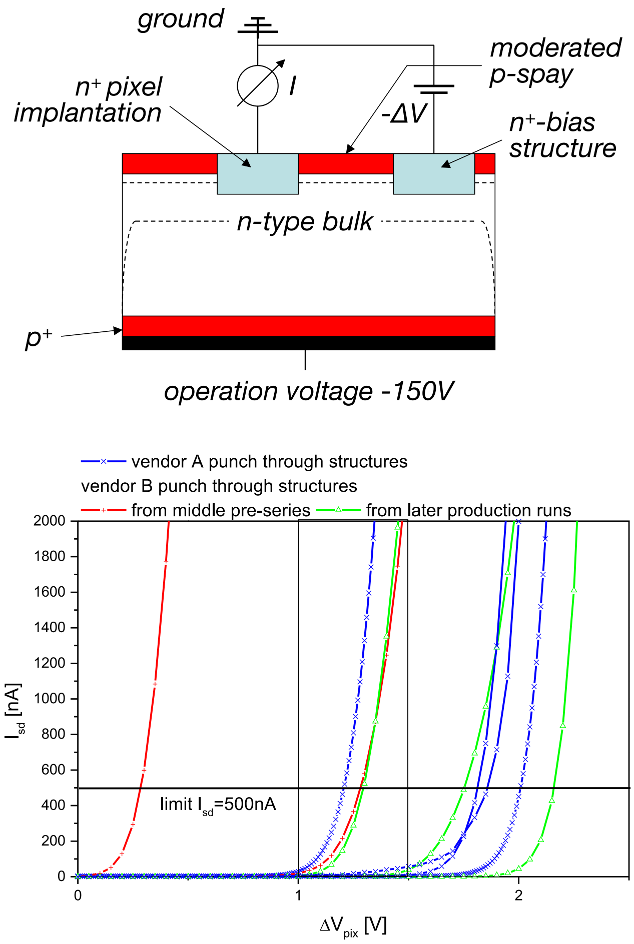


Figure 20. Examples of dark current vs. bias voltage curves on pre-series sensors tiles. While the two blue curves are examples of nearly perfect diodes, the black curve shows a break down between 150 and 200 V, and the red curve shows a very steep break down behaviour near the typical depletion voltage, indicated a defect on the n-side of the sensor.

ments performed during the prototype phase. The two blue curves are examples of nearly perfect diodes, the black curve shows a breakdown between 150 and 200 V and the red curve shows a very steep breakdown behaviour near the typical depletion voltage, indicating a defect on the n-side of the sensor.

Since the moderated p-spray dose is one of the critical steps in the sensor design, the measurement of the p-spray dose is an important quality control test. Here, a dedicated punch-through structure as well as an oxide structure is needed to determine the oxide capacitance. An example of a punch through measurement is shown in Fig. 21. The idea of this measurement is to determine the current I between an individual pixel and the bias grid (Fig. 21a) as a function of the potential difference ΔV, while the sensor bulk is biased at -150 V. The resulting current (Fig. 21b) increases for good isolations at $\Delta V > 1$ V. This together with the oxide measurement (not shown) leads to the p-spray dose [57]. This example demonstrates the need for advanced quality control measurements to assure the radiation hardness of production sensors. A few sensors were rejected during the production process.

One important aspect of the present ATLAS pixel sensor is the operation under irradiation, especially near the end of the sensor's lifetime. Here, the main limitation of the sensor is the trapping of charge carriers in the silicon bulk, which leads to decreasing values for the collected charge during the operation time of the detector. Trapping times have been determined in test beams [58], and laboratory set-ups [59]. Based on the operation model (see Fig. 17) of the ATLAS pixel sensor, the expected collected charge for minimum ionizing particles passing through the 250 μm thick bulk is predicted to be between 15 and 19 ke after irradiation fluxes of 8–12 $\times 10^{14}\,\text{cm}^{-2}$ [60]. These values are expected after 10 years of operations for sensors in Layer 1 of the ATLAS pixel detector. The values agree nicely with those derived from test beam results performed using production-like sensors [61]. Further performance features, including those for the sensors, were



(a)

(b)

Figure 21. (a) Electrical set-up to monitor the bias dot current vs. the potential difference test on a depleted substrate. (b) Example of punch-through current measurements on several prototype structures at the nominal bias voltage of 150 V. The left red curve is an example of a below specification low potential difference, which occurred during early prototyping, compared to later production, which fulfilled the isolation criteria of more than 1 V.

extracted under test beam conditions, the results of which are summarized in section 7.

5.3 Production and Quality Assurance

Sensor tiles have been produced by two independent vendors[9], who went through the prototype phase and qualification process. Based on the experience during prototype development, specialized quality assurance procedures were employed for the series production of sensors [62, 63] and were carried out as a collaborative effort at four different pixel sensor institutes. An extensive cross calibration of mechanical and electrical measurements was performed during these processes.

[9]CiS Institut fuer Mikrosensorik gGmbH Konrad-Zuse-Strasse 14, D-99099 Erfurt, Germany http://www.cismst.de and ON Semiconductor Czech Republic, a.s. 1. maje 2230, CZ-75661 Roznov pod Radhostem, Czech Republic http://www.onsemi.com

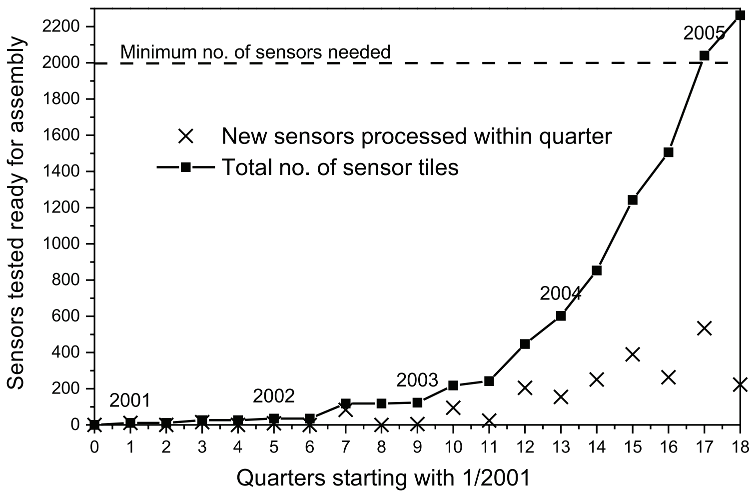


Figure 22. Tested sensor tile output in total and per quarter during the production process.

The production rate of ATLAS pixel sensors is shown in Fig. 22. More than 2200 sensors successfully passed through the quality assurance process and were available for hybridisation [64] to the front-end electronics.

6. Modules

6.1 Overview

The sensitive area of $\sim$1.7 m^2 of the ATLAS pixel detector is covered with 1744 identical modules with a small exception (see below). Each module has an active surface of $6.08 \times 1.64\,\text{cm}^2$. A module is assembled from the following parts:

- the sensor tile containing 47232 pixels as described in section 5;
- sixteen front end electronics chips (FE) each containing 2880 pixel cells with amplifying circuitry, connected to the sensor by means of fine-pitch bump bonding (see section 6.2);
- a fine-pitch, double-sided, flexible printed circuit (referred to as a flex-hybrid) with a thickness of about 100 μm to route signals and power;
- a module control chip (MCC) situated on the flex-hybrid;
- for the barrel modules, another flexible foil, called a pigtail, that provides the connection to electrical services via a microcable, whereas for the disk modules, the microcables were attached without the pigtail connection [4].

The concept of the ATLAS hybrid pixel module is illustrated in Fig. 23. Sixteen front-end chips are connected to the sensor by means of bump bonding and flip-chip technology. Each chip covers an area of $0.74 \times 1.09\,\text{cm}^2$ and has been thinned before the flip-chip process to $195 \pm 10\,\mu$m thickness by wafer-back-side grinding. A sizeable fraction ($\approx$25%) of the front-end chip is

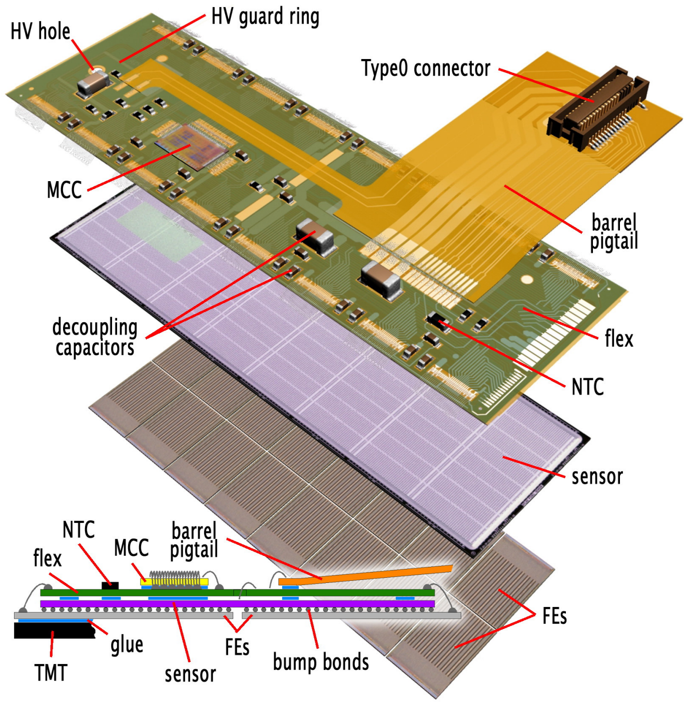


Figure 23. The elements of a pixel barrel module. Most of the thermal management tile (TMT) on to which the module is glued is suppressed.

dedicated to the End-of-Column (EoC) logic. Once bonded, most of the EoC logic extends beyond the sensor area. Wire bonding pads at the output of the EoC logic are thus accessible to connect each front-end chip to the flex-hybrid by means of aluminum-wire wedge bonding. Copper traces on the flex-hybrid route the signals to the MCC. The MCC receives and transmits digital data out of the modules. The flex-hybrid is also used to distribute decoupled, low-voltages to all the chips. The traces are dimensioned such that the voltage drop variation is limited to ≈50 mV in order to keep all the chips in the same operating range. The back-side of the flex-hybrid must be pinhole free, since it is glued to the high-voltage side of the sensor. A multiple solder mask layer was, therefore, used and all parts were tested up to 1000 V. Since all module components must withstand the lifetime radiation dose, polyimide was used as the base materials for the flex-hybrid with adhesiveless metalisation. Passive components are added to the flex-hybrid for decoupling and filtering of the front-end chips. The module temperature is remotely monitored via a Negative Temperature Coefficient (NTC) thermistor loaded on the kapton circuit, and a fast interlock powers off a module when overheating occurs.

After a lifetime radiation dose, a module is expected to draw 1.3 A at 1.7 V from the analog supply and 0.9 A at 2.1 V from the digital supply. This includes the voltage drops from the pigtail (for barrel modules) and the flex-hybrid, but not the voltage drop from the microcables. In addition, the sensor bias draws 1 mA at 600 V, giving a total power of about 4.7 W. However, it is possible that the analog or digital supply voltages may need to be increased in order to recover performance, which could result in a total power of up to about 6 W.

The bump bonding and flip-chip operation results in a so-called bare module. The sixteen chips of an assembled bare module are first tested on a probe station to detect defects. Rework on modules can still be done at this point of the assembly sequence.

Region in between Chips

The sensor pixels have dimensions of 50 μm$\times$400 μm, with the exception of about 11% which have a size of 50 μm$\times$600 μm, to allow for a contiguous sensitive area between chip boundaries in the long pixel direction. In the other direction, 2 x 4 pixels under each of the two adjacent chips cannot be covered by active pixel circuitry. These special pixels are ganged through metal lines on the sensor, with one of 4 + 4 neighboring electronics pixels at the top of the columns, as is illustrated in Fig. 24. The resulting hit ambiguity is resolved by off-line pattern recognition software. There are five pixel types with decreased performance due to added input-capacitance and ambiguities (see section 6.6). These special pixels are: long (10.6%), ganged (2.2%), inter-ganged (1.6%), long-ganged (0.3%) and long inter-ganged (0.2%).

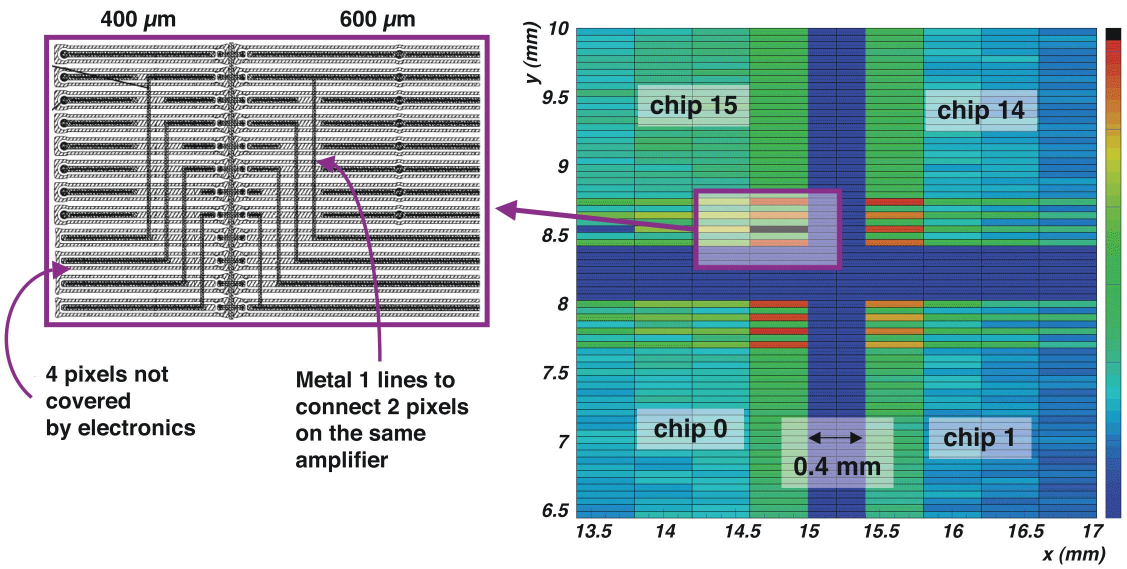


Figure 24. End-region of the pixel detector at the edge of four FE-chips. The area of the sensor covered by the chip edges is marked in grey. The pixels in between the chips (white rectangles) are connected through metal lines to another pixel underneath the chips.

6.2 Bump Bonding

Bump bonding is extensively used in the electronics industry for the attachment of integrated circuit die to printed circuit boards or other substrates. Two different bump bonding techniques have been used for ATLAS: electroplated-solder (PbSn) bumping [65–67] and evaporative-indium bumping [68]. Both bump deposition processes are done at the wafer level. The principle of a bumped sensor – electronics pixel element is sketched in Fig. 25. The substantial demands on the handling require that the wafers be bumped with their original thickness ($\sim$ 700 μm for the FE-I3

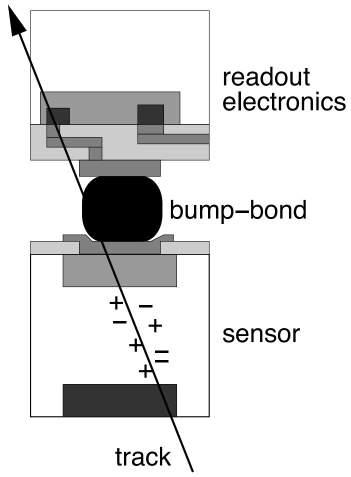


Figure 25. Sketch (not to scale) of the cross section of a hybrid pixel detector, showing one connection between a sensor and an electronics pixel cell. A particle track releases ionisation in the sensor volume.

wafers). Wafer thinning is done after bump deposition by covering the bumps with a photoresist layer and a UV releasing tape for bump protection and for handling. The integrated circuit wafers are then thinned by backside grinding to about 195 μm. They are diced immediately afterwards and then the die are tested again on a probe station to assure that they are still functional and ready for the flip-chip process. The dicing was performed before thinning by making 250 μm deep cuts in the 700 μm thick wafers. Separation of the chips occurs by the end of the back-grinding operation (so-called dicing-before-grinding). This was done to obtain high-quality diced edges.

6.2.1 The Solder Bumping and Bonding Process

In eutectic PbSn solder bumping [65–67], the solder is deposited through electroplating. Under bump metalisation (UBM), which consists of several metal layers, is deposited on the contact pads. A PbSn cylinder is galvanically grown and melted to a sphere on the integrated circuit wafer (see Fig. 26a), while the sensor wafer receives only the UBM [66, 69]. The parts are mated by flip-chip assembly with reflow, which provides self-alignment. The process flow is described in [70]. The distance between a chip and the sensor is about 20 – 25 μm, thus minimizing the cross-talk between the electronics and the sensor. The connection resistance is smaller than 1 Ω, and the ultimate shear stress is $\approx$50 MPa. A picture of PbSn bumps after reflow on an ATLAS FE-chip is shown in Fig. 26b.

6.2.2 The Indium Bump Bonding Process

In the case of indium bonding, the bumps are grown by depositing evaporated indium on both mating parts [71]. No under bump metalisation is needed. The bump pitch is also 50 μm, but the bump height is limited to 10 μm due to the use of a lift-off process for the removal of the polyimide evaporation mask. Mating is obtained by In-In thermocompression. The process flow is described in [70]. Fig. 27 shows a micrograph of 50 μm pitch indium bumps deposited on two

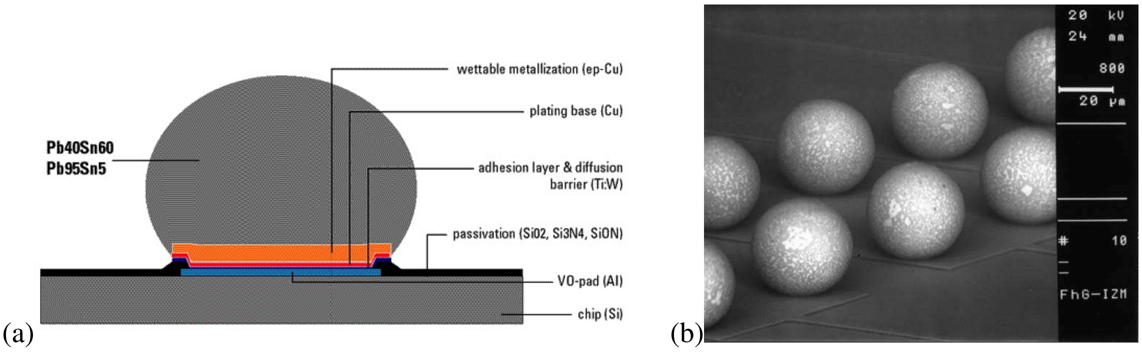


Figure 26. (a) Schematic description of a eutectic PbSn solder bump [65–67] and (b) rows of a PbSn bumps (courtesy IZM-Berlin).

glass samples and then flip-chipped together [68] at a temperature of $\sim$100°C applying a pressure of about 20 N/cm^2 per chip. The distance between chip and sensor after bonding is $\approx$10 μm.

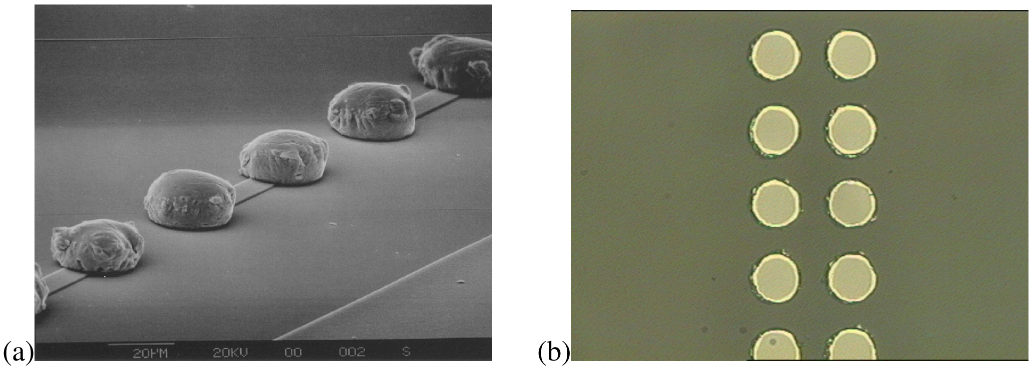


Figure 27. Micrograph of a Indium bump deposition on silicon at 50 μm pitch (a) and of a flip-chip assembly of two 50 μm pitch bump arrays (b) on glass substrates (courtesy SELEX Sistemi Integrati, Rome) [68].

6.3 Quality Control of Bump Bonded Assemblies

Inspections before and after flip-chip assembly were crucial to obtain the highest yield for functional pixel modules. Automated inspection of bumped wafers with the combined use of a video camera and laser interferometry allowed the manufacturer to find missing bumps, merged bumps, deformed bumps or other defects as well as to measure bump heights on wafers. Inspection with high resolution (2 μm) X-ray machines allowed one to detect misalignment or merged/bridged bumps previously not detected or caused by the flip-chip process. Both solder (about 45%) and indium (about 55%) bump bonding have been used to produce pixel modules with bump defect rates of $\approx 10^{-5}$–10^{-4} at the wafer level and $\approx 10^{-4}$–10^{-3} after the flip-chip process.

6.4 Reworking of Bump Bonded Assemblies

All modules were built with known good die (KGD) i.e. all die were tested prior to flip-chip and only the good ones were used. This is a crucial requirement as the module yield goes with the n^{th}

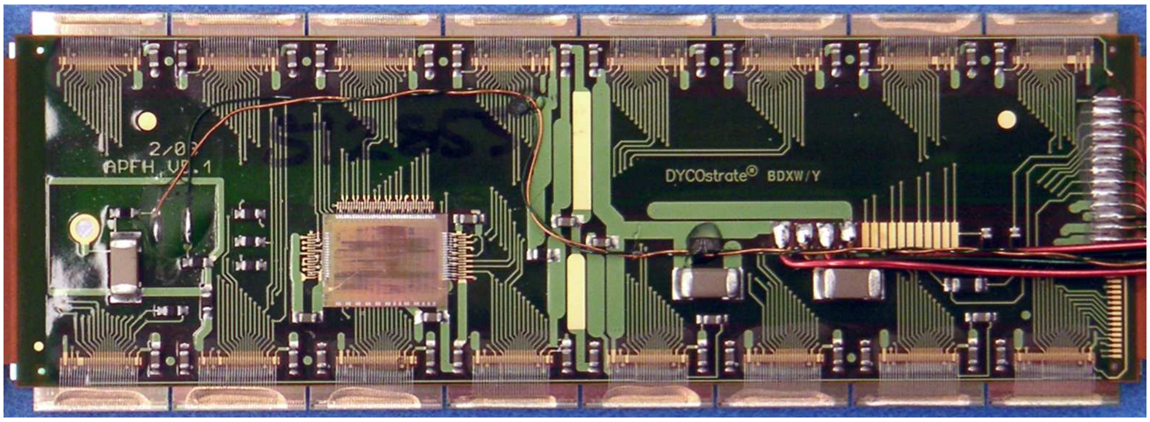


Figure 28. Picture of an ATLAS pixel disk module.

power of the electronics chip yield, n being the number of chips-per-module.

All front-end chips were also electrically tested after bump bonding in order to check for damage to the front-end electronics and to assess if the quality of the electrical contact was adequate.

Both solder and indium bump bonded modules have been successfully reworked [69,72] with a success probability of more than 95%. In both cases, the operation required heating and application of a force to remove the integrated circuit, while leaving some metal on the bond pads. Afterwards, a new IC is flipped to the sensor. The probability of properly connecting all pixels during a second flipping is near 100%.

6.5 Module assembly

Once a bare module passed the acceptance test, it could be equipped with a flex-hybrid to provide the connections between the Module Controller Chip and the front-end electronics and from the Module Controller Chip to a microcable. A photograph of a disk module is shown in Fig. 28.

The flex-hybrid is a double-sided, flexible printed circuit with a 50 μm substrate thickness and 25 μm thick copper lines[10]. It has been specifically designed to withstand the maximum 600 V depletion voltage applied to the sensor. It also includes passive components for local decoupling and an NTC for monitoring the module temperature.

To facilitate testing of flex-hybrids, they were attached to custom-made printed circuit boards (flex support card or FSC), which were used for handling the flex-hybrids themselves and for handling after attaching the flex-hybrid to a module. A module is cut out from the FSC just prior to loading on a local mechanical support [4].

Flex-hybrids for barrel and disk modules are identical. A difference appears only when the connection to the services is made. For barrel modules, an additional flex circuit (pigtail) is glued on top of the flex-hybrid and electrically connected by wire bonding. It has a 30-pin surface mount connector that was fixed to the backside of the barrel-region local mechanical support (stave) and used for attachment of the low-mass microcables. Disk modules, on the other hand, have the microcable soldered directly to the flex-hybrid [4].

[10]Manufactured by Dyconex AG Bassersdorf, Switzerland.

There is a significant difference in the coefficient of thermal expansion between kapton and silicon. The glue used for attachment of the flex- hybrid to the bare modules needed to be distributed to avoid any excessive mechanical coupling between the two. On the other hand, a strong connection is required in the places where wire bonds are needed. Therefore, a strip of silicone adhesive was deposited along the pads lines used for the interconnection between the flex-hybrids and the front-end electronics, below the MCC, near the high voltage bonding pad and, for barrel modules, below the pigtail attachment point.

6.6 Testing and Selection Procedures

After loading on a FSC, a module can be connected to a test setup using cables. The test setup in the laboratory used LVDS signals. The readout chain and control software was the same as that used for the front-end electronics and bare module testing, except now configured to communicate via the MCC and using the microcable instead of probe needles for communication with the integrated circuits.

A characterisation procedure [73,74] was used to certify if a module was acceptable for operation, both electrically and mechanically. A ranking value was determined such that better modules could be selected for the most critical parts of the detector. Different weights were assigned to the number of missing or short bumps, the minimum digital voltage required for error-free operation, sensor bias current, number of reworked wire bonds and other parameters. In particular, a module had to satisfy the following conditions:

- the electronics should be tunable and have enough operation range to guarantee that there be tuning capability to operate successfully even after radiation damage up to the lifetime dose;
- the bump bonding had not been damaged by the assembly procedure;
- the wire bonding of MCC and FE produced test bonds exceeding a minimum pull force (every module had a number of spare wire bond locations that were pull tested).

The testing sequence proceeds as follows:

- a basic series of electronics tests is performed at room temperature after module assembly;
- modules undergo a mechanical stress test, being cycled 10 times between room temperature and -30 °C, with a cycle length of about 2 hours;
- electronics tests at room temperature are repeated after thermal cycling and compared to the initial tests;
- a complete module characterization is performed at approximately -10 °C, which is the expected operating temperature.

The last test was the most relevant for the definition of module quality and selection. Reduced electronics test were also performed after loading modules onto the local supports. This was done to monitor for possible damage after loading, which could trigger the repair or replacement of a module.

The room temperature tests consisted of:

1. a basic functionality test: the module was configured, the readout chain tested by digital injection and the amplifier cells by analog injection;
2. a test of module tunability: thresholds are equalized to about 4000 e;
3. a threshold scan without depletion voltage applied to the sensor.

The first test was mainly a check of the wire bonding or for electrostatic discharge damage to the electronics. In the second test, pixels can usually be tuned to the target threshold with a dispersion of 60 e, and a noise which ranges between 120 e for standard pixels to 300 e for long and ganged pixels (see Fig. 29).

The second and third tests were also sensitive to bump bonding properties. Pixels that failed the tuning usually corresponded to a cluster of merged bumps. In this case, several cell amplifiers were shorted together, resulting in reduced sensitivity to the injected pulse. In the case of an undepleted sensor, normal pixels are affected by the large parasitic capacitance of the sensor, but pixels not connected to the detector stand out because the noise level remains low, independent of the bias voltage applied to the sensor side. An example of a module with such defects is shown in Fig. 30.

The testing of modules before and after the thermal cycles was also important. A systematic problem in the encapsulation of wire bonds on the MCC was found, which resulted in unreliable wire bonds. Correcting this problem required that a number of modules be reworked, and this carried a ranking penalty. The comparison of bump damage between the initial assembly and after thermal cycling, allowed one to disentangle damage due to bad handling during the assembly, and damage due to weak bump bonds, for which there is a steady increase of disconnected bumps over time. The full characterisation at the nominal operational temperature of -10 °C included additional checks of tunability and operational range:

- the MCC operation was checked between 1.6 and 2.5 V, showing a typical turn-on at 1.8 V;
- front-end IC operation was tested within wide ranges of analog and digital low voltage supply values (VDDA in the range 1.5-2.0 V, VDDD in the range 1.9-2.3 V);
- The amplifier feedback current was tuned so that the average ToT response to a minimum ionising particle corresponded to 30 clock cycles. With the LVL1 trigger latency expected during operation, this setting provided 99.5% efficiency in a test beam (see section 7);
- Timing measurements have been performed to check the timewalk performance of the FE electronics when attached to the sensor. The overdrive needed to assign a signal to the correct beam crossing is about 1000 e;
- A measurement with the 60 keV x-ray from an ^{241}Am source checked the sensors's response (see Fig. 30).

The source measurement was particularly relevant in assessing module quality, since it is very sensitive to noisy channels. The duration of the measurement wass chosen to reach an expected occupancy of at least 10 hits for every pixel channel. Therefore, it was also effective in finding

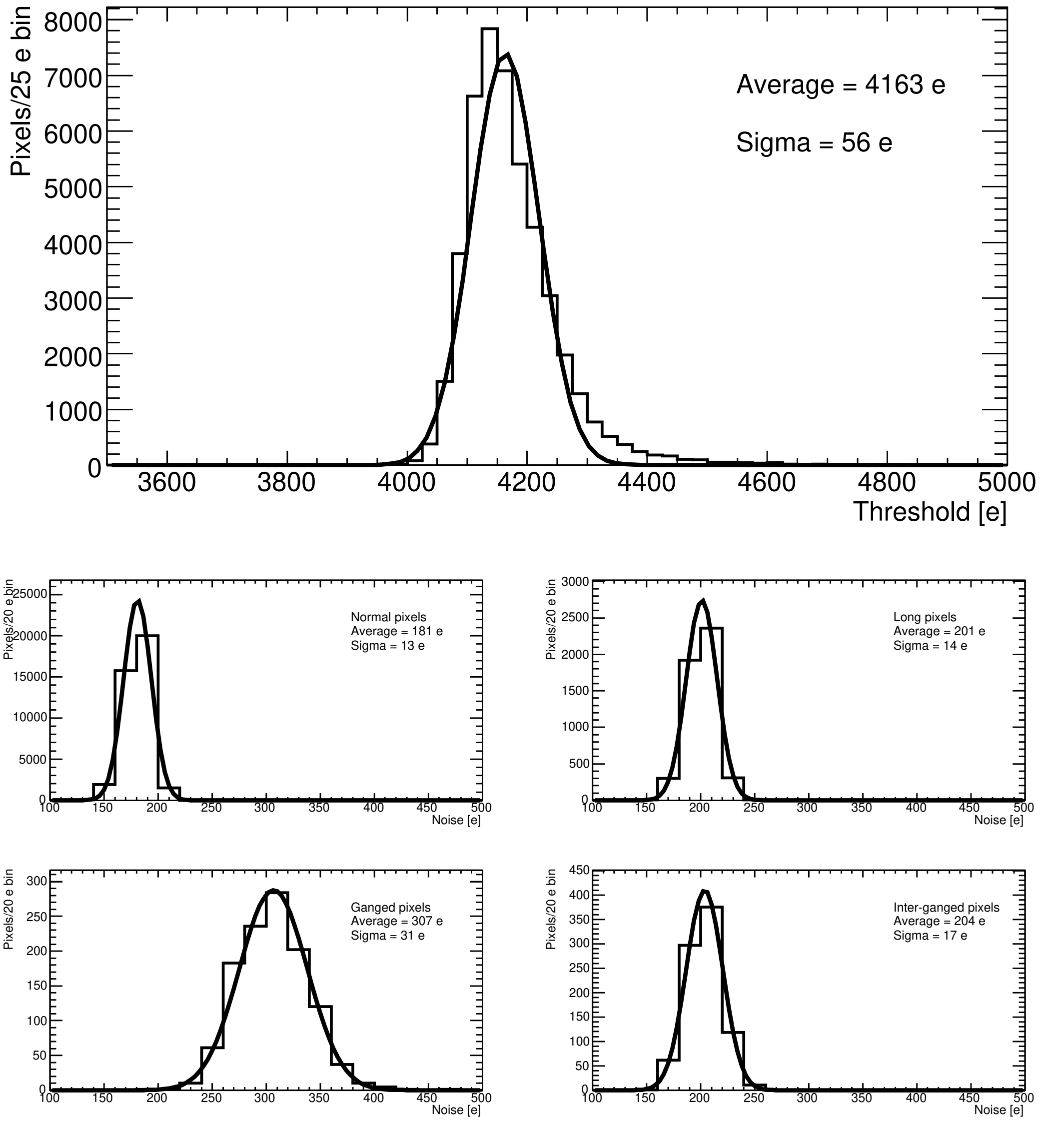


Figure 29. Threshold (top) and four noise (bottom) distributions - for different locations and types/sizes of pixels - of a typical module (normal, long, ganged, inter-ganged).

inefficient cells, coming from merged or disconnected bumps. The execution of the testing and selection procedure was time consuming. The assembly of a module and its subsequent characterization took a total of about seven days. Therefore the module assembly and testing capability was replicated at six production sites. Sets of four or eight modules were generally processed in parallel at each site.

Modules were ranked using a single value, calculated from the test results. Different weights were assigned to test measurements with the number of dead channels from the source test carrying unit weight. The information combined in the overall ranking value included:

- number of bad channels, including source scan results, digital tests and other analog measurements;
- a χ^2-like term, describing how the analog performance of a module differs from the average;
- penalties for anomalous values of the leakage current or module bowing, which could give problems during operation;
- any repair operations performed, including the number of reworked wire bonds.

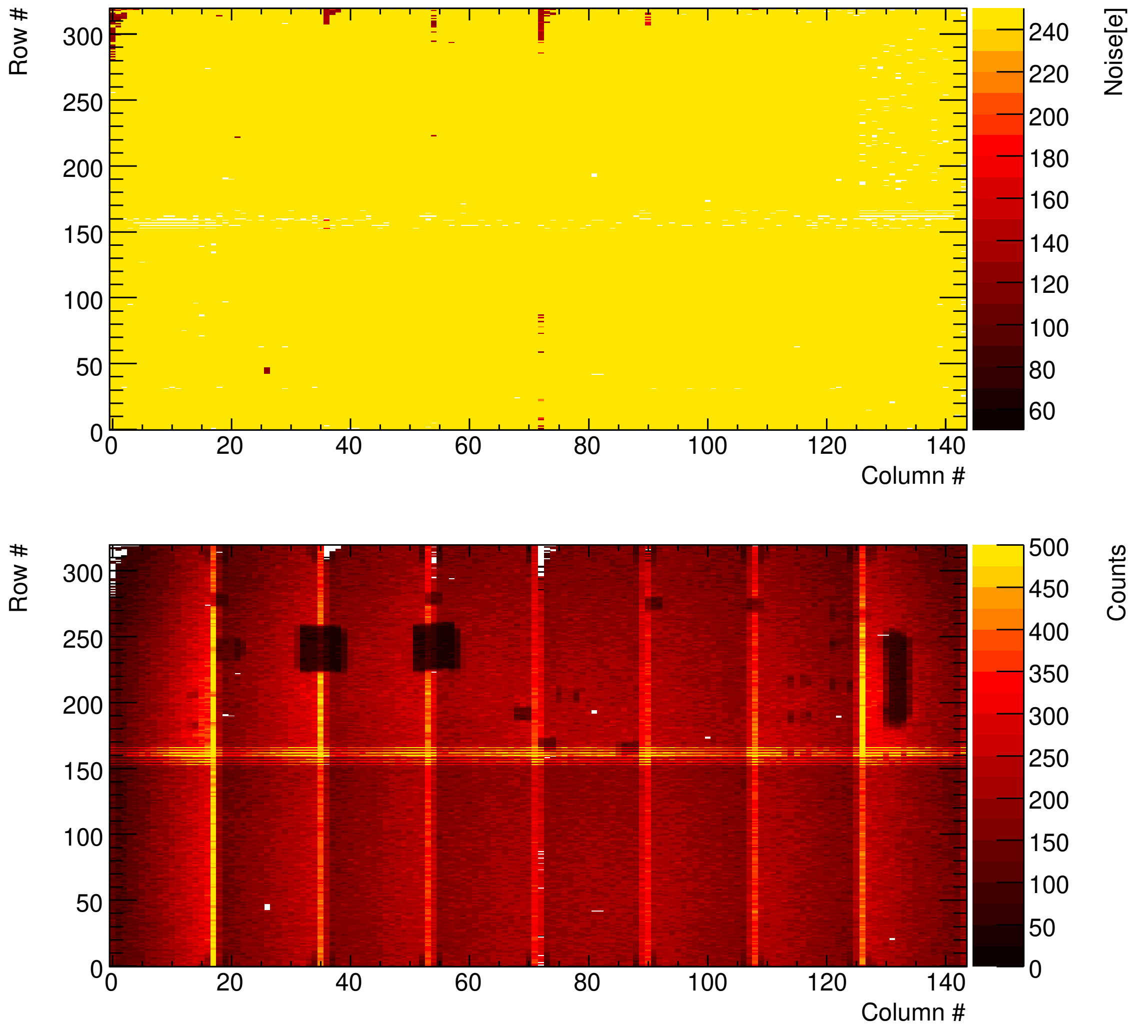


Figure 30. Noise distribution for an indium-bumped module without sensor bias (top). Disconnected regions are visible as low noise spots. For comparison (bottom) is a hitmap obtained with an ^{241}Am source. The very dark rectangles correspond to capacitors or other components that shield the sensor from the source.

This ranking value was used for module selection for mounting on local supports. The distribution of the ranking values is displayed in Fig. 31. The excess around 300 corresponds to the set of

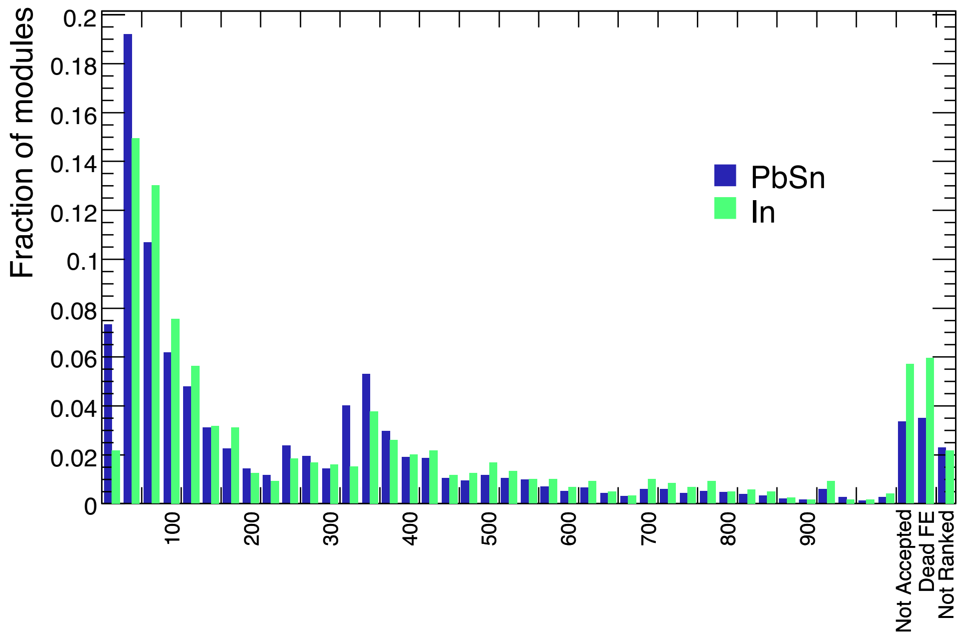


Figure 31. Module ranking distribution as described in the text.

modules that needed a full rebonding of the MCC, because of the encapsulation problem mentioned above. The b-layer has been built using modules with ranking values lower than 60, corresponding to a channel inefficiency better than 0.13%. Modules with ranking values higher than 1000 were not accepted for assembly.

Analysis of the ranking showed an overall equivalence for all the assembly sites, while pointing out a clear difference between the two bump vendors. The main reason for the difference is the higher number of disconnected bumps in the In-bumped modules. As stated before, a clustered set of disconnected bumps may be the seed for a widening of a disconnected region. Because of this, a ranking penalty was added for each FE chip containing more than 30 disconnected bumps. In hindsight this penalty has been found to be quite conservative, but it is the main reason for the tails in Fig. 31.

During the final phase of module production, when it was clear that there were a sufficient number of spare bare modules, only the ones with clusters of less than four disconnected bumps were selected for module assembly, resulting in an improvement of the ranking for modules mounted on local supports.

6.7 Production Yield

The production yield of bare modules is summarized in Table 6. Most losses were due to sensor damage, bad bumping and front-end IC damage.

Sensor damage usually is detected by an early breakdown voltage in the sensor tiles previously passing the sensor quality cuts. This loss rate was similar for both bump vendors and resulted in about 3% of the modules being rejected.

	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted (total)	1296	88.3%	1122	97.0%	2418	92.1%
Accepted as delivered	1101	75.0%	1035	89.5%	2136	81.4%
Accepted after reworking	195	13.3%	87	7.5%	282	10.7%

Table 6. Bare module production yields.

Bad bump bonding and FE damage were repairable according to the reworking procedures outlined previously. The failure rate and the possibility of reworking differed between the two bump vendors. In the case of bump problems, the solder-bump vendor often performed internal reworking after the in-house X-ray inspection, reprocessing the bumps. For indium bumps, there was no possibility to reprocess the bump deposition. In this case, if the damage was too widespread, the module was not submitted for reworking. This resulted in an overall higher failure rate for indium bumping.

FE damage was due to silicon shards trapped between the sensor and the FE chips. During flip-chip, the shards break the surface of the FE chips, resulting in shorts between the metal layers. The problem was more severe for indium-bumps, given the smaller bump height. Replacement of the FE chip usually resolved the problem, but manually removing the shards from the detector surface was required in order to attain a good rework efficiency. The production yield of assembled modules is summarized in Table 7.

Modules were also rejected due to mechanical damage observed after the assembly procedure, either induced by handling or because of weakness in parts that passed previous quality control steps.

Modules containing one or more FE which could not be operated were also discarded from the production path. A loss of about 1% was due to defects in the path from the MCC to the FE through the flex-hybrid. For In-bumped modules, the additional yield loss is due to shorts on the FE, similar to the behavior observed on bare modules. These defects were concentrated on reworked modules and modules that underwent multiple shipments. They can be assumed to be the same defect of shards as seen on bare modules, which is not present after the initial bonding, but is finally produced by the additional mechanical stress during module assembly. The difference in the ranking distribution between the Indium and solder bump modules is mainly due to regions of disconnected bumps, discussed in section 6.6. Overall the yield for module production exceeded the target, which was initially 90%, for each step in the bare module assembly, and subsequently for the full module assembly and characterisation.

7. Test Beam Studies

The performance of the pixel detector modules has been measured systematically in beam tests throughout their development. Initially, sensor properties were studied with single chip assemblies,

	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1190		1122		2312	
Accepted	1025	86.1%	1075	95.8%	2100	90.8%
b-layer quality	281	23.6%	445	39.7%	726	31.4%
not b-layer quality	744	62.5%	630	56.1%	1374	59.4%
Not accepted	165	13.9%	47	4.2%	212	9.2%
Ranking > 1000	68	5.7%	10	0.9%	78	3.4%
at least one dead FE	71	6.0%	10	0.9%	81	3.5%
testing not completed	26	2.2%	27	2.4%	53	2.3%

Table 7. Assembled module production yields.

namely reduced size sensors, which were read out by a single front-end chip. Later, full pixel modules were analysed in test beams. Results from test beams can be found in [55, 61, 75–84]. In this section we summarise beam measurements performed using the ATLAS pixel modules during the final stages of development and qualification.

7.1 The Test Beam Setup

Test beam measurements were performed at the H8 beamline of the Super Proton Synchrotron (SPS) at CERN, using a beam of 180 GeV charged pions. A beam telescope [85] was used to track beam particles independently of the devices under test. The telescope consisted of four planes of double-sided silicon strip detectors, with perpendicular strips at 50 μm pitch, that provided a reference track with an extrapolation uncertainty of about 6 μm. Pixel assemblies under test were placed between the second and third strip planes. Irradiated modules were inserted into a thermally insulated box, which maintained a temperature of about -7°C, as foreseen in ATLAS.

A trigger was provided by the coincidence of three fast scintillators. For each event, a TDC measured the difference in time between the particle passage and the edge of a 40 MHz clock, seen by the pixel electronics. For each trigger, data from eight consecutive cycles were read out in order to study the pixel signal behaviour in a 200 ns window.

For a fraction of the data taking, a high intensity beam was provided by the CERN SPS in order to study the efficiency of the readout architecture when the particle rate was comparable to that expected for the b-layer at the design luminosity of the LHC, namely 10^{34} cm^{-2}s^{-1}. At the beam center, the flux reached approximately 10^8 particles/cm^2/s. At this particle flux, both the scintillator system and the microstrip telescope were inoperable. Data were, instead, collected with a random trigger, and particle trajectories were reconstructed using four pixel modules.

7.2 Irradiation of Tested Assemblies

A major design requirement for the pixel detector is its radiation tolerance during the lifetime of the experiment at the LHC. Single chip assemblies and modules were systematically irradiated before operation in the test beam with 24 GeV/c protons at the CERN Proton Synchrotron (PS) proton irradiation facility. The proton fluence was 2×10^{15}cm^{-2}, corresponding to a 1 MeV neutron equivalent fluence of 1×10^{15} $n_{eq}cm^{-2}$and a dose of about 500 kGy. This corresponds to the expected dose resulting from five years of LHC operation with a 10^{34} $cm^{-2}s^{-1}$ luminosity at the b-layer position. Throughout the irradiation, subsequent storage and test-beam operation, the modules were kept at about -7 ^{0}C. Unless otherwise specified, the irradiated modules were operated at 600 V in the test beam, while the unirradiated ones were operated at 150 V.

7.3 Event Reconstruction and Analysis

Tracks were reconstructed using information from the telescope microstrip detectors only (except during the high rate tests), in order to have an unbiased extrapolation of the tracks through the pixel detectors under test. Events were selected [86] with one and only one track reconstructed by the silicon microstrip telescope. Tracks were required to extrapolate to a fiducial region inside the pixel sensors (at least 40 μm from the edges of the detector). In addition, only events with a χ^2 probability of the track fit greater than 0.02 were kept. For each event selected, the intersection of the trajectory of the beam particle with the pixel detector was calculated.

Neighboring pixel cell hits were clustered together. The mean cluster size ranged from 1 to 3.5 pixels for unirradiated sensors and from 1 to 2 pixels for sensors irradiated to 1. 10^{15} $n_{eq}cm^{-2}$, depending on the angle incidence of a track. [75] The bunch crossing identifier of the earliest pixel hit in the cluster was assigned to the whole cluster. The cluster position was typically reconstructed as the geometric mean position of the pixel cell centres. However, for the measurement of spatial resolution, the cluster position was reconstructed with a charge interpolation algorithm.

7.4 Measurements of Detection Efficiency

The efficiency was computed by requiring a pixel cluster near the intersection of the trajectory of the beam particle with the pixel detector and in the expected bunch crossing. The width of the window used to associate a cluster to a track was ± 0.2 mm along the short pixel side direction and ± 0.4 mm along the long pixel side direction.

The efficiency was computed as a function of the time $t = t_0 + n \times 25$ ns, where t_0 is the TDC phase between the trigger and the edge of the clock operating the modules, and n is the bunch crossing ID of the cluster. Efficiency curves at perpendicular beam incidence are shown in Fig. 32a for an unirradiated module and in Fig. 32b for a module irradiated to 10^{15} $n_{eq}cm^{-2}$.

At the LHC, only hits with a time stamp associated with a level 1 trigger are readout, i.e. only hits for which the leading edge rises in the 25 ns window corresponding to the clock cycle associated with the trigger are recorded. The position of this window can be tuned by setting the delay of the clock edge with respect to the bunch crossing time. The timewalk, i.e. the delay between the particle crossing and the leading edge of the signal passing the discriminator threshold, results in a spread in the time when hits are generated. It is, therefore, important to find the delay of the clock edge that maximises the number of hits collected within one clock cycle. Moreover, the performance should be stable for small variations in this delay, and a plateau in the relationship between efficency and time delay is required.

A good detector should have a high efficiency over a large range of clock phases. For the unirradiated detector of Fig. 32a, the plateau efficiency was 99.90%, and this value was maintained for about 14 ns (plateau width). For the irradiated detector of Fig. 32b, the efficiency decreased

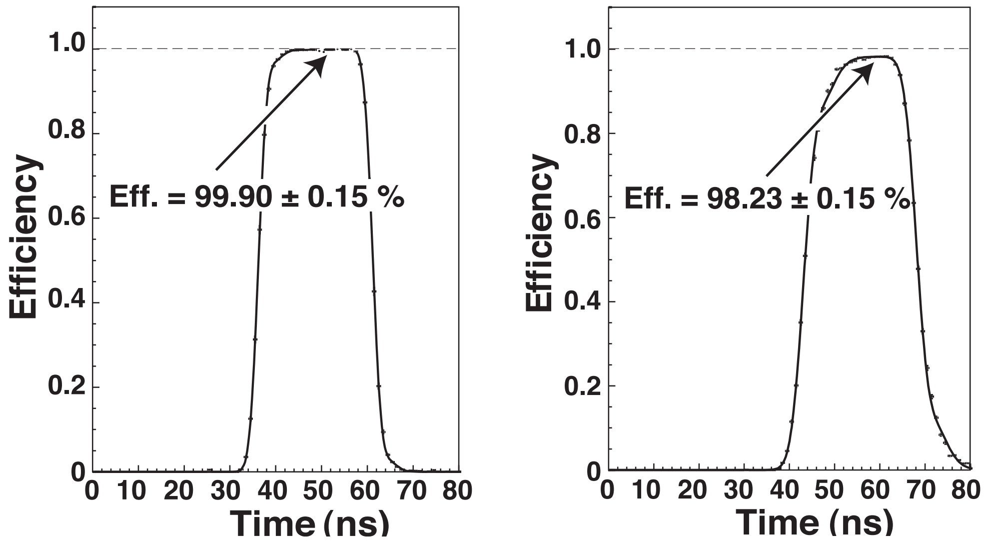


Figure 32. (Left) Detection efficiency at perpendicular beam incidence as a function of particle arrival time for an unirradiated module and (Right) for a module irradiated to 10^{15} $n_{eq}cm^{-2}$.

to 98.23% but was still well above the ATLAS pixel module specification ($\geq$ 97%). The timing characteristics were affected by irradiation, resulting in slower rising and falling edges, leading to a narrower efficiency plateau. However, the rise time was only slightly degraded by irradiation and a large plateau was still obtained, with a width of about 9 ns.

A summary of measurements performed on several pixel production modules is given in Table 8, for data collected at normal incidence. The detection efficiency was 99.9% for an unirradiated module, while for the irradiated modules it varied from a minimum of 96.4% to a maximum of 98.4%, with an average and r.m.s of 97.8% and 0.7%, respectively. All irradiated modules had similar timing constants. The width of the efficiency plateau for the irradiated detectors was (9.7 ± 1.1) ns. No statistically significant difference was observed between the two sensor producers or the two bump-bonding techniques.

For each module, the efficiency losses were reported separately when due to missing hits (0-hits) or due to timing losses (i.e. out-of-time hits, primarily recorded in subsequent bunch crossings). Two thirds of the efficiency losses, (1.5 $\pm$0.4)%, were typically in the 0-hits class and the remaining (0.7$\pm$0.3)% fell into the timing loss class. Missing hits were caused by various effects: pixels not giving a signal (due to detached bumps), noisy pixels masked at the readout (see below) and pixels collecting a signal lower than the threshold. This last cause of efficiency loss as well as timing losses in irradiated detectors were related to regions of poor charge collection located near the bias grid described in section 5 [55].

7.4.1 Noise

Noisy pixels, identified prior to the test beam, were masked in the front-end chip configuration file. This procedure introduced an inefficiency which contributed to the 0-hit class. In addition, a few noisy pixel cells were also detected and masked during the offline reconstruction [79, 83], as now

module	510332	510337	510689	510704	510823	510852	510910	510929
irradiated	YES	YES	YES	YES	YES	YES	YES	NO
sensor producer	ON	CIS	ON	CIS	CIS	CIS	CIS	CIS
bonding	Indium	Indium	Indium	Indium	PbSn	PbSn	Indium	Indium
efficiency [%]	97.7	98.4	96.4	98.2	98.4	98.0	97.4	99.9
0 hits [%]	1.4	1.1	2.3	1.3	1.2	1.4	1.6	0.0
late hits [%]	0.9	0.5	1.3	0.5	0.4	0.6	1.0	0.1
plateau [ns]	8.6	9.2	8.5	9.3	10.2	11.4	10.8	13.9
masked [%]	0.0	0.1	0.0	0.0	0.3	0.0	0.0	0.0

Table 8. Summary of the pixel efficiency measurements performed at normal incidence with the standard bias voltage (150 V for modules without irradiation and 600 V for the irradiated modules). The first row provides the module identifier, the second indicates whether it was irradiated before operation at the test beam, the third presents the producer of the sensor, and the fourth indicates the bump-bonding technique. Subsequent rows report the detection efficiency, the fraction of losses due to undetected particles (0 hits), the time-walk losses (late hits), the width of the efficiency plateau and the fraction of pixels that were found to be noisy in the offline analysis and hence excluded from the efficiency analysis.

described. In any given run the level-1 timestamp of pixel hits, correlated with a trigger, had a well defined value l_0. In order to search for noisy pixel cells, hits with a level-1 which occurred either before l_0 or far after the most probable value l_0 ($l < l_0 - 1$ or $l > l_0 + 3$) were selected. If a pixel cell contributed four or more times to these events and for a fraction larger than 10^{-5} of the total number of events, then it was flagged as noisy and masked.

The track extrapolation was required to be at least 50 μm away from the pixel cells masked during the offline reconstruction. Thus, the pixel cells masked by the offline reconstruction did not contribute to the inefficiency. The number of noisy cells was, however, very small. Using the procedure described above, only two noisy pixels (out of 47232 i.e. 4×10^{-5}) were found in the unirradiated module. For all but one of the irradiated modules, the number of noisy, masked, pixel cells ranged from 0 (for three modules) to 32. One exceptionally noisy module (510704) had 129 noisy pixels, still only a fraction, 0.3% of the total number of pixels.

7.4.2 Timing Studies

In ATLAS the clock phase can be adjusted for each individual pixel detector module, but it is the same for all the pixels within a module. Hence, in order to achieve a good efficiency, it is important that the timing differences (i.e. the spread of the t_0 values in the efficiency curve) between different pixels of a module is smaller than the width of the efficiency plateau. The timing differences between different types of pixels (ganged, long and standard) and between the 16 front-end chips of a module were found to be smaller than 2 ns (see Table 9). Since this difference is smaller than the width of the efficiency plateau, it should have a negligible effect on the module efficiency at the LHC.

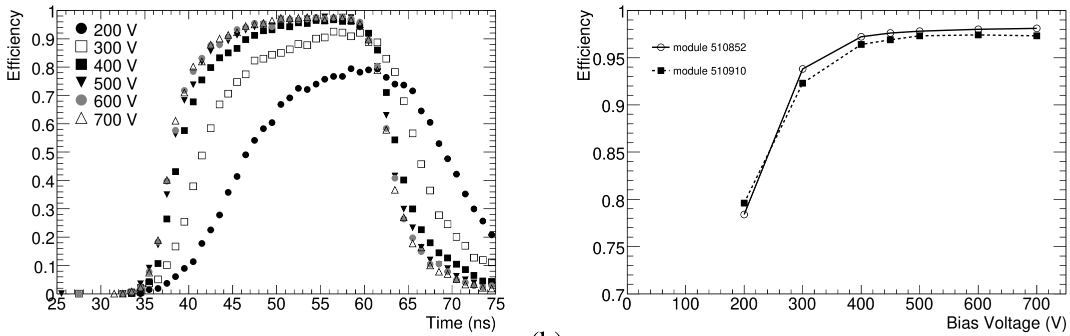
7.4.3 Detection Efficiency and Bias Voltage

The in-time efficiency for an irradiated module is reported in Fig. 33a as a function of the operating bias voltage. For low values of bias voltage, the collected charge is small, since the detector is not

pixel type	ε [%]	t_0 [ns]	plateau [ns]
standard	98.0	11.7	11.7
long	99.1	12.4	10.8
ganged	97.7	13.7	11.3

Table 9. Detection efficiency and timing parameters measured for different types of pixels (standard, long and ganged, see section 5 for their description) for a module irradiated to 10^{15} 1 MeV $\mathrm{n_{eq}cm^{-2}}$.

fully depleted. Hence the maximum efficiency is reduced. The effect of time-walk is also evident: when the collected charge is smaller, the hits are detected later and the efficiency curve moves to the right. The lower amount of collected charge affects the timing characteristics of the module. As the detector bias voltage decreases, less charge is collected. As a result, the module shows slower rising and falling edges and the efficiency plateau becomes narrower. Fig. 33b presents the peak efficiency as a function of the bias voltage for two modules irradiated to 10^{15} $\mathrm{n_{eq}cm^{-2}}$. Full efficiency is reached at 500 V, when the detector is fully depleted.



(a) (b)

Figure 33. (a) Detection efficiency as a function of time in ATLAS pixel modules irradiated to 10^{15} $\mathrm{n_{eq}cm^{-2}}$, for different values of the operating bias voltage. (b) Maximum detection efficiency as a function of operating bias voltage in ATLAS pixel modules irradiated to 10^{15} $\mathrm{n_{eq}cm^{-2}}$.

7.4.4 Detection Efficiency and Incidence Angle.

In ATLAS, tracks will not generally be incident perpendicular to a pixel module plane. Consequentially, the influence of incidence angle on module performance needs to be evaluated. When particles traverse the detector at an angle, the charge released in the sensor is spread over a larger area and is usually divided among more than one pixel cell. This creates two competing effects for the detection efficiency. Because of charge sharing, each individual pixel has a lower signal. This increases the hit losses due to the time-walk. On the other hand, the probability to lose the cluster is reduced, since both hits need to be lost. As discussed above, at normal incidence most of the hit losses occur when the particle transverse the detector in a spatially limited region of the pixel cell. This region is located close to the edge between two pixel cell, where the bias grid is located. Here, charge sharing occurs also at normal incidence because of diffusion, and the charge collection efficiency is low. When the particle incidence angle is in the range of 10°, the charge released in the sensor is spread over a length much larger than the region with poor charge collection, so that the overall charge collection efficiency is higher.

Table 10 presents the detection efficiencies for particles at 0° and 10° for both irradiated and unirradiated modules. The results indicate that the spread of charge over a larger region actually dominates so that the efficiency is larger when the detectors are tilted. The results reported in this paper, which are mostly obtained with measurements at normal incidence, are thus conservative.

module	510852	510910	510929
normal incidence	98.0%	97.4%	99.9%
10°	98.4%	98.5%	>99.93%

Table 10. Detection efficiency measured for the unirradiated module 510929 and the irradiated modules 510852 and 510910, at two values of incidence angles.

7.4.5 Efficiency in a High Intensity Beam

Beam tests of production modules were performed with a high intensity pion beam at various beam intensities, up to the value foreseen for the innermost pixel layer at the design LHC luminosity of 10^{34} cm^{-2}s^{-1}, in order to test the readout system in the presence of high occupancy conditions. At each intensity, data were taken with different configurations of the front-end chip. There are several mechanisms which can induce hit losses, depending on the rate of particles crossing the detector:

- If additional charge is deposited while the discriminator is above threshold, it is added to the initial one and the second hit is lost;
- After the discriminator goes below threshold, the pixel cell is unable to accept new hits until the sparse scan logic has transferred the hit data to the end of column memory buffers;
- Finally, if all the memory buffers are occupied when the hit is transferred, it is lost due to lack of memory space

The first effect depends on the local occupancy of the pixel cell, i.e. the probability to get a hit in a bunch crossing, and on the average Time-over-Threshold response for a charged particle.

The other effects are sensitive to the hit rate per column pair, since all pixel cells in a column pair share the same sparse scan logic and memory buffer. Therefore, results are quoted as a function of the occupancy per column pair (cp) per bunch crossing (BC). The expected occupancy [11] for the innermost layer at the LHC at 10^{34}cm^{-2}s^{-1} is 0.17 hits/cp/BC, which is approximately equivalent to 10^8 hits/cm^2/s, with an average multiplicity of 1.5 hits per track. At the test beam, the pixel detection efficiency was studied for the entire range of occupancies expected at the LHC and beyond.

A summary of efficiency measurements are reported in Table 11 with an indication of the maximal occupancy per column pair. With the standard front-end electronics settings, the detector

[11] These figures can be obtained by rescaling the results documented in Ref. [3] and taking into account the increase of the pixel long pitch from 300 μm to 400 μm. These results have been confirmed by simulation studies done with the updated layout.

efficiency of irradiated detectors remains unchanged and close to 98% up to an occupancy of 0.24 hits per clock cycle per column pair. This value exceeds by about 40% the maximum occupancy foreseen.

At larger occupancies, a small inefficiency arises from saturation of the end-of-column buffers of the front-end electronics chip. This saturation is properly flagged by the FE Buffer Overflow flags. Removing the events with the error flag restores the hit efficiency to its value at a lower intensity. The maximum value of column pair occupancy reached at the test beam was 0.27 hits per clock cycle for irradiated modules, and 0.30 hits per clock cycle for the module without irradiation. The corresponding efficiencies were about 96% for irradiated modules and 89.8% for the modules that were not irradiated.

Non-standard settings of the front-end electronics were also studied. When the latency is increased from 130 to 250 clock cycles, the intensity at which hit losses are observed is reduced by the same factor. The reduction of the frequency of the column pair readout clock from 40 MHz to 20 MHz results in a sharp efficiency loss when the occupancy exceeds 0.14 hits per clock cycle per column pair, because some pixel hits are not transferred to the end-of-column buffers within the latency of 130 clock cycles. With the usual 40 MHz operation, hit losses due to this mechanism are not expected unless the occupancy is larger than twice this value (0.28 hits per clock cycle per column pair). The efficiency also decreases when the amplifier feedback current is changed, so that the peak of the ToT distribution increases. The effect is due to the passage of a second particle through a pixel cell before the signal produced by the first event has fallen below the discriminator threshold. The efficiency loss is compatible with expectations, and it is very small. For an average ToT of 15 clock cycles and the nominal b-layer occupancy, the efficiency loss due to this effect is 0.75%. Buffer occupancy can also be increased by activating the double-writing of hits below a certain ToT threshold (see section 4.2.2).

The test beam results demonstrate that at the hit rates expected for the b-layer at the LHC design luminosity, the pixel detector modules have an efficiency larger than 98%. However, it should be noted that while the testbeam did simulate the high rate of hits in the modules, it did not simulate the high Level-1 rate and high data transmission rate that would be expected at the LHC, so the test only represents a partial simulation of operation at the highest luminosities. The effect of possible inefficiencies due to untested parts of the data acquisition chain will, however, appear as a reduction in the global DAQ live-time and not as a specific reduction of the pixel detector efficiency.

The b-layer hit detection efficiency may also be reduced by a few percent if the occupancy significantly exceeds the nominal value. This may occur for several reasons, such as track loopers at low momenta, a *pp* cross section at the LHC larger than the current estimate, or a machine luminosity exceeding the design value. Very large values of occupancy will also be reached during the heavy ion runs.

7.5 Spatial Resolution

We describe here measurements of the spatial resolution using pixel modules equipped with the final production sensors and the final or nearly final readout electronics (the FE-I family of read-out chips - see section 4). Measurements done with older prototypes have been published elsewhere [75–78].

Occupancy irradiated [hits/cp/BC]	ε 510689	ε 510852	ε 510910	Occupancy not irr. [hits/cp/BC]	ε 510929	ToT [BC]	lat. [BC]	read. [MHz]	hit dupl.
0.030-0.043	0.981	0.984	0.986	0.040	0.988	15	130	40	NO
0.069-0.084	0.981	0.984	0.985	0.082	0.986	15	130	40	NO
0.100-0.124	0.980	0.982	0.983	0.124	0.983	15	130	40	YES
0.199-0.202	0.978	0.982	0.985	0.239	0.984	15	130	40	NO
0.269-0.282	0.964	0.967	0.944	0.306	0.898	15	130	40	YES

Table 11. Measurements of detection efficiency performed with a high intensity beam. The first column reports the average occupancy of the irradiated modules for the column pair where the beam was most intense. The range corresponds to different positions of each module relative to the beam, and the occupancy varies slightly from module-to-module. The second to the fourth columns report the measured detection efficiency of the three modules irradiated to 10^{15} $\mathrm{n_{eq}cm^{-2}}$. The fifth and the sixth column show, respectively, the occupancy and the efficiency of the unirradiated module. The last columns give the front-end electronics settings, in the following order: the ToT peak tuning value and the latency, the column readout frequency, and whether hit duplication was on.

Spatial resolution is mainly determined by the pixel cell size, the choice between analog or digital readout and the degree of charge sharing between adjacent pixels. Charge sharing is affected by intrinsic sensor properties (e.g. inter-pixel capacitance and pixel capacitance to the backplane), operational parameters (such as the reverse bias operating voltage and radiation damage, etc.) and by parameters related to electronic readout (threshold, crosstalk, charge resolution, etc.). A substantial role is also played by the incident particle track angle and by the $\vec{E} \times \vec{B}$ effect.

If there is no charge sharing, all of the charge carriers locally generated around the incident particle trajectory are collected on a single pixel (single hit clusters) and the spatial resolution is related to $\sigma = L/\sqrt{12}$, where L is the pixel pitch. If the liberated charge is collected on neighbouring pixels (two or more pixel clusters), charge interpolation becomes possible, which provides for improved resolution. The charge sharing between adjacent pixels was studied using tracks at normal incidence. The width of the charge sharing region ranged between approximately $\pm$ 3 and $\pm$ 7 μm depending on the threshold, depletion depth and bias voltage (which influences diffusion).

When a particle is incident upon the charge sharing region, it may generate two-pixel-clusters. This depends on sensor charge collection efficiency and the electronics threshold. Two different algorithms were used to reconstruct the spatial position of two-pixel-clusters. A *digital* algorithm, which uses the center position between the two pixels, and an *analog* algorithm that corrects the binary position just described using an interpolation of the charge collected by the two pixels. Since it was observed that the ratio of the charge collected on the right-hand side pixel (Q_r) over the total charge collected by the two pixels $\eta = Q_r/(Q_l + Q_r)$ (where Q_r and Q_l are the charges collected by the right-hand side and left-hand side pixels in the cluster, respectively) had a dependence on the position of the passing particle, the following interpolation was adopted [87]:

$$x_{\mathrm{an}} = x_{\mathrm{dig}} + \frac{\Delta}{N_0} \int_0^{\eta} \frac{dN}{d\eta} d\eta \qquad (7.1)$$

where x_{an} and x_{dig} are the spatial positions reconstructed by the analog and digital algorithms, respectively. This formula assumes that N_0 particles are spread uniformly over an interval Δ that is the width of the region within which charge sharing occurs.

An equivalent procedure was adopted for multi-pixel clusters. These occur when particles traverse the pixel sensor at an angle. For inclined particles, the charge is collected over a region approximately given by $D \times tg(\alpha)$, where D is the sensor depletion depth, and α is the angle between the particle trajectory and the normal to the sensor surface. Charged particles with large incident angles produce signals on many pixels and the average charge per pixel decreases, despite the longer trajectory in the silicon. Since only the signal amplitudes on the edge pixels in the clusters carry information on the position of the passing particle, the digital and the analog algorithms described above were used to reconstruct the coordinate, but only taking into account the first and the last pixel in the clusters [76]. Referring to (7.1), Δ depends on the angle, cluster multiplicity and sensor design and is extracted from a fit to data for each configuration.

As the track length in a pixel is geometrically limited by $p/\sin\alpha$ (p being the pixel size), charges on a pixel exceeding $Q_{\text{cut}} = \lambda\ p/\sin\alpha$ (where λ is the mean number of electrons generated per unit path length) are due to energy loss fluctuations and δ electrons. The impact of these fluctuations on resolution was reduced by setting pulse heights exceeding Q_{cut} to Q_{cut}, when computing η.

In what follows, x describes the short (50 μm) and y the long (400 μm) pitch dimension of the pixel assembly.

7.5.1 Determination of the Telescope Extrapolation Uncertainty

The pixel spatial resolution was determined by computing the residuals between the coordinate measured by the pixel detector and that predicted by the silicon microstrip telescope. The extrapolation uncertainty depends on many parameters, e.g. the position of the microstrip planes and of the pixel detector under study, the microstrips intrinsic resolution, the amount of material along the beam path, etc. The telescope resolution was improved by applying a tight selection on the track reconstruction χ^2 probability.

The resolution of the telescope can be evaluated using the residuals for both single pixel and double pixel clusters at normal incidence. An example of these distribution is shown in Fig. 34. Single pixel clusters occur when incident particles cross the pixel central region of width L=p-2*Δ. The distribution of these residuals can be parametrised as a uniform distribution of width L, convoluted with a Gaussian distribution that takes into account the resolution of the silicon strip telescope, threshold effects and δ-rays [84]. An alternative method to estimate telescope resolution is a Gaussian fit to the two-pixel cluster analog residuals whose width is expected to be dominated by the telescope uncertainty.

The two methods give values in statistical agreement for the telescope resolution. At 0°, the telescope resolution values between 3 and 6 μm were measured, depending on the different amount of material along the beam line. At higher angles, slightly worse values were measured, due to the projection on the pixel detector plane (which yields a telescope resolution proportional to $1/\cos\alpha$) and the presence of more material along the beam when the detectors are tilted.

The quoted values are the standard deviations obtained by fitting the residual distributions with a Gaussian function. These are less sensitive to statistical fluctuations than the rms and give a reasonably good description of the width of the distributions even when the distributions are not Gaussian. This occurs at angles where a limited charge sharing is present.

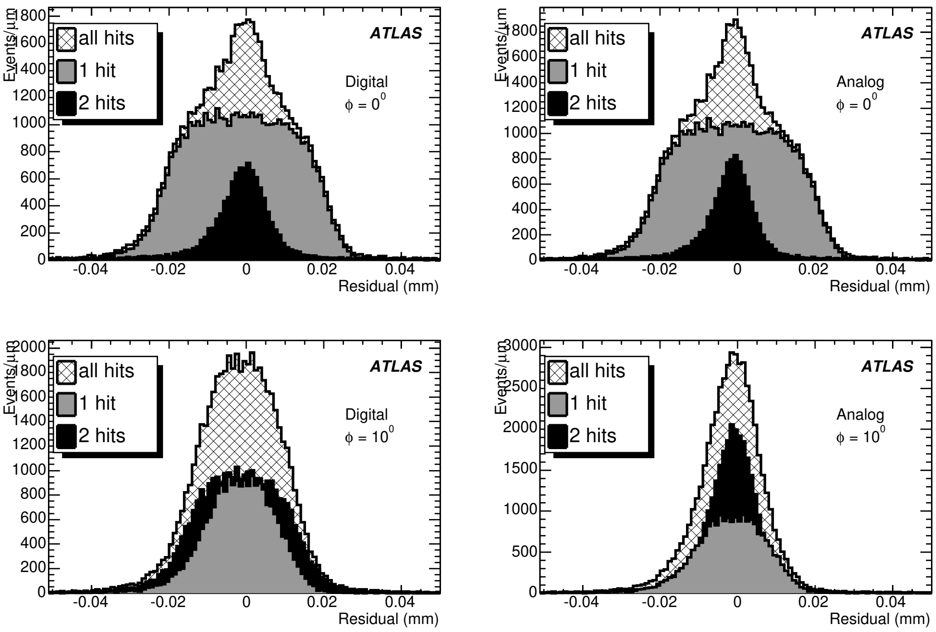


Figure 34. Left: residuals between the position measured by an unirradiated pixel detector (LBL22) using the digital algorithm and by the telescope extrapolation, for two different angles of incidence of the beam (0° upper plots, 10° lower plots). Different shadings indicate different sizes of the pixel clusters. Right: residuals between the position measured by the pixel detector using the analog algorithm and by the telescope extrapolation. After subtraction of the telescope extrapolation uncertainty, the r.m.s. are 12.2 and 12.1 μm at 0° for digital and analog algorithms, respectively, and 10.1 and 7.2 μm at 10°.

7.5.2 x-Spatial Resolution at Normal Incidence

At normal incidence, mainly single-pixel and double-pixel-clusters occur. The resolution is determined by their relative abundance and is dominated by the single-hit cluster resolution. The combined distribution of single- and double-pixel clusters for the FE-I2 module shown in Fig. 34, upper plots, has a standard deviation of 12.2 μm.

The relative weights of single-pixel and double-pixel-clusters are listed in Table 12, where the results for eight FE-I modules are presented. The difference between analog and digital resolutions or between unirradiated and irradiated modules is not large. Note that the latter were still fully depleted at the operating bias voltage of 600 V (see section 7.6).

7.5.3 x-Spatial Resolution as a Function of the Angle of Incidence

The dependence of the spatial resolution on the angle (α) of the incident particle with respect to the normal to the sensor surface was studied. The standard deviations of the all-cluster residual distributions are shown in Fig. 35. The data were not corrected for the silicon microstrip telescope extrapolation uncertainty.

Module	Irradiated	1 hits [%]	2 hits [%]	Digital resolution [μm]	Analog resolution [μm]
GE04	NO	76.3	22.2	11.8	11.7
LBL20	NO	77.0	21.5	11.6	11.4
LBL22	NO	77.0	21.1	12.2	12.1
IZMc	YES	70.1	28.8	10.6	10.3
AMS310b	YES	67.8	30.9	10.0	9.6
510929	NO	78.6	19.9	10.7	10.6
510910	YES	76.7	19.2	11.1	10.9
510689	YES	82.5	14.4	11.8	11.7

Table 12. Measurements of spatial resolution performed at normal incidence. The fraction of single- and double-pixel clusters is also reported. Telescope extrapolation has been subtracted.

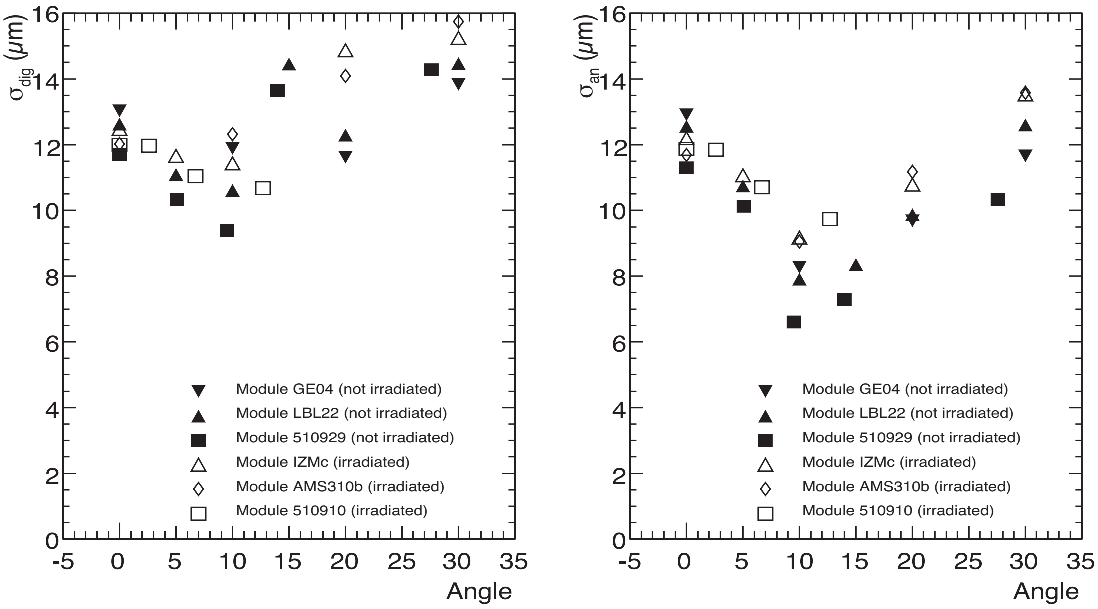


Figure 35. Measured digital (left) and analog (right) resolution as a function of the angle (in degrees) of incidence of the beam, without subtraction of the telescope extrapolation uncertainty. The charge interpolation used by the analog algorithm allows one to obtain a dramatic improvement in the spatial resolution, except for small incidence angles, when the single-pixel clusters are dominant.

As the tilt angle is increased, the fraction of double-pixel clusters increases, their residual distribution gets wider and the single-pixel cluster distribution narrower. This is a consequence of single-pixel clusters occurring in a more restricted region.

The best digital resolution is obtained when the two distributions are equally populated. For any given angle, about 98 % of clusters are formed from only two multiplicities (1 and 2, 2 and 3 and so on, depending on the angle). When they are equally populated the digital resolution is of the order of $p/2/\sqrt{12} = 25\ \mu\text{m}/\sqrt{12}$. When the angle is such that nearly all of the events belong to one multiplicity only, the digital resolution is of the order of $p/\sqrt{12} = 50\ \mu\text{m}/\sqrt{12}$. The digital resolution as a function of angle (Fig. 35a) oscillates between these two extreme values. [12]

The spatial resolution obtained with the analog algorithm (Fig. 35b and Fig. 34, lower right) is always better than the corresponding digital resolution once the incidence angles become larger than 0°. The charge interpolation used by the analog algorithm allows one to obtain a dramatic improvement in the spatial resolution for clusters with two or more pixels. The best resolution occurs when the proportion of single-pixel clusters becomes negligible. This occurred between 10° and 15°. The best resolution for the unirradiated devices was 6.6 μm before correcting for the telescope resolution. The best resolution for a device irradiated to 10^{15} $\mathrm{n_{eq}cm^{-2}}$ was 9.1 μm before correcting for the telescope resolution. The spatial resolution is not significantly degraded post-irradiation, showing that no inhomogenities are introduced in the sensor after irradiation. The differences in spatial resolution before and after irradiation are completely explained by a reduced charge collection efficiency. As the angle of incidence increases further, the charge collected by every pixel is reduced and energy loss fluctuations introduce inefficiencies in the first and last pixel in the cluster, thus degrading the resolution.

7.5.4 Lorentz Angle

In the presence of an electric field and a magnetic field, the charge carriers liberated by a passing particle within silicon drift along a direction at an angle Θ_L (Lorentz angle) with respect to the electric field direction, due to the $\vec{E} \times \vec{B}$ effect. This will happen in the barrel of the pixel detector, where the electric and magnetic field are at right angles (but not in the disks where they are parallel).

The Lorentz effect produces a systematic shift between the position of the signal induced on the electrodes and the position of the track. While this shift is in principle absorbed by the alignment correction, the knowledge of the Lorentz angle will help for the understanding of the alignment corrections and their time dependence. In addition, the Lorentz effect is expected to change the angular dependence of the spatial resolution. The Lorentz angle was measured using test beam data and a detailed report of these measurements is published elsewhere [75]. A short summary is given here.

The Lorentz angle for irradiated and unirradiated sensors was determined by measuring the minimum of the mean cluster size plotted as a function of the angle of the incident beam particles. The minimum occurs for an incident angle equal to the Lorentz angle. The results of the measurements are reported in Table 13. The measured values are compared to the predictions of a model [75, 78] which computes the Lorentz angle as a function of the magnetic field and mobility inside the sensor, the latter depending on the temperature and the electric field. A good agreement is found. Irradiated sensors have a lower Lorentz angle because a larger bias voltage is applied on a smaller depletion depth. A discussion of the Lorentz angle values expected for the pixel detector during operation in ATLAS can be found in [88].

The effect of the Lorentz force on the spatial resolution is expected to be a shift of the angular dependence of the resolution on the incidence angle by an amount equal to the Lorentz angle. This has been verified with the test beam data, namely the spatial resolution as a function of incidence angle in the presence of a magnetic field was indeed similar to that obtained without the magnetic field, once the angular shift was taken into account [75, 78].

[12]The silicon microstrip telescope extrapolation uncertainty was not subtracted.

Fluence [$\mathrm{n_{eq}cm^{-2}}$]	Bias voltage [V]	T [K]	Magn. field [T]	Θ_L (meas.) [°]	Θ_L (th.) [°]
0	150	300	1.48 ± 0.02	$9.0 \pm 0.4 \pm 0.5$	9.3 ± 0.4
0.5×10^{15}	150	264	0.95 ± 0.05	$5.9 \pm 1.0 \pm 0.3$	3.7 ± 0.5
0.5×10^{15}	600	264	0.95 ± 0.05	$2.6 \pm 0.2 \pm 0.3$	2.7 ± 0.2
10^{15}	600	264	1.01 ± 0.05	$3.1 \pm 0.4 \pm 0.6$	2.1 ± 0.2
10^{15}	600	264	0.74 ± 0.05	$2.7 \pm 0.4 \pm 0.4$	1.8 ± 0.2

Table 13. Lorentz angle measurement results.

7.6 Depletion Depth of Irradiated Sensors

The depletion depth of irradiated sensors is an important parameter, since its value affects the detector's performance. It has therefore been studied in detail. The measurement of the depletion depth was performed according to the technique described in [75–77]. Data were taken exposing the pixel assemblies to the beam at an angle of 30° w.r.t. the normal to the pixel plane, and then the average depth of charge deposition under each pixel was computed and histogrammed. The depth of charge collection region was extracted from the upper edge of this distribution. In Figure 36 the depletion depth measurements of the irradiated assemblies are shown as a function of the applied bias voltage and for three different annealing protocols.[13] In agreement with expectations made using the radiation damage parameters of the ROSE Collaboration [50], at 600 V, 250 μm thick, diffused-oxygenated-float-zone (DOFZ) silicon detectors are almost fully depleted after the full LHC dose from 10 years of operation and independently of their annealing history.

7.7 Charge Collection in Irradiated Sensors

Charge collection of irradiated sensors is an important characteristic, since its value affects detector performance, both in terms of efficiency and spatial resolution. In Figure 37, the average charge of pixel clusters with a normal incidence beam is shown as a function of operating voltage for irradiated assemblies. The maximal efficiency for the charge collection is reached at about 400 V for the detector annealed at the minimum value of depletion voltage V_{fd} (expected V_{fd} = 350 V), and its charge collection efficiency does not increase at larger operating voltages, i.e. at larger electric fields. This is related to the choice of the n-side readout. Since the pixel width is much smaller than the substrate thickness, most of the signal is induced by charges moving near the n-side [89], where the electric field has a maximum and the drift velocity is already saturated (i.e. independent on the electric field) at 400 V. For the detectors annealed at the end of lifetime at LHC, the plateau in charge collection is reached at 600 V (i.e. at their V_{fd}). One can notice that at the foreseen operating voltage of 600 V, the charge collected by the detectors will be well above the threshold of FE electronics. One should note the different asymptotic values of charge collection efficiency for the two annealing protocols: at 600 V or higher operating voltage, where irradiated sensors were completely depleted, the average Charge Collection Efficiency was (87 ± 14) % (w.r.t.

[13] The three annealing scenarios considered in the measurement and reported in the figure are: no significant annealing; the annealing which results in the minimum value of depletion voltage for a given thickness (at the end of the so called beneficial annealing); 25h of annealing at 60°C, roughly corresponding to the total annealing foreseen for the pixel detector sensors during their operating lifetime at the LHC.

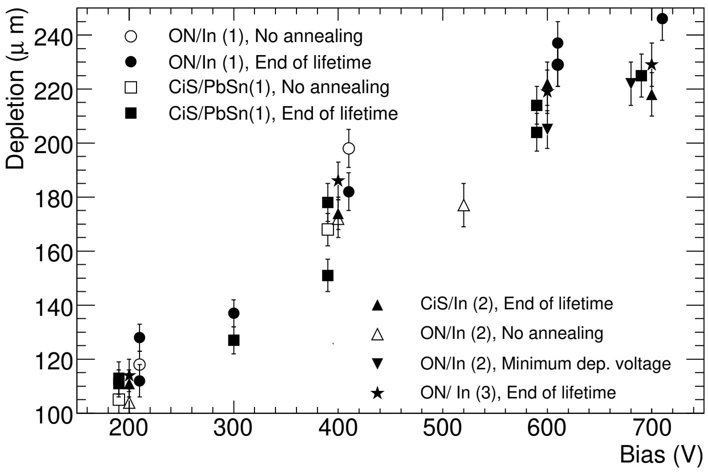


Figure 36. Measured depletion depth as a function of operating voltage for DOFZ silicon pixel detectors after irradiation of $1\times\ 10^{15}\ \mathrm{n_{eq}cm^{-2}}$. The applied annealing protocol is indicated, as well as the sensor manufacturer (CiS and ON) and bump bonding (AMS and IZM) producers. At a bias voltage of 600 V or larger, the sensors are almost completely depleted.

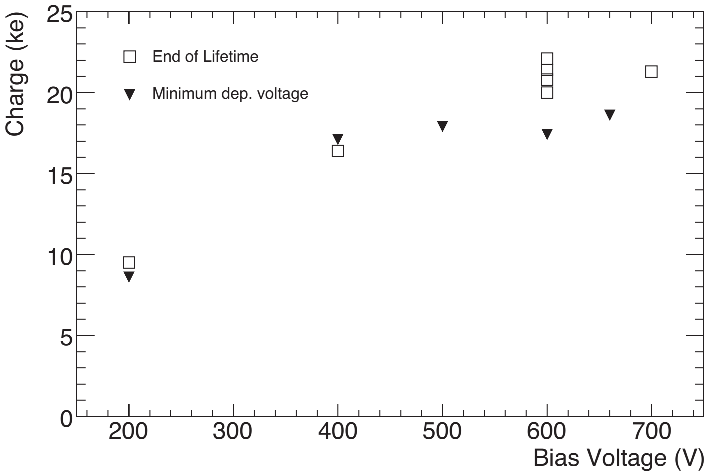


Figure 37. Average collected charge as a function of operating voltage for DOFZ silicon pixel detectors after irradiation of $1\times\ 10^{15}\ \mathrm{n_{eq}cm^{-2}}$. The four end-of-lifetime values shown at 600 V correspond to four different modules.

the one of unirradiated sensors operating at 150 V) for sensors annealed for 25h at 60° (end of lifetime at LHC), and (72 ± 14) % for the sensor annealed to minimum V_{fd}. The errors come from the uncertainty in the charge-ToT calibration. Since detectors were completely depleted as discussed above (see depletion depth measurements), this inefficiency is completely due to charge trapping.

7.8 Charge Trapping in Irradiated Sensors

Data taken at an angle of 30° between the track and the normal to the sensor surface were also used to measure charge trapping with a new method described in [58, 80]. Because of electron trapping, the deeper the track subtended by a pixel, the lower charge it collects. Hole trapping produces a much smaller and opposite effect [14]. In Fig. 38, the charge collected by a pixel is reported as a function of the average track segment depth for an unirradiated and two irradiated detectors. In the unirradiated detector the collected charge is constant as long as the track segment subtended by the pixel is entirely within the sensor. In the two irradiated detectors, charge trapping results in a decrease of charge collection efficiency with depth. This effect is more severe in the detector annealed to the minimum in V_{fd} than in the four detectors annealed to the end-of-lifetime scenario.

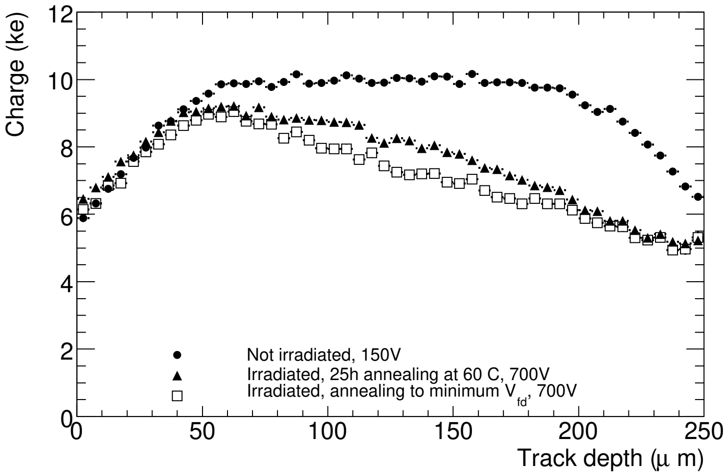


Figure 38. Pixel charge as a function of track depth for three fully depleted DOFZ silicon pixel detectors: one unirradiated operated at 150 V and two irradiated at 1×10^{15} $n_{eq}cm^{-2}$with two different thermal annealing levels and operated at 700 V.

In order to be independent of the charge scale uncertainty, the charge collection profiles were normalized and only the shape of the distribution was used to investigate trapping effects. In order to extract the charge carrier lifetimes, these experimental charge collection profiles were compared to the output of a numerical simulation [89], where the interactions of charged particles with silicon were simulated using the Geant4 package [90]. The drift of holes and electrons in silicon was described in detail, taking into account diffusion and trapping, and using parametrisations of data for the charge drift properties [91]. The signal on the pixels was computed using the Ramo theorem [92], and taking into account the electronics threshold, noise, and cross-talk.

[14] Since the pixel pitch is much smaller than the sensor thickness, most of the signal induced on a single pixel is due to charges moving close to the implant. As a consequence, the trapping of an electron anywhere in the bulk of the sensor results in nearly a total loss of the signal induced on the corresponding pixel cell. The trapping of a hole, however, causes a significant reduction of the signal only if it occurs in a small region near the pixel implant. This is more unlikely and only affects the signal for low track depths.

Sensor	annealing	τ (ns)	$\beta(10^{-16}\text{cm}^2\text{ns}^{-1})$
A	25h at 60°C	$5.5 \pm 0.7 \pm 0.8$	1.7 ± 0.4
B	25h at 60°C	$3.4 \pm 0.4 \pm 0.3$	2.7 ± 0.4
I	25h at 60°C	$4.1 \pm 0.5 \pm 0.3$	2.2 ± 0.3
T3	25h at 60°C	$4.8 \pm 0.6 \pm 1.4$	1.9 ± 0.6
average	25h at 60°C	$4.1 \pm 0.3 \pm 0.6$	2.2 ± 0.4
T2	minimum V_{fd}	$2.3 \pm 0.2 \pm 0.8$	4.0 ± 1.4

Table 14. Measured values of charge trapping lifetime and radiation damage parameter β for five irradiated detectors at 700 V bias voltage, assuming equal lifetime for electrons and holes.

The resulting values for the charge trapping lifetimes and the radiation-damage parameter $\beta = 1/\tau\Phi$ are reported in Table 14, assuming the same lifetime for holes and electrons. There is some evidence [93] that the hole lifetime is smaller. Assuming that $\tau_e = 2 * \tau_h$, the best fit values of the electron lifetime decrease by about 12 %. The measurements were performed at 700 V bias voltage in order to be well above V_{fd}. The second systematic uncertainty on trapping lifetimes is associated with the approximation of a constant electric field inside the sensor that is correlated for different sensors. While it is difficult to precisely evaluate this correlation, there is some evidence of a dependence of the trapping probability on annealing: trapping appears to be less severe after 25 hours of annealing at 60°C than for sensors annealed to the minimum of V_{fd}, after beneficial annealing only. This result is consistent with the changes in trapping times of electrons and holes derived with other methods [59, 93, 94]. The ATLAS pixel sensor read-out is dominated by the electron signal and it is expected that the trapping times of electrons increase for annealing beyond the minimum of V_{fd}.

7.9 Combined Test Beam

A dedicated effort to understand the combined performance of a complete slice of the ATLAS detector, from the pixel detectors to the outermost stations of the muon chambers, took place in 2004 with the large-scale combined test beam exercise [95]. The setup included six pixel modules, placed inside a 1.4 T magnetic field. The setup integrated the hardware and software to approximate as closely as possible what will exist in the full ATLAS detector. The combined test beam ran in 2004 and provided an opportunity to test the software and to study the tracking performance using real data.

The pixel detector performed well in the combined test beam, producing good quality data. Using ATLAS offline software, tracks were successfully reconstructed. Residuals obtained after alignment showed agreement with simulation. The impact parameter and z_0 resolutions were comparable with what is projected for the ATLAS experiment.

The use of standard ATLAS components in the software chain was successful and the combined test beam was a valuable development test bed for the online and offline software. This effort has led to first sets of calibration and alignment procedures, essential to the initial understanding of the detector performance and to the extraction of the first physics results.

8. System Test and Cosmic Rays Operation

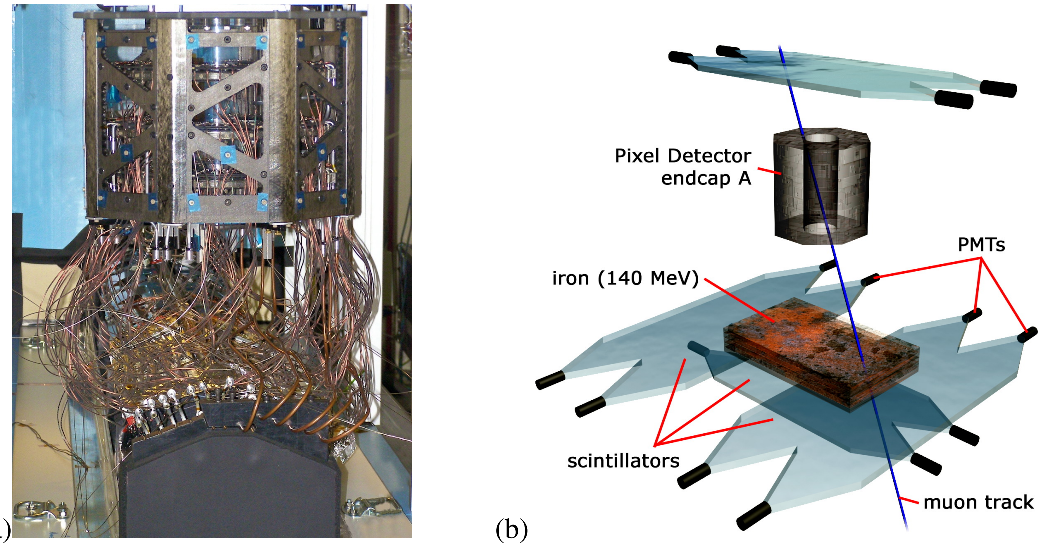
A system test with one endcap (three disks) of the pixel detector has been performed as a realistic test of the detector operation. To achieve this goal, a setup consisting of the endcap and about 10% of the detector services has been installed in the CERN SR1 facility. Production and pre-production parts were used to establish the realism of the test.

The system test program included the commissioning of the setup and the detector readout, measurements of the analogue performance of the detector modules and data taking with cosmic rays. The following sections give a brief overview of the system test [96].

8.1 Setup

One endcap of the pixel detector was operated in the system test setup. The endcap was connected to a prototype service quarter panel, as shown in the photograph in Fig. 39a, and cooled with evaporative C_3F_8, also to be used for final operations. All services connected to the endcap were made from production or pre-production parts in order to create a realistic model of the final setup inside ATLAS.

The endcap was oriented vertically for data taking with cosmic rays. Several scintillators were used to generate the trigger. The scintillator arrangement, which is shown in Fig. 39b, was designed to maximise the number of tracks passing through the three disks of the endcap and at same time allow for inclined tracks.



(a) (b)

Figure 39. (a) Photograph of the endcap in the system test, connected to the prototype service quarter panel, and (b) schematic drawing of the scintillator setup for the cosmics trigger.

8.2 Commissioning of the Setup

8.2.1 Service Tests

As a first step in the commissioning of the setup, a complete test of the electrical services was performed. This was done using a dedicated test setup, which was designed to automatically test all electrical services belonging to one Patch Panel 0. This first application of the services test procedures was essential for developing the final protocol used for services commissioning of the detector that has been installed in ATLAS.

8.2.2 Cooling Operation

Evaporative C_3F_8-cooling was used for the endcap in the system test. Temperature measurements at different supply voltages and module configurations were performed in order to simulate the evolving power consumption expected during the detector lifetime and to assess the cooling performance under these conditions. The module temperature for power off was about $-24°$C and about $-17°$C for nominal (non-irradiated) power values and about $-12°$C (extrapolated) for power values after irradiation to a lifetime dose [97].

8.2.3 Calibration of the Optical Links

For a reliable communication between the pixel detector modules and the off-detector electronics, several parameters of the optical links (section 4.4) have to be calibrated. The algorithms for this tuning procedure were partially developed and refined during the system test. Whereas the setting of the parameters for the links from the off-detector electronics to the modules is not critical, the tuning of the returning-data links requires more care. The first parameter to be adjusted was the light output power of the VCSELs on the opto-boards. This power was determined with a control current I_{Set} that is common for all VCSELs on an opto-board. The power can be measured by monitoring the current in the PiN-diodes at the receiving end. The control current has to be set such that all VCSELs on the opto-board are safely above the laser threshold.

For a given laser power, the threshold and the data delay at the receiving end need to be set. The first parameter determines the discrimination between a logical 0 and a logical 1, whereas the second determines the sampling time within the clock cycle of the 40 MHz clock. Figure 40 shows a two-dimensional plot of the number of bit errors measured during a scan of these two parameters. The horizontal axis corresponds to the sampling time, while the vertical axis corresponds to the sampling threshold. A region with errors at low thresholds can be seen. This comes mainly from bit flips from 0 to 1 due to a threshold setting near the noise floor. A region with errors at high thresholds is apparent, which is given by bit flips from 1 to 0 due to a too high sampling threshold. The vertical error region is caused by a sampling time which is set on the clock edge, where the data are not stable. The operating point of the receiver has to be set in the error free region taking into account that not all boundaries between error-free and error regions are equally stable. The noise floor and the trailing edge of the signal are more stable than the upper signal level and the leading edge. The most reliable operating point is not in the centre of the error-free region, but closer to the stable boundaries. A difficulty arises if the spread in the output power between the different lasers of one opto-board is too large. In such a case, it can be difficult to find a value for I_{Set} such that all channels show a sufficiently large error-free region from which a stable set of operating parameters can be chosen. In the system test it was discovered that the power spread increases for lower opto-board temperatures. It was, therefore, decided to equip the opto-boards in the detector with dedicated heaters to be able to regulate their temperature up to $\sim 30°$C. [4]

Some of the VCSELs on the opto-boards produced very little or no optical power on all channels. The optical power on one channel was found to depend on the current on the other channels.

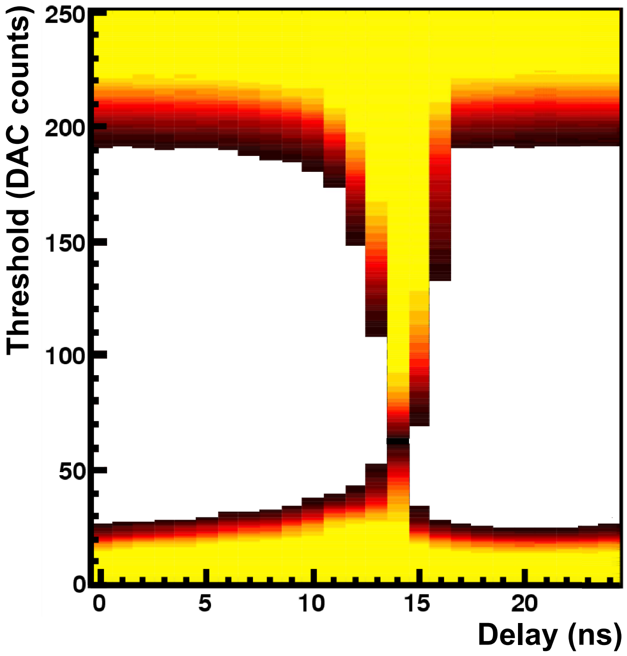


Figure 40. Scan of the receiver parameters for the optical data link. The horizontal axis gives the sampling phase. The vertical axis presents the sampling threshold. The colours represent the number of errors for a given set of parameters (white corresponds to no errors in the given bit pattern).

This can be modeled with a common series resistance (CSR). The voltage drop on the CSR resulted in inadequate voltage to drive the VCSELs. A procedure was formulated to estimate the CSR and opto-boards with a high CSR were excluded from the production service quarter panels, corresponding to about 7% of total production (see section 4.4.5).

8.3 Analogue Performance of the Modules

Several measurements of the analogue performance of the modules were performed during the system test. Table 15 shows the average values of the threshold dispersion and noise for all tested modules in the endcap. The thresholds were adjusted to 4000e$^-$. Both threshold and noise values are comparable to single module measurements without any notable influence coming from the operation within a large scale system. The uniformity of the measured thresholds of all modules, which is necessary for the reliable operation of the full pixel detector, is apparent [97].

Average threshold	$4002 \pm 1.3\,e^-$
Threshold dispersion	$33 \pm 1\,e^-$
Average noise	$166 \pm 8.5\,e^-$

Table 15. Values for threshold, threshold dispersion and noise for all modules in the system test of the endcap.

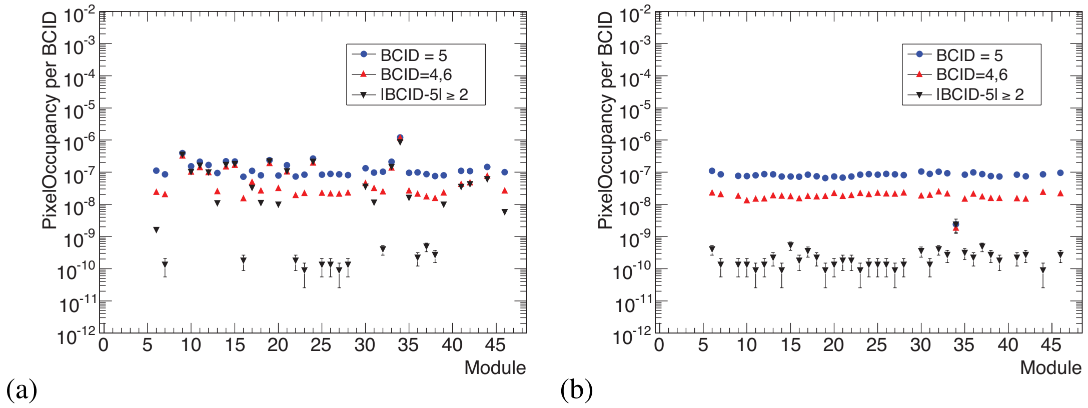


Figure 41. Occupancy per pixel in all modules of one pixel disk before (a) and after (b) masking off hot pixels for bunch crossings (BCID) within and outside the cosmic trigger (BCID=5).

8.4 Cosmic Ray Operation

The endcap detector was operated with an external trigger generated from a set of scintillators arranged above and below the endcap. The rate of cosmic ray tracks crossing all three disks of the endcap in the sensitive area was about 6 Hz. The detector noise was studied [98] using several runs with different detector configurations, and it was found that the noise signal was uncorrelated with the timing relative to the trigger. Pixel occupancy, (i.e. the fraction of pixel hits per readout event) was used to classify "hot" pixels. Pixels with an occupancy per Bunch Crossing Identification (BCID) of 10^{-5} or greater were defined as "hot" pixels. Approximately 90% of these "hot" pixels were already identified as defective during module characterization. Their total fraction is below 0.2%. After removal of "hot" pixels, the noise occupancy drops from 10^{-7} to 10^{-10}, as shown in Fig. 41.

Data from cosmic ray operation were used to exercise the full chain of offline reconstruction. Digitisation parameters were taken from the characterisation tests performed during module production. The simulation produced with these parameters has been found to be in a good agreement with the data, providing an important test of the ATLAS pixel detector simulation. The tracking studies, especially related to tracks passing through the overlap regions between adjacent modules in the same disk, were useful for identifying problems in the description of the detectors geometry.

A benchmark for analogue performance is the pulse height distribution measured using the Time-over-Threshold method (see section 4.2.2). Fig. 42 shows a comparison between the pulse height distribution in cosmic ray events for single- and double-hit clusters, which are the most relevant for LHC running. The calibration of the detector response to charge deposition, obtained during module production and characterisation, describes well the observed data. The characteristics of pixel clustering in the data (the number of clusters on a track, the cluster size and the quality of the track fit) were checked and found to agree with the Monte Carlo simulation as also shown in Fig. 42.

The pixel hit efficiency was measured to be close to 100%. This was done by checking how often a pair of hits was found in the overlap region compared to expectations. Approximately 24%

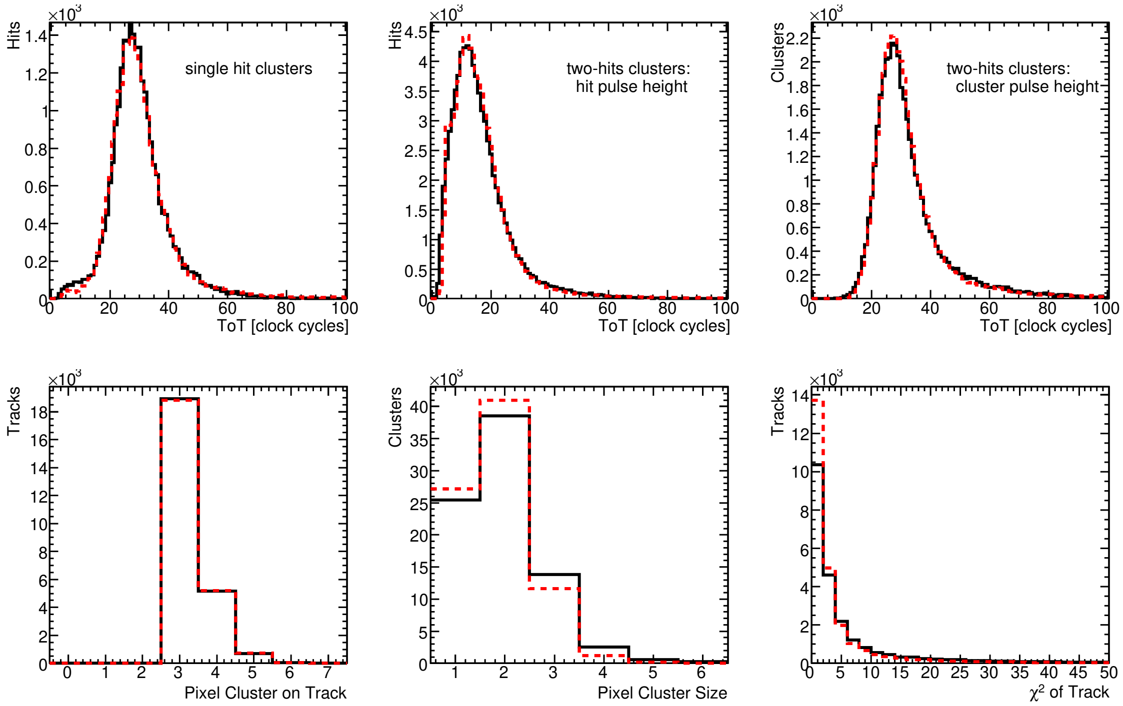


Figure 42. Comparison between cosmic ray data (histogram) and Monte Carlo (dashed) as measured in the system test. The Time-over-Threshold(ToT) distribution for single-hit clusters (top left), individual hits of a two-hit cluster (top middle) and the sum of the ToT for two-hit clusters (top right) are shown. The number of pixel clusters (bottom left), the distribution of cluster size (bottom middle) and the fitted track χ^2 (bottom right) are also given.

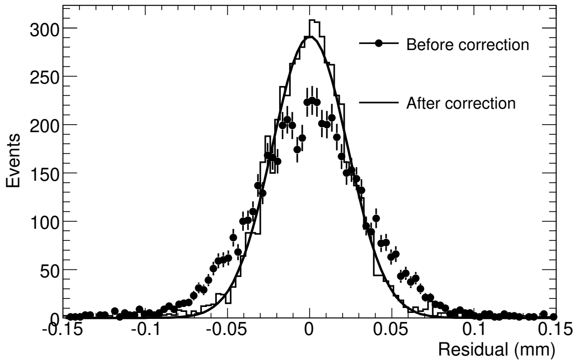


Figure 43. Distribution of overlap residuals before and after alignment corrections. A Gaussian fit to the residuals after correction is also shown.

of tracks passed through the overlap region, and were used to estimate the relative alignment between adjacent modules using residuals from overlap hits. Fig. 43 shows the resolution in the short pixel direction before and after the alignment correction. Using the nominal geometry, an initial resolution of 23 μm was obtained. After an alignment correction, this improves to 16 μm, which is close to the 14 μm expected from the Monte Carlo simulation. The relative alignment constants were also cross checked by comparing the data with the survey obtained during the detector assembly for modules with enough overlap hits (≥ 50). [4] A strong correlation between the two methods indicates that the survey is a reasonable starting point for the final detector alignment.

9. Conclusion

The design and fabrication of the ATLAS pixel detector electronics, sensors and modules have been described in this paper. A brief description of the mechanics and electrical and cooling services has been given, and more details on these elements of the pixel detector may be found in Ref. [4]. The performance for first operation of the pixel detector in ATLAS and with colliding beams from the Large Hadron Collider will be described in subsequent papers.

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