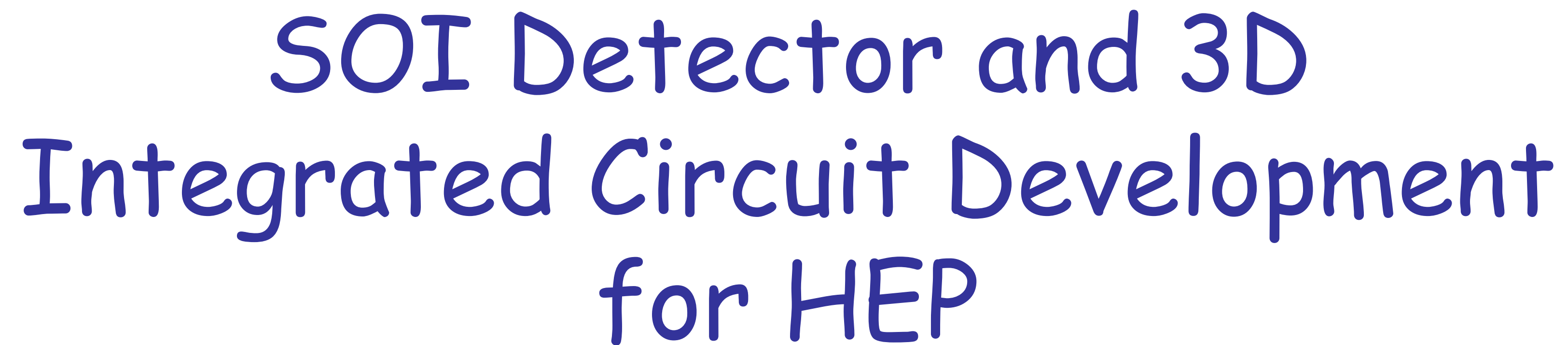


R. Yarema
For ILC Pixel Group at FNAL

Fermi National Accelerator Lab
Batavia, Illinois

February 22, 2007

Outline

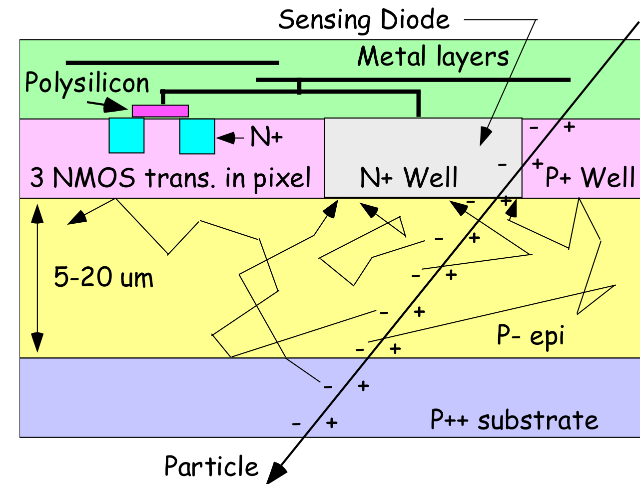
- MAPS - integrated sensor and readout
- SOI Detector development
  - Present Fermilab initiatives with 2 SOI foundries
- 3D integrated circuit development
  - Several examples of 3D IC imaging arrays.
  - ILC vertex detector requirements.
  - 3D readout chip based on ILC vertex needs.

Introduction

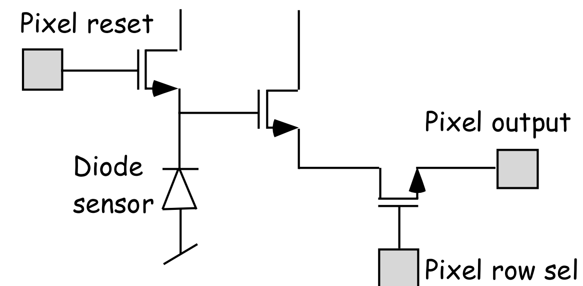
- Requirements for HEP pixel electronics and detectors continue to push the limits for lower mass and power, and higher resolution.
- Significant progress has been made in the last decade to address these issues by integrating sensors and front end electronics within the pixel cell.
  - Monolithic Active Pixel Sensors
  - SOI Pixel Sensors
    - Offers improvements over MAPS
  - 3D integrated circuits
    - Offers improved performance over SOI pixel sensors for HEP and related applications.

MAPS Development

- Monolithic Active Pixel Sensors have generated a lot of interest and excitement in High Energy Physics [1, 2]
  - Combine detector and front end electronics on same substrate in a commercial CMOS process (low resistance substrate).
  - Some issues
    - Relatively small signal level
    - Pixel electronics generally limited to NMOS devices in P-well
    - Limited functionality possible in small pixels
- Currently numerous groups are working on MAPS



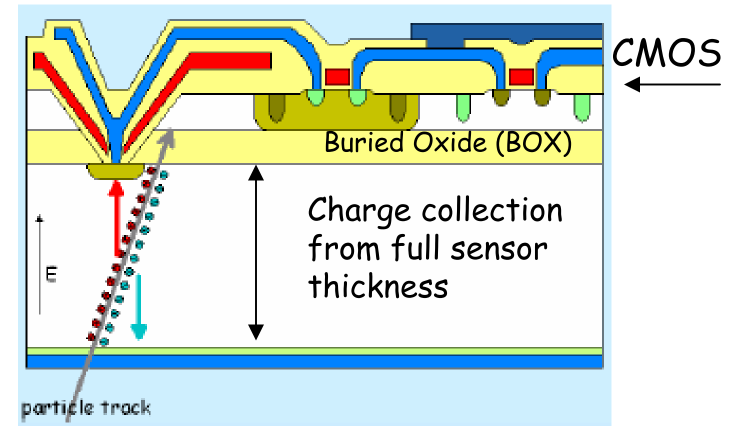
Pixel Cross Section (not to scale)



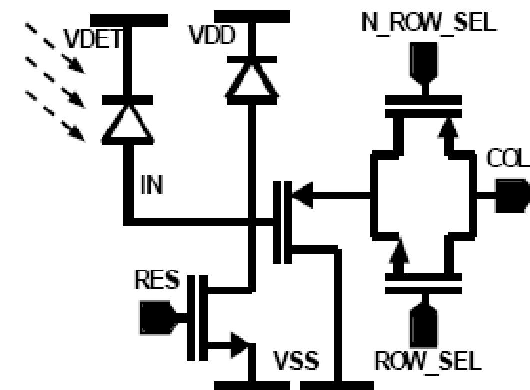
3 NMOS transistors in Pixel

SOI Active Pixel Sensors

- SOI APS have advantages over MAPS
  - Larger signal proportional to high resistivity substrate thickness.
  - Less charge spreading
  - CMOS instead of NMOS in pixel
- Early work done in 3 μm process[3]
  - Large pixels cells not useful for high resolution detectors
- Recent work has moved to smaller feature processes => smaller pixels
  - Collaboration of many groups using the OKI 0.15 μm SOI[4]
  - Fermilab has arrangements to work with the ASI (American Semiconductor Inc.) and OKI on SOI detector development
- Useful for HEP, X-ray and gamma imaging, electron microscopes



SOI Pixel Cross Section[7]



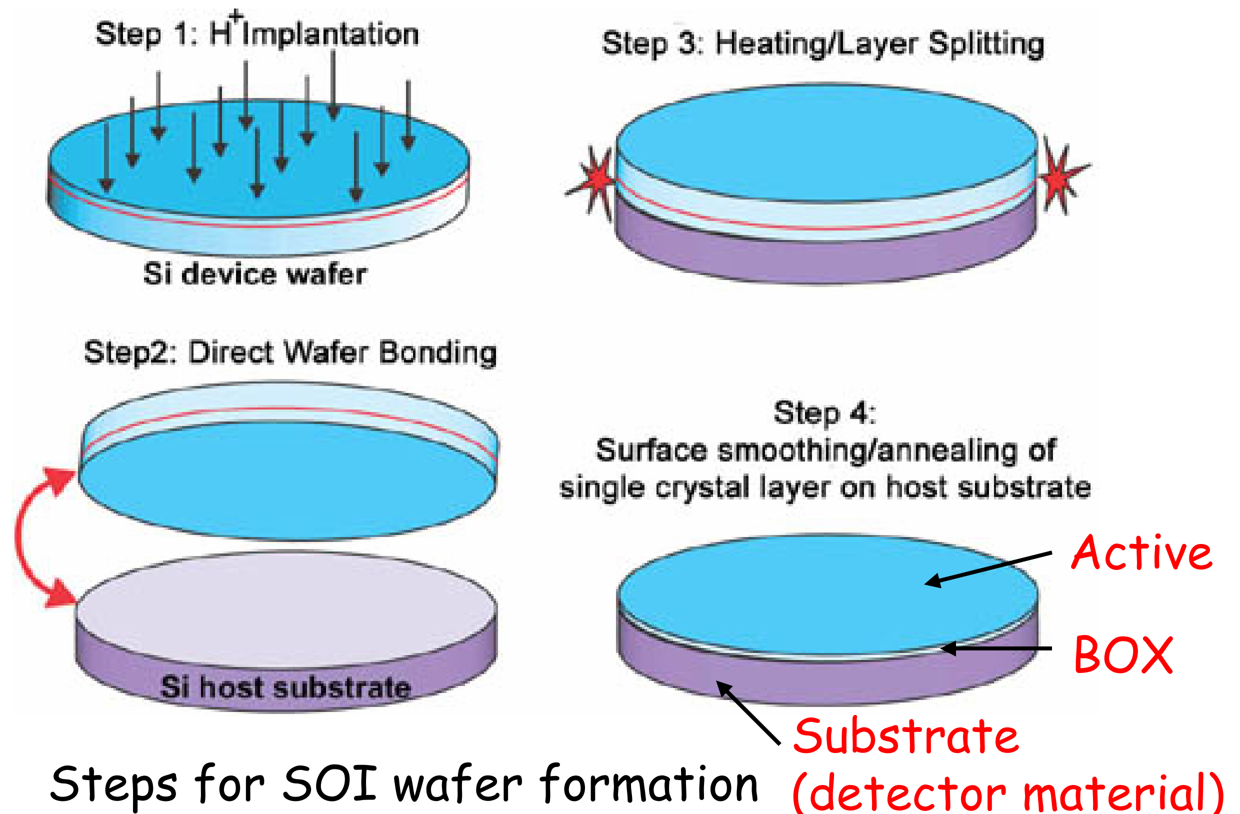
CMOS Transistors in SOI Pixel[7]

SOI Wafer Formation

SOI is based on a thin, 40 nm thick, active circuit layer for transistors that is bonded on top of an insulating layer that is typically 200 nm thick. The insulating layer or BOX (Buried Oxide) is formed on top of a handle wafer.

The handle wafer can be high quality detector grade silicon.

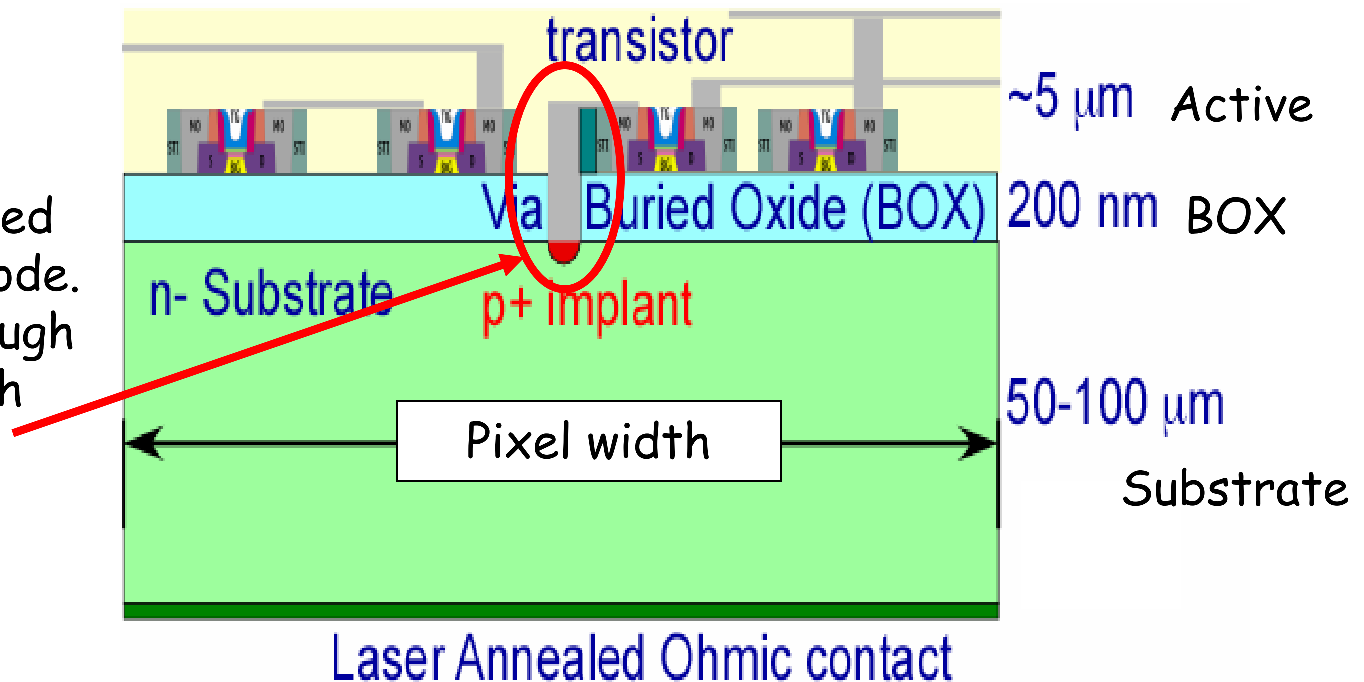
Thus full CMOS circuits Can be built in the active layer and connected to fully depleted sensing diodes beneath the BOX.



Steps for SOI wafer formation

SOI Pixel Detector Concept

P+ material implanted to form sensing diode. Via is formed through BOX and filled with metal.



Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at two different foundries (OKI in Japan, and ASI in US) . The two processes have different characteristics as seen below

Process	**0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).**
SOI wafer	**Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment*), 650 μm thick (SOITEC)**
Backside	**Thinned to 350 μm, no contact processing, plated with Al (200 nm).**

OKI Process

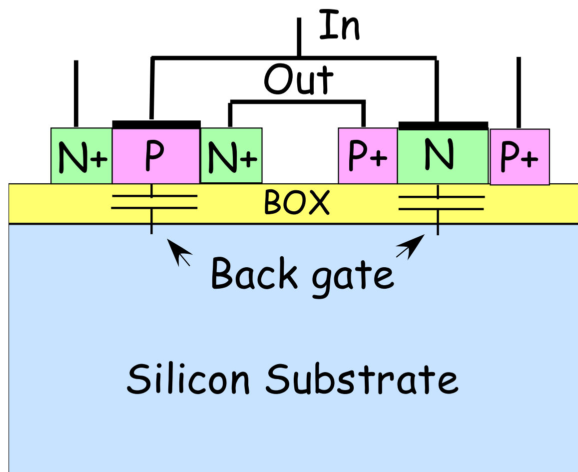
Process	**0.18μm partially-Depleted dual gate SOI CMOS process, Dual gate transistor (Flexfet), No poly, 5 metal (American Semicondutor / Cypress Semiconductor.)**
SOI wafer	**Wafer Diameter: 200 mmϕ, Handle wafer: FZ>1k Ω-cm (*n type*)**
Backside	**Thinned to 50-100 μm, polished, laser annealed and plated with Al.**

ASI Process

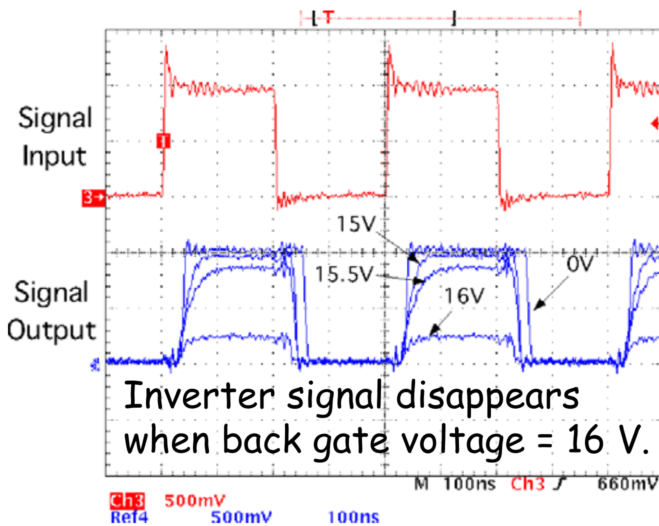
Pixel Design in OKI Process

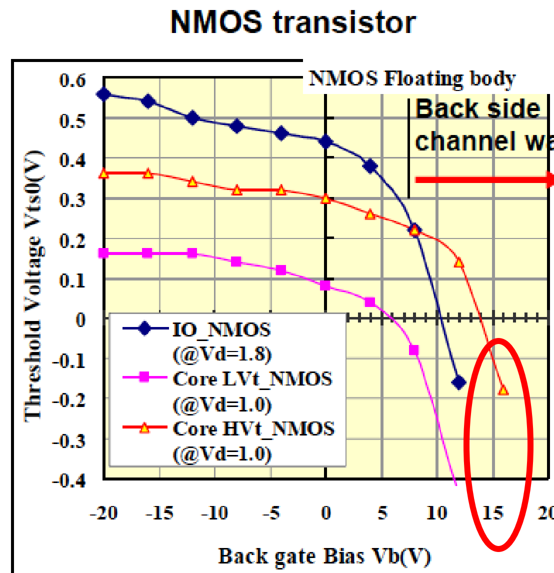
- A chip has been designed in the OKI 0.15 micron process to understand the advantages and problems of SOI detector design.
  - The chip is a wide dynamic range counting pixel detector chip that is sensitive to 100-400 KeV electrons, high energy X-rays, and minimum ionizing particles.
- The back gate effect is an important design consideration.

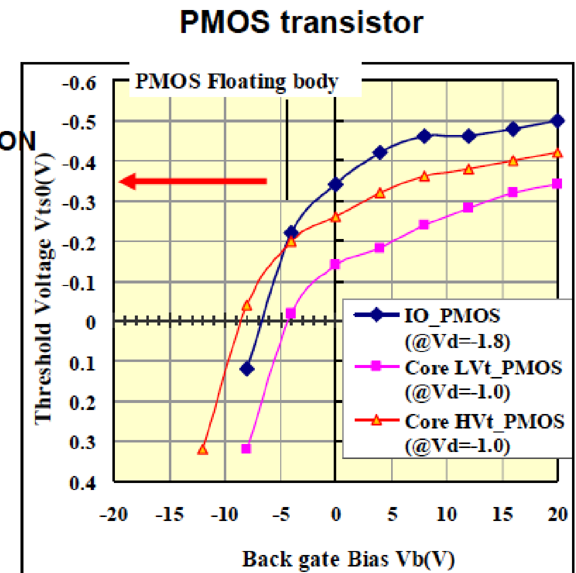
Back gate Effect in OKI Process



Substrate voltage acts as a back gate bias and changes transistor threshold



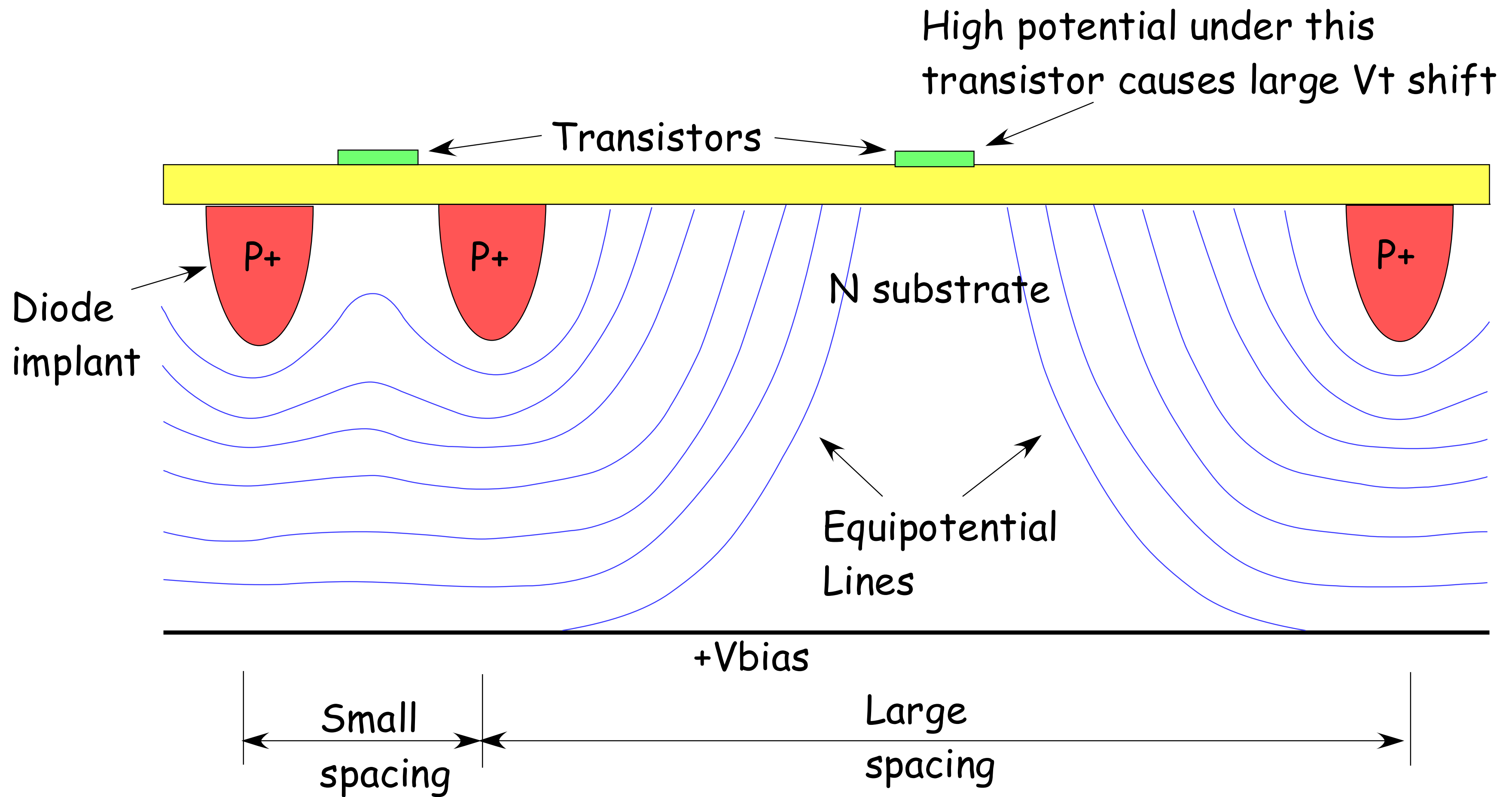




The threshold shift problem exists for SOI transistors in processes like OKI which have a floating body. The ASI process has a discreet back gate which shields the transistor from the substrate and thus eliminates the problem.

2006.9.12yasuo.arai@kek.jp(STD6)

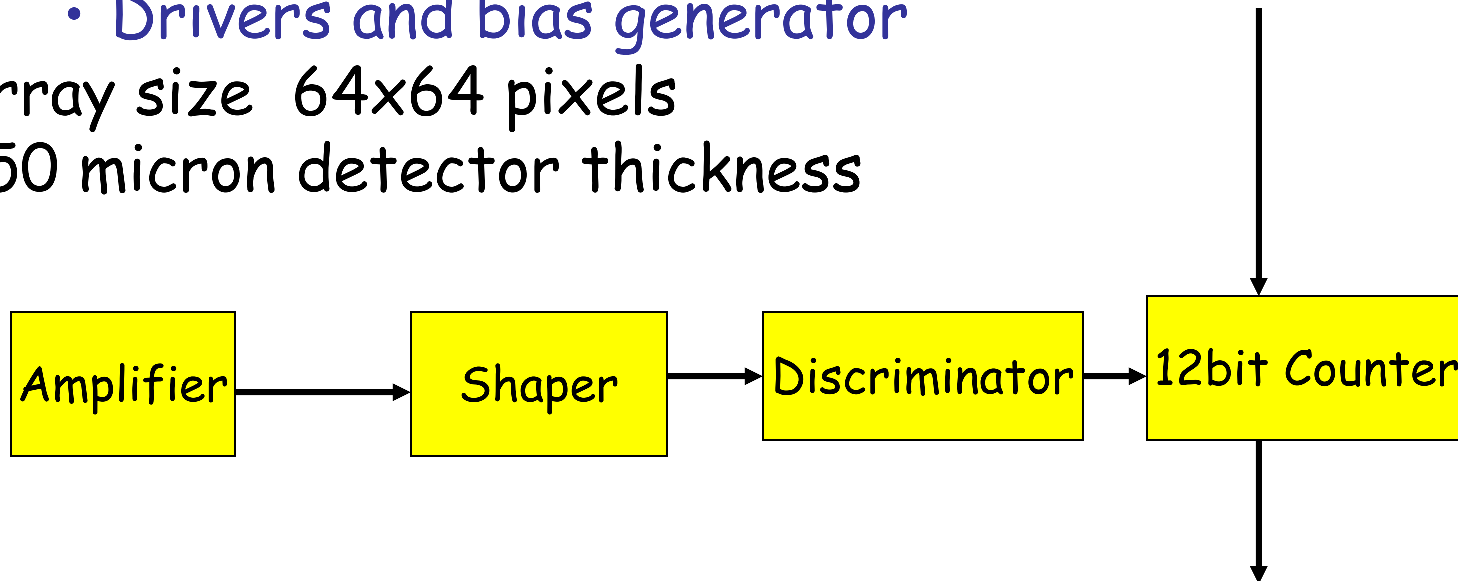
Equal Potential Lines Under BOX



To reduce voltage under the transistors, keep P+ implants close together.

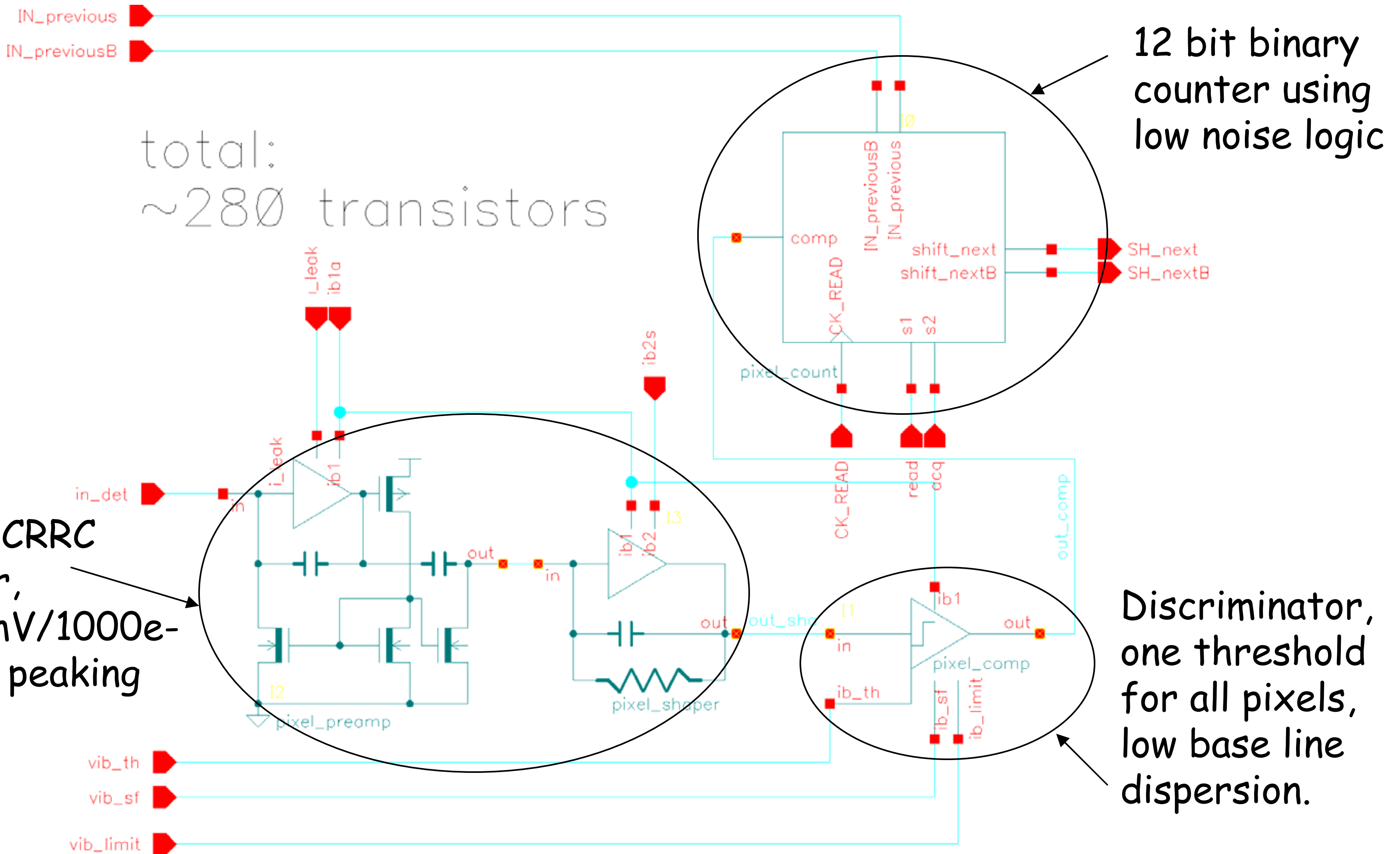
Fermilab Design for OKI

- Counting pixel detector plus readout circuit
- Simplified architecture
  - Reconfigurable counter/shift register
    - 12 bit dynamic range
  - Limited peripheral circuitry
    - Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness



Pixel Design in OKI Process

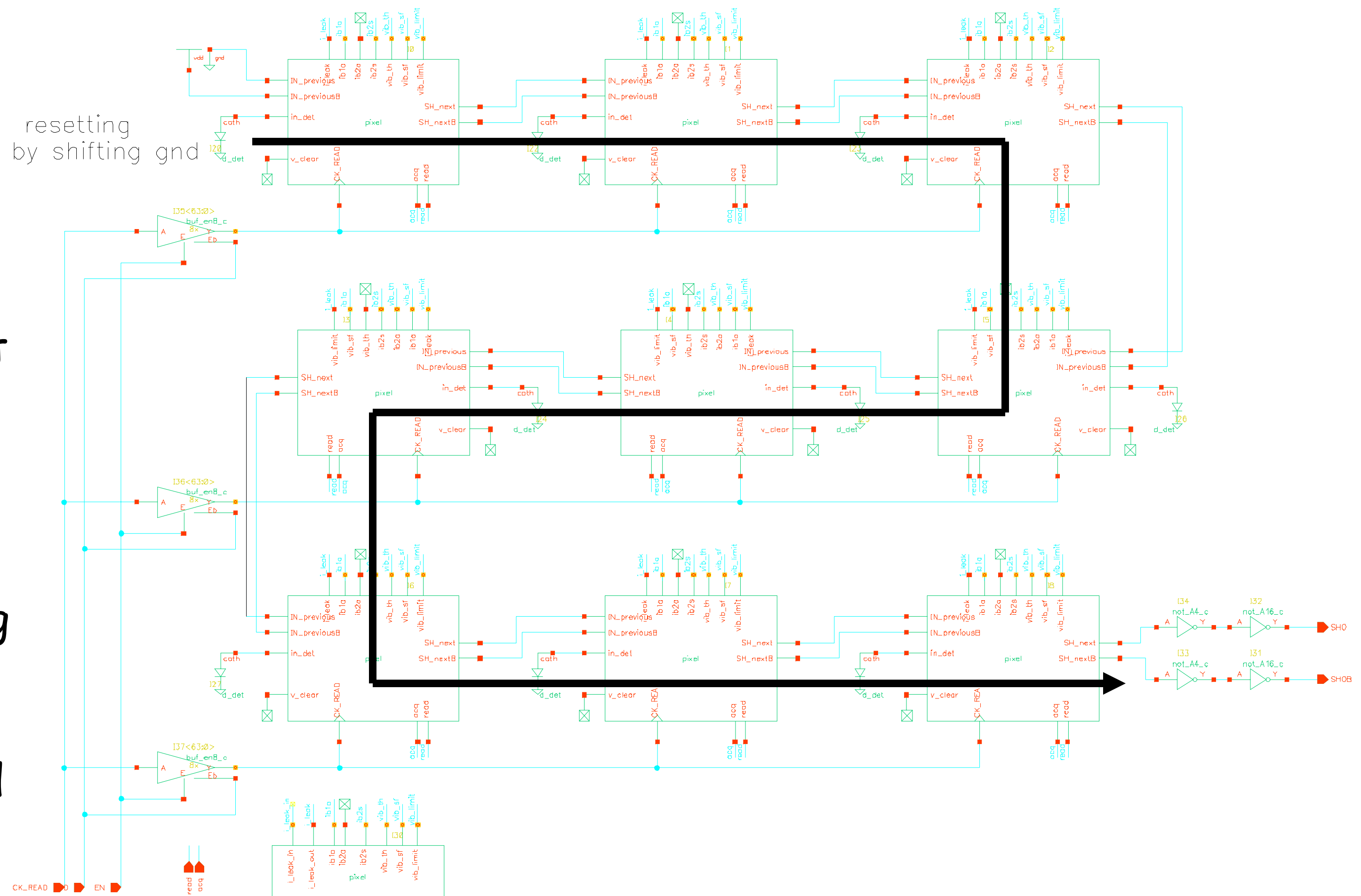
CSA + CRRC Shaper,
~150 mV/1000e-
150 ns peaking time



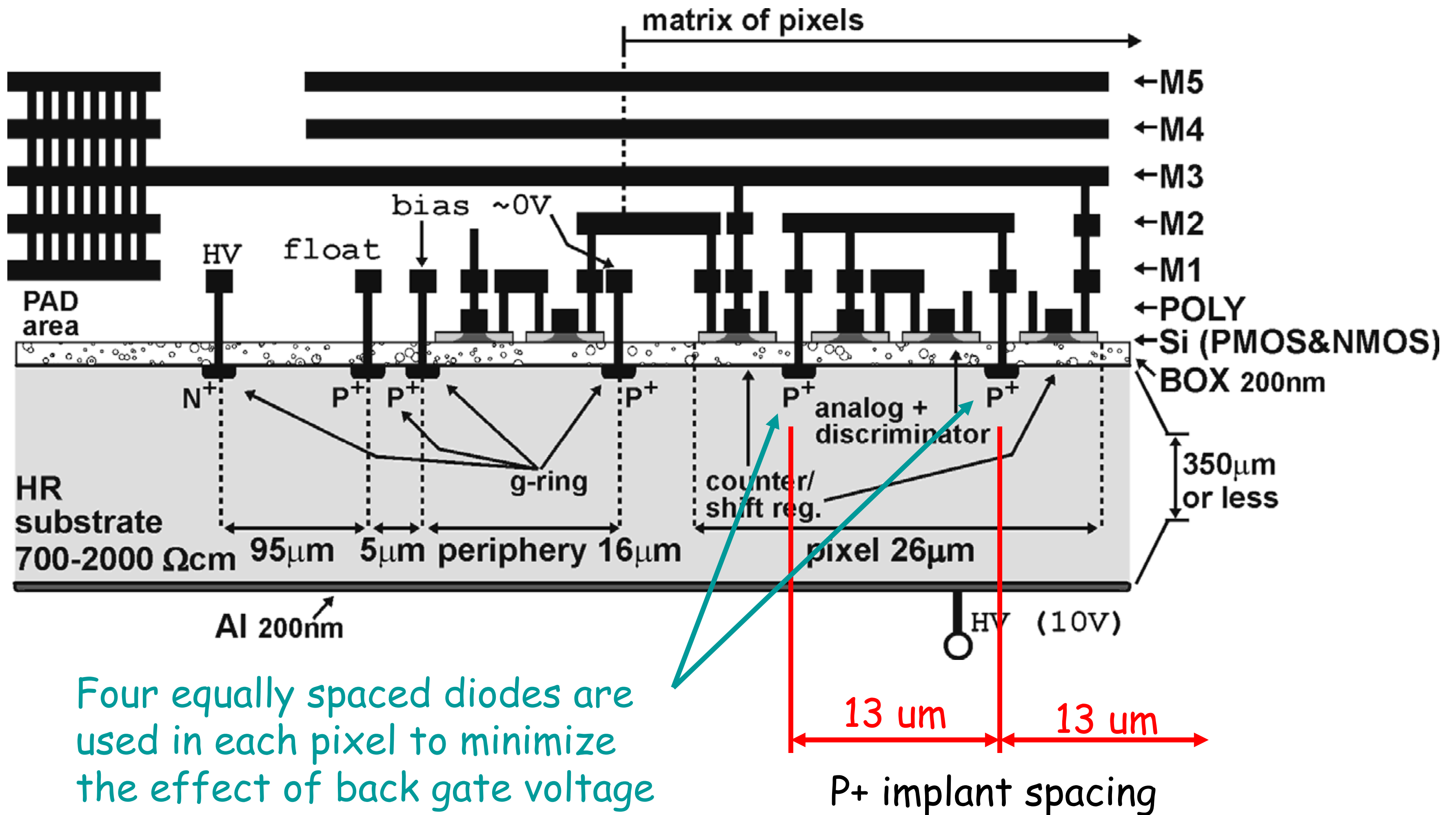
Simplified 3 x 3 Pixel Matrix

Operates in two modes:
Acquire/Read out

12 bit counter is reset by changing counter to a shift register configuration and shifting in zeros during read out.

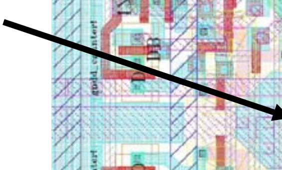


OKI Pixel Detector Cross Section



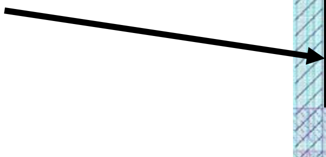
Pixel Cell Layout

One of four detector diodes



All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

One of twelve D flip-flops arranged around perimeter of pixel cell



26 microns

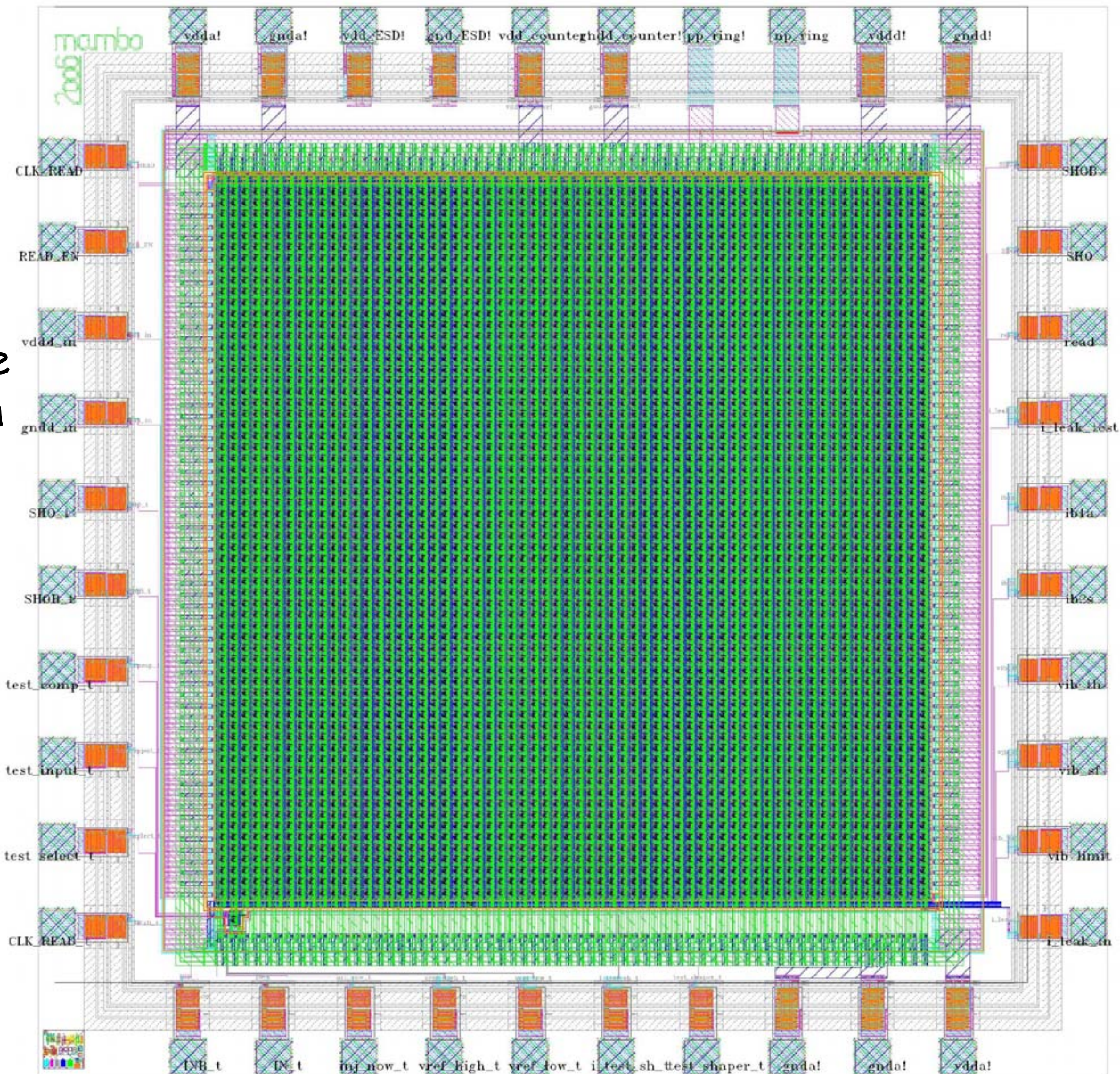
4K Pixel Design in OKI Process

Chip name is MAMBO:

Monolithic Active pixel Matrix with Binary cOunters

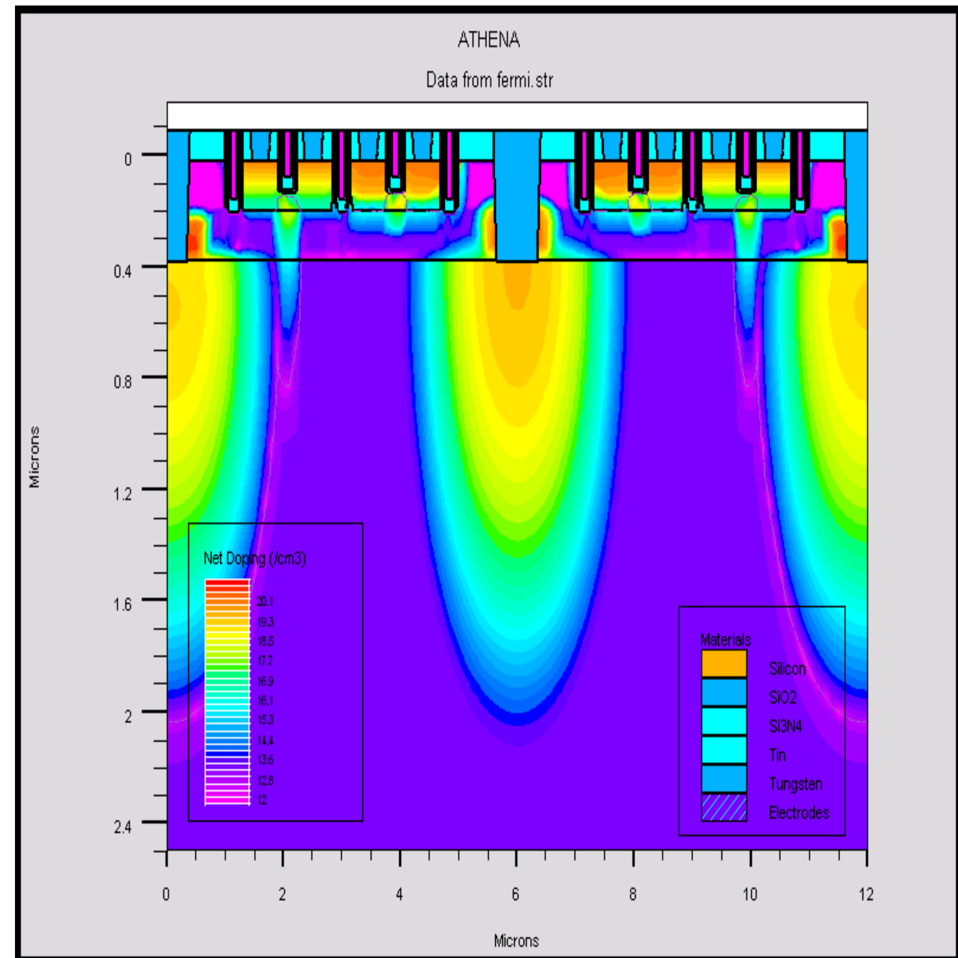
Chip size:
64 x 64 array
2.5 mm x 2.5 mm

Designed by Gregory Deptuch



Pixel Design in ASI Process

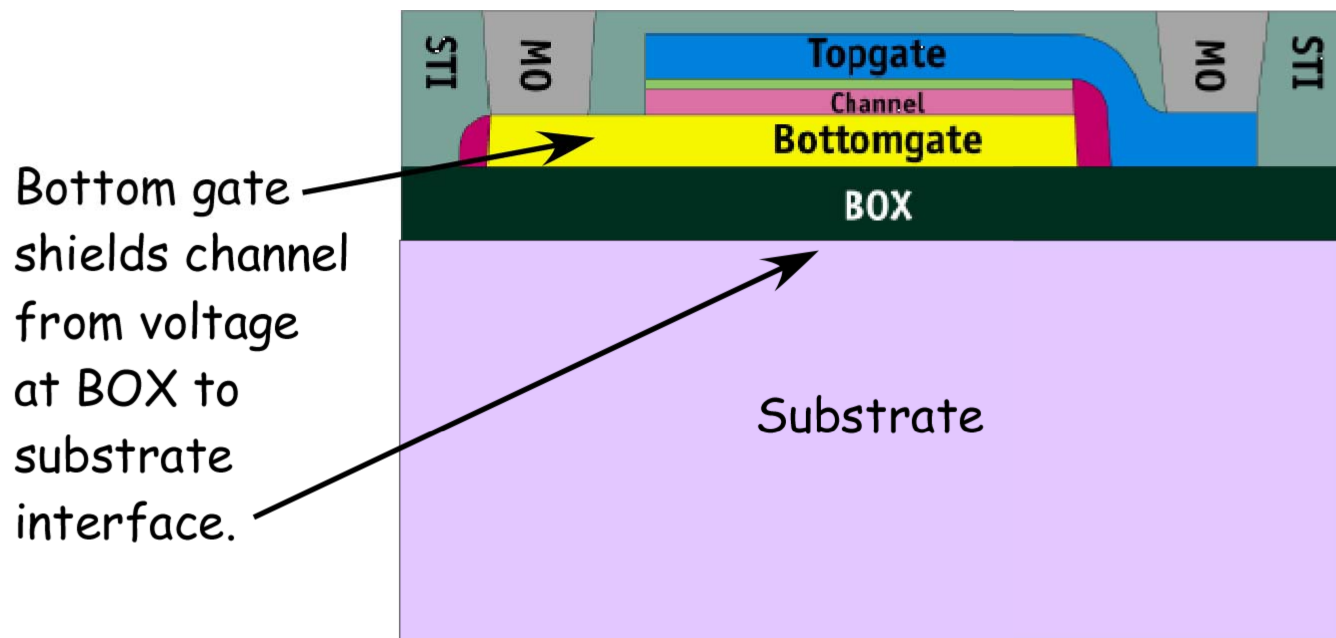
- SBIR phase 1 funding
- Modeling and process simulation of a thinned, fully depleted sensor/readout device.
- Studies of backside thinning, implantation, and laser annealing.
- Work in progress



Diode simulation in Flexfet process

Back Gate in ASI Process

- Design of a pixel circuit using dual gate transistors in which the back gate is used to remove radiation and backside bias effects.

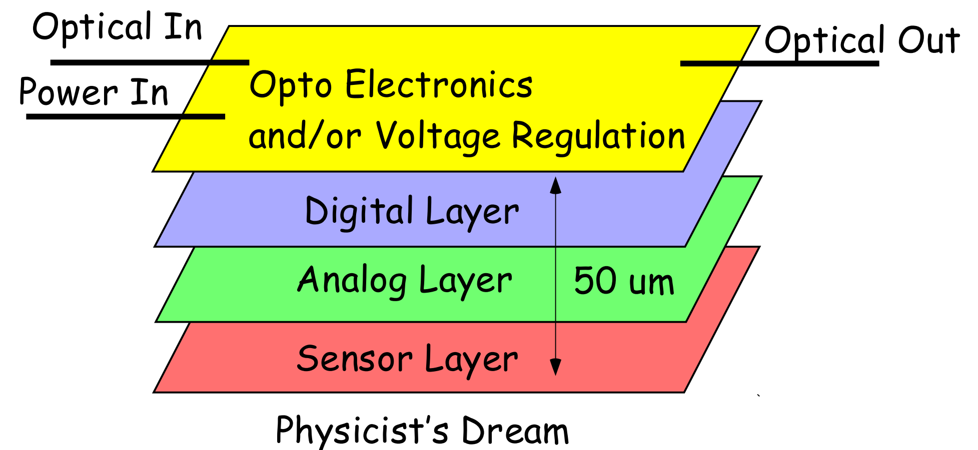


Looking further Ahead

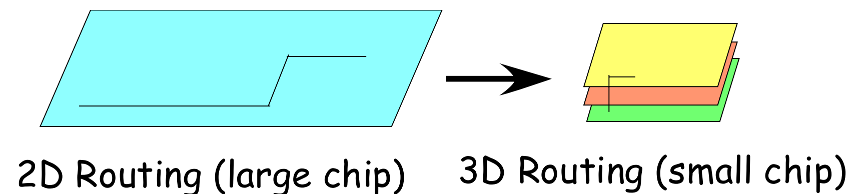
- Another technology, is emerging that offers advantages over SOI detectors. This technology is called vertical scale integration or 3D for short.
  - Increased circuit density
  - Independent control of substrates for detector, analog circuits, and digital circuits.

3D Integrated Circuit Development

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



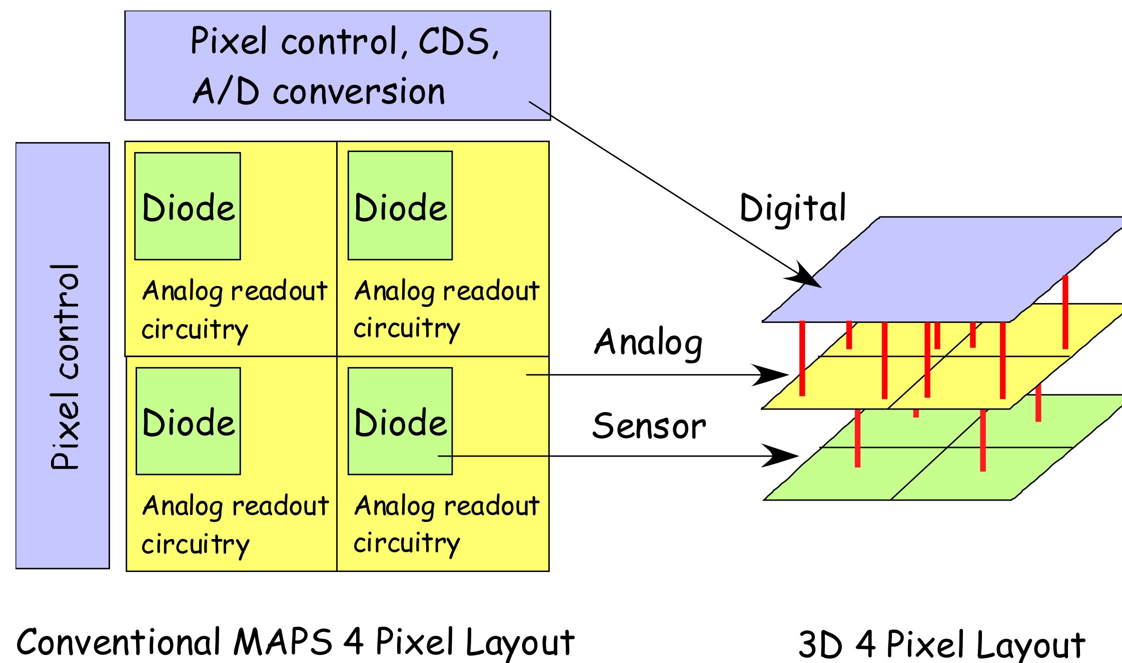
Physicist's Dream



2D Routing (large chip) 3D Routing (small chip)

Advantages of 3D for Pixels

1) More functionality is possible in a given area.
2) Unlike Monolithic Active Pixel Sensor designs,
a designer can freely use NMOS and PMOS devices
3) Processing of each layer (tier) can be optimized.
4) Perimeter logic can be greatly reduced.

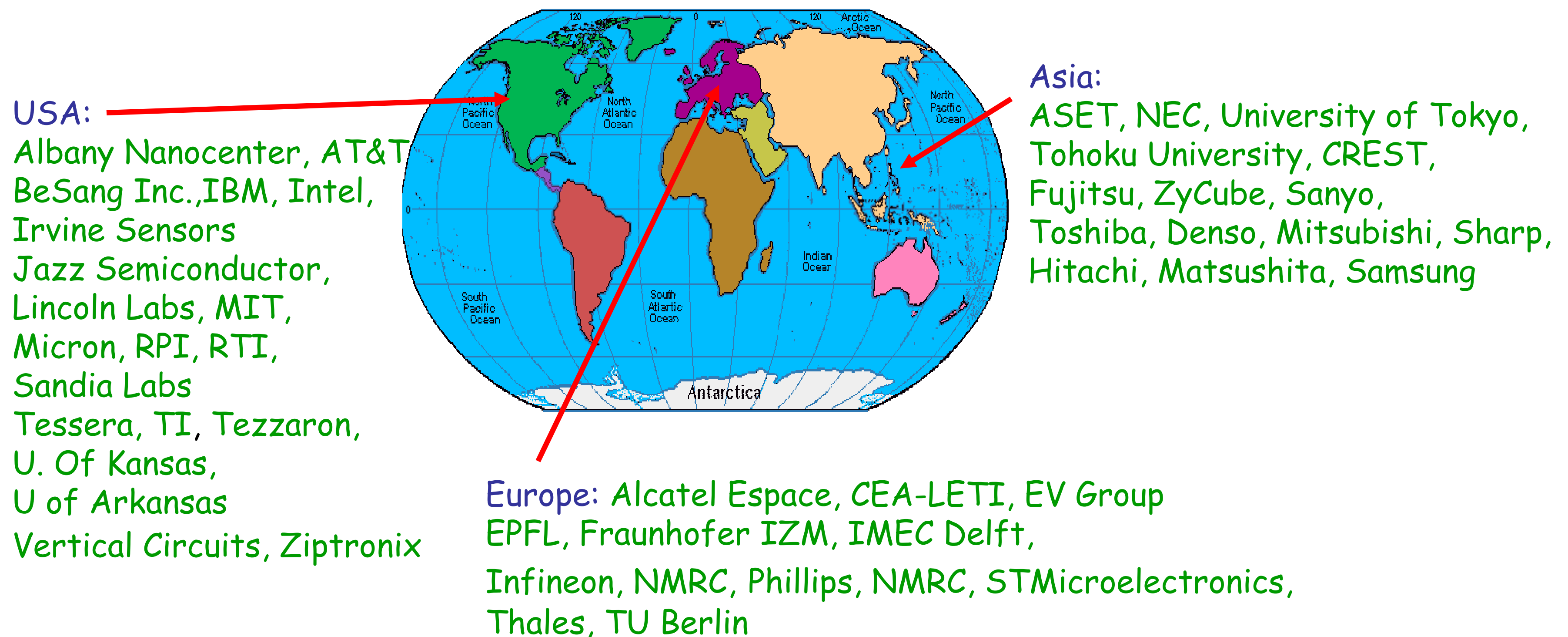


Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

3D Integrated Circuit Design

3D electronics development is being pursued by many different organizations.



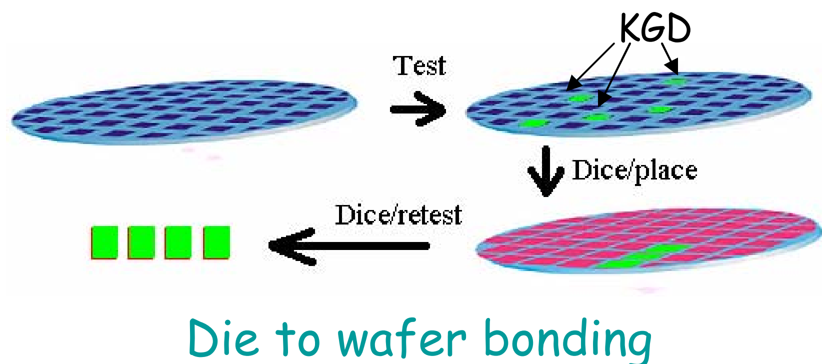
Two Different 3D Approaches for HEP

1) Die to wafer, (or die to die) bonding

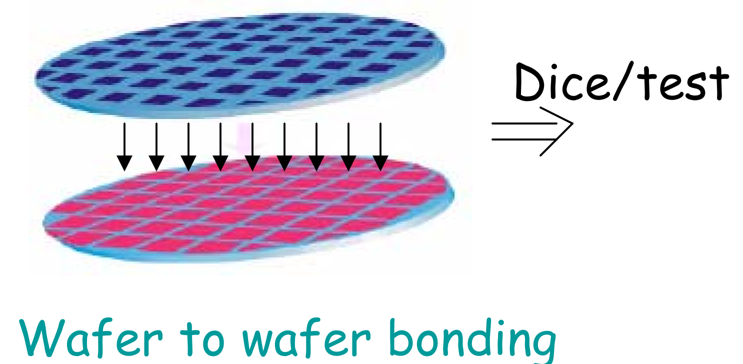
- Permits easy usage of different processes and different size wafers (SOI+CMOS, CCD+CMOS, DEPFET+CMOS)
- Lends itself to using KGD for higher yields

2) Wafer to wafer bonding

- Very thin layers for reduced mass
  - Short, small vias
- Layers must align at the wafer level



Die to wafer bonding



Wafer to wafer bonding

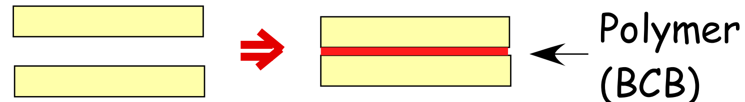
Key Technologies for 3D[5]

1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation
4) High precision alignment

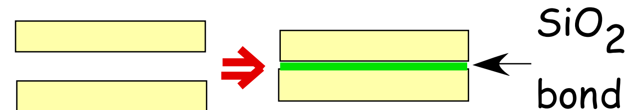
Key Technologies

1) Bonding between Die/Wafers

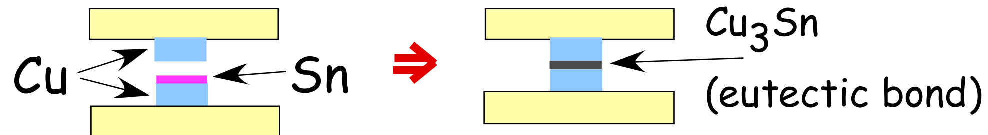
a) Adhesive bond



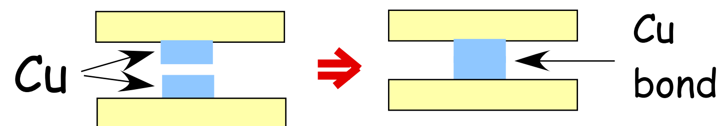
b) Oxide bond (SiO2 to SiO2)



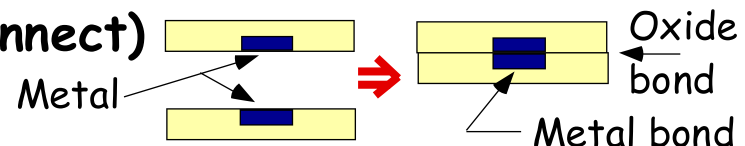
c) CuSn Eutectic



d) Cu thermocompression



e) DBI (Direct Bond Interconnect)

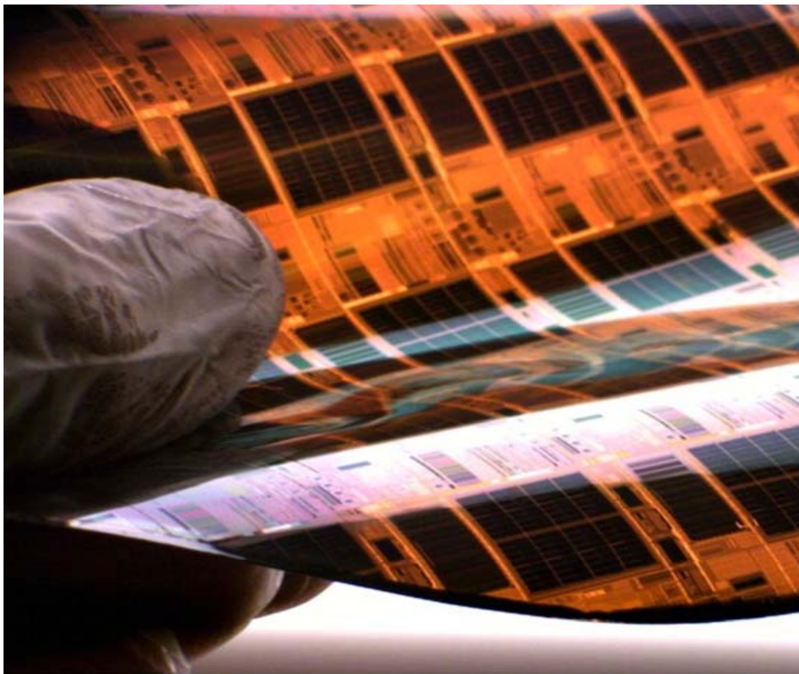


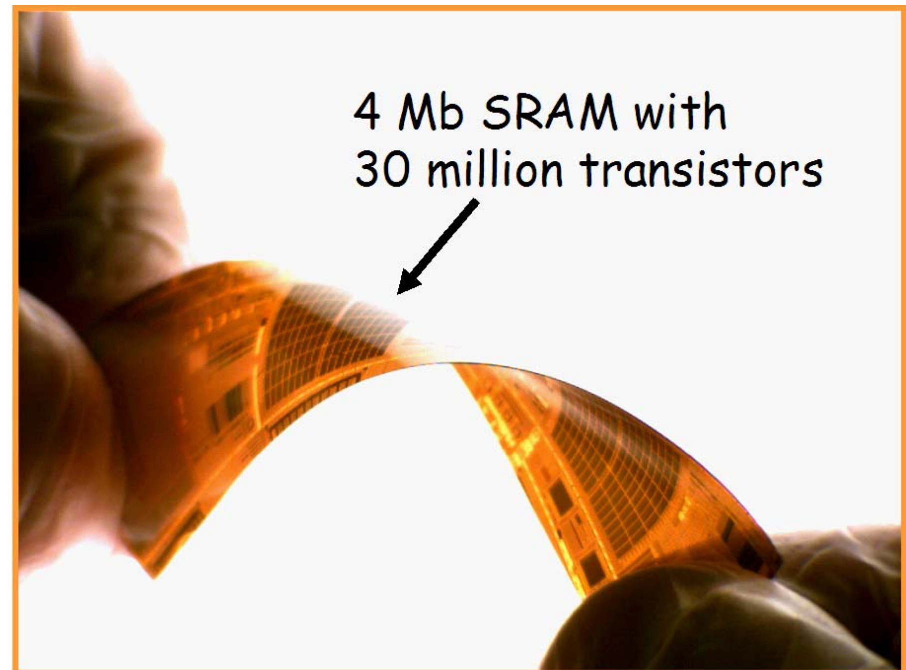
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

Key Technologies

2) Wafer thinning

Through wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area associated with the via as small as possible, the wafers should be thinned as much as possible. Thinning is typically done by a Combination of grinding, lapping, and chemical or plasma etching.





Six inch wafer thinned to 6 um and mounted to 3 mil kapton.

Key Technologies

3) Via formation and metalization

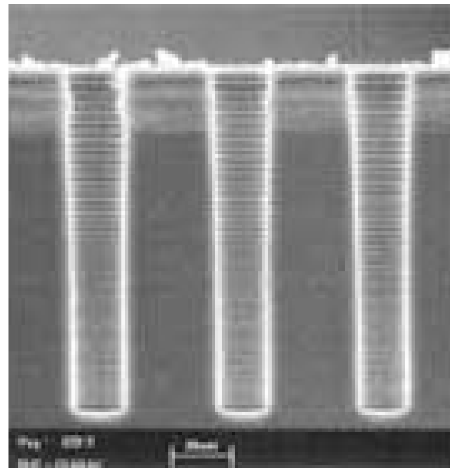
Two different proceedures are generally used:

Via First - vias holes and via metalization take place on a wafer before wafer bonding.

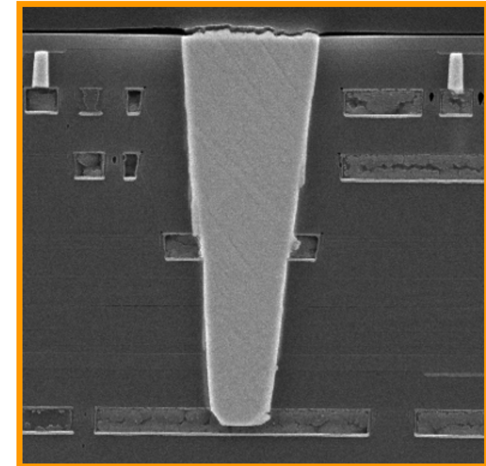
Via Last - vias holes and via metalization take place on a wafer after wafer bonding.

Vias in CMOS are formed using the Bosch process and must be passivated before filling with metal while Vias in SOI are formed using an oxide etch are filled without passivation.

SEM of 3 vias using Bosch process



Via using oxide etch process (Lincoln Labs)

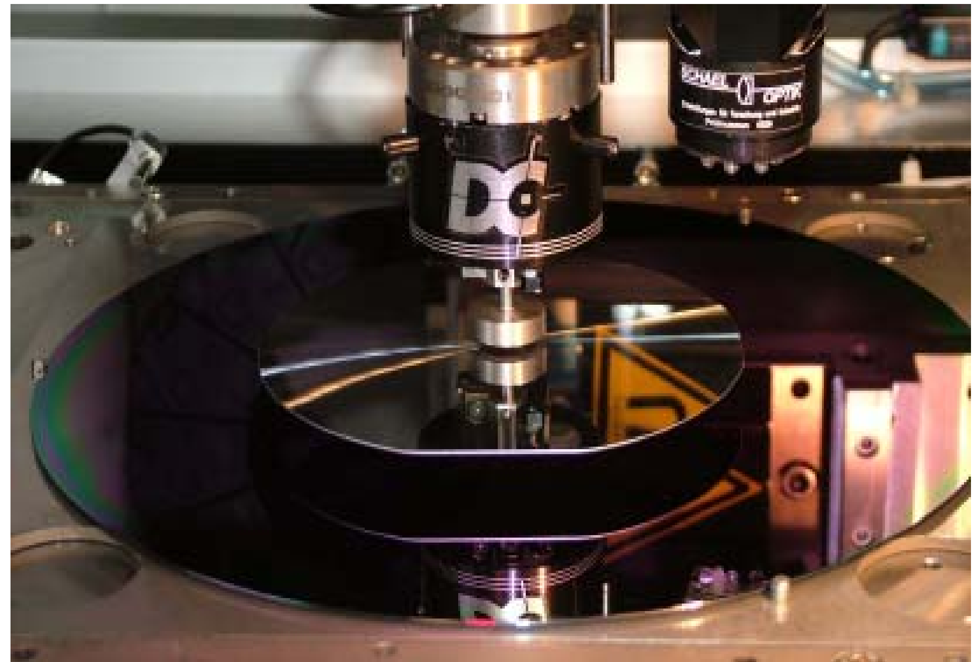


Key Technologies

4) High Precision Alignment

Alignment for both die to wafer and wafer to wafer bonding is typically better than one micron. (Photos by Ziptronix.)

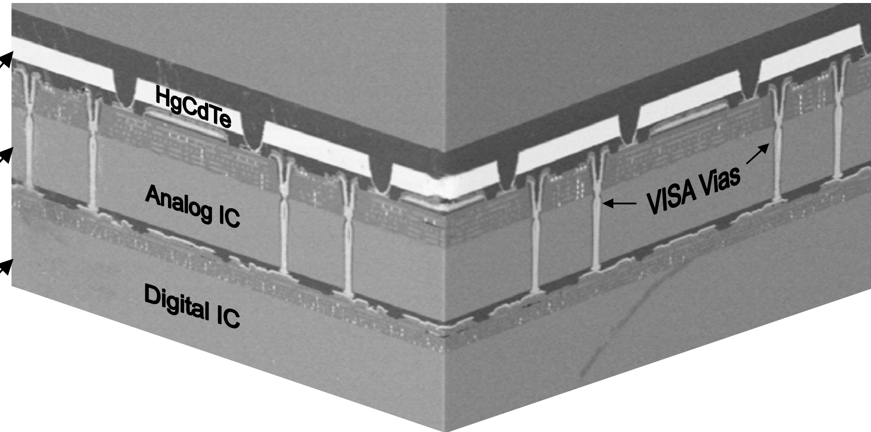
Die to Wafer alignment and placement



Wafer to Wafer alignment and placement

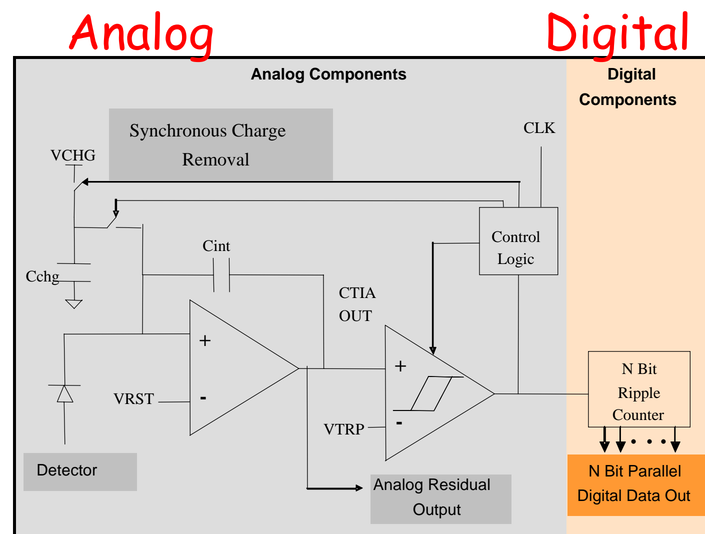
RTI 3D Infrared Array Example[6]

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section

Analog   Digital

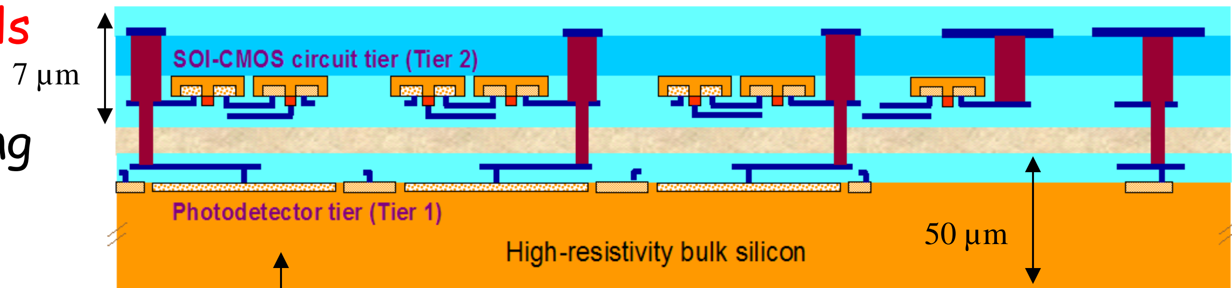


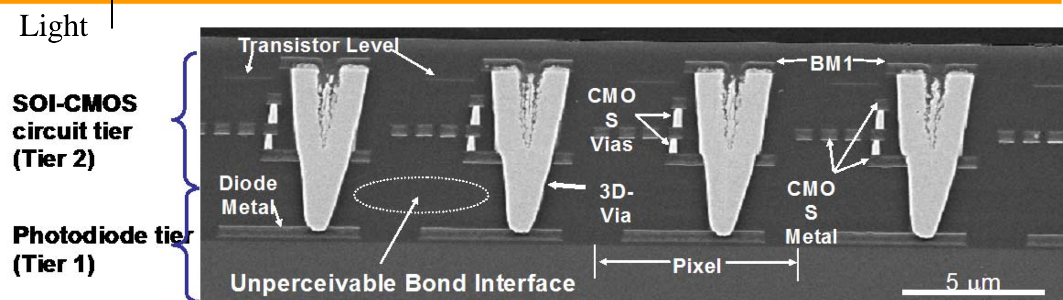
3 Tier circuit diagram

Infrared image

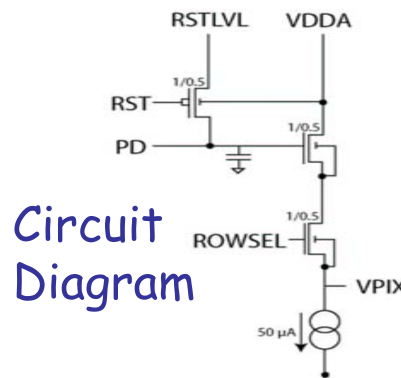
3D Megapixel CMOS Image Sensor[8]

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section

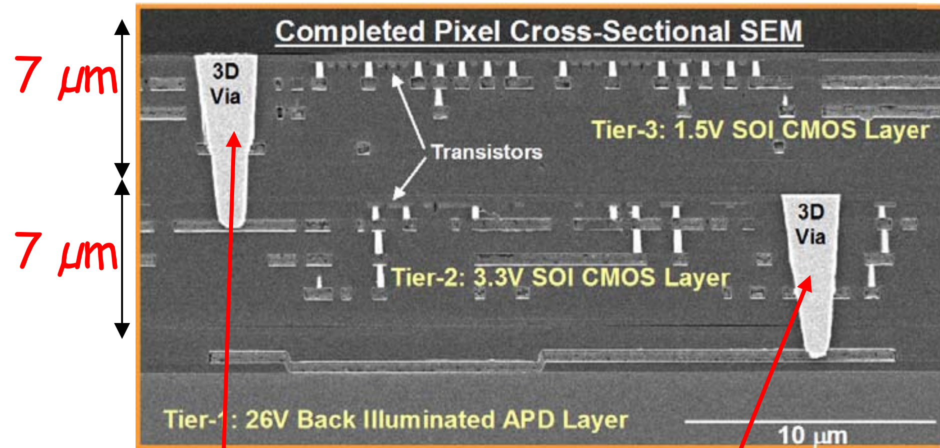


Circuit Diagram

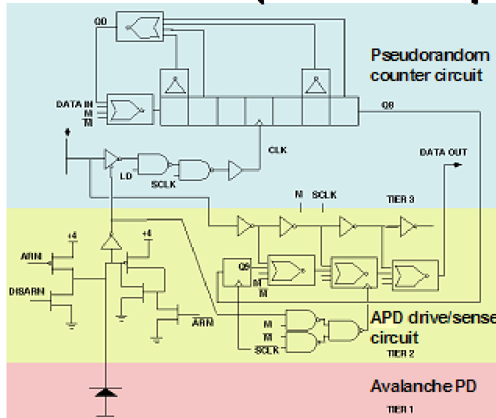
Image

3D Laser Radar Imager[9]

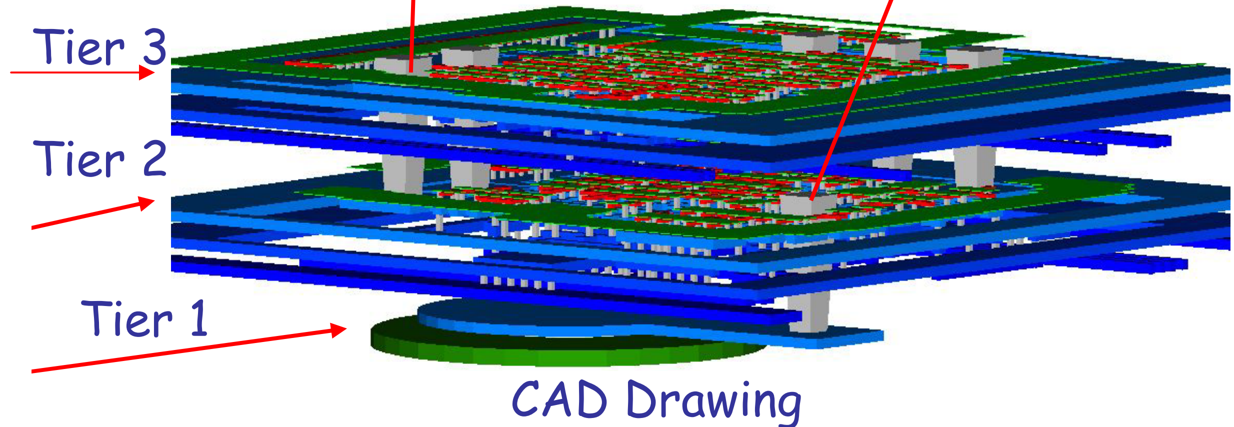
- 64 x 64 array, 50 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel



SEM Cross section



Schematic



CAD Drawing

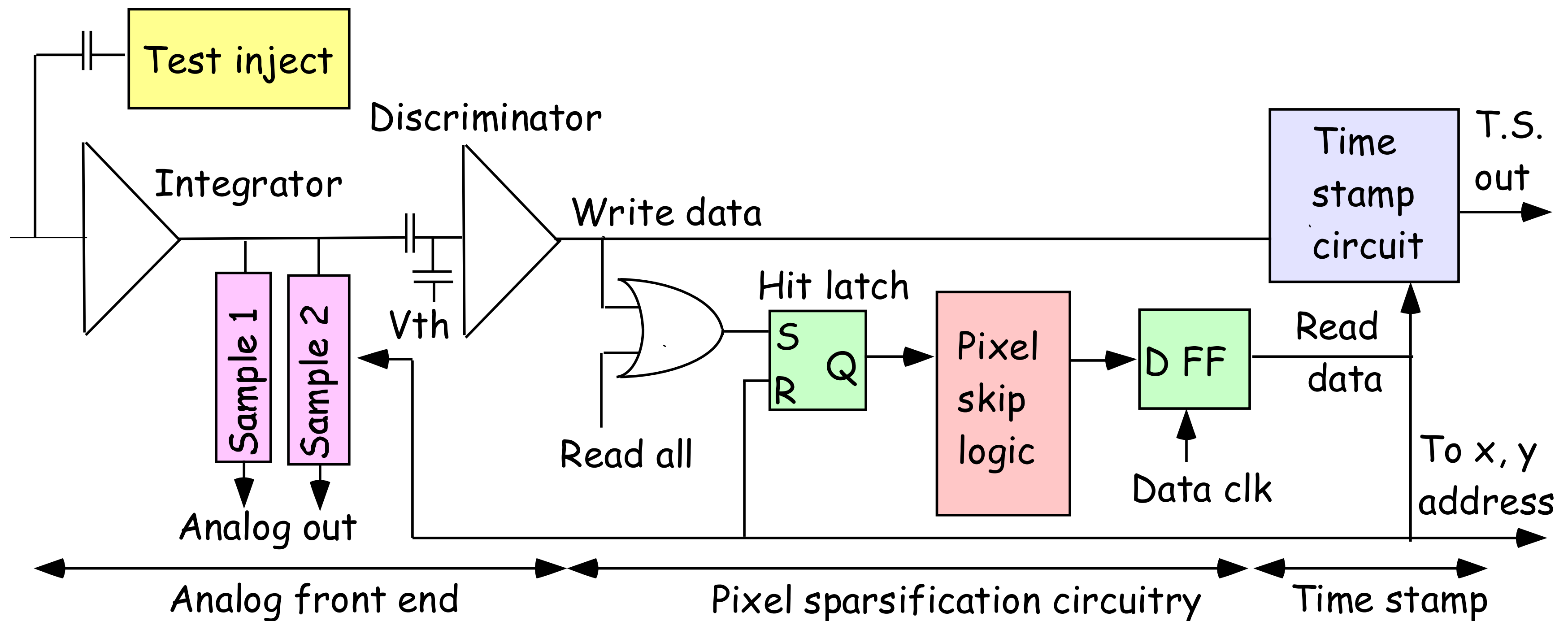
3D Demonstrator Chip for ILC Pixels

- ILC expected to have beam structure with 2820 crossings in a 1 msec bunch train with 5 bunch trains/sec.
- Maximum hit occupancy is about 250 hits/mm^2/train
  - Read out >99% of hits unambiguously
  - Have pixel resolution of 5 microns or better.
  - Include data sparsification on chip to reduce data and power.
  - Provide sufficient time stamping in order to easily reconstruct hits.

Demonstrator Chip Design Choices

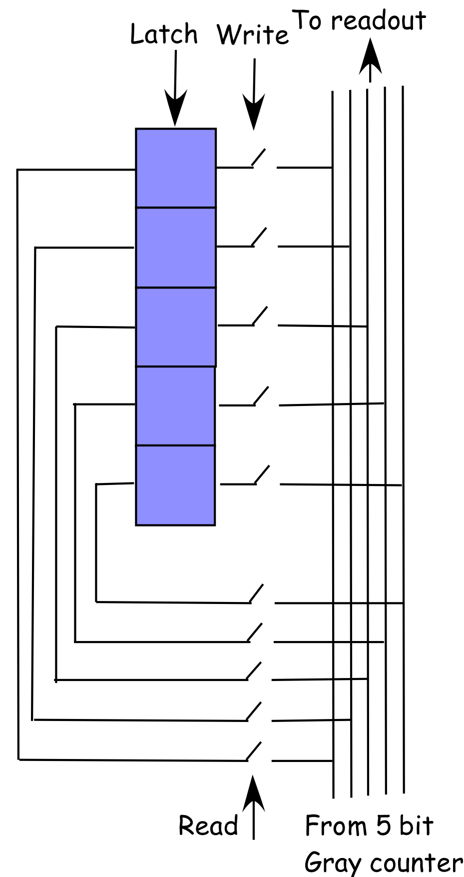
- Provide analog and binary readout information
- Divide the bunch train into 32 time slices. Each pixel stores one time stamp equivalent to 5 bits of time information.
- Store the time stamp in the hit pixel cell.
- Use token passing scheme with look ahead feature to sparsify data output.
- Store pixel address at end of row and column.
- Divide chip design into 3 tiers or layers of ROIC
- Make pixel as small as possible but with significant functionality.
- Design for 1000 x 1000 array but layout only for 64 x 64 array.
- Submit to Lincoln Lab multi-project run without detector substrate.

Simplified Pixel Cell Block Diagram



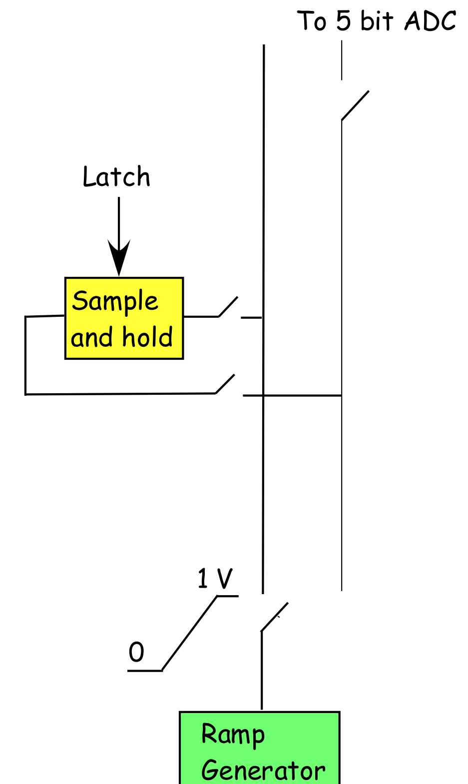
Pixel Time Stamping

- Various MAPS schemes for ILC have suggested 20 time stamps to separate hits in the 2820 bunch train.
- ILC 3D chip has 32 time stamps.
- Time stamp can be either analog or digital.
- ILC demonstrator chip will have both



Counter operates at a slow speed, 32 KHz, (30 usec/step)

All digital - 10 transistors/bit

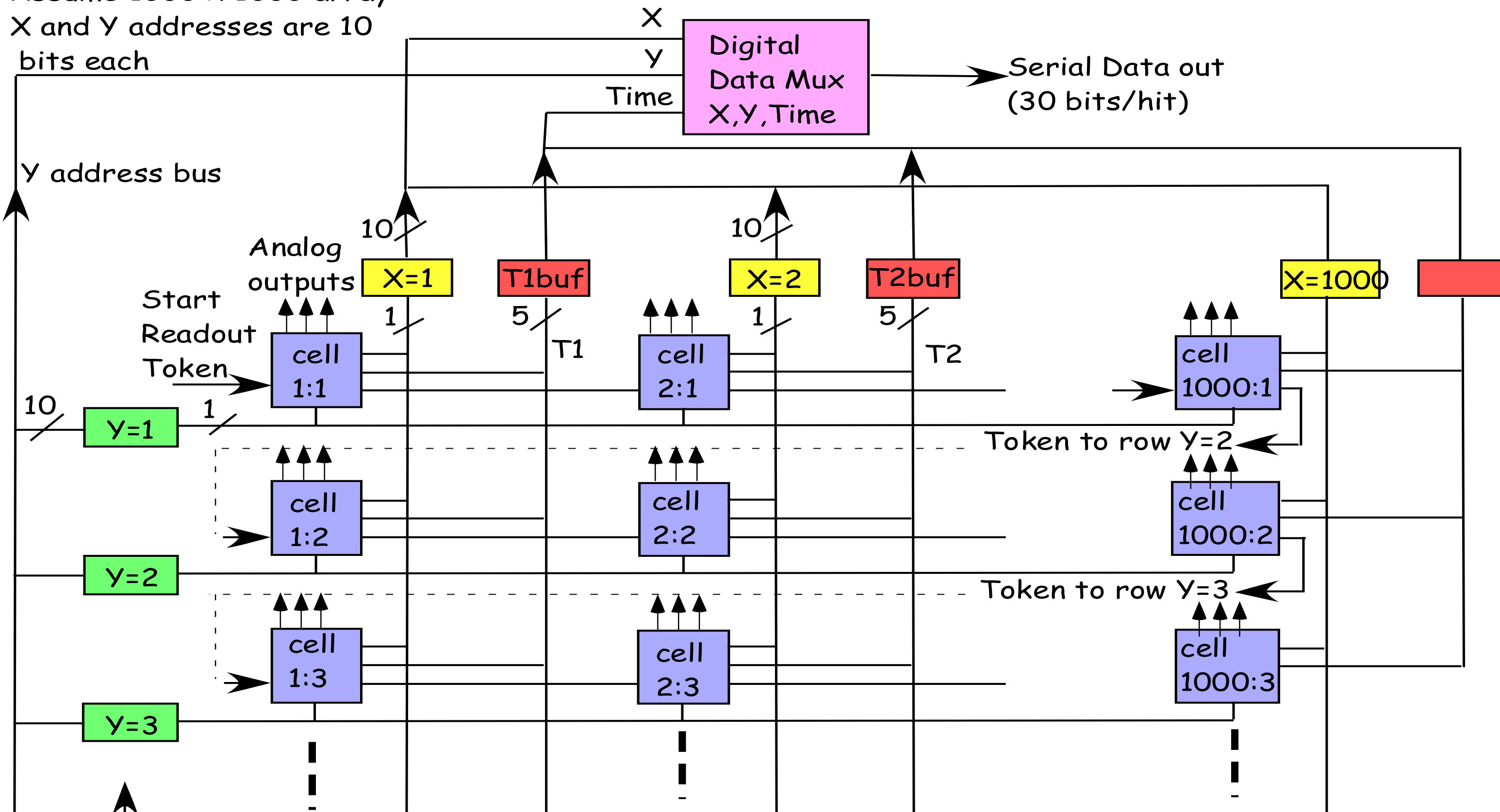


Ramp operates at low speed for low power.

Analog approach - fewer transistors

Pixel Readout Scheme

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out.
- During pixel readout, token scans ahead for the next hit pixel



Sparsified Readout Operation

- During data acquisition, a hit sets a latch.
- Sparse readout performed row by row.
- To start readout, all hit pixels are disabled except the first hit pixel in the readout scan.
- The pixel being read points to the X address and Y address stored on the perimeter and at the same time outputs the Time Stamp and analog information from the pixel.
- While reading out a pixel, a token scans ahead looking for next pixel to readout.
- Chip is set to always readout at least one pixel per row in the array.
- Assume 1000 x 1000 array (1000 pixels/row)
  - Time to scan 1 row = .200 ns x 1000 = 200 ns (simulated)
  - Time to readout cell = 30 bits x 20 ns/bit = 600 ns
  - Plenty of time to find next hit pixel during readout

Readout Time Example

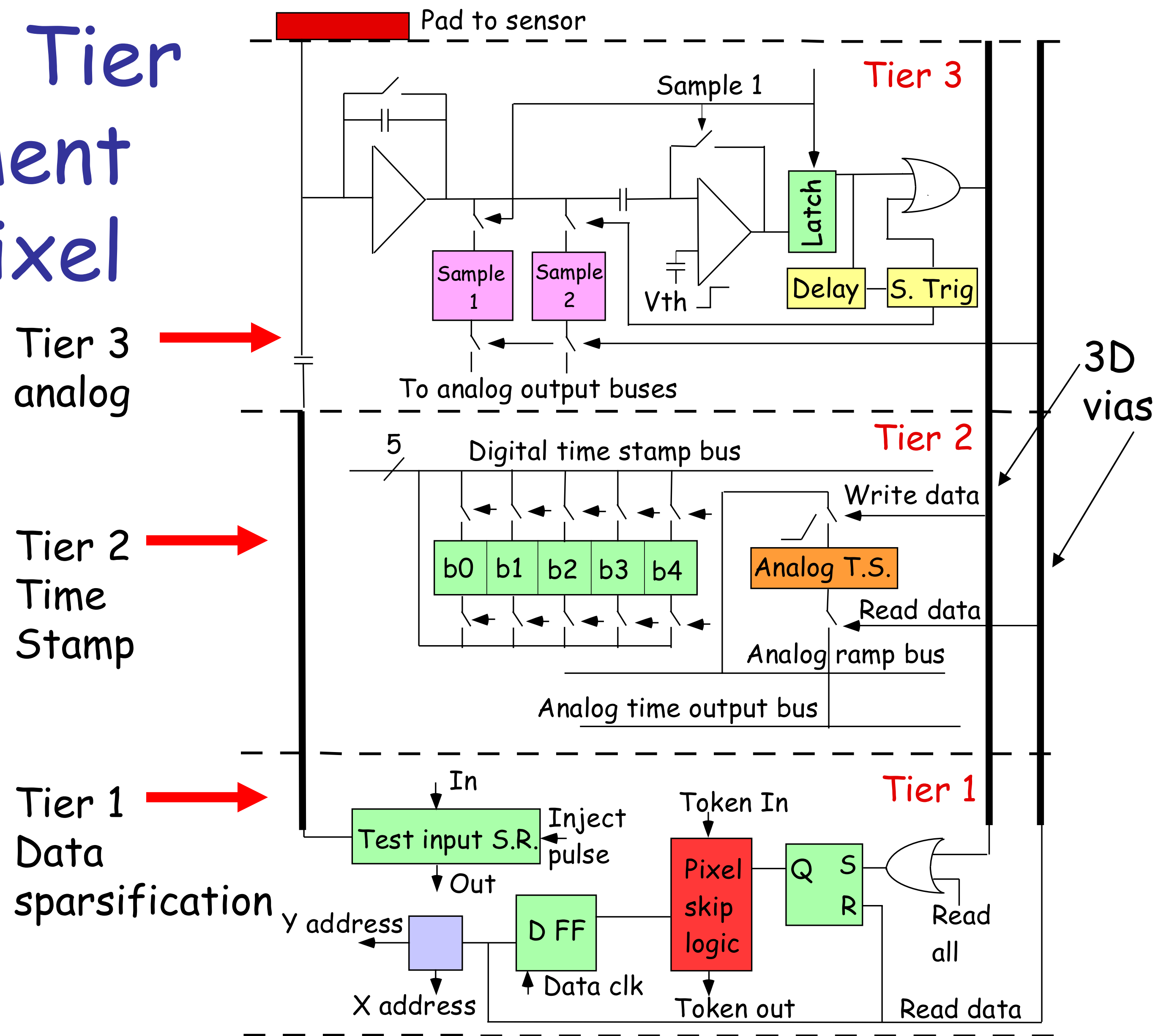
- Chip size = 1000 x 1000 pixels with 15 um pixels.
- Max hits/chip = 250 hits/mm^2 x 225 mm^2 = 56250 hits/chip.
- If you read all pixels with X=1, add 1000 pixels (small increase in readout data).
- For 50 MHz readout clock and 30 bits/hit, readout time = 57250 hits x 30 bits/hit x 20 ns/bit = 34 msec.
- For a 1000 x 1000 array of 20 um pixels, the readout time is 60 msec.
- Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips.
- Digital outputs are CMOS. The output power is only dependent on the number of bits and not the length of time needed to readout.

3D Three Tier Arrangement for ILC Pixel

Tier 3 analog

Tier 2 Time Stamp

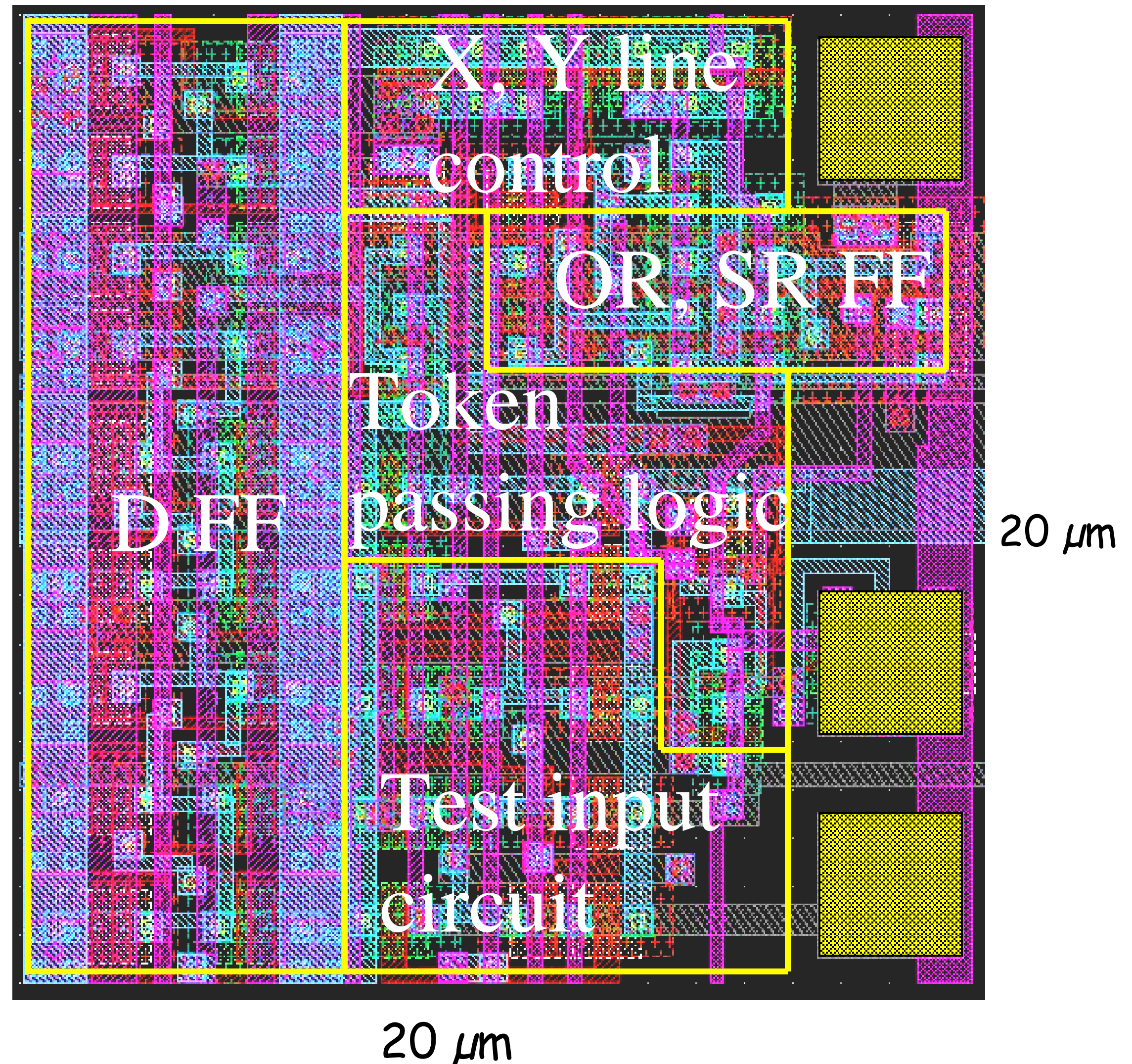
Tier 1 Data sparsification



Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff

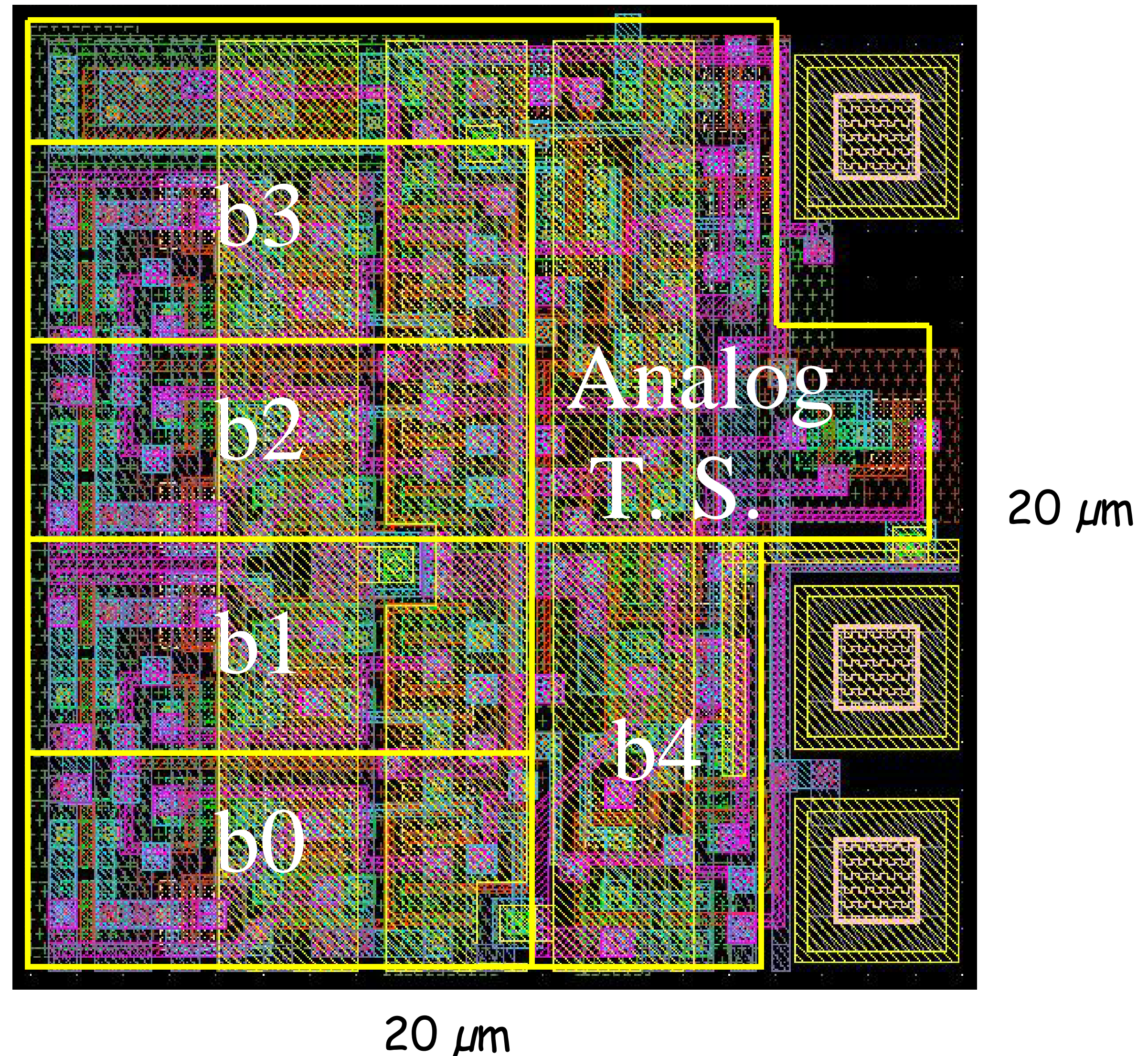
Sparsification Tier 1

- OR for READ ALL cells
- Hit latch (SR FF)
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



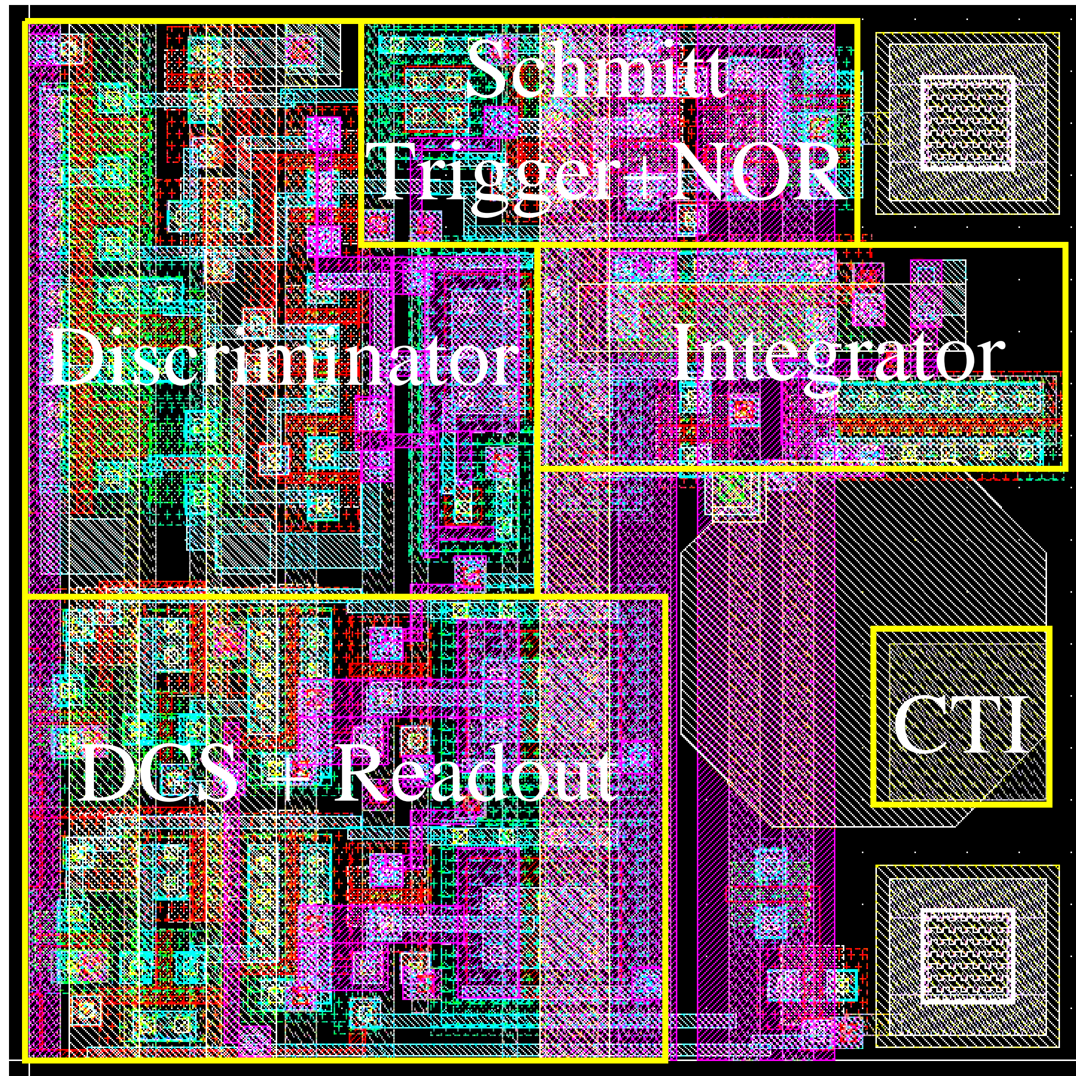
Time Stamp - Tier 2

- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Either analog or digital T. S.to be used in final design.
- Gray code counter on periphery
- 72 transistors
- 3 vias

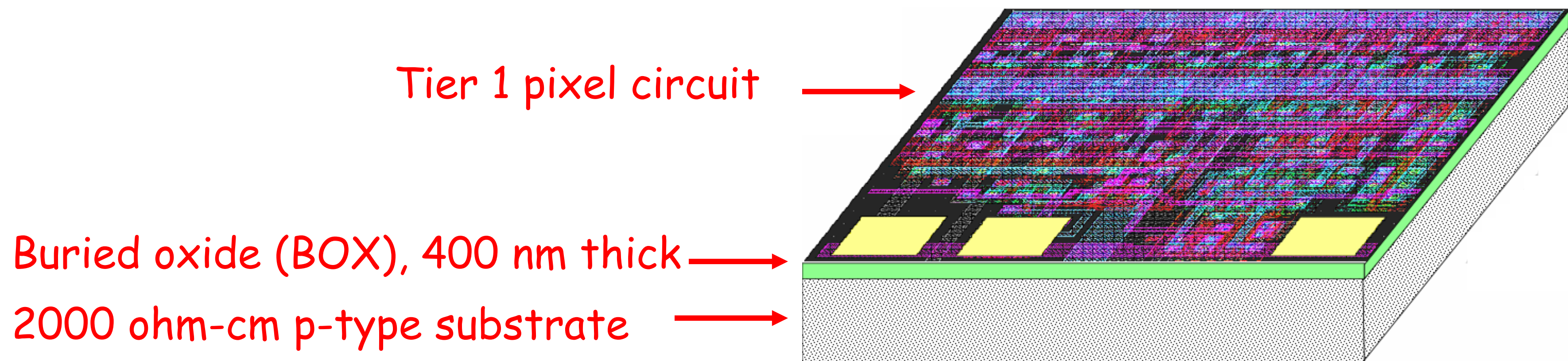


Analog Tier 3

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input (CTI)
- 38 transistors
- 2 vias

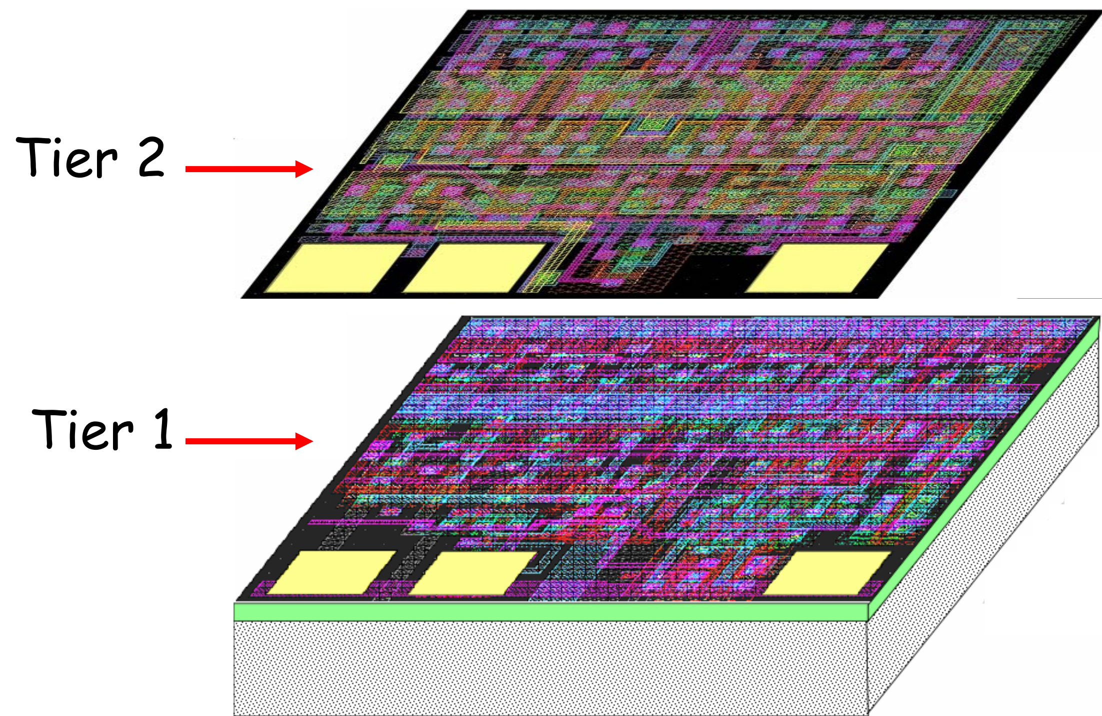


3D Stacking with Vias (step 1)



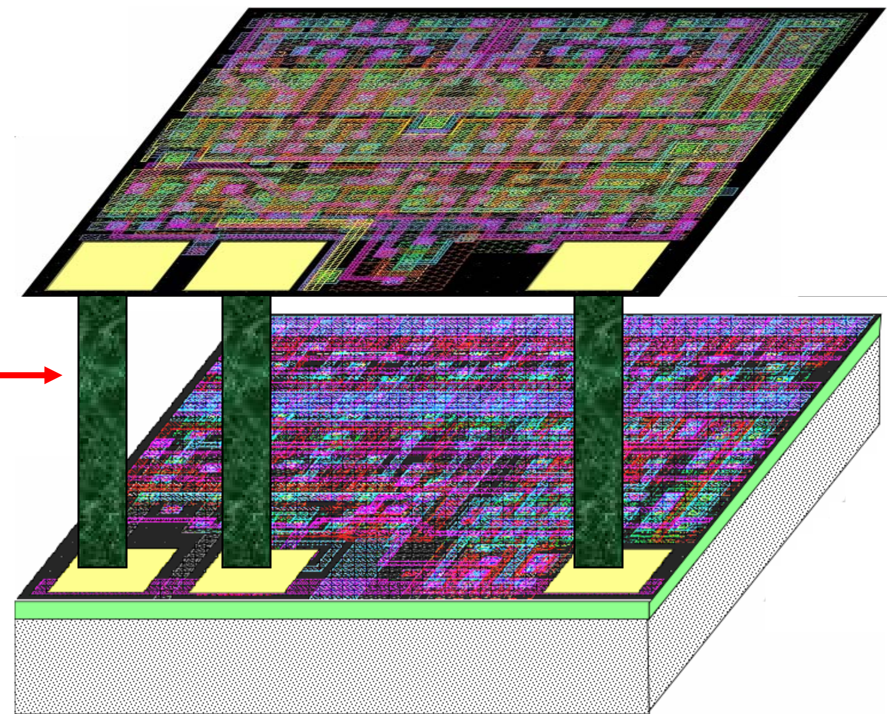
3D Stacking with Vias (step 2)

Bond tier 2 to tier 1



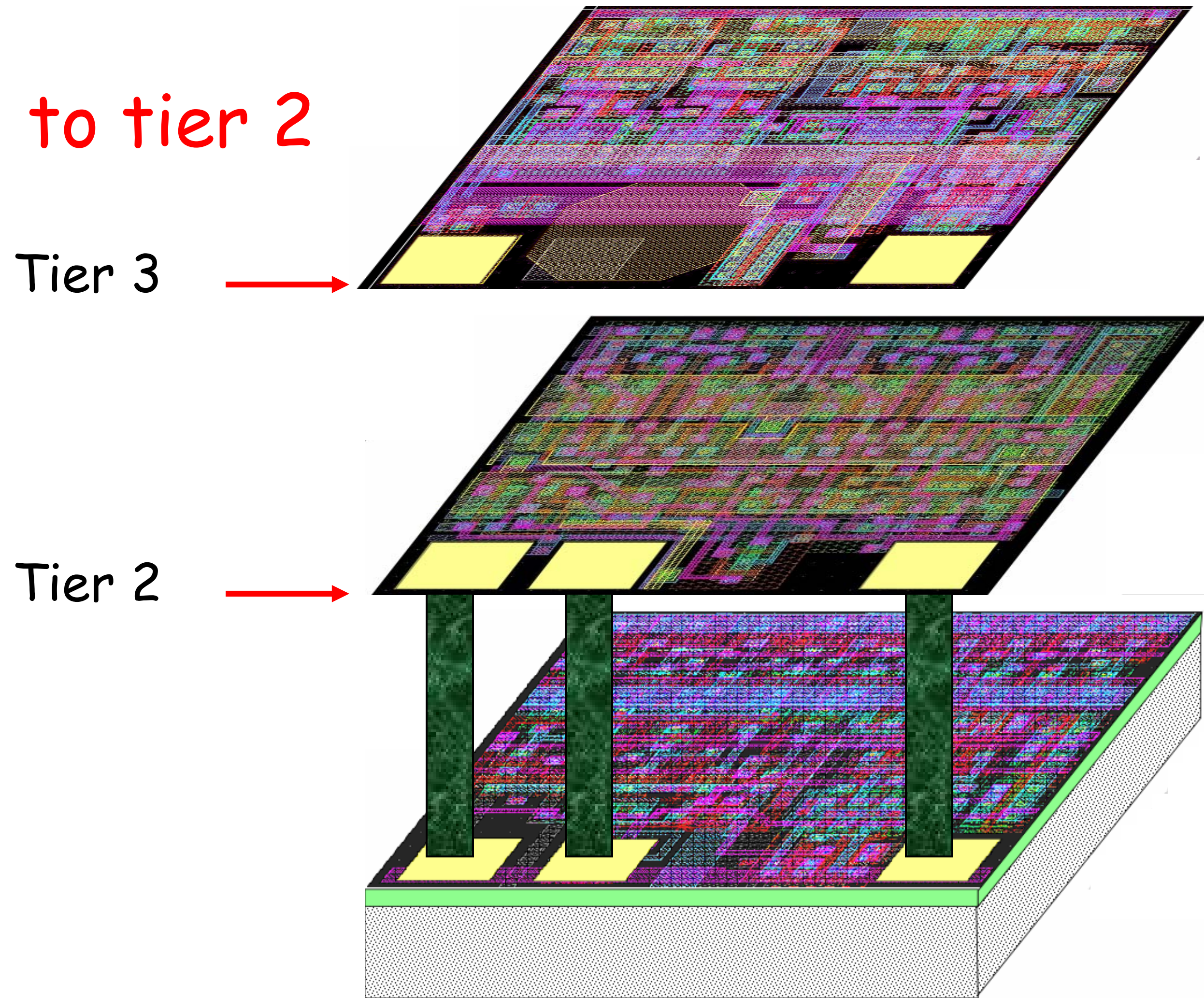
3D Stacking with Vias (step 3)

Form 3 vias, 1.5 x 7.3 μm, through Tier 2 to Tier 1



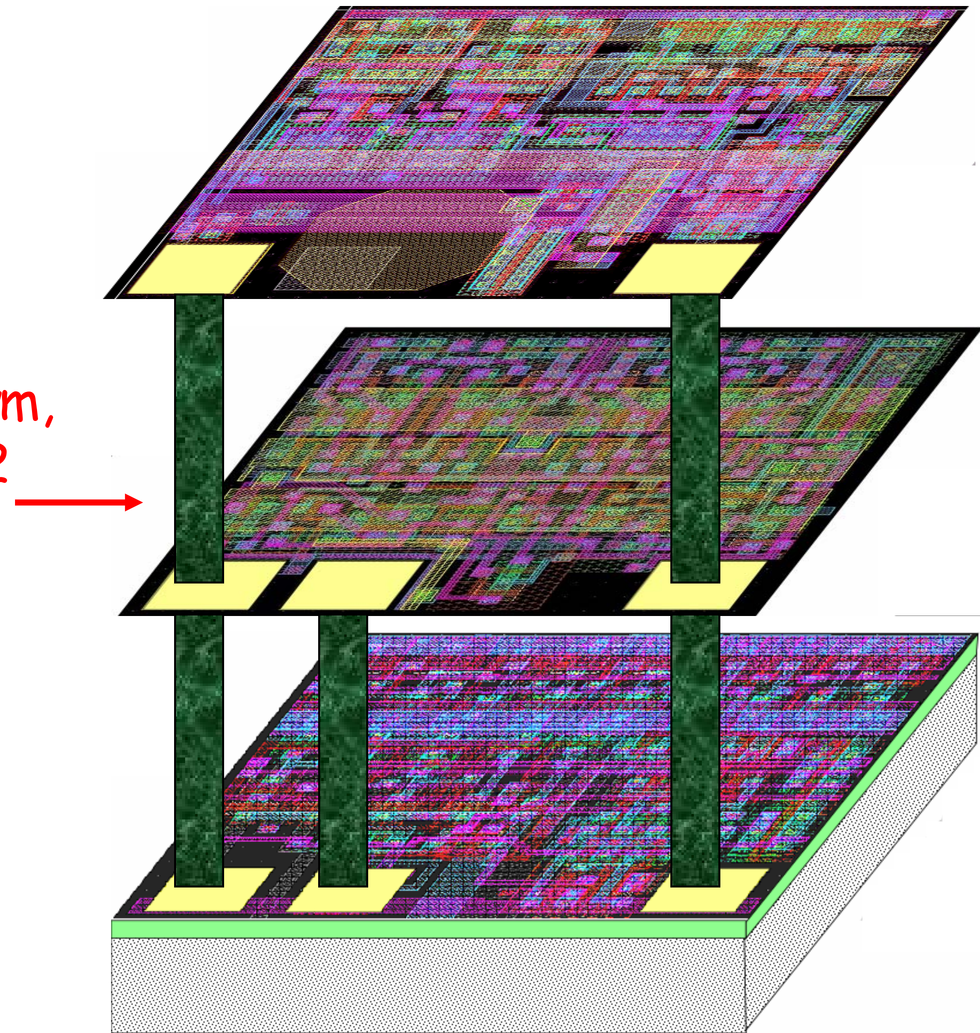
3D Stacking with Vias (step 4)

Bond tier 3 to tier 2



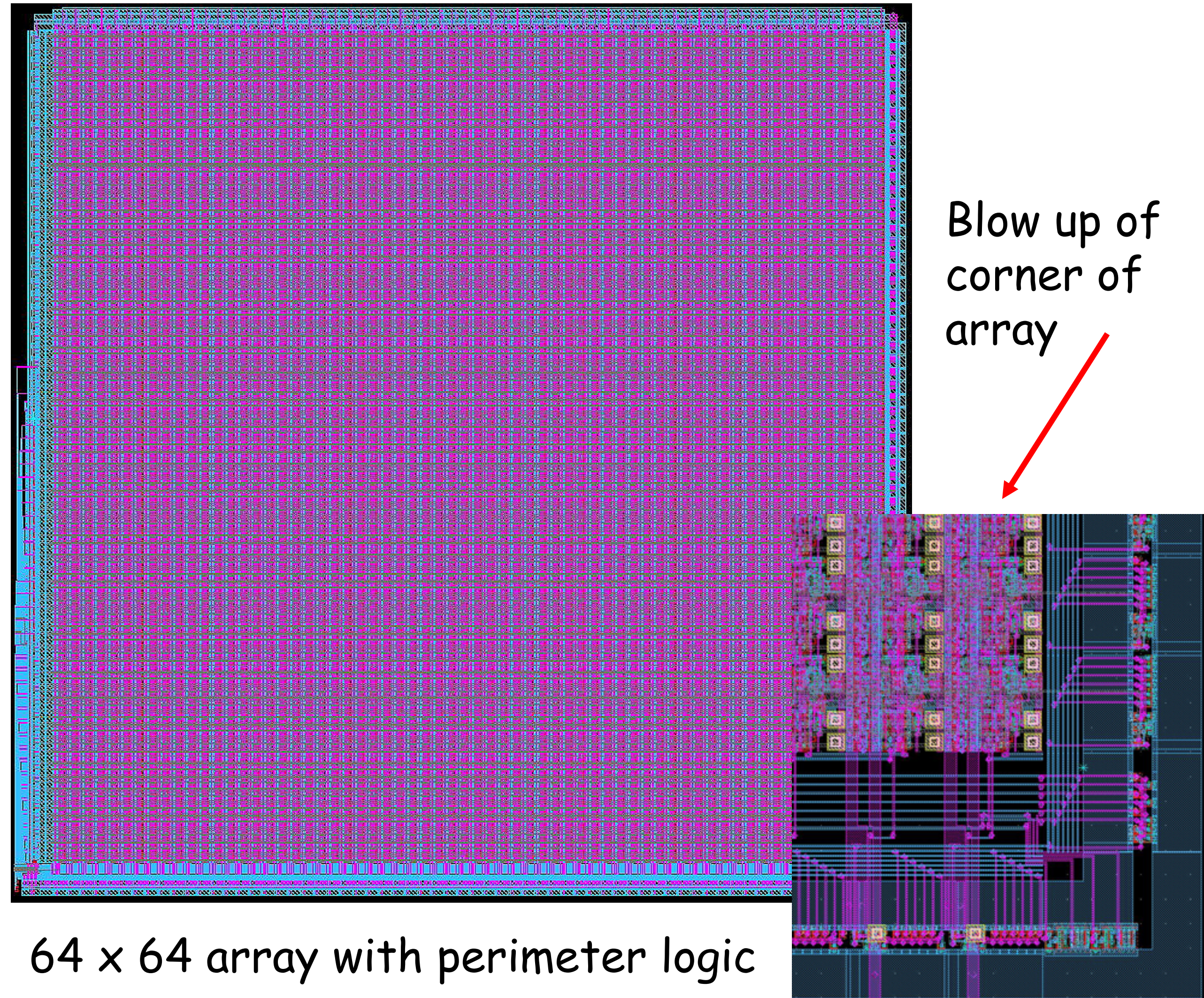
3D Stacking with Vias (step 5)

Form 2 vias, 1.5 x 7.3 μm, through tier 3 to tier 2



Perimeter Logic

- Perimeter circuitry for the ILC Demonstrator chip occupies a small amount of space.
- Area for the perimeter logic could be reduced in future designs.

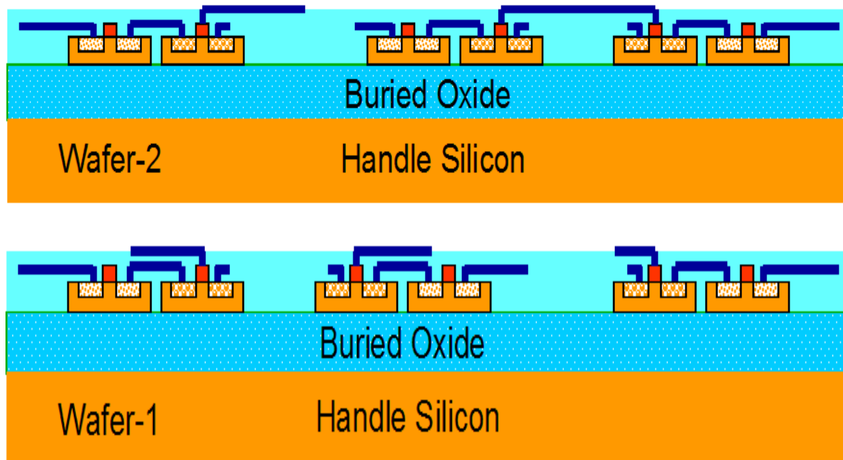


64 x 64 array with perimeter logic

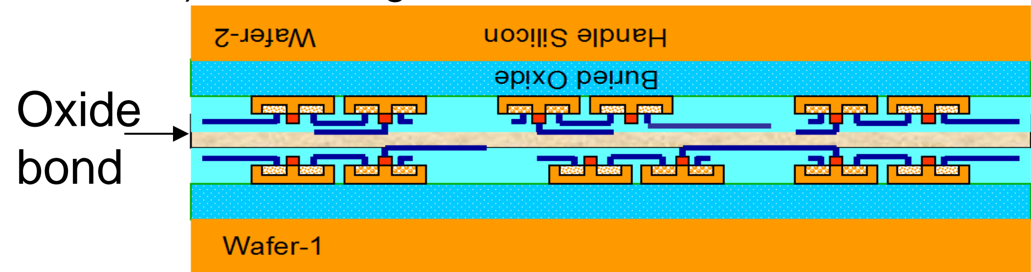
Lincoln Labs 3D SOI Process Flow used for ILC Chip[10]

- 3 tier stacking
- 6 inch 0.18 um SOI wafers

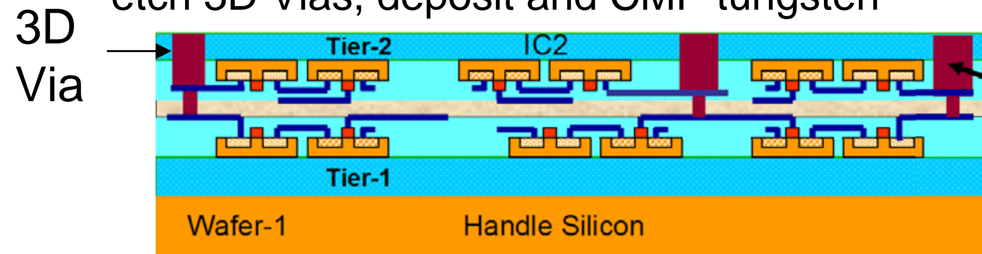
1) Fabricate individual tiers



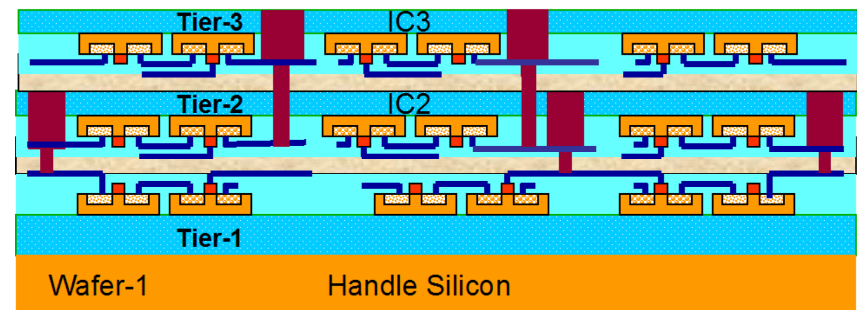
2) Invert, align, and bond wafer 2 to wafer 1



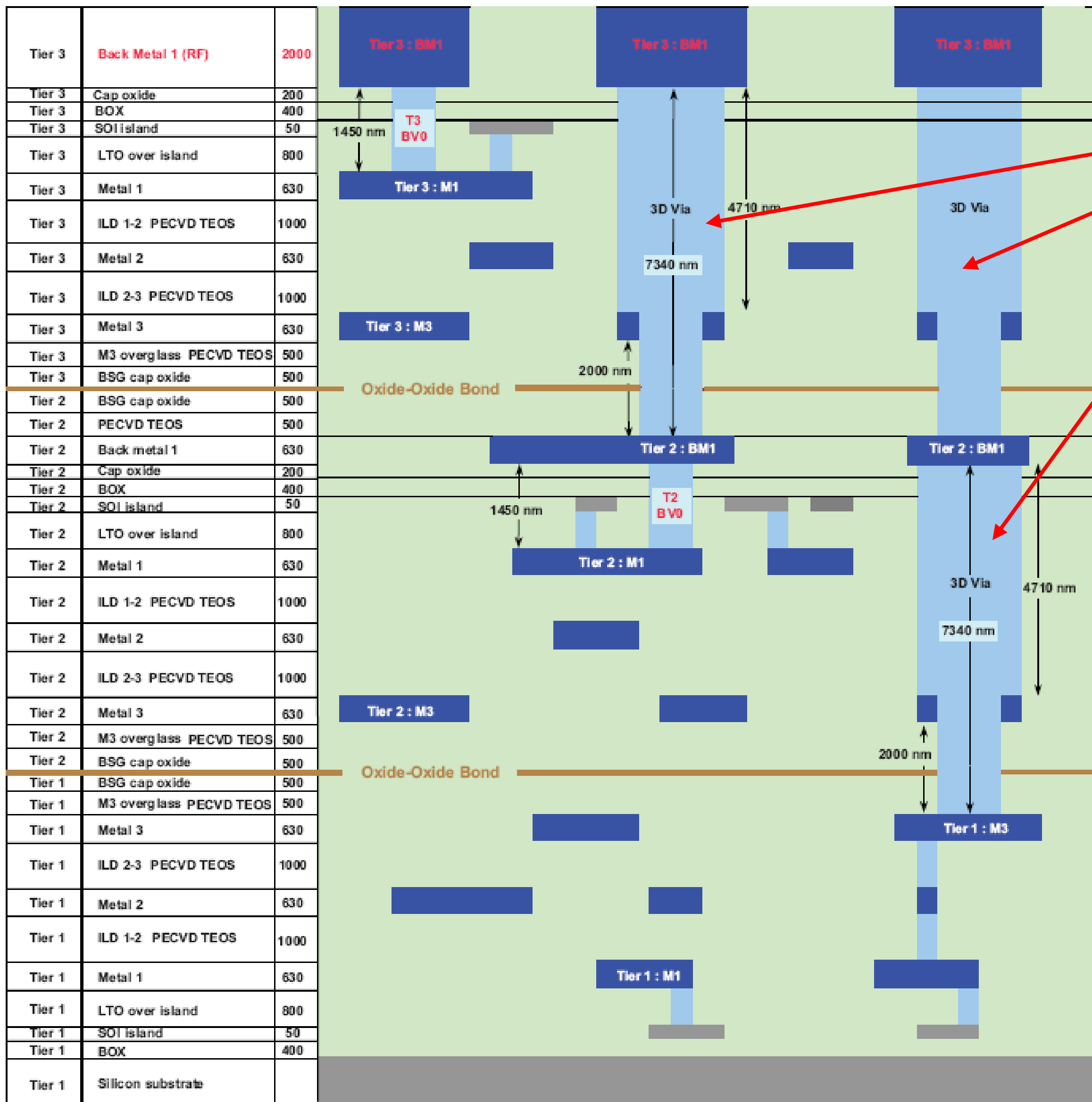
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



MIT LL 3D Multiproject Run



Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	

3D vias

8.2 µm

7.8 µm

6.0 µm

Three levels Of transistors, 11 levels of metal in a total vertical height of only 22 um.

Demonstrator Chip Summary

- Multi functional device used as a proof of concept
- 64 x 64 array that can be expanded to 1000 x 1000.
- 175 transistors in 20 micron pixels
- 3 tiers of transistors with an active circuit thickness of 22 microns
- Pulse height information (analog output) may not be required in the final design
- Sparsification with look ahead skip speed of 200 ps/cell for token passing.
- Two types of time stamping (only one chosen for the final application). 32 time stamps available, can be expanded to 64.
- Test input for every cell. Can be expanded to include a disable for every cell with little or no increase in size.

Demonstrator Chip Summary (con't)

- Serial digital output on one line
- Small peripheral circuitry.
- Chip power dissipation set by analog needs
  - For air cooling, power should not exceed 20 $\mu w/mm^2$
  - Assuming 1/200 duty cycle for analog power, the power of the demonstrator chip is estimated to be 18.75 $\mu w/mm^2$.
- Noise is expected to be in the range of 20-30 e- when connected to the detector.
- Multi-project submission date October 1

3D IC Advantages

- Increased circuit density without going to smaller feature sizes
  - ILC demonstrator has 175 transistors in a 20 μm pixel
- Unlimited use of PMOS and NMOS transistors
- 100% diode fill factor
- SOI Advantages
  - High resistivity substrate for diodes provide large signals
  - Minimum charge spreading with fully depleted substrate
  - Inherently isolated vias
- 3D may be used to add layers above other sensors types currently under development.

Summary

- There are many group world wide studying MAPS in CMOS processes.
- Fermilab is currently investigating various SOI processes that have advantages over conventional MAPS
  - SOI Detectors
    - OKI
    - ASI
  - Vertical scale integration (3D)
    - MIT Lincoln Labs
    - Others
- Potential applications include ILC, SLHC, etc.

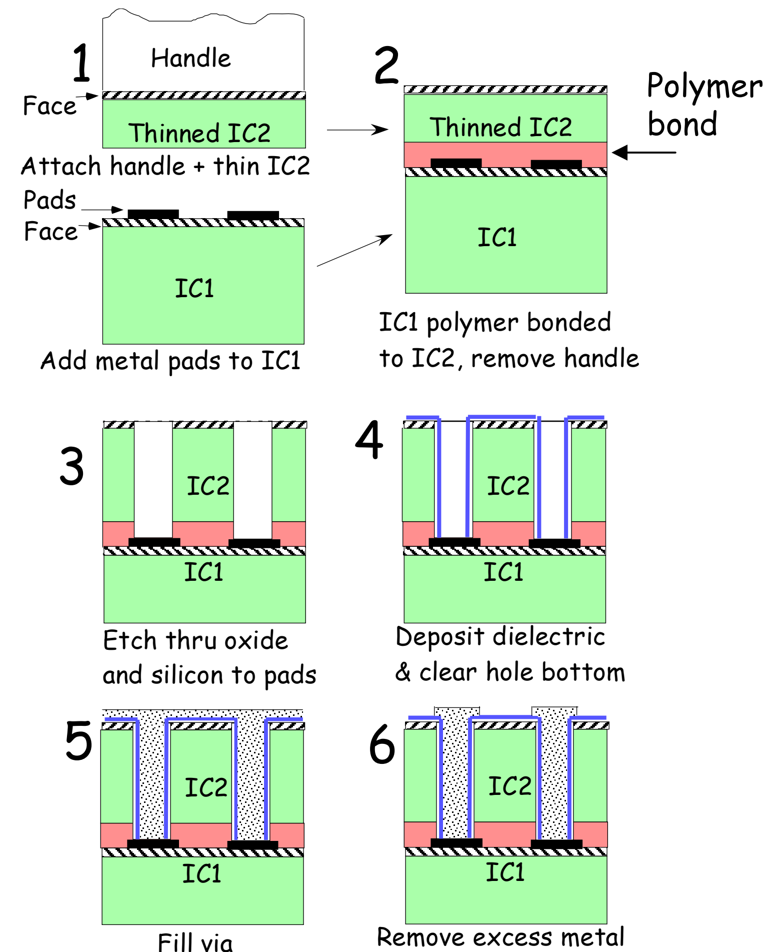
References

- 1) R. Turchetta, et. al., "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology," Nucl. Instrum. Meth. A 458, pp 677-689, Jan. 2001.
- 2) G. Deptuch, et. al., "Design and Testing of Monolithic Active Pixel Sensors for Charged particle Tracking," IEEE Trans. on Nucl. Sci., vol 49, No 2, pp 601-610, April 2002.
- 3) J. Marczewski, et. al., "SOI Active Pixel Detectors of Ionizing radiation – Technology and Design Development," IEEE Trans. On Nucl. Sci., vol 51, No 3, June 2004, pp. 1025 – 1028.
- 4) Y. Arai, et. al., "First Results of 0.15 um CMOS SOI Pixel Detector," SNIC Symposium, Stanford, Califorina, April 3-6, 2006.
- 5) R. Yarema, "3D Integrated Circuits for HEP," Sixth International Meeting on Front End Electronics, Perugia, Italy , May 17- 20, 2006
- 6) C. Bower, et. al., "High Density Vertical Interconnects for 3D Integration of Silicon ICs," 56th Electronic Components and Technology Conference, San Diego, May 30-June 2, 2006
- 7) A. Klumpp, "3D System Integration," Sixth International Meeting on Front End Electronics, Perugia, Italy, May 17-20, 2006.
- 8) V. Suntharalingam, et. al., Megapixel CMOS Image Sensor Fabricated in Three-dimensional Integrated Circuit Technology," IEEE SSCC 2005, pp356-7.
- 9) B. Aull, et. al., "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing layers," IEEE SSCC 2006, pp. 26-7.
- 10) C. Keast, et. al., "MIT Lincoln Laboratory's 3D Circuit Integration technology Program," 3D Architectures for Semiconductor Integration and Packaging," Tempe AZ, June 13-15 2005
- 11) C. Baltay, "Monolithic CMOS Pixel Detectors for ILC vertex Detection," 2005 International Linear Collider Workshop, Stanford, CA, March 18-22, 2005

Back up Slides

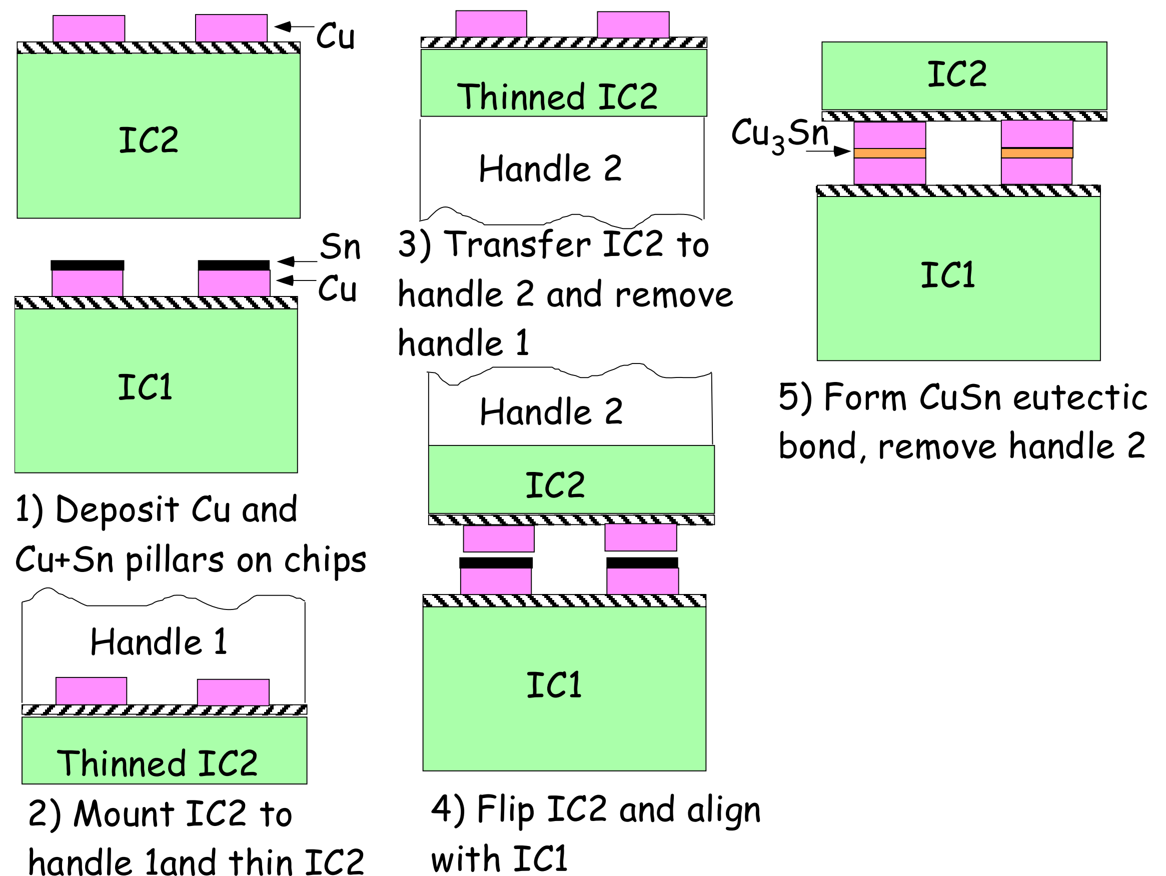
Die to Wafer (back to face)

- Need to leave space in design for vias
- Thin die before bonding (1)
- Polymer bond between parts (2)
- High aspect ratio via Bosch process (3)
- Insulated vias needed for CMOS (4)
- Low temperature via metalization needed to protect polymer bond (5,6)
- Variations of this process are found in different groups (copper vias)

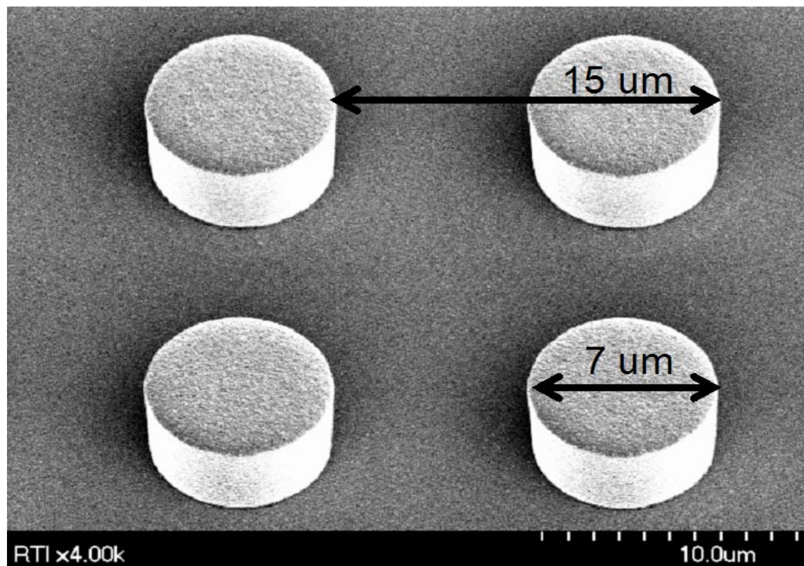


Cu/Sn Bond process

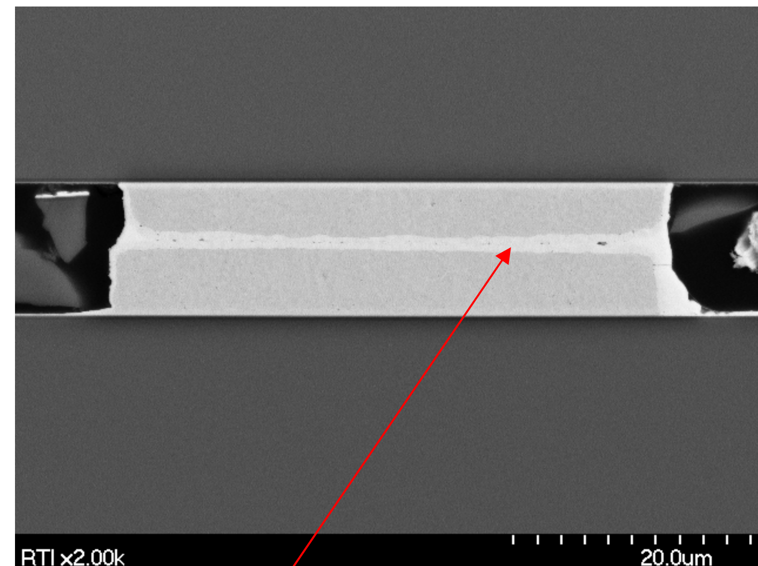
- Cu pillar placed on face of one device and copper pillar with Sn on other (1).
- Requires double handle wafer transfer (2, 3).
- Cu and Sn form eutectic bond between devices (4, 5)
- Variations of this process are found in different groups
- Process is compatible with standard CMOS processing



Fine Pitch CuSn Pillars from RTI for Bonding Along with Cross Section to Show Eutectic Bond

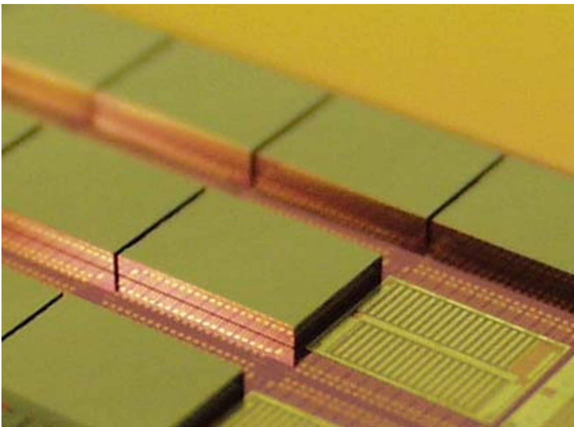


5 micron tall Cu pillars

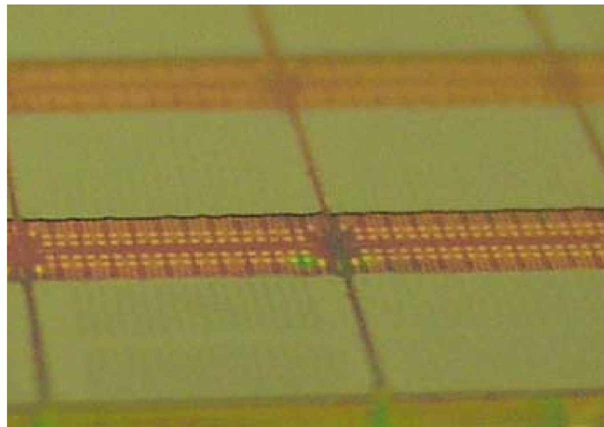


Cross section of bond showing Cu_3Sn eutectic

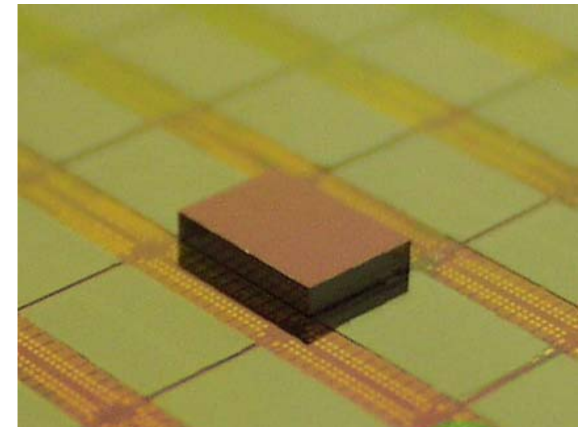
Thinned Die Photos from IZM[7]



500 μm thick chips placed on target Substrate using CuSn eutectic bond



Chips thinned to 10 μm on target substrate



500 μm chip placed on top of 10 μm thick chips for comparison.

3D Demonstrator Chip for ILC Pixels

- ILC expected to have beam structure with 2820 crossings in a 1 msec bunch train with 5 bunch trains/sec.
- ILC Maximum hit occupancy
  - Assumed to be 0.03 particles/crossing/mm^2
  - Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)
  - Hit rate = 0.03 part./bco/mm^2 x 3 hits/part. x 2820 bco/train = 252 hits/train/mm^2. [11]
- Study analog and binary read out approach
  - Want better than 5 μm resolution
  - Binary readout
    - 15 um pixel gives $15/\sqrt{12}$ = 4.3 um resolution
    - 20 um pixel gives 5.8 um resolution

Requirements (continued)

- Occupancy in a pixel for 2820 bco
  - Occupancy in 15 μm pixel = 250 hits/mm^2 x (15μm x 15μm) = 0.056 hits/bunch train
    - Chance of a single cell being hit twice in a bunch train = .056 x .056 = .0031 => 0.3%
    - Therefore, with a pipeline depth of only one, 99.7% of hits are recorded unambiguously.
  - Occupancy in a 20 μm pixel = 0.1
    - Chance of a cell being hit twice in a bunch train = 0.1 x 0.1 = 0.01 =>1.0%
    - Therefore, with a pipeline depth of only one, 99% of hits are recorded unambiguously.