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Long-Term Characterization of 6H-SiC Transistor Integrated Circuit Technology Operating at 500 °C

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ABSTRACT

NASA has been developing very high temperature semiconductor integrated circuits for use in the hot sections of aircraft engines and for Venus exploration. This paper reports on long-term 500 °C electrical operation of prototype 6H-SiC integrated circuits based on epitaxial 6H-SiC junction field effect transistors (JFETs). As of this writing, some devices have surpassed 4000 hours of continuous 500 °C electrical operation in oxidizing air atmosphere with minimal change in relevant electrical parameters.

INTRODUCTION

Extension of the operating envelope of useful transistor integrated circuits (ICs) to temperatures well above the effective 300 °C limit of silicon-on-insulator technology is expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems [1,2]. For example, extreme temperature ICs capable of T = 500 °C operation are considered vital to realizing improved sensing and control of turbine engine combustion leading to better fuel efficiency with significantly reduced pollution. The ability to place 500 °C ICs in engine hot-sections would reduce weight and reliability penalties (from added wires and liquid cooling plumbing) that arise because silicon combustion-control ICs are restricted to operating temperatures well below 300 °C. In general, competitive performance benefits to large systems enabled by extreme temperature ICs are recognized as quite substantial, even though most such systems require only a relatively small number of extreme temperature chips [1].

One critical requirement for all ICs, including extreme temperature ICs, is that they function reliably over a designed product lifetime. Previous reports of extreme temperature (≥ 500 °C) transistor or IC operation enabled by wide bandgap semiconductors have focused on current-voltage (I-V) properties and gain-frequency performance with little or no mention of how long such parts operated at high temperature. Without thousands of hours of useful operating life, extreme temperature semiconductor ICs will not benefit (and will not be inserted into) the vast majority of important intended applications. Aside from work at NASA Glenn Research Center [3-8], we are unaware of any published reports claiming stable semiconductor transistor operation for more than 10 hours at temperatures at or above 500 °C.

This paper reports semiconductor transistors and small ICs that have achieved thousands of hours of stable electrical operation at 500 °C. In particular, this work updates and expands our initial reports of transistor and differential amplifier testing for up to 3000 hours at 500 °C [6,7].

The results establish a new technology foundation for realizing usefully durable, extreme temperature ICs to benefit important harsh-environment applications.

EXPERIMENTAL

Driven by the need to realize integrated circuits with prolonged 500 °C operational durability, an epitaxial n-channel 6H-SiC junction field-effect transistor IC technology, shown in schematic cross-section in figure 1, was selected for development. In particular, the epitaxial SiC pn-junction gate structure (with low operating gate current) is believed inherently more robust against high temperature degradation than other (insulated gate, Schottky gate, bipolar, heterojunction and/or III-N) transistor technology approaches that would otherwise offer frequency, power dissipation, and/or circuit design and performance benefits. Though it is non-planar, the mesa-etched p^+ epi-gate structure avoids defects and extreme activation temperatures associated with high-dose p-type implants in SiC [9]. Despite inferior mobility compared to 4H-SiC, 6H-SiC was selected as having demonstrated better structural stability during some thermal processing steps [10,11]. Even though SiC is known to be chemically near-inert and diffusion resistant compared to silicon and III-V/III-N semiconductors, thermally activated degradation mechanisms at interfaces (such as metal-SiC, and/or SiC-insulator interfaces) or materials outside the semiconductor (such as metals, insulators, and/or packaging) have previously limited extreme temperature (i.e., ≥ 500 °C) stability/durability [3-5,12,13]. However, recently developed durable high temperature contacts to n-type SiC and high-temperature SiC packaging have demonstrated prolonged 500 °C operational capability in oxidizing air atmosphere [4,14]. The successful integration of these high temperature technologies into the epitaxial 6H-SiC JFET process is believed to be critical to the greatly prolonged 500 °C transistor and IC operation reported in this work.

A quarter wafer of small-signal 6H-SiC JFETs and simple ICs (configured using a single a metal interconnect layer) was fabricated starting from commercially purchased [15] epilayer substrate. Most fabrication process details are described elsewhere [3-8,12,14]. On-chip resistors were formed from the JFET n-channel layer and implants/contacts with the overlying p^+ gate layer removed. Interconnects and wire bond pads were simultaneously formed by patterning $TaSi_2$/Pt on top of reactive-sputtered Si_3N_4 dielectric.

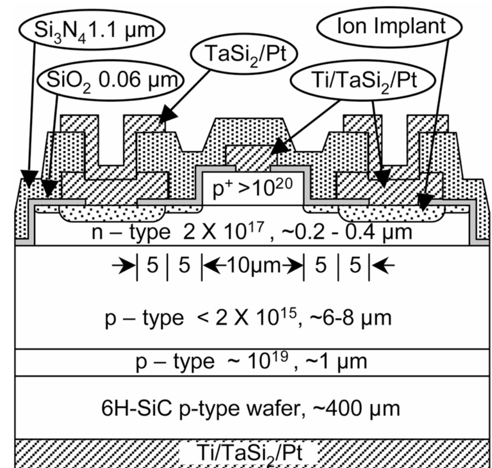

Figure 1. Simplified cross-sectional schematic of 6H-SiC JFET. Designed gate length (10 µm), gate edge to n^+ contact edge (5 µm) and n^+ contact edge to insulator via edge (5 µm) spacings are illustrated.

A few SiC chips from the saw-diced quarter-wafer were custom-packaged without any lids (i.e., exposed to air) and mounted onto two custom high-temperature circuit boards using the high temperature packaging approach detailed in [4]. Two 6H-SiC JFETs (one with 200 µm wide / 10 µm long gate and another with 100µm/10µm gate dimensions) were packaged and tested as discrete devices. Several integrated circuits were packaged and tested, including an inverting amplifier stage, a differential amplifier stage, a digital inverter (i.e., NOT logic gate) and a two-input NOR digital logic gate. The circuit boards with test chips

were placed in two laboratory ovens with ~ 30 cm long, 10 mil diameter unshielded Au wires running outside the ovens to nearby terminal strips connected to computer-controlled test instruments. The devices and circuits were operated continuously under electrical bias throughout the 500 °C test duration, with measurement data periodically (hourly at first, expanding to every 20 hours later) stored onto computer. The atmosphere inside the oven was ordinary room air (~ 21% O_2).

RESULTS

Discrete JFETs

All twenty one 100µm/10µm JFETs that were probe tested across the quarter-wafer prior to saw-apart demonstrated excellent room-temperature I-V behavior. However, threshold voltage (V_T) and saturated drain current (I_{DSS}) were respectively at maximum values around -14 V and 3.4 mA near the "top" of the wafer piece, and decreased across the wafer to minimum values around -7 V and 1.2 mA near the wafer piece "bottom". Until more-uniform commercial SiC JFET epilayers become available, SiC integrated circuit designs will need to account for such variability of these important transistor parameters.

Figure 2 compares drain current I_D versus drain voltage V_D characteristics of a packaged 200µm/10µm JFET measured by source-measure units (SMUs) during the 1st, 100th, and 4000th hours of 500 °C operation under V_D = 50 V and gate bias V_G = -6 V. Similar results were obtained for the 100µm/10µm JFET measured by a digitizing 60 Hz curve-tracer continuously operated with 50 V drain bias sweeps and -2V gate steps from V_G = 0 V to V_G = -16 V.

Figure 3 illustrates the measured variation of DC on-state I_{DSS}, transconductance g_m, drain-to-source resistance R_{DS}, and V_T for both packaged JFETs as a function of 500 °C operating time up to 4000 hours. The figure 3 plots are normalized to each transistor's measured value of I_{DSS0}, g_{m0}, R_{DS0}, and V_{T0} recorded at the 100 hour mark of 500 °C testing (i.e., after "burn-in"). Figure 3a shows I_{DSS} recorded at V_D = 20V, V_G = 0V. Figure 3b shows the g_m benchmarked at V_D = 20 V from V_G = 0V and -2V steps, and figure 3c shows the time evolution of R_{DS}. It is important to note that the y-axis scale limits for figure 3a-c plots are set to ±10% of each parameter's measured 100-hour value. With the exception of a few data points from the curve-tracer-measured 100µm/10µm JFET, the figure 3 data falls within this 10% parameter variation window. Figure 3d shows the precise time variation of V_T extracted from the computer-fit x-intercept of the SMU-measured $\sqrt{I_D}$ vs. V_G of the 200µm/10µm JFET. The measured V_T changes by less than 1%. This excellent stability reflects the fact that JFET V_T is determined by the as-grown 6H-SiC epilayer structure.

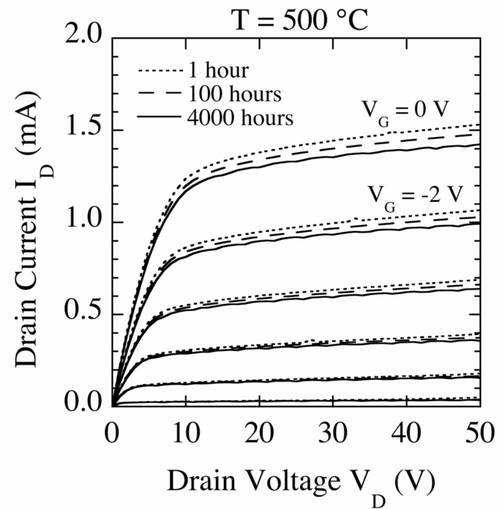

Figure 2. Drain I-V characteristics of packaged 200µm/10µm 6H-SiC JFET measured during the 1st, 100th, and 4000th hour of operation at 500 °C.

Integrated Circuits

The highly durable transistor properties summarized above enabled stable operation of prototype integrated circuits for thousands of hours at 500 °C. The inverting amplifier (inv-amp) and differential amplifier (diff-amp) are vital building blocks needed to realize more complex analog and digital circuits. Figure 4 summarizes the 500 °C durability data collected from packaged inv-amp and diff-amp ICs. The inv-amp consisted of two paralleled 40µm/10µm JFETs connected to a 20-square (516 kΩ at 500 °C) SiC load resistor. The diff-amp consisted of two source-coupled 20µm/10µm JFETs interconnected with three SiC epitaxial load resistors (see [6] for schematic). A 1 V peak-to-peak sine wave test input was applied (with -5 V DC bias for the inv-amp) and the V_{DD} supply voltage was 40 V with chip substrates grounded for both circuits. Figure 4a illustrates that there was less than 5% change in the 500 °C gain vs. frequency characteristics of these amplifiers measured at the beginning (black) and end (grey) of almost 4000 hours of 500 °C operation. The voltage gain drop-offs at higher frequency (above 10 kHz) are primarily due to un-optimized (un-buffered) circuit outputs and high capacitances associated with the unshielded wires of the oven-test setup. Figure 4b illustrates both amplifiers' gain vs. time data measured at low frequency (1 kHz or 2 kHz). Prior to failure, the inverting amplifier gain drifts less than 3%. For unknown reasons the diff-amp gain spiked some (~ 20%) between 1050 and 1600 hours, but afterwards, the amplifier gain stabilized with negligible apparent drift. After more than 3900 hours of 500 °C operation, the inverting amplifier failed suddenly. The inv-amp chip has not yet been removed from the oven for failure analysis because other chips (including the two JFETs and diff-amp IC) on the same printed circuit board remain under test at 500 °C.

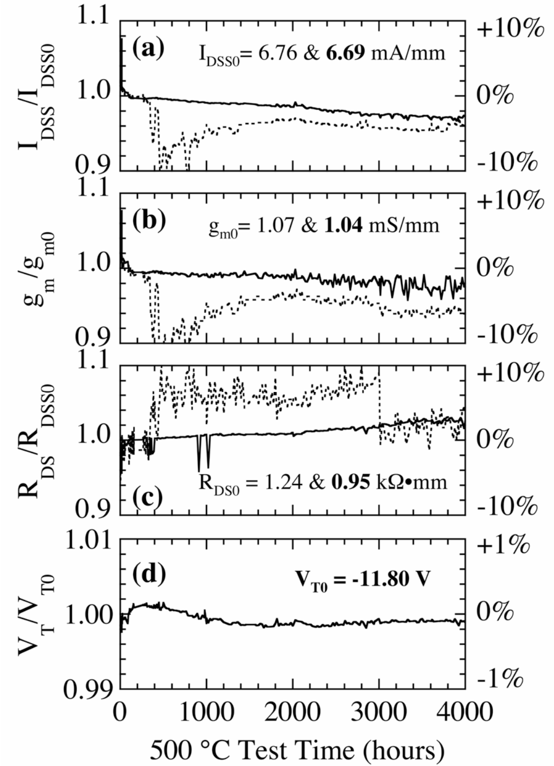

Figure 3. Normalized (see text) JFET parameters versus 500 °C test time for packaged devices with gate dimensions of 100µm/10µm (dashed, plain text, measured by digitizing curve-tracer) and 200µm/10µm (solid, **bold text**, measured by SMU).

Digital logic gate ICs were also implemented and packaged from the same 6H-SiC wafer piece. This demonstration logic circuit family features negative logic voltage levels (V_{High} ~ -2.5 V and V_{Low} ~ -7.5 V) and two power supplies (positive $+V_{DD}$ and negative $-V_{SS}$ in the range of 20 to 25 V). Figure 5 summarizes electrical results from prolonged 500 °C durability testing of two prototype digital logic gates. The packaged NOT gate successfully operated for over 3600 hours at 500 °C. Comparison of the figure 5a 1st hour and 3600th hour 500 °C output waveforms reveal that negligible change in NOT gate output signal occurred throughout the test duration. Figure 5b shows testing waveforms from the packaged two-input NOR gate collected during the 1st and 2405th hour of 500 °C operation. For a few days of this test, the setup was re-wired to

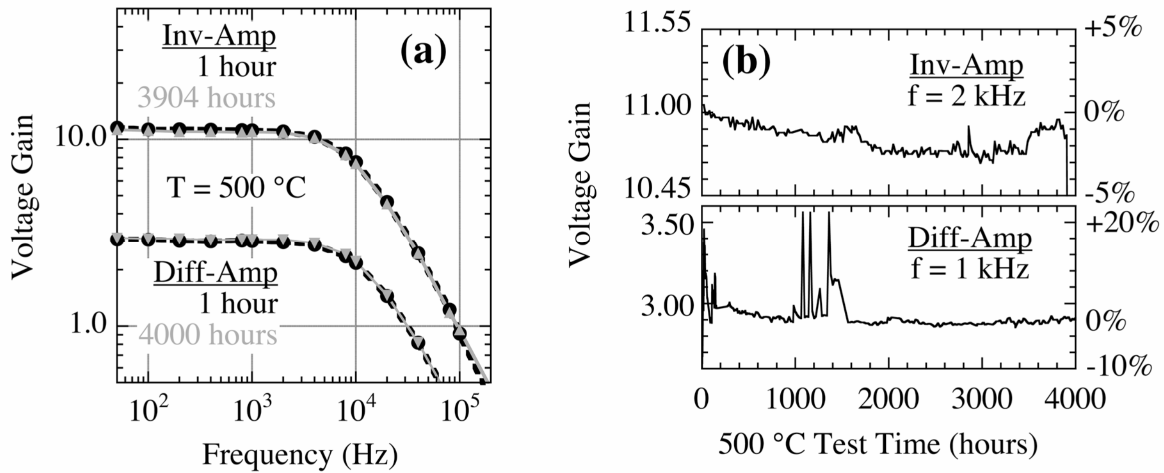

Figure 4. Analog amplifier circuit results recorded during prolonged 500 °C IC operation. (a) Gain vs. Frequency characteristics at beginning (black) and end (grey) of test. (b) Low-frequency voltage gain vs. 500 °C test time.

demonstrate the NOT gate output successfully driving the NOR gate inputs. Both logic gates failed suddenly soon after the maximum times shown in figure 5. The electrical failure of the NOR gate occurred in the form of an electrical near short-circuit, so failure of the insulating layer beneath a biased metal interconnect trace is suspected. However, detailed failure analysis is awaiting completion of 500 °C oven testing of other components on this board.

SUMMARY DISCUSSION

The increased 500 °C IC durability and stability demonstrated in this work is now sufficient for sensor signal conditioning circuits in jet-engine test programs. Although only a small number of devices have been packaged and tested for thousands of hours at high temperature, this demonstration establishes the feasibility of producing SiC integrated circuits

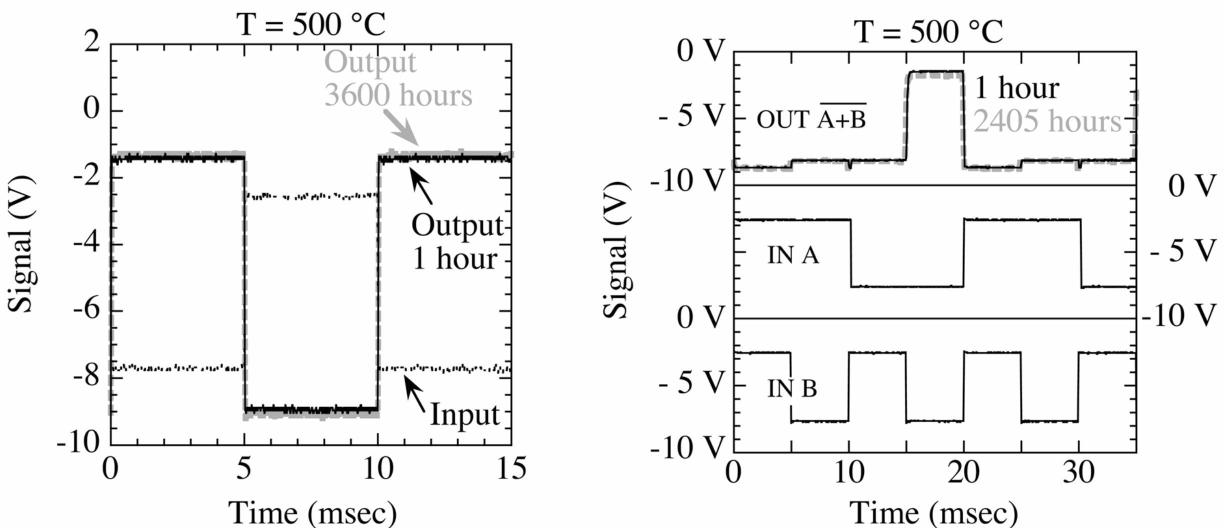

Figure 5. Digitized waveforms recorded near the beginning (black) and end (grey) of logic gate testing in 500 °C air-ambient oven. (a) Packaged NOT gate IC, and (b) NOR gate IC.

that are capable of prolonged 500 °C operation. This result was achieved through the integration of fundamental materials and/or processing advancements, including the development of high temperature n-type ohmic contacts [14] and high temperature packaging technology [4]. We speculate that the choice of epitaxial JFET technology and its designed operation at relatively low electric fields and low current densities are also important to the demonstrated 500 °C durability. For many envisioned applications, far greater circuit complexity than the few-transistor ICs demonstrated in this initial work will be needed. Shrinkage of device dimensions and operating biases, and implementation of multilayer interconnects are obvious important further steps towards realizing durable 500 °C SiC integrated circuitry with greater complexity, higher frequency performance, and increased functionality.

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