FTPC controls - expert manual - hardware

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1 Introduction

This manual is directed to the detector experts. It describes the hardware involved in the slow control system and its configuration. A list of spear parts is also included. Most of this hardware is located in the STAR south platform and it is not accessible at runtime.

The hardware concept of the FTPC slow control system is partly different from the TPC slow control system. While the latter uses a separate CPU (and a separate VME crate) for each task is performing, the former uses a single CPU and a single VME crate to run all the needed processes. While this brought to a considerable effort in trying to solve conflicts between different modules (interrupts, base addresses, memory issues), the saving in money and in space on the platform was remarkable.

2 General description

The slow control system's state machine is `sc.star.bnl.gov`(SUN), located in the STAR control room. The control and monitor software runs on a CPU (MVME167) located in the FTPC slow control crate in the first floor of the south platform (rack #$1B5$, see figure 1).

This CPU is interconnected with modules (inside the VME crate) that allow communication between the CPU itself and the FTPC subcomponents.

Most part of the FTPC slow control components are located on the first floor of the STAR south platform, in rack #$1B5, 1B6$, and $1B7$. The cooling system is located on the first floor of the north platform and the gas system is in the gas mixing room.

The support electronic for the subcomponents of the detector consists of:

cathodes	2 Heinzinger PNC 20000 3NEG power supplies
anodes	Le Croy 1454 power supply with 2 high voltage modules #1471
low voltages	8 custom made power supplies (LBL, Fred Bieser)
gating grid	2 gating grid drivers (UCLA, Vahe Ghazikhanian)

The read out boards installed on the FTPCs are also used to supply a voltage to thermistors located in strategic points of the detector and read the voltage drop across them, thus measuring indirectly the temperature.

The voltages present on the read out boards and the temperature data can be read through the HDLC (High-level Data Link Control) link by the Radstone board at the VME crate.

The gas system supplies data to the slow control bouncing them on several computers in order to make them readable and available.

The core of the system is the FTPC slow control crate, where the CPU and all the electronic modules needed to read the slow control data and to control the equipment are located.

A schematic drawing of the system is shown in figure 2:

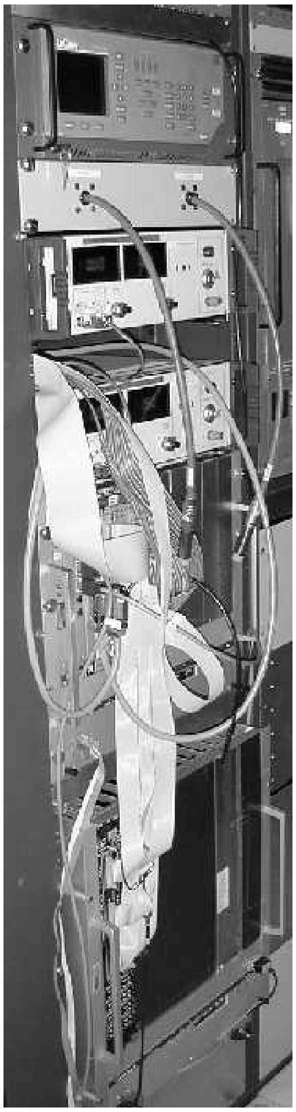

Figure 1: The slow control rack 1B5. Are visible from the top the Le Croy, the soft ground panel for the cathode high voltages, the two Heinzinger power supplies, the FTPC slow control VME crate (6U) and the 9U VME crate hosting the two gating grid drivers.

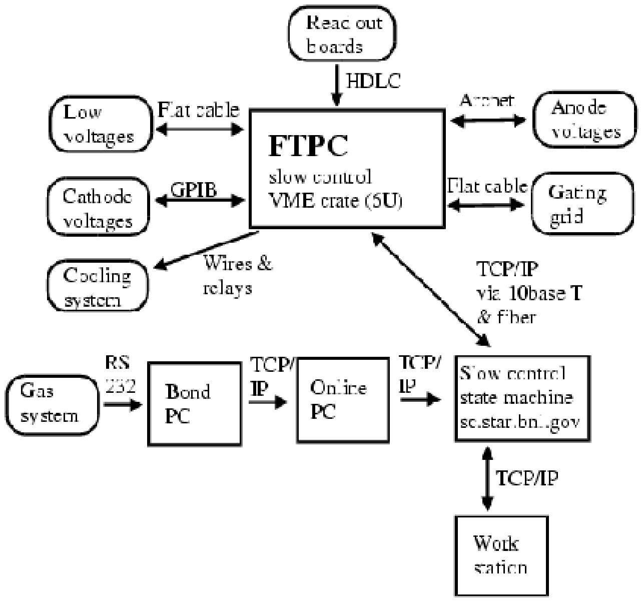

Figure 2: The slow control hardware architecture.

The link between the FTPC MVME167 CPU and the external world is more complex than shown in figure 2. The CPU is directly connected via flat cable to the transition module MVME712M in the backplane of the FTPC VME crate (figure 3)

Documentation of the transition module can be found at:

`http://library.mcg.mot.com:80/mcg/boards/vme/712maih/@ebt-link;`
`td=4;pt=29?target=%25N%13_582_START_RESTART_N%25`

The transition module supplies four serial ports and one port for telnet. Data transmission via telnet goes through a transducer directly connected to the MVME712M.. The two 10*baseT* cables seen in figure 3 go to the terminal (Computone) and the telnet servers on the second floor of the south platform (2A8). The terminal cable is connected to port #33 of the terminal server, and the telnet cable is connected to port #1 of the TCP/IP server. These servers are then connected to the network via fiber optics.

Communication between the platform and the control room, where the slow control state machine (`sc.star.bnl.gov`) is located is made possible only via fiber optics to minimize the noise introduced into the detector.

A summary of the subcomponents, their electronics, the VME modules needed to monitor and control them and their main parameters of operation is supplied in table 1:

Four digits base addresses actually are offsets to the start of the VMEbus short I/O space, located in $0xFFFF0000$.

It is important to underline that the order in which the modules are stacked into the VME crate matters. This has to do with the interrupt configuration of the modules. It is strongly advised to maintain the order described in table 1 (also see figure 4.

Figure 3: The MVME712M transition module in the backplane of the FTPC slow control crate.

Component	Hardware	Address	Protocol	VME module	Base address	Slot #
W cath.	Heinzinger	4	GPIB	NI1014-EH	0x8000	4
E cath.	Heinzinger	8	GPIB	NI1014-EH	0x8000	4
Anodes	Le Croy	0x240	ARCNET	CC121	0xD000	5
E LV	LBL	-	Flat cable	Acromag 948x	0x0400	6
W LV	LBL	-	Flat cable	Acromag 948x	0x0000	9
W GG	UCLA driver	-	Flat cable	UCLA controller	0x5000	7
E GG	UCLA driver	-	Flat cable	UCLA controller	0x5040	8
RDOB	LBL	1 to 10	HDLC	Radstone	0x88407000	3
Memory	-	-	-	MM-6390	0x18000000	2
CPU	-	-	-	MVME167	-	1

Table 1: Summary of the slow control electronics. The abbreviations stand for: W, E = West, East, LV = Low Voltages, GG= Gating Grid, RDOB = Read Out Boards

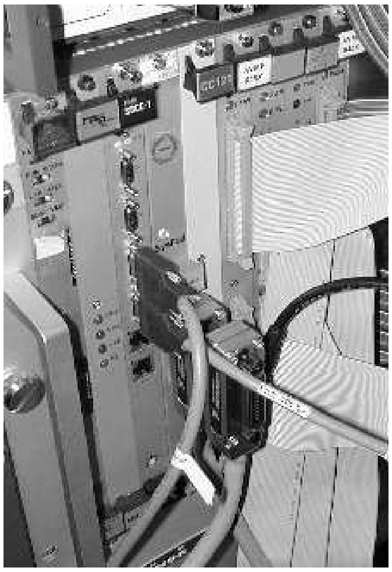

Figure 4: The slow control VME crate. Notice the order in which the modules are stacked in.

Only the data concerning external measurements such as temperatures and pressures and the operating voltages are read from the RDOB by slow control.

A general recommendation is to always verify the configuration of an existing module before replacing it with a new one.

Particular care has been taken in minimizing the number of wires going from the north platform, where the cooling system is located (no clean ground here), to the south platform (clean ground). Four wires in 2 shielded cables are stretched between the two platforms. On the north platform these wires have contacts only with isolated relays.

3 Cathodes

The units used to supply the cathode voltage are power supplies from Heinzinger, model $\#PNC20000 - 3negPNC72$. They have been modified in BNL according to manufacturer's specifications in order to allow interlock operation. The modification is documented in detail on page 15 of the Heinzinger English manual. It only required to remove the bridge between pins 3 and 7 on the ST1 connector (PCB-Board ON/OFF, right behind the on/off button on the front panel).

Another modification implemented by the manufacturer allows the power supply to trip (turn high voltage generation off) when the current limit is reached.

The communication protocol used is GPIB. The unit supports also RS232, but several problems were encountered when trying to connect to the serial ports of the MVME712M transition module. On the back of the unit is located the dip switch to select the GPIB address of the device. The west cathode address is 4, the east is 8.

The two power supplies are daisy chained to the NI1014-EH (National Instrument) module in the FTPC slow control VME crate. The base address of this module is selectable through jumpers, the factory default was 0x5000 but it had to be reassigned to 0x8000 due to conflicts with other modules (gating grid controllers).

A spare of this module is available (owned by MPI).

The interlock has to be cleared in order to allow high voltage (HV) generation. This is done shortening pins 12 and 13 from the 15 pins connector in the front panel of the unit (page 10 of the English manual). For the interlock conditions read the specific FTPC interlock manual.

For safety reasons and to avoid ground loops a soft ground is implemented in the panel located on top of the power supplies in rack $1B5$.

4 Anodes

Voltage to the anodes is supplied by the Le Croy 1454 mainframe and its boards module $\#1471P$, modification $\#010$. Three boards are placed in the back of the mainframe, and only the top-most two (which are labelled) are used to power the FTPC anodes. The third board is a spare. However it can be powered up from the software GUI (Graphical User Interface) as long as it is left in its present slot. If the slot is changed a change in the software is required (see the software manual, on the chapter related to the anodes).

The communication protocol used is Arcnet, the "bus" is a coaxial cable with a 93Ω impedance and consequently terminated at the power supply and at the Arcnet interface in the VME crate. The interface module used is a Compcontrol CC121 whose manual is available to the FTPC group.

The Le Croy mainframe also has a serial connection which is used as a backup in case the connections with the slow control state machine or the FTPC slow control CPU are not active. In this case the unit cannot be controlled by the FTPC slow control software (read the "Terminal session" section in the "Detector expert manual - software").

The "Interlock" connection in the back of the mainframe should be left terminated. This is due to a critical "feature" of the power supply. If this line is used to interlock the unit, access is required to clear any interlock situation. The "Macro" line is used instead. However this required a modification of the small "interlock" board of the mainframe. The logic of the "Macro" line was such that an open connection would give permission to operate to the unit and a short circuit would switch the high voltage generation off. This is not safe in case of a disconnection or a break of the cable. An on-board modification (addition of an inverter amplifier with gain -1) solved this problem. In figure

5 is shown the back of the mainframe with the serial and arcnet interfaces and the interlock and "Macro" lines.

In order to operate properly the "Macro" connection, the "sysdef" parameter had to be set to $0x008B$ (factory default is $0x000B$). This could be done via the slow control GUI using the "Debug" window from the anode control window (see the Anodes chapter on the "Detector expert manual - software") or using the serial connection to the mainframe. The command to be issued is in both cases:

```
sysdef 008B
```

This operation should not be needed anymore, since the mainframe keeps this value in memory also when disconnected from the power line thanks to its internal battery.

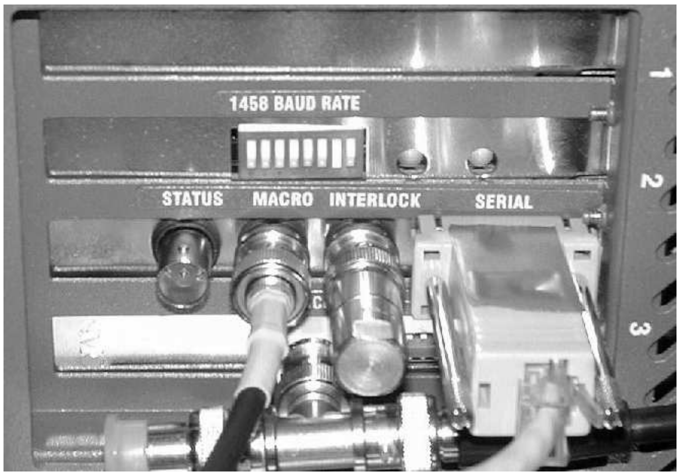

Figure 5: The Le Croy 1454 slots, located in the back of the mainframe.

The address of the Le Croy mainframe is set to the factory default: $0x0240$ via a DIP switch. The base address of the Arcnet interface board is set via three hex rotary switches to $0xFFD000$.

Although the high voltage modules are capable to supply up to $6000V$, the maximum supply voltage can be regulated by a potentiometer on the front panel of the $1471P$ module (which is located in the back panel of the 1454 mainframe !) and measured by a test point with a 1000 to 1 reduction. The hardware high voltage limit is currently set to $2000V$.

The current measurement resolution is on the order of $15nA$, and a dead zone smaller than that may result in an increase of traffic in the Arcnet bus and a crash of the system

The trip detect time is of the order of $2ms$.

5 Low voltages

The eight low voltage power supplies chassis are build by LBL (Fred Bieser) and are the same which are used by the TPC. However, in order to limit the power consumption on the read out boards a modification was implemented on all eight low voltage power supplies used by the FTPC. One outgoing positive line and one outgoing negative line were removed, and to the remaining two outgoing lines a 0.1Ω $(20W)$ resistor has been added. This allows to supply to the read out boards about $+6.5V$ and $-7.5V$.

The FTPC needs twenty such power supplies (one per read out board). Each low voltage power supply chassy hosts three independent power supplies. A column of four chassies per chamber (rack $\#1B6$ for the west and rack $\#1B7$ for the east FTPC) is used, leaving two power supplies per rack as spares.

The power supplies are controlled via two Acromag 948x with base addresses $0x0000$ and $0x0400$.

Each of the two Acromag modules is capable of controlling up to 64 I/O channels and is responsible to monitor and control four of the FTPC power supply chassies (12 channels). Fifty conductors flat ribbon cables connect the Acromag modules to patch panels (developed at LBL, Fred Bieser) whose main purpose is to fan out the digital I/O information. The patch panels were designed for the TPC and, through six 10 pin connectors (named J-1 to J-6, of which only four are used) they can fan out signals to six low voltage chassies. The I/O information is carried from the patch panel to the individual chassies by ten conductors flat ribbon cables.

Some channels of the east Acromag (slot 6) do not work, for this reason the $J-5$ connector of the patch panel in rack 1B6 was used instead than the $J-2$ to operate the second chassy from the top.

The $J-6$ connector of the same patch panel is used to switch the cooling system via the Acromag.

6 Gating grid

The gating grid hardware was entirely produced by UCLA (Vahe Ghazikhanian). It consists of two gating grid driver placed in a 9U VME crate and 2 gating grid controller modules placed in the FTPC slow control VME crate.

A TTL trigger signal is extracted from the FTPC TCD (trigger module) from rack 1A2 and delivered to the gating grid drivers, where it is split in two (half of the TTL signal is enough to trigger the driver). The delay introduced by such cables is $51ns$.

Flat ribbon cables connect the controllers to the drivers. Cables coming from the FTPCs connect to the back of the drivers.

The calibration procedure requires physical access to the gating grid drivers and it is described in a document by Eugene Yamamoto:

`http://www.star.bnl.gov/STAR/html/ftpc_l/DOC/gating_grid.ps`

Also he set up a nice "F.A.Q." page:

`http://www.physics.ucla.edu/~geno/pages/gating_grid_trouble.html`

The gating grid controllers have base addresses $0x5000$ and $0x5040$ settable by jumpers.

7 FTPC temperatures and pressures monitoring

Every read out board can supply two temperature measurements or one pressure measurement (with the present pressure sensor). Temperature and pressure data digitized by the read out boards are transmitted to the slow control through the HDLC link to the Radstone board.

Thermistors are connected to a $5V$ voltage regulator and to an ADC chip on the read out boards. In this way the voltage drop across the thermistor, and therefore the temperature are measured. Before the ADC stage the voltage is amplified by a feedback amplifier with feedback resistor of $17.8k\Omega$. Thermistors were supposed to measure $10k\Omega$ at $25C$, but unfortunately the wrong batch of thermistors was installed. Their resistance is $2.25k\Omega$ at $25C$. This, taken into account the amplification factor, sets the measurement out of the range of the ADC $(-10V/+10V)$ for reasonable temperature values. To overcome this problem an external resistor of $5.6k\Omega$ was put in series with the thermistor.

Read out boards #10 were modified on both the east and west side in order to supply enough power to drive a pressure transducer ($\Omega\ PX143-15BD5V$) to measure the incoming pressure of the cooling water.

Every read out board has a DIP switch to select its own identity or node number (from 1 to 10). A switch in the "ON" position sets the corresponding node number bit to zero, and the switch corresponding to the least significant bit is marked #1.

The ten read out boards on each FTPC are chained together to the same HDLC bus. The whole west FTPC is connected to channel 1 of the Radstone board, the whole East FTPC is connected to channel 2.

The read out boards address mapping is shown in the web page:

`http://www.star.bnl.gov/STAR/html/tpc_l/hard/rdo_map.html`

The FTPC read out boards, given the small amount of space available, do not have a memory buffer, therefore the event buffer cannot be stored. The temperatures and the pressures are stored in the addresses $0x02000A$ and $0x02000C$. The 16 bits ADC range is $-10V$ to $+10V$ and the data are written in two's complement.

8 Pulser

Although the pulser has nothing to do with the slow control a short reminder will not hurt. The pulser is located in rack 2A5. The signal from the pulser gets distributed to a set of boards and then to patch panels, all located above the pulser itself. The fan out board and the patch panel pertaining the FTPC is the rightmost one. Only one cable per FTPC is used to convey the pulser signal to the Frisch grid. Before connection at the FTPC the cable is terminated with a 100Ω resistor to match the pulser impedance. The two pins at the connector on the chambers are short circuited.

9 Cooling system remote control

The cooling system remote control only allows the detector operator to turn on/off the main power to the unit and the circulation pump. It makes use of two channels of one Acromag module (slot 6) and one output socket of the low voltage patch panel fan out (J6 in rack 1B6). A two relays board (AR-2 from Electronic Energy Control Inc.) is assembled inside the electronic chassy of the cooling system. It uses a voltage switched by the Acromag through the low voltage patch panel to power up the two relay coils. The relays are optically isolated to avoid to contaminate the clean ground of the south platform. Contact to the relay board is through a DB9 connector. Pin 4 and pin 7 are connected to pin 2 (main power control) and pin 1 (circulation pump control) of the connector J6 respectively. Pin 5 is connected to the north platform ground. A detailed description is presented in figure 6.

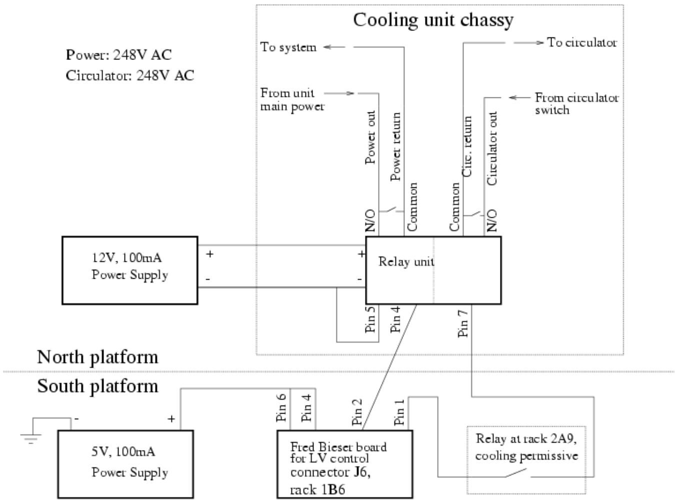

Figure 6: The cooling system remote control and interlock..

The wire going to the circulation pump's relay is broken and sent through a relay in rack 2A9 which gives permission to operate to the water systems (no detector leak).

10 Gas system monitor

This section describes only the hardware involved in the transmission of the gas system data to the slow control. The gas system has a serial interface which sends data that could be addressed to a printer or a serial listener. Data are sent through a grey, 25 pins connector serial cable. The other 9 pins grey cables visible in the system can be connected to a laptop to re-program the PLC (grey cable) or the display module (black cable). The serial line is connected to the serial port #1 of the windows NT computer `bond.star.bnl.gov`. A Labview program runs continuously which read and decodes the gas system data and posts them in a disk of the online machine (`online.star.bnl.gov`) which is cross mounted. The slow control state machine and the FTPC slow control CPU (MVME167) have access to this disk, and from it they retrieve the data. Details of the connections are shown in figure 2.

11 Bake out of the beam pipe

When baking out the beam pipes at the beginning ov every run the cooling shields should be installed and connected to the cooling system. Wires to connect the thermistors to a data acquisition board (Blitzer, presently in Munich) installed in the windows NT PC (`bond.star.bnl.gov`) are already in place and marked. They stretch from the north side of each magnet pole tip (within the magnet) to the cooling system on the north platform. The data acquisition software is located on the desktop of `bond.star.bnl.gov`and it is simple and self explanatory.

12 List of available spare modules

Unit	location	owner	pieces
NI1014	FTPC cabinet	MPI	1
Radstone	STAR slow control cabinet	STAR	3
Acromag	STAR slow control cabinet	STAR	1
gating grid controllers and drivers	VME crates in DAQ room	STAR	few.

13 Known problems

- The Radstone board often fails to acknowledge the presence of one or both channels. After some time also a new board has shown the same problem. It seems plausible that the module is damaged by rebooting the system often.

- The thermistor #4 on the body of the east FTPC is broken.

- If the slow control looses connection for a long time or if the Radstone does not supply data and the water flow stops in one of the chamber there is no protection, and the low voltage power supplies will stay on. This is the single point of failure of the system. For the next run an electronic flow meter, insensitive to magnetic fields, should be installed on the water line of each chamber and interlocked with the low voltages power supplies.