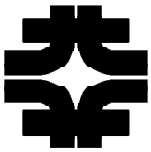

Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project
Readout Electronics

FIB FANOUT MODULE (FFO) TESTs

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Document # ESE-SVX-991015

Index

1 TESTS

1.1 System Configuration

Crate configuration:

GSTM in Slot 8
FIB Fanout in Slot 14 (red backplane) or in Slot 15 (green backplane).
FIB floating around.

SVXDAQ files:

system.cfg
(Note: contains the name of the configuration file that in our case is " fibfan.crate)
fibfan.crate
(Note: contains the configuration information, including the VME CPU name which should be edited to match the CPU used).

VME script files:

test01.txt, test02.txt, test04a.txt, test04b.txt, test04c.txt, test05.txt, test06a.txt, test06b.txt, test06c.txt, test06d.txt, test06e.txt.

GSTM FIFO files:

glink_0F.fifo, GSTM.fifo.

Programmable logic files:

FIFO_CTL.JED, CLK_CTL.JED, VME_INT.JED, ERRLATCH.JED, ERRDEC1.JED, LEDCTL1.JED, LEDCTL2.JED, ERRDEC2.JED, ERR_PIPE.JED, FAN_GDX.JED, 100599xx.dld.

Logic Analyzer setup files:

a) Setup_1.__, Setup_1._E,

b) Setup_2.__, Setup_2._E,

c) Setup_3.__, Setup_3._E.

d) Setup_4.__, Setup_4._E.

Software:

a) ISP Daisy Chain Download Version 5.1 from Lattice Semiconductor Co. to verify the checksum of the programmable logic. The Lattice Semiconductor ISP Daisy Chain Download (ispDCD) software provides a tool for downloading (programming) designs into programmable logic devices (PLDs) either singly or in a daisy chain. The FIB Fanout has ten Lattice programmable chips that can be reprogrammed using the ispDCD software, a PC and a parallel port cable connected to the PC and to the front panel ISP connector of the Fanout. For further instruction see the ispDCD software help file.

b) ISP GDX Version 1.5.1 from Lattice Semiconductor to modify and recompile the programming file for the GDX part.

Hardware:

HP16500 Logic Analyzer having a 16550A module (or equivalent) in slot E.

IBM compatible Personal Computer (486 or greater) and a parallel port cable.

6 chip clips for the 84-Pin PLCC chips (Newark part #90F2334).

2 chip clips for the 28-Pin PLCC chips (Newark part #87F010).

1 chip clip for the 16-Pin 300mil DIP chips.

1.2 TEST 0 (pre-test)

This test is to verify the correct setup of the teststand, the ISP logic programming and to make sure that the FFO is powered correctly.

1) Verify the FIB Fanout module keying:

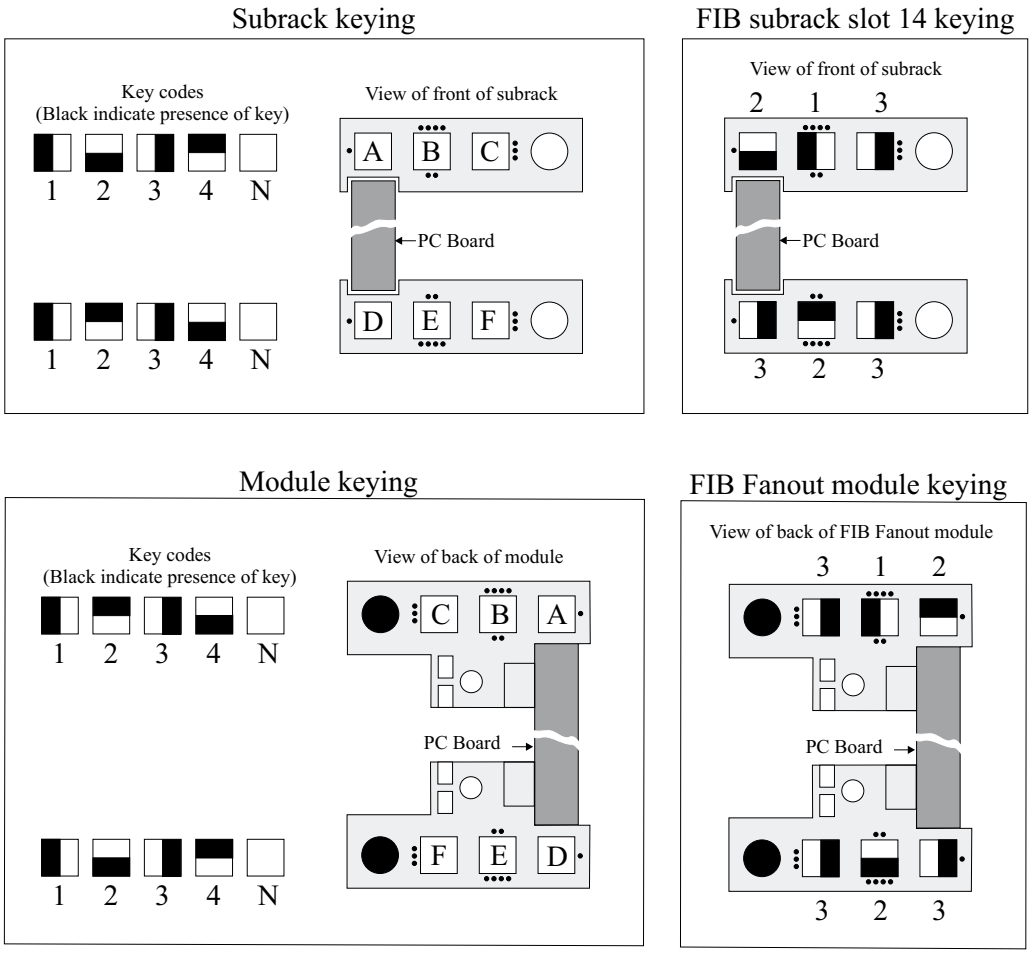

Figure 1.1, Keying of Fanout module and FIB subrack slot 14.

2) Check the position of the G-Link jumper settings (JP1 and JP2):

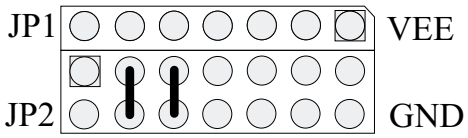

Figure 1.2, G-Link jumper settings.

3) Check the position of the jumper J54, J90, J91, J92, J93, J94, J101, J102, J103, J104, J137, J138:

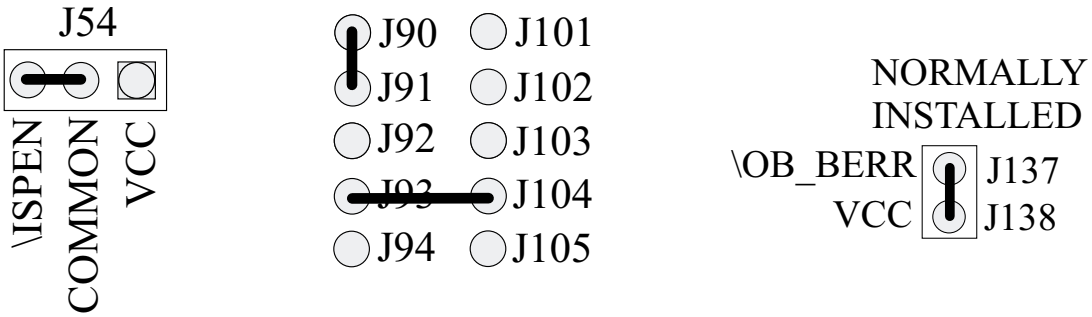

Figure 1.3, Jumper settings.

4) Perform a visual inspection of the board.
5) Check that the subrack power is OFF.
6) Insert the FIB Fanout in Slot 14 (red backplane) or in Slot 15 (green backplane).
7) Insert the GSTM module in Slot 8.
8) Connect the fiber optic jumper between the GSTM G-Link Tx Daughter Card and FIB Fanout Module G-Link Receiver.
9) Power ON the subrack.

10) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	ON	
RUN	OFF	
FAULT	OFF	
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from the Fanout.
LOCK	OFF	
ERR	ON or OFF	The G-Link is not in lock but the G-LINK Error LED can be OFF if the GSTM G-Link Tx is sending "fill frame 0".
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	OFF	

11) Check the following voltages on the PCB with a multimeter:
+5.0 Volts (VCC) at test point J140.
-5.2 Volts (VEE) at test point J141.
-2.0 Volts (VTT) at test point J79.
-1.28 Volts (VBB) at test point J61. This voltage can be adjusted using R44.

+0.640 Volts (optical power ref.level) at U29 pin 6. This voltage can be adjusted using R46.
Note: If (due to the test-stand power supply) the +5.0V supply is not at +5.0V on the module the percentage difference of the voltages should also be applied to the above adjustment.
Example: if VCC at J140 is 4.9Volts this mean that VCC differs from the standard 5.0 Volt value by 100*(1- 4.9/5.0) = 2%. The Voltage at U29 pin 6 should than be adjusted to:
0.640*(4.9/5.0) = 0.627 Volts.

12) Check the on board LEDs:
GL_VCC (G-Link VCC power) ON.
GL_VEE (G-Link VEE power) ON.
RX SIGNAL DETECT on the G-Link Receiver card ON.

13) Use the Software: ISP Daisy Chain Download Version 5.1 from Lattice Semiconductor Co. to program all of the programmable logic.
Data needed to program the programmable logic:
FIFO_CTL.JED, CLK_CTL.JED, VME_INT.JED, ERRLATCH.JED, ERRDEC1.JED, LEDCTL1.JED, LEDCTL2.JED, ERRDEC2.JED, ERR_PIPE.JED, FAN_GDX.JED,

Download configuration file (extension .DLD): 111000xx.dld (November 10, 2000)

To reprogram device number 10 (GDX chip) select the programming file (if available) corresponding to the board PREP Tracking Number or (if the file is not available) use the ispGDX Version 1.5.1 software from Lattice Semiconductor to open, modify (with the board PREP Tracking Number) and recompile the programming file for the GDX part.

a) Connect the parallel port cable to the PC and to the front panel ISP connector of the Fanout.

b) Window: LSC ISP Daisy Chain Download Version 1.5.1
Menu: FILECommand: OPEN Select the ".DLD" file.

c) Select the operation “Program&Verify” for each of the 10 devices.

d) Window: LSC ISP Daisy Chain Download Version 1.5.1
Menu: COMMANDCommand: RUN OPERATION

e) It takes about 15 minutes for the software to complete the “Program&Verify” operation. Verify that the message window shows the following message:
"Run Operation: successful".

f) If the “Program&Verify” operation fails, try to reprogram the failing PLD, if it fails again replace the part (Before replacing the part make sure that you are able to reprogram other parts on the board which would act as a software/daisy chain integrity check).

g) Verify the checksum for each of the devices proceding as in step b, c, d and e selecting the operation “Checksum” for the all the devices.
Verify the checksums with the those reported in the following table. The GDX device has a different checksum for each Fanout because it's programming code contains the PREP Tracking number (which is different for every board).
Note: on some PCs the checksum may result incorrect, in this case use the VERIFY operation to be sure that the PLDs showing the incorrect checksum are correctly programmed.

Index #	Lattice Device	Orcad schematic chip identifier	Programmable logic name	Jedec file	Checksum (November 11 1999)
1	1032E	U28	FIFO controller	FIFO_CTL.JED	*B6EA*
2	1032E	U42	Clock controller	CLK_CTL.JED	*AA1B*
3	1032E	U56	VME interface	VME_INT.JED	*FEEB*
4	1032E	U26	Error latch	ERRLATCH.JED	*1547*
5	1032E	U36	Error decoder 1	ERRDEC1.JED	*B027*
6	2032	U7	LED controller 1	LEDCTL1.JED	*BF75*
7	2032	U8	LED controller 2	LEDCTL2.JED	*C344*
8	1032E	U14	Error decoder 2	ERRDEC2.JED	*B027*
9	1032E	U43	Error pipe	ERR_PIPE.JED	*B98A*
10	GDX160	U37	GDX	FAN_GDX.JED	see Table 1.1

Table 1.1, Programmable logic daisy chain information.

Board serial number	PREP tracking number	GDX part checksum
100	550302	*FC17*
101	550303	*FC1B*
102	550304	*FBDB*
103	550305	*FBDF*
104	550312	*FC1B*
105	550313	*FC1F*
106	550314	*FBDF*
107	550315	*FBE3*
108	550316	*FC1F*
109	550317	*FC23*
110	550318	*FC1B*
111	550319	*FC1F*
112	550320	*FC17*
113	550321	*FC1B*

Table 1.2, FIB Fanout GDX part checksums.

1.3 TEST 01 (VME registers and general functionality)

1) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
2) Reset the FIB Fanout pushing the front panel "reset" button.
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	OFF	
FAULT	ON	Fanout in Mode Fault, transitioning from INIT to RUN Mode.
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from Fanout.
LOCK	ON	G-Link in lock.
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON or OFF	

5) Window: SVXII DAQ Menu: VME Command: Read/Write Script
6) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test01.txt.
7) Window: Read/Write Script
   Select tab: A32/D32
   Set crate: 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).
8) Window: Read/Write Script, click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test01.txt).

9) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	ON	Fanout in RUN Mode
FAULT	OFF	
SRC	ON	Backplane is driven with the clock from G-Link.
LOCAL	OFF	
LOCK	ON	G-Link in Lock
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON	Protocol Error on TTL data bus because the data frames sent by GSTM to the FFO on the G-Link optical link are not respecting the protocol (data frame should be 7 clock cycles long, the data bit should not change inside a frame, the SYNC bit should be high only for the last two clock cycles of the data frame). In this case the error is because no sync pulse is sent (SYNC Error).

10) Window: SVXII DAQ Menu: VME Command: Read/Write

11) Put the FIB Fanout in INIT Mode.
Window: Read/Write
Select tab: A32/D32
Set crate: 0
Set Address: ox70000020 (red backplane) or ox78000020 (green backplane).
Set Data: ox4001 0300
Click on the “write” button.

12) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	ON	Fanout in INIT Mode.
RUN	OFF	
FAULT	OFF	
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from the Fanout.
LOCK	ON	G-Link in Lock
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	OFF	

13) Send the FIB Fanout in RUN Mode.
Window: Read/Write
Set Data: ox8001 0300
Click on the “write” button.

14) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	ON	Fanout in RUN Mode
FAULT	OFF	
SRC	ON	Backplane is driven with the clock from G-Link.
LOCAL	OFF	
LOCK	ON	G-Link in Lock
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON	G-Link Error because no sync pulse is sent (SYNC Error).

15) Disconnect the optical fiber from the FIB Fanout and put the protection caps on the optical fiber and the Finisar RX module that resides within the FFO Module.

16) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	ON	Fanout in INIT Mode.
RUN	OFF	
FAULT	OFF	
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from the Fanout.
LOCK	OFF	G-Link in not Lock
ERR	ON	G-Link Error because the G-Link is not in lock.
OPT PWR LOW	ON	Optical Power below threshold.
TEST	OFF	
ERROR	OFF	

17) Reconnect the optical fiber to the FIB Fanout.

18) Window: SVXII DAQ Menu: GSTM Command: GSTM FF=1

19) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	ON	Fanout in RUN Mode
FAULT	OFF	
SRC	ON	Backplane is driven with the clock from G-Link.
LOCAL	OFF	
LOCK	ON	G-Link in Lock
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON	Protocol Error because no sync pulse is sent (SYNC Error).

1.4 TEST02 (TEST FIFO)

1) Reset the FIB Fanout pushing the front panel "reset" button.
2) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	OFF	
FAULT	ON	Fanout in Mode Fault, transitioning from INIT to RUN Mode.
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from Fanout.
LOCK	ON	G-Link in lock.
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON or OFF	Protocol Error because no sync pulse is sent (SYNC Error).

5) Reset the FIB Fanout pushing the front panel "reset" button.
6) Window: SVXII DAQ Menu: VME Command: Read/Write Script
7) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test02.txt.
8) Window: Read/Write Script
   Select tab: A32/D32
   Set crate: 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).
9) Window: Read/Write Script, click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test02.txt)..

9) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	ON	
RUN	OFF	
FAULT	OFF	
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from the Fanout.
LOCK	OFF	
ERR	ON	G-Link Error because the G-Link is not in lock.
OPT PWR LOW	OFF	
TEST	ON	The Test FIFO is driving the J3 Backplane TTL data bus with data from the Test FIFO.
ERROR	OFF	

10) Load Setup2 on the logic analyzer and verify logic analyzer POD setup 2 connections. Clear the trigger setting. For POD1 and POD2 set the analyzer trigger level to 2.0Volts. Check the presence of the following signals:
J3DB [19..0] (Rolling 1s and rolling 0s)
GLD_P [19..0] (Rolling 1s and rolling 0s)
PC53_P (53MHz clock)
J3_09, /J3_09, J3_10, /J3_10, J3_11, /J3_11, J3_12, /J3_12, J3_13, /J3_13, J3_14, /J3_14, /J3_16, J3_16, /J3_16, /J3_17, J3_17, /J3_17, J3_18, /J3_18, /J3_19, J3_19, /J3_19, /J3_20, J3_20, /J3_20, J3_21, /J3_21.
To verify the presence of the ECL Clock on the J3 Backplane connect:
POD3 to U50 and POD4 to U52.
To verify the presence of the ECL SYNC on the J3 Backplane connect:
POD3 to U51 and POD4 to U53.

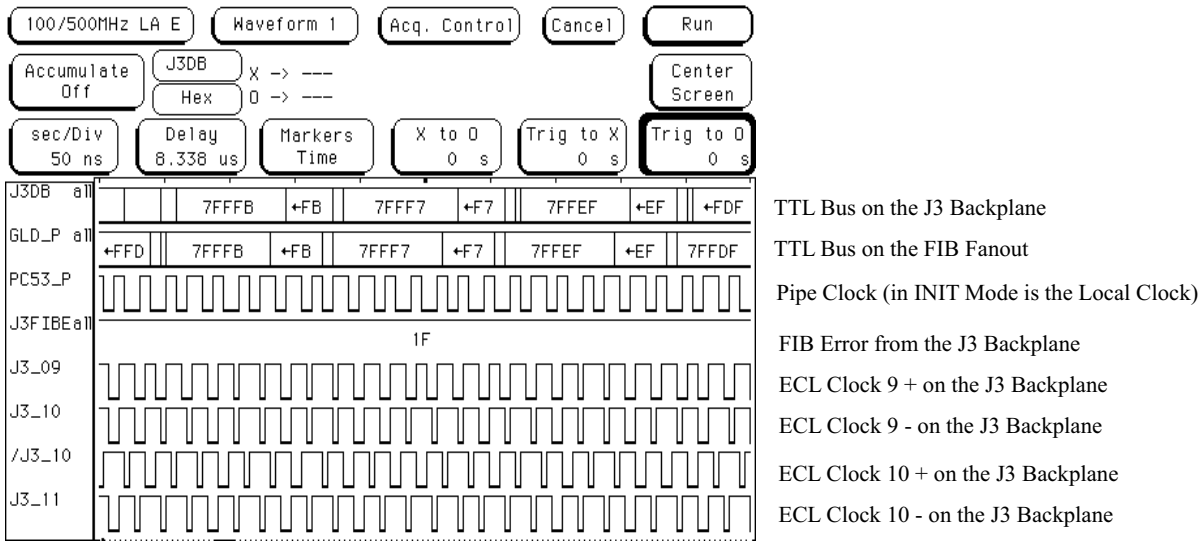

Figure 1.4, TTL Bus and ECL Clock signals.

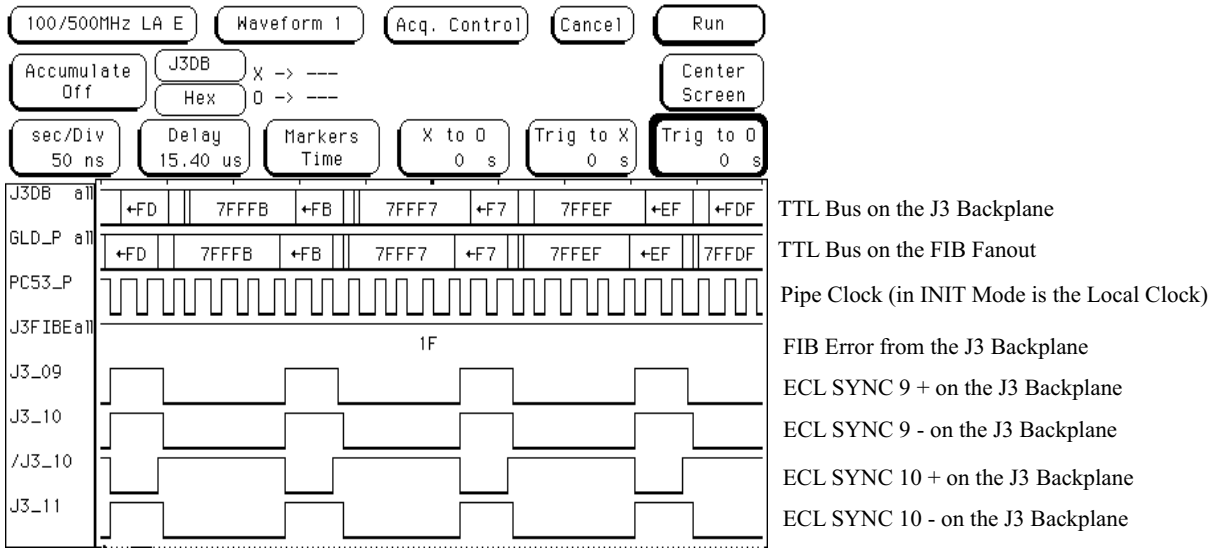

Figure 1.5, TTL Bus and ECL SYNC signals.

1.5 TEST03 (GLINK Data Link)

1) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
2) Reset the FIB Fanout pushing the front panel "reset" button.
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	OFF	
FAULT	ON	Fanout in Mode Fault, transitioning from INIT to RUN Mode.
SRC	OFF	
LOCAL	ON	Backplane is driven with the clock from Fanout.
LOCK	ON	G-Link in lock.
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON	Protocol Error because no sync pulse is sent (SYNC Error).

5) Window: SVXII DAQ
   Click on button GSTM to open the GSTM Status Page.
6) Window: GSTM Status Page Menu: STATUS Command: Clear FIFOs
7) Window: GSTM Status Page Menu: FIFOs
   Command: FIFO File Name, select file: "glink_0F.fifo".
   Command: Write FIFO.
8) Window: GSTM Status Page Menu: STATUS
   Select Transmission Control / Loopover
   Command: Write

9) Check the front panel LED Status on the FIB Fanout:

LED label	LED Status	Notes
SEL	OFF	
+5V	ON	
-5.2V	ON	
-2V	ON	
J3B	ON	
INIT	OFF	
RUN	ON	Fanout in RUN Mode
FAULT	OFF	
SRC	ON	Backplane is driven with the clock from G-Link.
LOCAL	OFF	
LOCK	ON	G-Link in Lock
ERR	OFF	
OPT PWR LOW	OFF	
TEST	OFF	
ERROR	ON	Protocol Error on TTL data bus because the file sent is not respecting the protocol (data frame should be 7 clock cycles long, the data bit should not change inside a frame, the SYNC bit should be high only for the last two clock cycles of the data frame).

10) Load Setup2 on the logic analyzer and verify logic analyzer POD setup 2 connections.
Check the presence of the following signals:
J3DB [19..0] (All 0s and all Fs).
GLD_P [19..0] (All 0s and all Fs).
PC53_P
J3_09, /J3_09, J3_10, /J3_10, J3_11, /J3_11, J3_12, /J3_12, J3_13, /J3_13, J3_14, /J3_14, /J3_16, J3_16, /J3_17, /J3_17, J3_18, /J3_18, /J3_19, J3_19, /J3_20, /J3_20, J3_21, /J3_21.
To verify the presence of the ECL Clock on the J3 Backplane connect:
POD3 to U50 and POD4 to U52.
To verify the presence of the ECL SYNC on the J3 Backplane connect:
POD3 to U51 and POD4 to U53.

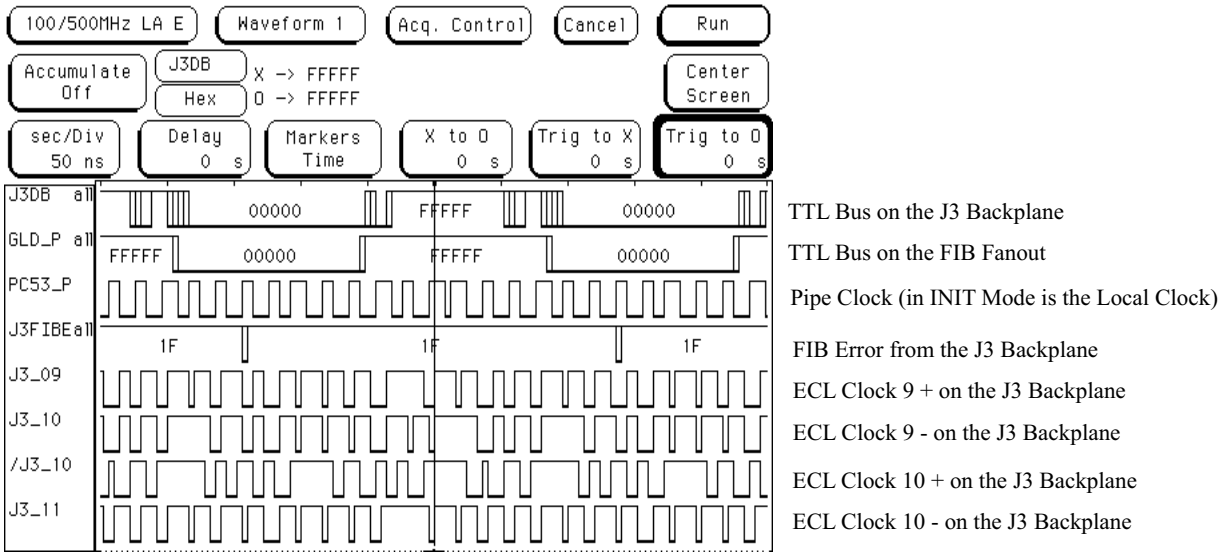

Figure 1.6, TTL Bus and ECL Clock signals.

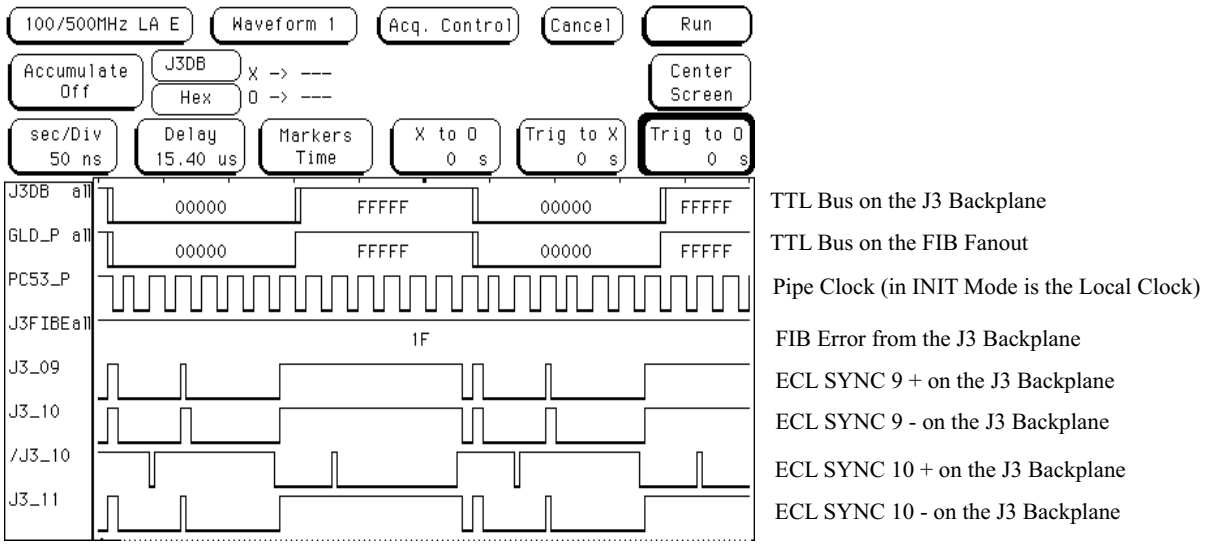

Figure 1.7, TTL Bus and ECL SYNC signals.

1.6 TEST04 (ERROR FIFO)

1) Reset the FIB Fanout pushing the front panel "reset" button.
2) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Reset the FIB Fanout pushing the front panel "reset" button.
5) Window: SVXII DAQ Menu: VME Command: Read/Write Script
6) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test04a.txt.
7) Window: Read/Write Script
   Select tab A32/D32,
   Set crate: 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).
8) Window: Read/Write Script, click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test04a.txt). This allows one to verify the functionality of the Error FIFO when used as transition memory triggered by VME.
9) Window: SVXII DAQ Menu: FIB Command: FIB Fanout Expert.
10) Window: FFO Expert Menus Menu: FIFOs Command: Read Error FIFO
11) Window: VME Hex Memory Dump
    Verify the content of the window (refer to Figure 1.8).
    The content should be something <u>similar</u> (the left digit can be different and the "8" in the 5th digit can be in a different position) to the following:

```
0x00000000:  c2080000 92080000 c2000000 92000000 92000000 92000000 92000000 92080000
0x00000020:  42080000 42000000 42000000 42000000 42000000 42000000 42080000 42080000
0x00000040:  42000000 42000000 42000000 42000000 42000000 d2080000 92080000 92000000
0x00000060:  92000000 92000000 d2000000 92000000 c2080000 92080000 c2000000 92000000
```

Example: "c2080000" means:
c => CAV*=1, DAV*=1, /DATA VALID=0, GLINK ERROR=0;
2 => GLINK STAT0=0, GLINK STAT1=0, /OPTICAL POWER LOW=1, FIB ERROR=0;
0=> No protocol errors detected;
80000=> SYNC BIT=1, DATA BITS[18..0]=000 0000 0000 0000 0000.

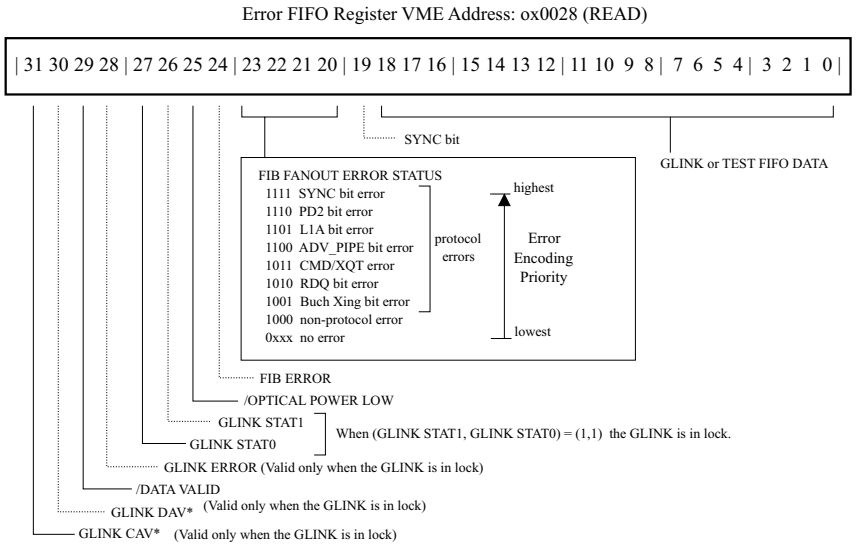

Figure 1.8, Error FIFO Register data format.

11) Window: Read/Write Script Menu: FILE Command: OPEN
Open file: test04b.txt.

12) Window: Read/Write Script, click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test04b.txt). This allows one to verify the functionality of the Error FIFO Test Mode.

13) Window: Read/Write Script Menu: FILE Command: OPEN
open file: test04c.txt.

14) Window: Read/Write Script click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test04c.txt). This allows one to verify the functionality of the Error FIFO and the Error Detection Logic.

15) Load Setup1 on the logic analyzer and verify logic analyzer POD setup 1 connections.
Check the presence of the following signals:
EFSM_F all.
LC53_F.
GLD_P all.
SYNC_P.
PC53_P.
EFE_F.
EFAF_F.
SVER_F.
SYER_P
Trigger on the rising edge of "SVER_F" and on the falling edge of"TACK_V".

16) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM

17) Window: SVXII DAQ
Click on button GSTM to open the GSTM Status Page.

18) Window: GSTM Status Page Menu: STATUS Command: Clear FIFOs

19) Window: GSTM Status Page Menu: FIFOs
Command: FIFO File Name, select file: “GSTM.fifo”.
Command: Write FIFO.

20) Window: GSTM Status Page Menu: STATUS
Select Transmission Control / Loopover
Command: Write.

21) Window: SVXII DAQ Menu: VME Command: Read/Write
Reset the Error FIFO and the Protocol Error Detection Logic (bit 29 Diagnostic Register).
Window: Read/Write
Select tab: A32/D32
Set crate: 0
Set Address: ox70000020 (red backplane) or ox78000020 (green backplane).
Set Data: ox2000 0000
Click on the “write” button.

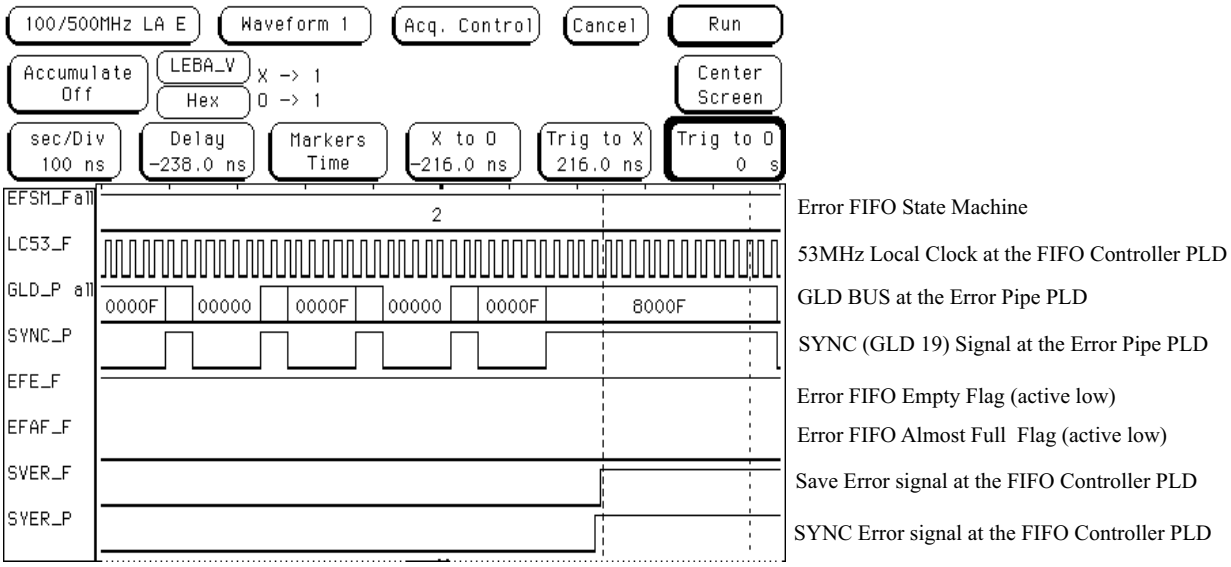

Figure 1.9, Error FIFO signals.

22) Window: SVXII DAQ Menu: VME Command: Read/Write
Arm the FIB Fanout Protocol Error Detection Mode (bit 23 Diagnostic Register).
Window: Read/Write
Select tab: A32/D32
Set crate: 0
Set Address: ox70000020 (red backplane) or ox78000020 (green backplane).
Set Data: ox0080 0000
Click on the "write" button.

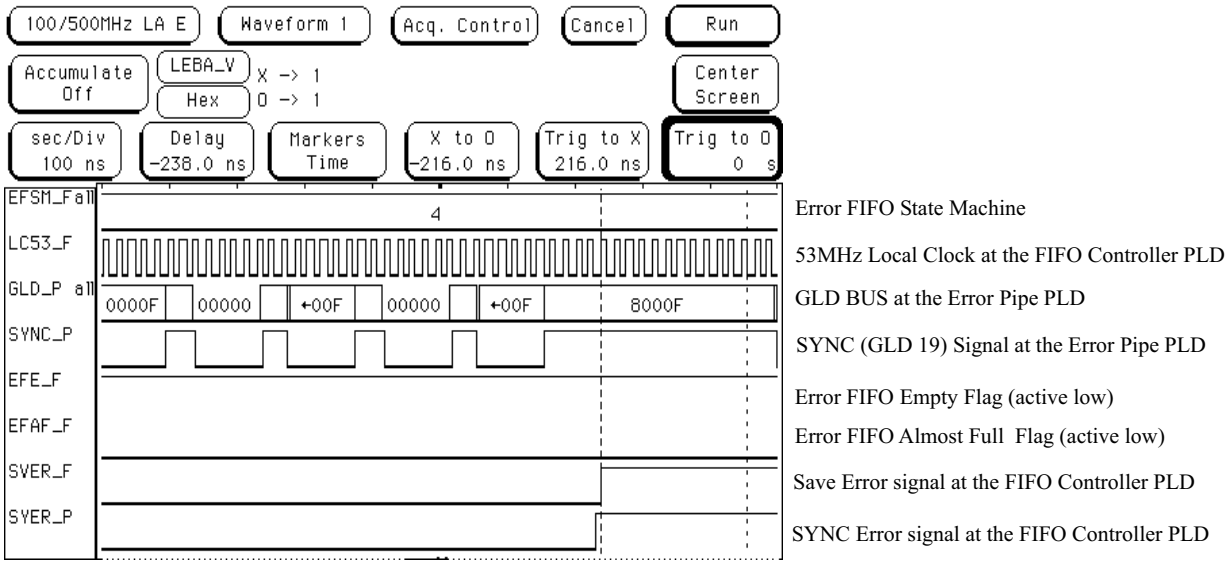

Figure 1.10, Error FIFO signals.

23) Window: SVXII DAQ Menu: FIB Command: FIB Fanout Expert.
24) Window: FFO Expert Menus Menu: FIFOs Command: Read Error FIFO
25) Window: VME Hex Memory Dump
Verify the content of the window (refer to Figure 1.8).
The content should be similar to the following:

```
0x00000000:  8e00000f 8e00000f 8e00000f 8e00000f 8e00000f 8e08000f 8e08000f 8e08000f
0x00000020:  8e08000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f
0x00000040:  8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef8000f 8ef00000 8ef00000
0x00000060:  8ef00000 8ef00000 8ef00000 8ef80000 8e080000 8e00000f 8e00000f 8e00000f
0x00000080:  8e00000f 8e00000f 8e08000f 8e08000f 8e000000 8e000000 8e000000 8e000000
```

1.7 TEST05 (ADC)

This test allows to verify the functionality of the on board ADC.

1) Reset the FIB Fanout pushing the front panel "reset" button.
2) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Reset the FIB Fanout pushing the front panel "reset" button.
5) Window: SVXII DAQ Menu: VME Command: Read/Write Script
6) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test05.txt.
7) Window: Read/Write Script
   Select tab A32/D32
   Set crate 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).
8) Window: Read/Write Script, click the "OK" button (run the script) and verify the responses of the board (using the comments included in the script file test05.txt). Table 1.3 provides a fast way to convert read data to the actual voltage values at the input of the ADC.
   Verify that:

   ADC Channel #0: G-Link Optical Power >-2dBm (typically –1.5dBm).
   Optical power [dBm] ≅ $10*\mathrm{Log}_{10}$ ($0.144*V_{ADC\text{-}ch0}$ [Volts]);

   ADC Channel #1: Room Temperature ≤ PCB Temperature top ≤ Room Temperature +12 F
   ADC Channel #2: Room Temperature ≤ PCB Temperature bottom ≤ Room Temperature +12 F

   Temp [F°] =32 + $36*V_{ADC}$ [Volts];

   ADC Channel #3: -5.2 Volt power supply ≅ -5.2 Volts

   $V_{EE} = -(100/47)*V_{ADC\text{-}ch3}$ [Volts]

   ADC Channel #6: -2.0 Volt power supply ≅ -2.0 Volts

   $V_{TT} = -V_{ADC\text{-}ch6}$ [Volts]

Hex Value Read	Volts	Hex Value Read	Volts	Hex Value Read	Volts	Hex Value Read	Volts	Hex Value Read	Volts	Hex Value Read	Volts	Hex Value Read	Volts
00	0.00	25	3.22	4A	1.61	6F	4.82	94	0.80	B9	3.08	DE	2.41
01	2.51	26	1.96	4B	4.12	70	0.27	95	3.31	BA	1.82	DF	4.92
02	1.25	27	4.47	4C	0.98	71	2.78	96	2.06	BB	4.33	E0	0.14
03	3.76	28	0.39	4D	3.49	72	1.53	97	4.57	BC	1.20	E1	2.65
04	0.63	29	2.90	4E	2.24	73	4.04	98	0.49	BD	3.71	E2	1.39
05	3.14	2A	1.65	4F	4.75	74	0.90	99	3.00	BE	2.45	E3	3.90
06	1.88	2B	4.16	50	0.20	75	3.41	9A	1.75	BF	4.96	E4	0.76
07	4.39	2C	1.02	51	2.71	76	2.16	9B	4.25	C0	0.06	E5	3.27
08	0.31	2D	3.53	52	1.45	77	4.67	9C	1.12	C1	2.57	E6	2.02
09	2.82	2E	2.27	53	3.96	78	0.59	9D	3.63	C2	1.31	E7	4.53
0A	1.57	2F	4.78	54	0.82	79	3.10	9E	2.37	C3	3.82	E8	0.45
0B	4.08	30	0.24	55	3.33	7A	1.84	9F	4.88	C4	0.69	E9	2.96
0C	0.94	31	2.75	56	2.08	7B	4.35	A0	0.10	C5	3.20	EA	1.71
0D	3.45	32	1.49	57	4.59	7C	1.22	A1	2.61	C6	1.94	EB	4.22
0E	2.20	33	4.00	58	0.51	7D	3.73	A2	1.35	C7	4.45	EC	1.08
0F	4.71	34	0.86	59	3.02	7E	2.47	A3	3.86	C8	0.37	ED	3.59
10	0.16	35	3.37	5A	1.76	7F	4.98	A4	0.73	C9	2.88	EE	2.33
11	2.67	36	2.12	5B	4.27	80	0.02	A5	3.24	CA	1.63	EF	4.84
12	1.41	37	4.63	5C	1.14	81	2.53	A6	1.98	CB	4.14	F0	0.29
13	3.92	38	0.55	5D	3.65	82	1.27	A7	4.49	CC	1.00	F1	2.80
14	0.78	39	3.06	5E	2.39	83	3.78	A8	0.41	CD	3.51	F2	1.55
15	3.29	3A	1.80	5F	4.90	84	0.65	A9	2.92	CE	2.25	F3	4.06
16	2.04	3B	4.31	60	0.12	85	3.16	AA	1.67	CF	4.76	F4	0.92
17	4.55	3C	1.18	61	2.63	86	1.90	AB	4.18	D0	0.22	F5	3.43
18	0.47	3D	3.69	62	1.37	87	4.41	AC	1.04	D1	2.73	F6	2.18
19	2.98	3E	2.43	63	3.88	88	0.33	AD	3.55	D2	1.47	F7	4.69
1A	1.73	3F	4.94	64	0.75	89	2.84	AE	2.29	D3	3.98	F8	0.61
1B	4.24	40	0.04	65	3.25	8A	1.59	AF	4.80	D4	0.84	F9	3.12
1C	1.10	41	2.55	66	2.00	8B	4.10	B0	0.25	D5	3.35	FA	1.86
1D	3.61	42	1.29	67	4.51	8C	0.96	B1	2.76	D6	2.10	FB	4.37
1E	2.35	43	3.80	68	0.43	8D	3.47	B2	1.51	D7	4.61	FC	1.24
1F	4.86	44	0.67	69	2.94	8E	2.22	B3	4.02	D8	0.53	FD	3.75
20	0.08	45	3.18	6A	1.69	8F	4.73	B4	0.88	D9	3.04	FE	2.49
21	2.59	46	1.92	6B	4.20	90	0.18	B5	3.39	DA	1.78	FF	5.00
22	1.33	47	4.43	6C	1.06	91	2.69	B6	2.14	DB	4.29		
23	3.84	48	0.35	6D	3.57	92	1.43	B7	4.65	DC	1.16		
24	0.71	49	2.86	6E	2.31	93	3.94	B8	0.57	DD	3.67		

Table 1.3, ADC read data to voltage conversion table.

1.8 TEST06 (RS485)

This test allows to verify the functionality of the on board RS485 Drivers.

1) Reset the FIB Fanout pushing the front panel "reset" button.
2) Start SVX DAQ Software (the software should be configured to use the files: "system.cfg" and "fibfan.crate".
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Reset the FIB Fanout pushing the front panel "reset" button.
5) Load Setup3 on the logic analyzer and verify logic analyzer POD setup 3 connections.
   Trigger on ST0J ⇑, ST1J ⇑, ST2J ⇑, ST3J ⇑.
   Monitor the following signals:
   ST0J, /ST0J,
   ST1J, /ST1J,
   ST2J, /ST2J,
   ST3J, /ST3J,
   SST0_J
   SST1_J
   SST2_J
   SST3_J
   SRC3A_P.
   SST0_G
   SST1_G
   SST2_G
   SST3_G
6) Window: SVXII DAQ Menu: VME Command: Read/Write Script
7) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test06a.txt.
8) Window: Read/Write Script
   Select tab A32/D32,
   Set crate: 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).

9) Window: Read/Write Script, click the “OK” button (run the script) and verify the responses of the board (using the comments included in the script file test06a.txt).

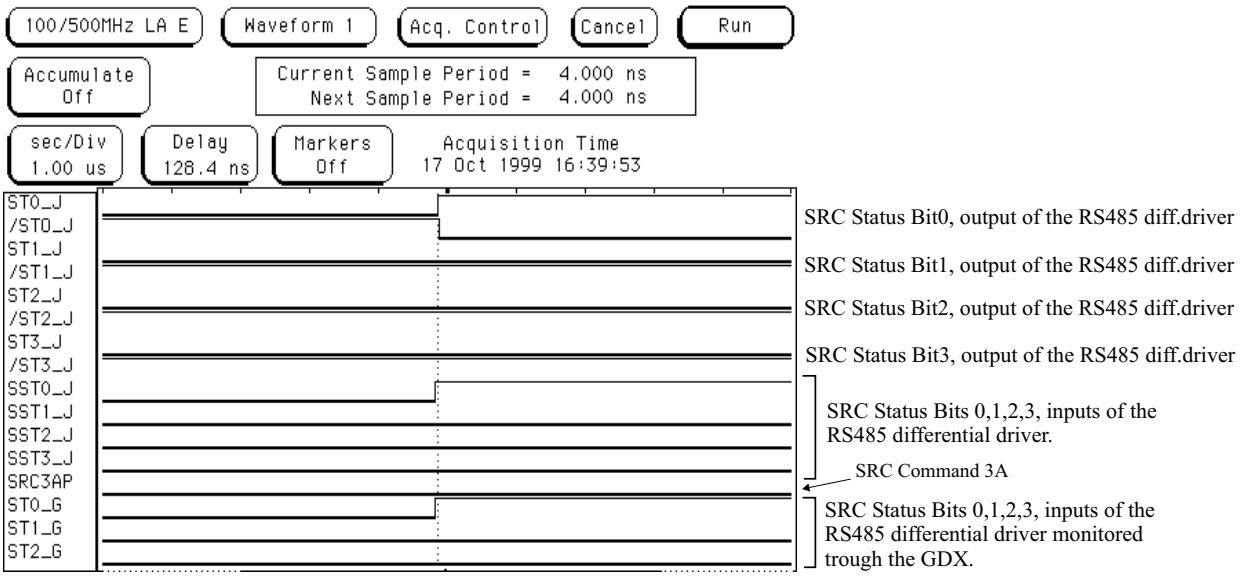

Figure 1.11, SRC Status bits signals.

10) Repeat the steps 6 to 8 using the files test06b.txt, test06c.txt, test06d.txt.

11) Window: Read/Write Script Menu: FILE Command: OPEN
Open file: test06e.txt.

12) Window: Read/Write Script
Select tab A32/D32
Set crate: 0
Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).

13) Window: Read/Write Script, click the “OK” button (run the script) and verify the responses of the board (using the comments included in the script file test06e.txt).

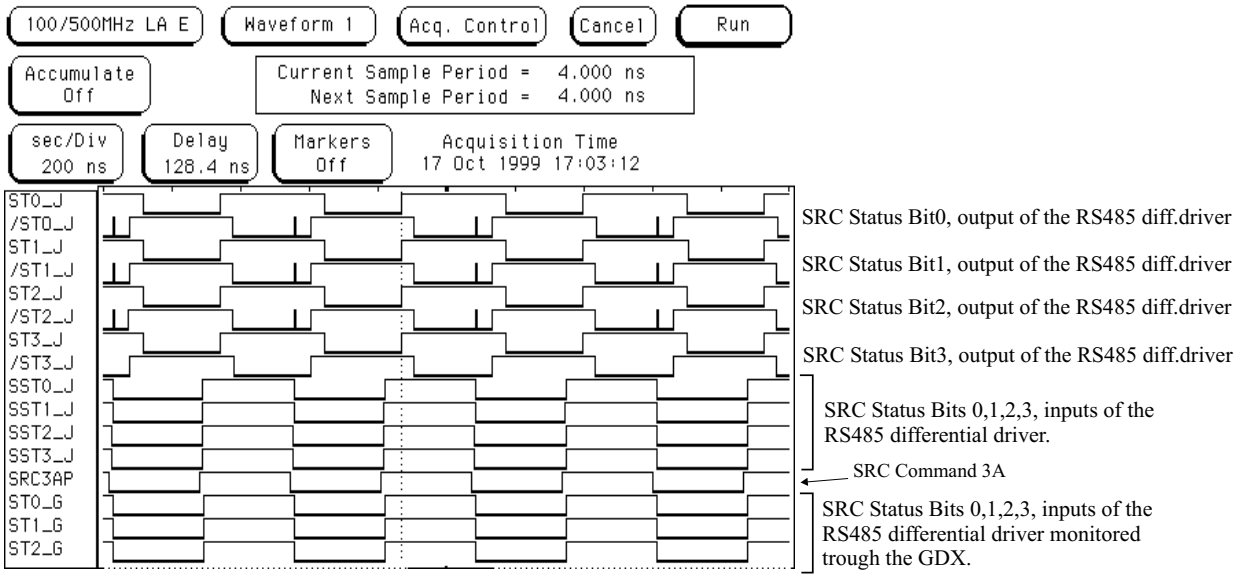

Figure 1.12, SRC Status bit signals.

1.9 TEST07 (FFO "DB" Local Bus)

This test allows to verify the functionality of the local bus "DB[0..31]".

1) Reset the FIB Fanout pushing the front panel “reset” button.
2) Start SVX DAQ Software (the software should be configured to use the files: “system.cfg” and “fibfan.crate”.
3) Window: SVXII DAQ Menu: DAQ Command: INIT SYSTEM
4) Reset the FIB Fanout pushing the front panel “reset” button.
5) Load Setup4 on the logic analyzer and verify logic analyzer POD setup 4 connections.
   Trigger on TACK_V ⇓
   Monitor the following signals:
   LEBA_V
   LEAB_V
   TACK_V
   WMP0_V
   RMP0_V
   WDRG_V
   RDRG_V
   DB_D_all

6) Window: SVXII DAQ Menu: VME Command: Read/Write Script
7) Window: Read/Write Script Menu: FILE Command: OPEN
   Open file: test07a.txt.
8) Window: Read/Write Script
   Select tab A32/D32,
   Set crate: 0
   Set Base Address: ox70000000 (red backplane) or ox78000000 (green backplane).
9) Window: Read/Write Script Menu: OPTIONS
   Select: SINGLE STEP COMMANDS (Box will be checked when selected).

10) Window: Read/Write Script, click the “OK” button twice (to run each command of the script) keep running one command at a time until the analyzer shows a read of the diagnostic register.

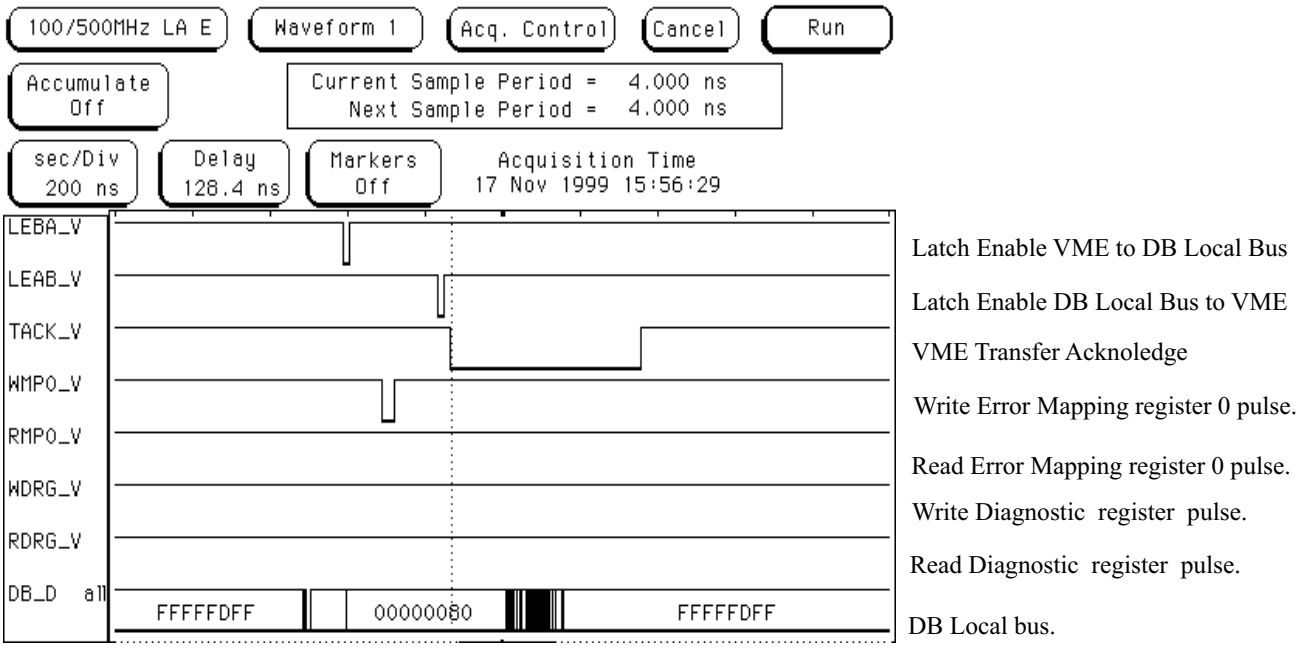

Figure 1.13, Test of the DB local bus.

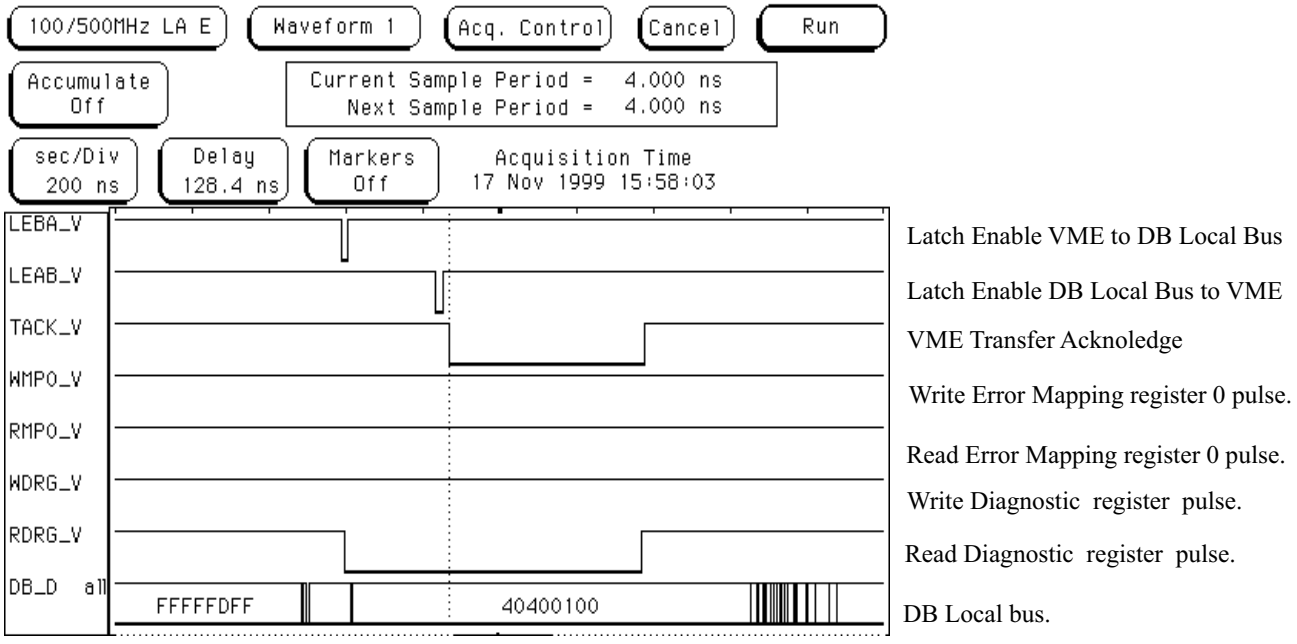

Figure 1.14, End of the test of the DB local bus..

2 LOGIC ANALYZER pod setup

2.1 Logic Analyzer SETUP 1

POD1: VME Interface (U56)

POD wire #	Chip pin #	Signal name	Notes
0			
1			
2	35	LEBA_V	"LEBA". Latch data from VME on VME writes.
3	38	LEAB_V	"LEAB". Latch data from module on VME reads.
4	79	RRT2_V	"REROUTE2" active high. Is true when the Board is addressed by VME with a D32 Cycle and a recognized address modifier (AM0-AM5).
5	16	SLED_V	"SLV_LED" active high. Is true when the board is addressd by VME (VME address = FFO Geographical Address).
6	29	TFSL_V	"TFIFO STOP LOOP"
7	14	SADC_V	"REROUTE0" active high. Start conversion signal for ADC.
8	8	R_ADC_V	"RD_ADC" active high. read ADC signal.
9	76	WMP0_V	"WRT_MAP0"
10	31	RMP0_V	"RD_MAP0"
11	58	WTFF_V	"WRT_TFIFO"
12	74	REFF_V	"REROUTE1" active low. Is the "RD_EFIFO" signal.
13	15	RDRG_V	"RD_DIAG", active low. Read Diagnostic Register.
14	78	WDRG_V	"WRT_DIAG" active low. Write Diagnostic Register.
15	55	TACK_V	"DTACK" active low. VME Data Transfer Acknowledge.
GND	1		"GND"
CLK J	20	LC53_V	"53MHZ". Local clock to VME Interface.

POD2: Error Latch (U26)

POD wire #	Chip pin #	Signal name	Notes
0	18	GST0_L	"GLINK_STAT0"
1	27	GST1_L	"GLINK_STAT1"
2	59	GERR_L	"GLINK_ERROR"
3	72	GCAV_L	"GLINK_CAV"
4	38	GDAV_L	"GLINK_DAV"
5	37	GOPL_L	"OPT_PWR_LOW"
6	56	FCOW_L	"FIB_CMD_OVERFLOW"
7	48	FFCT_L	"FIB_FLOW_CTL"
8	33	FTRC_L	"FIB_TRUNCATE"
9	83	FDCH_L	"FIB_DEAD_CHANNEL"
10			
11			
12			
13			
14			
15			
GND	1		"GND"
CLK K	20	LC53_L	"53MHZ". Local clock to Error Latch.

POD3: Clock Controller (U42)

POD wire #	Chip pin #	Signal name	Notes
0	32	MSM_C	"MSTATE0" (Test Point J88), Master State Machine state bit 0.
1	36	MSM_C	"MSTATE1" (Test Point J87), Master State Machine state bit 1.
2	37	MSM_C	"MSTATE2" (Test Point J86), Master State Machine state bit 2.
3	16	MSM_C	"MSTATE3" (Test Point J92), Master State Machine state bit 3.
4	80	RSM_C	"RM0" (Test Point J102), Run State Machine state bit 0.
5	77	RSM_C	"RM1" (Test Point J101), Run State Machine state bit 1.
6	8	RSM_C	"RM2" (Test Point J94), Run State Machine state bit 2.
7	52	SSM_C	"SSTATE0" (Test Point J121), Slave State Machine state bit 0.
8	48	SSM_C	"SSTATE1" (Test Point J120), Slave State Machine state bit 1.
9	58	SSM_C	"SSTATE2" (Test Point J119), Slave State Machine state bit 2.
10	83	SSM_C	"SSTATE3" (Test Point J105), Slave State Machine state bit 3.
11	71	LCSY_C	“LOCAL_SYNC”, Local SYNC generated by Clock Controller.
12	73	MCKS_C	"MCLK_SEL". Master Clock Select, 1:Local, 0:G-Link.
13	75	SYNS_C	"SYNC_SEL". SYNC Select, 1:Local, 0:G-Link.
14	72	PC53_C	"PIPE_CLK", 53MHz Pipe Clock, is either the G-Link (RUN Mode) or the Local Clock (Initialize Mode).
15	26	LC53_C	"YCLK", 53MHz Local Clock.
GND	1		"GND"
CLK L	15	GC53_C	"GLINK_CLK" (J91), 53MHz G-Link Clock

POD4: FIFO Controller (U28)

POD wire #	Chip pin #	Signal name	Notes
0	27	TFSM_F	"TF_S0", Test FIFO State Machine state bit 0.
1	26	TFSM_F	"TF_S1", Test FIFO State Machine state bit 1.
2	77	TFSM_F	"TF_S2", Test FIFO State Machine state bit 2.
3	76	TFSM_F	"TF_S3", Test FIFO State Machine state bit 3.
4	75	TFSM_F	"TF_S4" (Test Point J55), Test FIFO State Machine state bit 4.
5	12	EFSM_F	"EF_S0"(Test Point J46), Error FIFO State Machine state bit 0.
6	13	EFSM_F	"EF_S1"(Test Point J47), Error FIFO State Machine state bit 1.
7	30	EFSM_F	"EF_S2"(Test Point J49), Error FIFO State Machine state bit 2.
8	70	EFAF_F	"EFAFF" (Test Point J67), Error FIFO Almost Full Flag, active low.
9	73	EFE_F	"EFEF", Error FIFO Empty Flag, active low.
10	28	EFF_F	"EFFF", Error FIFO Full Flag, active low.
11	51	TFE_F	"TFEF", Test FIFO Empty Flag, active low.
12	58	TFF_F	"TFFF", Test FIFO Full Flag, active low.
13	20	SVER_F	"SAVE_ERROR" signal at the FIFO Controller PLD.
14			
15			
GND	1		"GND"
CLK M	83	LC53_F	"local_clock"

POD5: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	34	GLD_P	"GLD0". Bit 0 of GLD data bus.
1	76	GLD_P	"GLD1". Bit 1 of GLD data bus.
2	35	GLD_P	"GLD2". Bit 2 of GLD data bus.
3	45	GLD_P	"GLD3". Bit 3 of GLD data bus.
4	31	GLD_P	"GLD4". Bit 4 of GLD data bus.
5	53	GLD_P	"GLD5". Bit 5 of GLD data bus.
6	51	GLD_P	"GLD6". Bit 6 of GLD data bus.
7	18	GLD_P	"GLD7". Bit 7 of GLD data bus.
8	81	GLD_P	"GLD8". Bit 8 of GLD data bus.
9	77	GLD_P	"GLD9". Bit 9 of GLD data bus.
10	57	GLD_P	"GLD10". Bit 10 of GLD data bus.
11	40	GLD_P	"GLD11". Bit 11 of GLD data bus.
12	32	GLD_P	"GLD12". Bit 12 of GLD data bus.
13	72	GLD_P	"GLD13". Bit 13 of GLD data bus.
14	55	GLD_P	"GLD14". Bit 14 of GLD data bus.
15			
GND	1		"GND"
CLK N	63	PC53_P	"PIPE_CLK"

POD6: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	74	GLD_P	"GLD15". Bit 15 of GLD data bus.
1	17	GLD_P	"GLD16". Bit 16 of GLD data bus.
2	13	GLD_P	"GLD17". Bit 17 of GLD data bus.
3	39	GLD_P	"GLD18". Bit 18 of GLD data bus.
4	48	GLD_P	"GLD19". Bit 19 of GLD data bus, SYNC Signal.
5	26	SYER_P	"SYNC_ERR"
6	8	PDER_P	"PD2_ERR"
7	7	RDER_P	"RDQ_ERR"
8	73	BCER_P	"BC_ERR"
9	5	L1ER_P	"L1A_ERR"
10	10	ADER_P	"ADVP_ERR"
11	80	CXER_P	"CXQT_ERR"
12	46	SRC38_P	"SRC_SYSRESET", active low.
13	52	SRC3A_P	"SRC_FORCE_STAT_ON", active low.
14	59	SRC3D_P	"SRC_REQ_INIT_MODE", active low.
15	30	SRC3E_P	"SRC_RESET_ERRORS", active low.
GND	1		"GND"
CLK P	20	SYNC_P	"J3D19_COPY".

2.2 Logic Analyzer SETUP 2

POD1: Backplane and TTL Data BUS. Trigger set on 2.0Volt (User Defined)

POD wire #	J3 connector pin #	Signal name	Notes
0	C1	J3DB	J3 TTL Data Bus bit 1 (FIB commands).
1	C2	J3DB	J3 TTL Data Bus bit 2 (FIB commands).
2	C3	J3DB	J3 TTL Data Bus bit 3 (FIB commands).
3	C4	J3DB	J3 TTL Data Bus bit 4 (FIB commands).
4	C5	J3DB	J3 TTL Data Bus bit 5 (FIB commands).
5	C6	J3DB	J3 TTL Data Bus bit 6 (FIB XQT signal).
6	C7	J3DB	J3 TTL Data Bus bit 7 (Advance PIPE).
7	C8	J3DB	J3 TTL Data Bus bit 8 (Level 1 Accept).
8	C9	J3DB	J3 TTL Data Bus bit 9 (Bunch Crossing Number).
9	C10	J3DB	J3 TTL Data Bus bit 10 (Bunch Crossing Number).
10	C11	J3DB	J3 TTL Data Bus bit 11 (Bunch Crossing Number).
11	C12	J3DB	J3 TTL Data Bus bit 12 (Bunch Crossing Number).
12	C13	J3DB	J3 TTL Data Bus bit 13 (Bunch Crossing Number).
13	C14	J3DB	J3 TTL Data Bus bit 14 (Bunch Crossing Number).
14	C15	J3DB	J3 TTL Data Bus bit 15 (Bunch Crossing Number).
15	C16	J3DB	J3 TTL Data Bus bit 16 (Bunch Crossing Number).
GND			
CLK J			

POD2: Backplane, TTL Data BUS. Trigger set on 2.0Volt (User Defined).

POD wire #	J3 connector pin #	Signal name	Notes
0	C17	J3DB	J3 TTL Data Bus bit 17 (RDQ).
1	C18	J3DB	J3 TTL Data Bus bit 18 (RDQ).
2	C19	J3DB	J3 TTL Data Bus bit 19 (PIPE RD2).
3	C20	J3DB	J3 TTL Data Bus bit 20 (SYNC).
4	C21	J3FIBE	J3 OC TTL FIB to FFO bus (Reserved).
5	C22	J3FIBE	J3 OC TTL FIB to FFO bus (FIB Dead Channel).
6	C23	J3FIBE	J3 OC TTL FIB to FFO bus (FIB Truncate).
7	C24	J3FIBE	J3 OC TTL FIB to FFO bus (FIB Flow CTL).
8	C25	J3FIBE	J3 OC TTL FIB to FFO bus (FIB Command Overflow).
9			
10			
11			
12			
13			
14			
15			
GND			
CLK K			

POD3: ECL CLOCK (U50) and ECL SYNC (U51) Drivers

POD wire #	Chip pin #	Signal name	Notes
0	10	J3_09	ECL Master Clock 9 (U50) or ECL SYNC 9 (U51)
1	11	/J3_09	/ECL Master Clock 9 (U50) or /ECL SYNC 9 (U51)
2	12	J3_10	ECL Master Clock 10 (U50) or ECL SYNC 10 (U51)
3	13	/J3_10	/ECL Master Clock 10 (U50) or /ECL SYNC 10 (U51)
4	14	J3_11	ECL Master Clock 11 (U50) or ECL SYNC 11 (U51)
5	15	/J3_11	/ECL Master Clock 11 (U50) or /ECL SYNC 11 (U51)
6	17	J3_12	ECL Master Clock 12 (U50) or ECL SYNC 12 (U51)
7	18	/J3_12	/ECL Master Clock 12 (U50) or /ECL SYNC 12 (U51)
8	19	J3_13	ECL Master Clock 13 (U50) or ECL SYNC 13 (U51)
9	20	/J3_13	/ECL Master Clock 13 (U50) or /ECL SYNC 13 (U51)
10	21	J3_14	ECL Master Clock 14 (U50) or ECL SYNC 14 (U51)
11	22	/J3_14	/ECL Master Clock 14 (U50) or /ECL SYNC 14 (U51)
12			
13			
14			
15			
GND			
CLK L			

POD4: ECL CLOCK (U52) and ECL SYNC (U53) Drivers

POD wire #	Chip pin #	Signal name	Notes
0	21	J3_16	ECL Master Clock 16 (U50) or ECL SYNC 16 (U51)
1	22	/J3_16	/ECL Master Clock 16 (U50) or /ECL SYNC 16 (U51)
2	19	J3_17	ECL Master Clock 17 (U50) or ECL SYNC 17 (U51)
3	20	/J3_17	/ECL Master Clock 17 (U50) or /ECL SYNC 17 (U51)
4	17	J3_18	ECL Master Clock 18 (U50) or ECL SYNC 18 (U51)
5	18	/J3_18	/ECL Master Clock 18 (U50) or /ECL SYNC 18 (U51)
6	14	J3_19	ECL Master Clock 19 (U50) or ECL SYNC 19 (U51)
7	15	/J3_19	/ECL Master Clock 19 (U50) or /ECL SYNC 19 (U51)
8	12	J3_20	ECL Master Clock 20 (U50) or ECL SYNC 20 (U51)
9	13	/J3_20	/ECL Master Clock 20 (U50) or /ECL SYNC 20 (U51)
10	10	J3_21	ECL Master Clock 21 (U50) or ECL SYNC 21 (U51)
11	11	/J3_21	/ECL Master Clock 21 (U50) or /ECL SYNC 21 (U51)
12			
13			
14			
15			
GND			
CLK M			

POD5: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	34	GLD_P	"GLD0". Bit 0 of GLD data bus.
1	76	GLD_P	"GLD1". Bit 1 of GLD data bus.
2	35	GLD_P	"GLD2". Bit 2 of GLD data bus.
3	45	GLD_P	"GLD3". Bit 3 of GLD data bus.
4	31	GLD_P	"GLD4". Bit 4 of GLD data bus.
5	53	GLD_P	"GLD5". Bit 5 of GLD data bus.
6	51	GLD_P	"GLD6". Bit 6 of GLD data bus.
7	18	GLD_P	"GLD7". Bit 7 of GLD data bus.
8	81	GLD_P	"GLD8". Bit 8 of GLD data bus.
9	77	GLD_P	"GLD9". Bit 9 of GLD data bus.
10	57	GLD_P	"GLD10". Bit 10 of GLD data bus.
11	40	GLD_P	"GLD11". Bit 11 of GLD data bus.
12	32	GLD_P	"GLD12". Bit 12 of GLD data bus.
13	72	GLD_P	"GLD13". Bit 13 of GLD data bus.
14	55	GLD_P	"GLD14". Bit 14 of GLD data bus.
15			
GND	1		"GND"
CLK N	63	PC53_P	"PIPE_CLK"

POD6: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	74	GLD_P	"GLD15". Bit 15 of GLD data bus.
1	17	GLD_P	"GLD16". Bit 16 of GLD data bus.
2	13	GLD_P	"GLD17". Bit 17 of GLD data bus.
3	39	GLD_P	"GLD18". Bit 18 of GLD data bus.
4	48	GLD_P	"GLD19". Bit 19 of GLD data bus, SYNC Signal.
5	26	SYER_P	"SYNC_ERR"
6	8	PDER_P	"PD2_ERR"
7	7	RDER_P	"RDQ_ERR"
8	73	BCER_P	"BC_ERR"
9	5	L1ER_P	"L1A_ERR"
10	10	ADER_P	"ADVP_ERR"
11	80	CXER_P	"CXQT_ERR"
12	46	SRC38_P	"SRC_SYSRESET", active low.
13	52	SRC3A_P	"SRC_FORCE_STAT_ON", active low.
14	59	SRC3D_P	"SRC_REQ_INIT_MODE", active low.
15	30	SRC3E_P	"SRC_RESET_ERRORS", active low.
GND	1		"GND"
CLK P	20	SYNC_P	"J3D19_COPY".

2.3 Logic Analyzer SETUP 3

POD1: VME Interface (U56)

POD wire #	Chip pin #	Signal name	Notes
0			
1			
2	35	LEBA_V	"LEBA". Latch data from VME on VME writes.
3	38	LEAB_V	"LEAB". Latch data from module on VME reads.
4	79	RRT2_V	"REROUTE2" active high. Is true when the Board is addressed by VME with a D32 Cycle and a recognized address modifier (AM0-AM5).
5	16	SLED_V	"SLV_LED" active high. Is true when the board is addressd by VME (VME address = FFO Geographical Address).
6	29	TFSL_V	"TFIFO STOP LOOP"
7	14	SADC_V	"REROUTE0" active high. Start conversion signal for ADC.
8	8	R_ADC_V	"RD_ADC" active high. read ADC signal.
9	76	WMP0_V	"WRT_MAP0"
10	31	RMP0_V	"RD_MAP0"
11	58	WTFF_V	"WRT_TFIFO"
12	74	REFF_V	"REROUTE1" active low. Is the "RD_EFIFO" signal.
13	15	RDRG_V	"RD_DIAG", active low. Read Diagnostic Register.
14	78	WDRG_V	"WRT_DIAG" active low. Write Diagnostic Register.
15	55	TACK_V	"DTACK" active low. VME Data Transfer Acknowledge.
GND	1		"GND"
CLK J	20	LC53_V	"53MHZ". Local clock to VME Interface.

POD2: Error Latch (U26)

POD wire #	Chip pin #	Signal name	Notes
0	18	GST0_L	"GLINK_STAT0"
1	27	GST1_L	"GLINK_STAT1"
2	59	GERR_L	"GLINK_ERROR"
3	72	GCAV_L	"GLINK_CAV"
4	38	GDAV_L	"GLINK_DAV"
5	37	GOPL_L	"OPT_PWR_LOW"
6	56	FCOW_L	"FIB_CMD_OVERFLOW"
7	48	FFCT_L	"FIB_FLOW_CTL"
8	33	FTRC_L	"FIB_TRUNCATE"
9	83	FDCH_L	"FIB_DEAD_CHANNEL"
10			
11			
12			
13			
14			
15			
GND	1		"GND"
CLK K	20	LC53_L	"53MHZ". Local clock to Error Latch.

POD3: GDX Logic Analyzer Connector (J 139)

POD wire #	Connector pin #	Signal name	Notes
0	19	CAV_G	"ANALIZER0". Signal "/CAV_TTL".
1	18	DAV_G	"ANALIZER1". Signal "/DAV_TTL"
2	17	LKRD_G	"ANALIZER2". Signal "/GLINK_LINKRDY"
3	16	GST1_G	"ANALIZER3". Signal "STAT1_TTL"
4	15	GST0_G	"ANALIZER4". Signal "STAT0_TTL"
5	14	ERR0_G	"ANALIZER5". Signal "ERROR0".
6	13	ERR1_G	"ANALIZER6". Signal "ERROR1".
7	12	ERR2_G	"ANALIZER7". Signal "ERROR2".
8	11	ST0_G	"ANALIZER8". Signal "STATUS0".
9	10	ST1_G	"ANALIZER9". Signal "STATUS1".
10	9	ST2_G	"ANALIZER10". Signal "STATUS2".
11	8	ST3_G	"ANALIZER11". Signal "STATUS3".
12	7	FCOW_G	"ANALIZER12". Signal "/FIB_COMMAND_OVERFLOW".
13	6	FFCT_G	"ANALIZER13". Signal "/FIB_FLOW_CTL".
14	5	FTRC_G	"ANALIZER14". Signal "/FIB_TRUNCATE".
15	4	FDCH_G	"ANALIZER15". Signal "/FIB_DEAD_CHANNEL".
GND	20		
CLK L			

POD4: RS485 cable

POD wire #	Connector pin #	Signal name	Notes
0	U1-2	ST0_J	Signal "STATUS0".
1	U1-3	/ST0_J	Signal "/STATUS0".
2	U1-6	ST1_J	Signal "STATUS1".
3	U1-5	/ST1_J	Signal "/STATUS1".
4	U1-10	ST2_J	Signal "STATUS2".
5	U1-11	/ST2_J	Signal "/STATUS2".
6	U1-14	ST3_J	Signal "STATUS3".
7	U1-13	/ST3_J	Signal "/STATUS3".
8	U1-1	SST0_J	"SRC_STATUS0"
9	U1-7	SST1_J	"SRC_STATUS1"
10	U1-9	SST2_J	"SRC_STATUS2"
11	U1-15	SST3_J	"SRC_STATUS3"
12			
13			
14			
15			
GND			Connect to PCB ground.
CLK M			

POD5: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	34	GLD_P	"GLD0". Bit 0 of GLD data bus.
1	76	GLD_P	"GLD1". Bit 1 of GLD data bus.
2	35	GLD_P	"GLD2". Bit 2 of GLD data bus.
3	45	GLD_P	"GLD3". Bit 3 of GLD data bus.
4	31	GLD_P	"GLD4". Bit 4 of GLD data bus.
5	53	GLD_P	"GLD5". Bit 5 of GLD data bus.
6	51	GLD_P	"GLD6". Bit 6 of GLD data bus.
7	18	GLD_P	"GLD7". Bit 7 of GLD data bus.
8	81	GLD_P	"GLD8". Bit 8 of GLD data bus.
9	77	GLD_P	"GLD9". Bit 9 of GLD data bus.
10	57	GLD_P	"GLD10". Bit 10 of GLD data bus.
11	40	GLD_P	"GLD11". Bit 11 of GLD data bus.
12	32	GLD_P	"GLD12". Bit 12 of GLD data bus.
13	72	GLD_P	"GLD13". Bit 13 of GLD data bus.
14	55	GLD_P	"GLD14". Bit 14 of GLD data bus.
15	===	===	NOT WORKING ON THE ANALYZER
GND	1		"GND"
CLK N	63	PC53_P	"PIPE_CLK"

POD6: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	74	GLD_P	"GLD15". Bit 15 of GLD data bus.
1	17	GLD_P	"GLD16". Bit 16 of GLD data bus.
2	13	GLD_P	"GLD17". Bit 17 of GLD data bus.
3	39	GLD_P	"GLD18". Bit 18 of GLD data bus.
4	48	GLD_P	"GLD19". Bit 19 of GLD data bus, SYNC Signal.
5	26	SYER_P	"SYNC_ERR"
6	8	PDER_P	"PD2_ERR"
7	7	RDER_P	"RDQ_ERR"
8	73	BCER_P	"BC_ERR"
9	5	L1ER_P	"L1A_ERR"
10	10	ADER_P	"ADVP_ERR"
11	80	CXER_P	"CXQT_ERR"
12	46	SRC38_P	"SRC_SYSRESET", active low.
13	52	SRC3A_P	"SRC_FORCE_STAT_ON", active low.
14	59	SRC3D_P	"SRC_REQ_INIT_MODE", active low.
15	30	SRC3E_P	"SRC_RESET_ERRORS", active low.
GND	1		"GND"
CLK P	20	SYNC_P	"J3D19_COPY".

2.4 Logic Analyzer SETUP 4

POD1: VME Interface (U56)

POD wire #	Chip pin #	Signal name	Notes
0			
1			
2	35	LEBA_V	"LEBA". Latch data from VME on VME writes.
3	38	LEAB_V	"LEAB". Latch data from module on VME reads.
4	79	RRT2_V	"REROUTE2" active high. Is true when the Board is addressed by VME with a D32 Cycle and a recognized address modifier (AM0-AM5).
5	16	SLED_V	"SLV_LED" active high. Is true when the board is addressd by VME (VME address = FFO Geographical Address).
6	29	TFSL_V	"TFIFO STOP LOOP"
7	14	SADC_V	"REROUTE0" active high. Start conversion signal for ADC.
8	8	R_ADC_V	"RD_ADC" active high. read ADC signal.
9	76	WMP0_V	"WRT_MAP0"
10	31	RMP0_V	"RD_MAP0"
11	58	WTFF_V	"WRT_TFIFO"
12	74	REFF_V	"REROUTE1" active low. Is the "RD_EFIFO" signal.
13	15	RDRG_V	"RD_DIAG", active low. Read Diagnostic Register.
14	78	WDRG_V	"WRT_DIAG" active low. Write Diagnostic Register.
15	55	TACK_V	"DTACK" active low. VME Data Transfer Acknowledge.
GND	1		"GND"
CLK J	20	LC53_V	"53MHZ". Local clock to VME Interface.

POD2: unused

POD wire #	Chip pin #	Signal name	Notes
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
GND			
CLK K			

POD3: Error Decoder 1 (U36)

POD wire #	Chip pin #	Signal name	Notes
0	13	DB_D	"DB0". Bit 0 of DB data bus.
1	5	DB_D	"DB1". Bit 1 of DB data bus.
2	77	DB_D	"DB2". Bit 2 of DB data bus.
3	81	DB_D	"DB3". Bit 3 of DB data bus.
4	68	DB_D	"DB4". Bit 4 of DB data bus.
5	80	DB_D	"DB5". Bit 5 of DB data bus.
6	34	DB_D	"DB6". Bit 6 of DB data bus.
7	30	DB_D	"DB7". Bit 7 of DB data bus.
8	11	DB_D	"DB8". Bit 8 of DB data bus.
9	49	DB_D	"DB9". Bit 9 of DB data bus.
10	4	DB_D	"DB10". Bit 10 of DB data bus.
11	52	DB_D	"DB11". Bit 11 of DB data bus.
12	59	DB_D	"DB12". Bit 12 of DB data bus.
13	54	DB_D	"DB13". Bit 13 of DB data bus.
14	14	DB_D	"DB14". Bit 14 of DB data bus.
15	17	DB_D	"DB15". Bit 15 of DB data bus.
GND			
CLK L			

POD4: Error Decoder 1 (U36)

POD wire #	Chip pin #	Signal name	Notes
0	8	DB_D	"DB16". Bit 16 of DB data bus.
1	37	DB_D	"DB17". Bit 17 of DB data bus.
2	36	DB_D	"DB18". Bit 18 of DB data bus.
3	31	DB_D	"DB19". Bit 19 of DB data bus.
4	33	DB_D	"DB20". Bit 20 of DB data bus.
5	40	DB_D	"DB21". Bit 21 of DB data bus.
6	27	DB_D	"DB22". Bit 22 of DB data bus.
7	75	DB_D	"DB23". Bit 23 of DB data bus.
8	70	DB_D	"DB24". Bit 24 of DB data bus.
9	69	DB_D	"DB25". Bit 25 of DB data bus.
10	71	DB_D	"DB26". Bit 26 of DB data bus.
11	78	DB_D	"DB27". Bit 27 of DB data bus.
12	16	DB_D	"DB28". Bit 28 of DB data bus.
13	15	DB_D	"DB29". Bit 29 of DB data bus.
14	9	DB_D	"DB30". Bit 30 of DB data bus.
15	7	DB_D	"DB31". Bit 31 of DB data bus.
GND			
CLK M			

POD5: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	34	GLD_P	"GLD0". Bit 0 of GLD data bus.
1	76	GLD_P	"GLD1". Bit 1 of GLD data bus.
2	35	GLD_P	"GLD2". Bit 2 of GLD data bus.
3	45	GLD_P	"GLD3". Bit 3 of GLD data bus.
4	31	GLD_P	"GLD4". Bit 4 of GLD data bus.
5	53	GLD_P	"GLD5". Bit 5 of GLD data bus.
6	51	GLD_P	"GLD6". Bit 6 of GLD data bus.
7	18	GLD_P	"GLD7". Bit 7 of GLD data bus.
8	81	GLD_P	"GLD8". Bit 8 of GLD data bus.
9	77	GLD_P	"GLD9". Bit 9 of GLD data bus.
10	57	GLD_P	"GLD10". Bit 10 of GLD data bus.
11	40	GLD_P	"GLD11". Bit 11 of GLD data bus.
12	32	GLD_P	"GLD12". Bit 12 of GLD data bus.
13	72	GLD_P	"GLD13". Bit 13 of GLD data bus.
14	55	GLD_P	"GLD14". Bit 14 of GLD data bus.
15			
GND	1		"GND"
CLK N	63	PC53_P	"PIPE_CLK"

POD6: Error Pipe (U43)

POD wire #	Chip pin #	Signal name	Notes
0	74	GLD_P	"GLD15". Bit 15 of GLD data bus.
1	17	GLD_P	"GLD16". Bit 16 of GLD data bus.
2	13	GLD_P	"GLD17". Bit 17 of GLD data bus.
3	39	GLD_P	"GLD18". Bit 18 of GLD data bus.
4	48	GLD_P	"GLD19". Bit 19 of GLD data bus, SYNC Signal.
5	26	SYER_P	"SYNC_ERR"
6	8	PDER_P	"PD2_ERR"
7	7	RDER_P	"RDQ_ERR"
8	73	BCER_P	"BC_ERR"
9	5	L1ER_P	"L1A_ERR"
10	10	ADER_P	"ADVP_ERR"
11	80	CXER_P	"CXQT_ERR"
12	46	SRC38_P	"SRC_SYSRESET", active low.
13	52	SRC3A_P	"SRC_FORCE_STAT_ON", active low.
14	59	SRC3D_P	"SRC_REQ_INIT_MODE", active low.
15	30	SRC3E_P	"SRC_RESET_ERRORS", active low.
GND	1		"GND"
CLK P	20	SYNC_P	"J3D19_COPY".