Fermi National Accelerator Laboratory

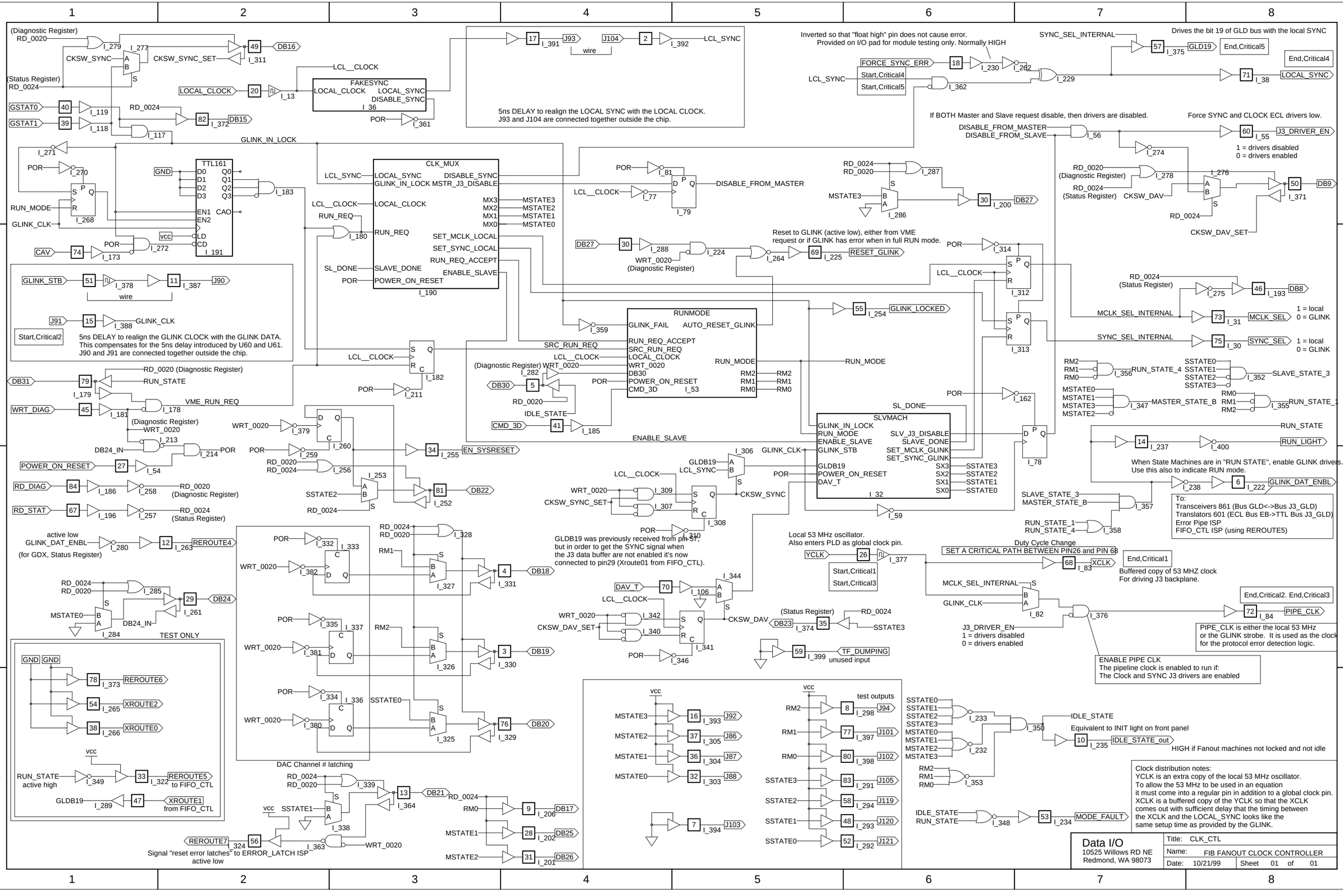
SVX II Silicon Strip Detector Upgrade Project Readout Electronics

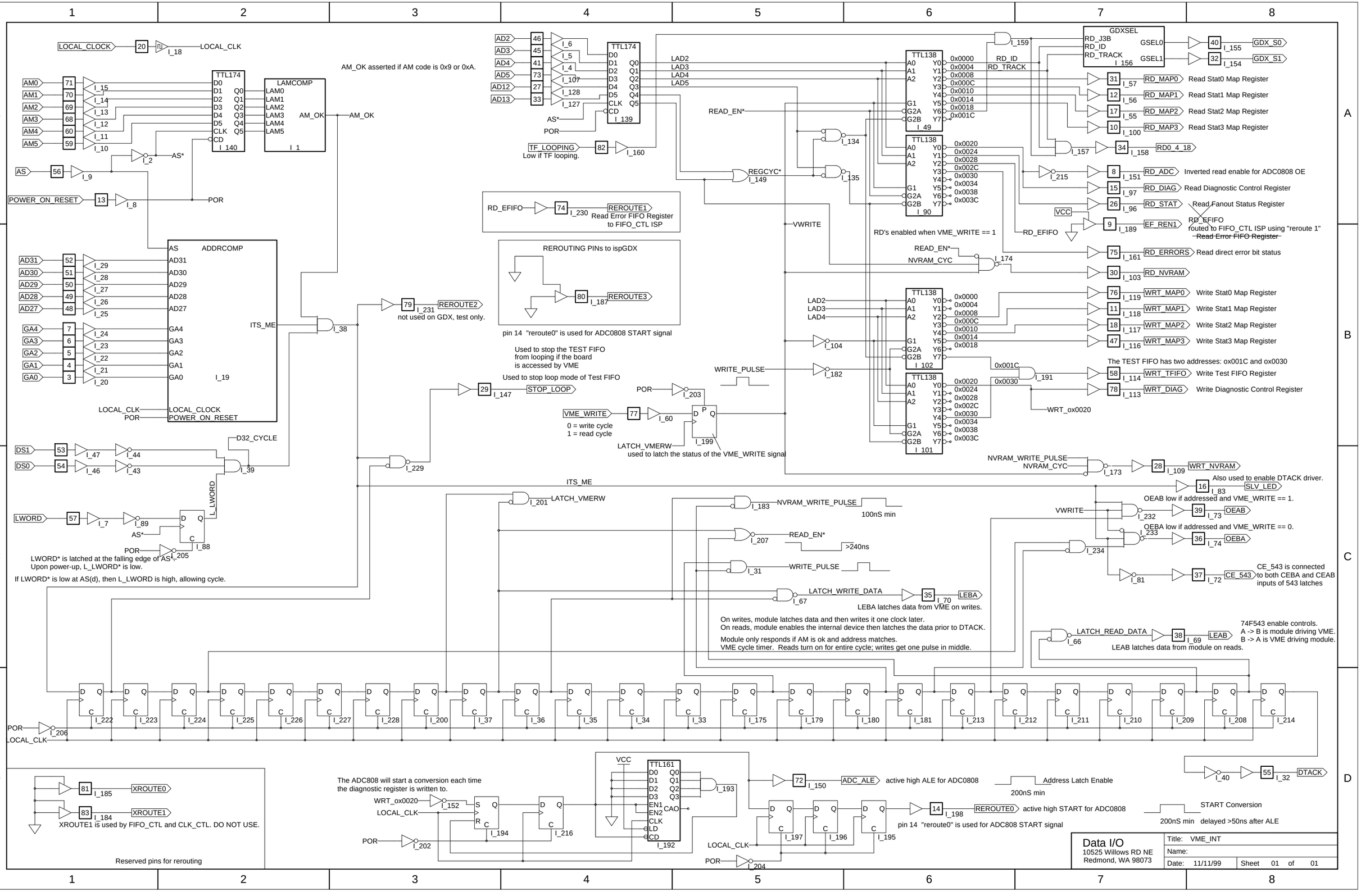
Programmable Logic Schematics of the FIB SUBRACK FANOUT MODULE (FFO) Revision B

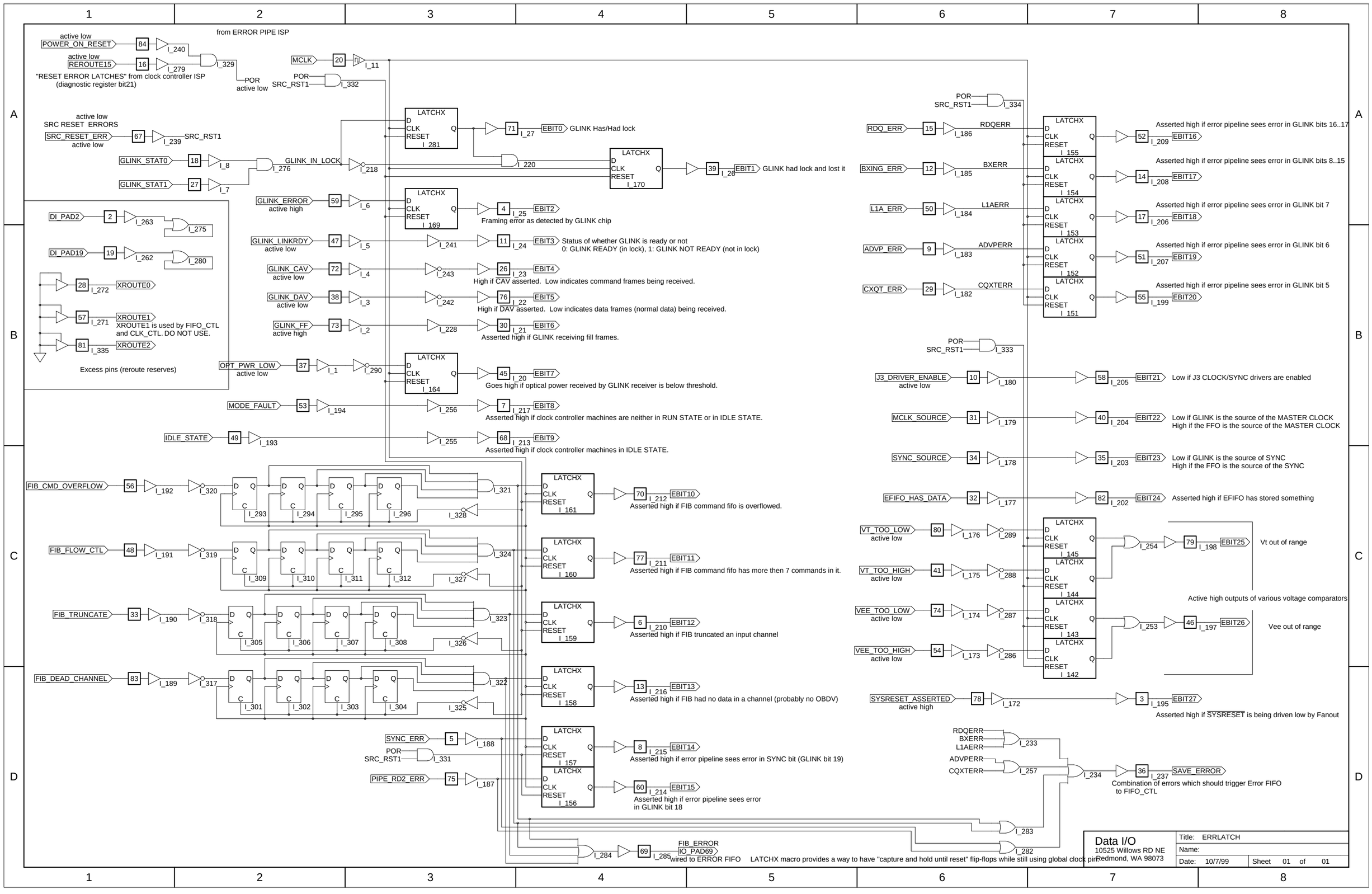
November 10, 2000

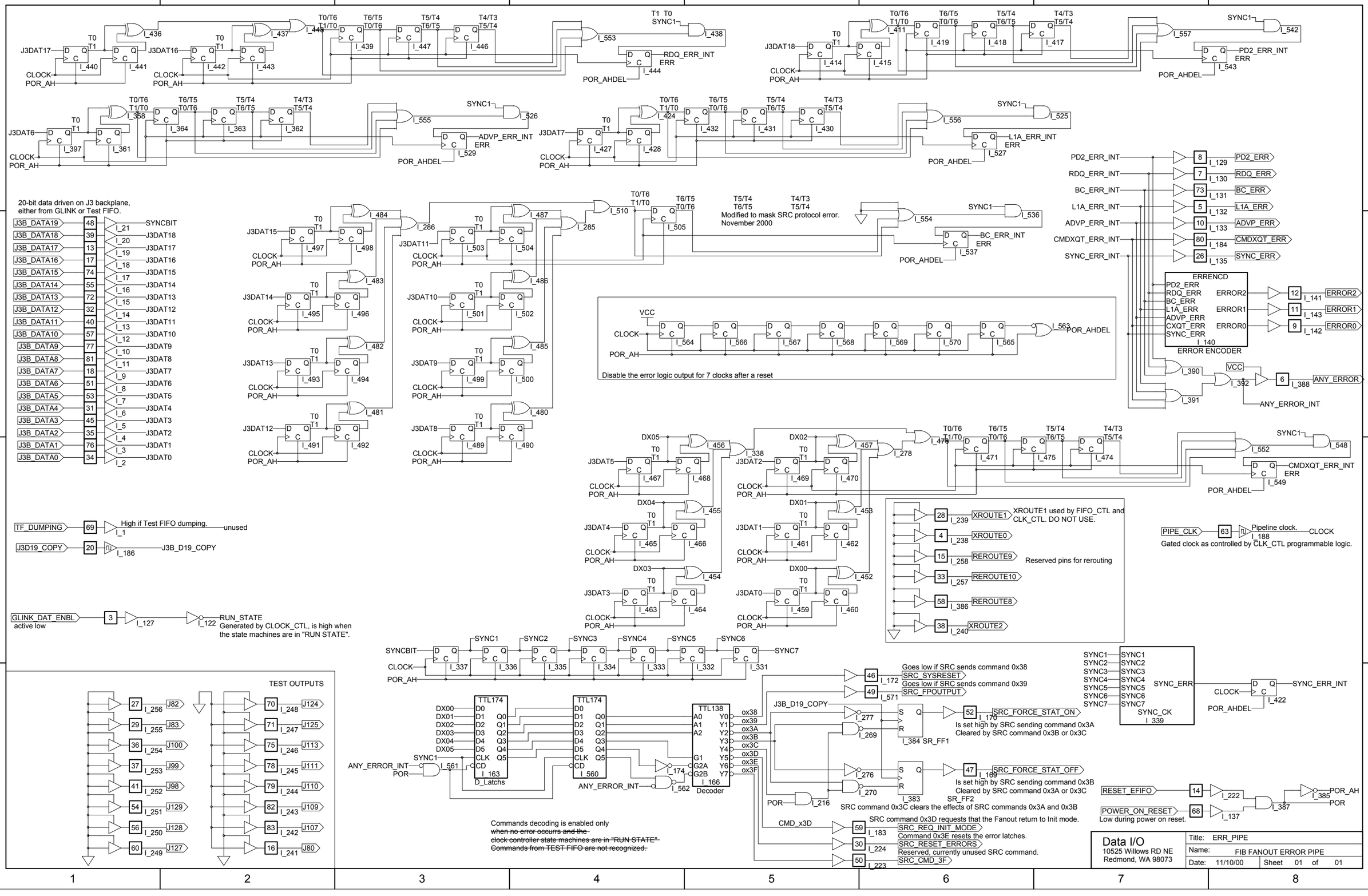
John Anderson, Kerry Woodbury, John Chramowicz, Stefano Rapisarda

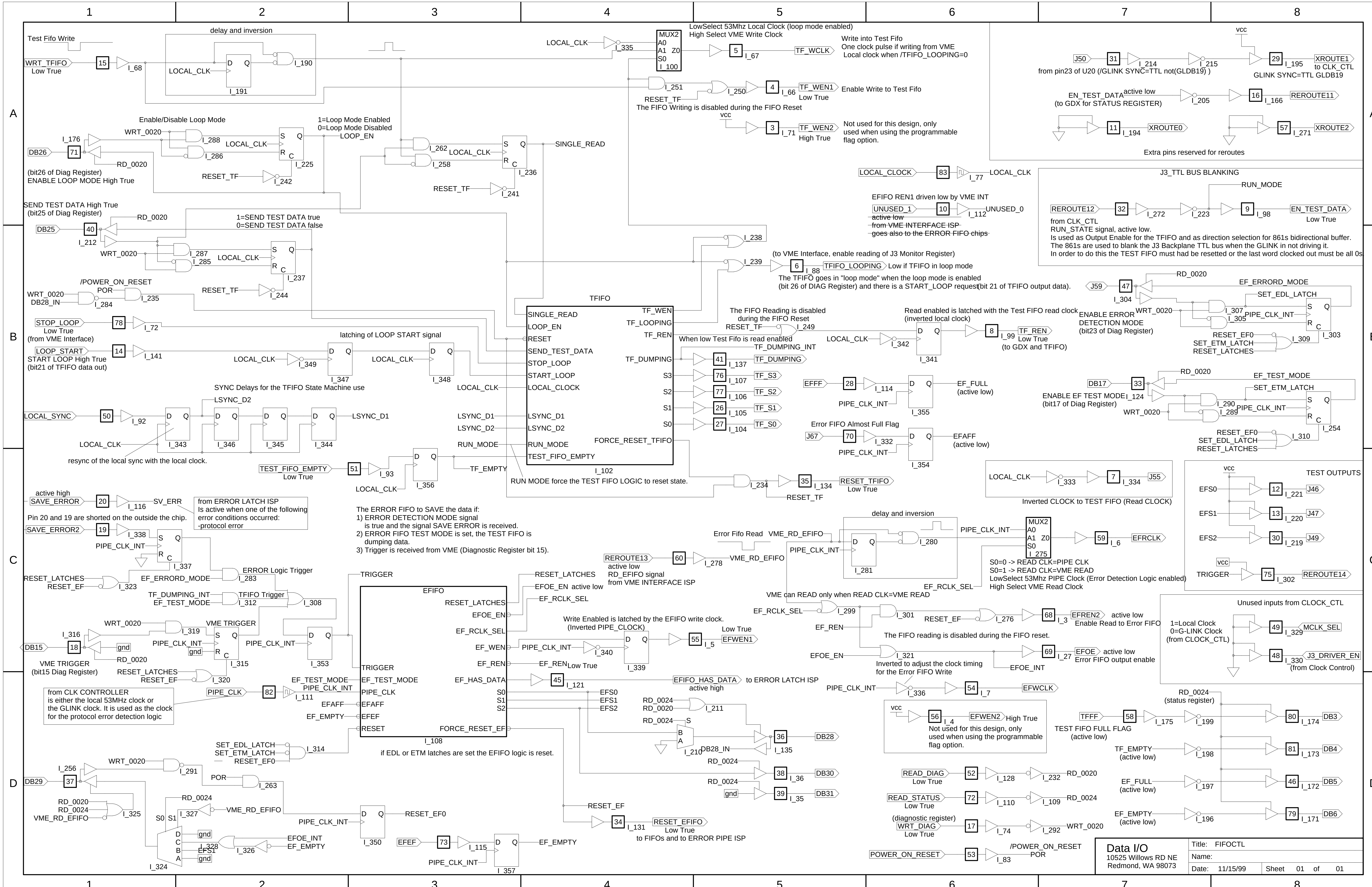
Document # ESE-SVX-990907


(Diagnostic Register)
RD_0020
I_279
I_277
CKSW_SYNC
CKSW_SYNC_SET
49
DB16
I_311
LCL__CLOCK
(Status Register)
RD_0024
LOCAL_CLOCK
20
I_13
FAKESYNC
LOCAL_CLOCK
LOCAL_SYNC
DISABLE_SYNC
I_36
POR
I_361
GSTAT0
40
I_119
GSTAT1
39
I_118
I_117
RD_0024
82
DB15
I_372
GLINK_IN_LOCK
17
I_391
J93
wire
J104
2
I_392
LCL_SYNC
5ns DELAY to realign the LOCAL SYNC with the LOCAL CLOCK.
J93 and J104 are connected together outside the chip.
Inverted so that "float high" pin does not cause error.
Provided on I/O pad for module testing only. Normally HIGH
FORCE_SYNC_ERR
18
I_230
I_262
LCL_SYNC
Start,Critical4
Start,Critical5
I_362
I_229
SYNC_SEL_INTERNAL
57
I_375
GLD19
End,Critical5
Drives the bit 19 of GLD bus with the local SYNC
End,Critical4
71
I_38
LOCAL_SYNC
If BOTH Master and Slave request disable, then drivers are disabled.
Force SYNC and CLOCK ECL drivers low.
DISABLE_FROM_MASTER
DISABLE_FROM_SLAVE
I_56
60
I_55
J3_DRIVER_EN
I_274
1 = drivers disabled
0 = drivers enabled
I_271
POR
I_270
TTL161
GND
D0
D1
D2
D3
Q0
Q1
Q2
Q3
EN1
EN2
CAO
CLD
CD
I_191
I_183
RUN_MODE
I_268
GLINK_CLK
vcc
CAV
74
I_173
POR
I_272
CLK_MUX
LCL_SYNC
LOCAL_SYNC
GLINK_IN_LOCK
DISABLE_SYNC
MSTR_J3_DISABLE
LCL__CLOCK
LOCAL_CLOCK
RUN_REQ
I_180
SL_DONE
SLAVE_DONE
POR
POWER_ON_RESET
MX3
MX2
MX1
MX0
MSTATE3
MSTATE2
MSTATE1
MSTATE0
SET_MCLK_LOCAL
SET_SYNC_LOCAL
RUN_REQ_ACCEPT
ENABLE_SLAVE
I_190
POR
I_81
LCL__CLOCK
I_77
D
P
Q
I_79
DISABLE_FROM_MASTER
RD_0024
RD_0020
I_287
MSTATE3
B
A
S
I_286
30
DB27
I_200
RD_0020
(Diagnostic Register)
RD_0024
(Status Register)
I_278
CKSW_DAV
I_276
A
B
S
RD_0024
50
DB9
I_371
CKSW_DAV_SET
DB27
30
I_288
WRT_0020
(Diagnostic Register)
I_224
I_264
69
I_225
RESET_GLINK
Reset to GLINK (active low), either from VME
request or if GLINK has error when in full RUN mode.
POR
I_314
LCL__CLOCK
S
P
Q
R
I_312
RD_0024
(Status Register)
I_275
46
I_193
DB8
MCLK_SEL_INTERNAL
73
I_31
MCLK_SEL
1 = local
0 = GLINK
SYNC_SEL_INTERNAL
75
I_30
SYNC_SEL
1 = local
0 = GLINK
I_313
GLINK_STB
51
I_378
11
I_387
J90
wire
J91
15
I_388
GLINK_CLK
Start,Critical2
5ns DELAY to realign the GLINK CLOCK with the GLINK DATA.
This compensates for the 5ns delay introduced by U60 and U61.
J90 and J91 are connected together outside the chip.
I_359
RUNMODE
GLINK_FAIL
AUTO_RESET_GLINK
RUN_REQ_ACCEPT
SRC_RUN_REQ
LOCAL_CLOCK
WRT_0020
DB30
POWER_ON_RESET
CMD_3D
I_53
RUN_MODE
RM2
RM1
RM0
55
I_254
GLINK_LOCKED
RUN_MODE
SRC_RUN_REQ
LCL__CLOCK
(Diagnostic Register) WRT_0020
I_282
DB30
5
RD_0020
IDLE_STATE
CMD_3D
41
I_185
POR
I_211
S
Q
R
C
I_182
RM2
RM1
RM0
MSTATE0
MSTATE1
MSTATE3
MSTATE2
I_356
RUN_STATE_4
SSTATE0
SSTATE1
SSTATE2
SSTATE3
I_352
SLAVE_STATE_3
I_347
MASTER_STATE_B
I_355
RUN_STATE_1
RD_0020 (Diagnostic Register)
DB31
79
RUN_STATE
I_179
VME_RUN_REQ
WRT_DIAG
45
I_181
I_178
(Diagnostic Register)
WRT_0020
I_213
DB24_IN
I_214
POR
POWER_ON_RESET
27
I_54
WRT_0020
I_379
D
Q
C
I_260
POR
I_259
RD_0020
RD_0024
I_256
34
I_255
EN_SYSRESET
I_253
SSTATE2
A
B
S
81
DB22
I_252
RD_0024
ENABLE_SLAVE
I_306
GLINK_CLK
GLDB19
LCL_SYNC
A
B
S
POR
LCL__CLOCK
WRT_0020
I_309
CKSW_SYNC_SET
I_307
S
Q
R
C
I_308
CKSW_SYNC
POR
I_310
SLVMACH
GLINK_IN_LOCK
RUN_MODE
ENABLE_SLAVE
GLINK_STB
GLDB19
POWER_ON_RESET
DAV_T
SLV_J3_DISABLE
SLAVE_DONE
SET_MCLK_GLINK
SET_SYNC_GLINK
SX3
SX2
SX1
SX0
SSTATE3
SSTATE2
SSTATE1
SSTATE0
I_32
I_59
SL_DONE
POR
I_162
D
P
Q
I_78
RUN_STATE
14
I_237
I_400
RUN_LIGHT
When State Machines are in "RUN STATE", enable GLINK drivers.
Use this also to indicate RUN mode.
I_238
6
I_222
GLINK_DAT_ENBL
SLAVE_STATE_3
MASTER_STATE_B
I_357
RUN_STATE_1
RUN_STATE_4
I_358
To:
Transceivers 861 (Bus GLD<->Bus J3_GLD)
Translators 601 (ECL Bus EB->TTL Bus J3_GLD)
Error Pipe ISP
FIFO_CTL ISP (using REROUTE5)
RD_DIAG
84
I_186
I_258
RD_0020
(Diagnostic Register)
RD_STAT
67
I_196
I_257
RD_0024
(Status Register)
active low
GLINK_DAT_ENBL
(for GDX, Status Register)
I_280
12
I_263
REROUTE4
POR
I_332
I_333
C
D
Q
WRT_0020
I_382
RD_0024
RD_0020
I_328
RM1
S
B
A
I_327
4
DB18
I_331
RD_0024
RD_0020
I_285
29
DB24
MSTATE0
B
A
S
DB24_IN
I_261
I_284
TEST ONLY
POR
I_335
I_337
C
D
Q
WRT_0020
I_381
RM2
S
B
A
I_326
3
DB19
I_330
POR
I_334
I_336
C
D
Q
WRT_0020
I_380
SSTATE0
S
B
A
I_325
76
DB20
I_329
DAC Channel # latching
GLDB19 was previously received from pin 37,
but in order to get the SYNC signal when
the J3 data buffer are not enabled it's now
connected to pin29 (Xroute01 from FIFO_CTL).
Local 53 MHz oscillator.
Also enters PLD as global clock pin.
YCLK
26
I_377
Start,Critical1
Start,Critical3
Duty Cycle Change
SET A CRITICAL PATH BETWEEN PIN26 and PIN 68
68
I_83
XCLK
End,Critical1
Buffered copy of 53 MHZ clock
For driving J3 backplane.
DAV_T
70
I_106
I_344
A
B
S
LCL__CLOCK
WRT_0020
I_342
CKSW_DAV_SET
I_340
S
Q
R
C
I_341
CKSW_DAV
POR
I_346
(Status Register)
DB23
I_374
35
RD_0024
SSTATE3
59
I_399
TF_DUMPING
unused input
MCLK_SEL_INTERNAL
GLINK_CLK
S
B
A
I_82
I_376
J3_DRIVER_EN
1 = drivers disabled
0 = drivers enabled
End,Critical2. End,Critical3
72
I_84
PIPE_CLK
PIPE_CLK is either the local 53 MHz
or the GLINK strobe. It is used as the clock
for the protocol error detection logic.
ENABLE PIPE CLK
The pipeline clock is enabled to run if:
The Clock and SYNC J3 drivers are enabled
GND
GND
78
I_373
REROUTE6
54
I_265
XROUTE2
38
I_266
XROUTE0
vcc
RUN_STATE
active high
I_349
33
I_322
REROUTE5
to FIFO_CTL
GLDB19
I_289
47
XROUTE1
from FIFO_CTL
RD_0024
RD_0020
I_339
13
I_364
DB21
vcc
SSTATE1
A
B
S
I_338
REROUTE7
56
I_324
Signal "reset error latches" to ERROR_LATCH ISP
active low
I_363
WRT_0020
RD_0024
RM0
9
I_206
DB17
MSTATE1
28
I_202
DB25
MSTATE2
31
I_201
DB26
vcc
MSTATE3
16
I_393
J92
MSTATE2
37
I_305
J86
MSTATE1
36
I_304
J87
MSTATE0
32
I_303
J88
7
I_394
J103
vcc
RM2
test outputs
8
I_298
J94
RM1
77
I_397
J101
RM0
80
I_398
J102
SSTATE3
83
I_291
J105
SSTATE2
58
I_294
J119
SSTATE1
48
I_293
J120
SSTATE0
52
I_292
J121
SSTATE0
SSTATE1
SSTATE2
SSTATE3
MSTATE0
MSTATE1
MSTATE2
MSTATE3
I_233
I_232
I_350
IDLE_STATE
Equivalent to INIT light on front panel
10
I_235
IDLE_STATE_out
HIGH if Fanout machines not locked and not idle
RM2
RM1
RM0
I_353
IDLE_STATE
RUN_STATE
I_348
53
I_234
MODE_FAULT
Clock distribution notes:
YCLK is an extra copy of the local 53 MHz oscillator.
To allow the 53 MHz to be used in an equation
it must come into a regular pin in addition to a global clock pin.
XCLK is a buffered copy of the YCLK so that the XCLK
comes out with sufficient delay that the timing between
the XCLK and the LOCAL_SYNC looks like the
same setup time as provided by the GLINK.
Data I/O
10525 Willows RD NE
Redmond, WA 98073
Title: CLK_CTL
Name: FIB FANOUT CLOCK CONTROLLER
Date: 10/21/99
Sheet 01 of 01

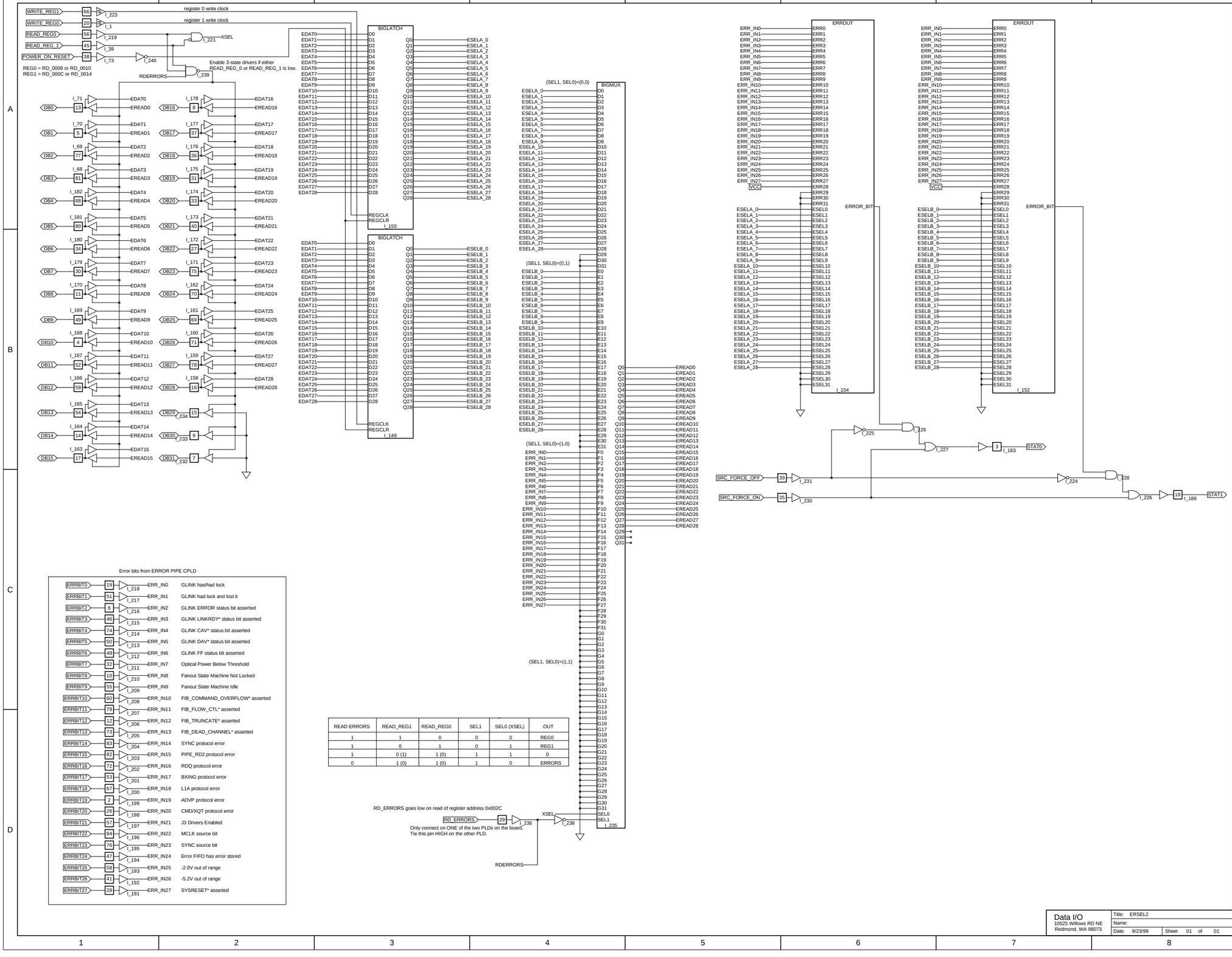

LOCAL_CLOCK
20
I_18
LOCAL_CLK
AM_OK asserted if AM code is 0x9 or 0xA.
AM0
AM1
AM2
AM3
AM4
AM5
71
70
69
68
60
59
I_15
I_14
I_13
I_12
I_11
I_10
TTL174
LAMCOMP
LAM0
LAM1
LAM2
LAM3
LAM4
LAM5
AM_OK
I_140
I_1
I_2
AS*
AS
56
I_9
POWER_ON_RESET
13
I_8
POR
AD2
AD3
AD4
AD5
AD12
AD13
46
45
41
73
27
33
I_6
I_5
I_4
I_107
I_128
I_127
I_139
LAD2
LAD3
LAD4
LAD5
TF_LOOPING
Low if TF looping.
82
I_160
READ_EN*
REGCYC*
I_149
I_134
I_135
VWRITE
TTL138
I_49
I_90
I_102
I_101
0x0000
0x0004
0x0008
0x000C
0x0010
0x0014
0x0018
0x001C
0x0020
0x0024
0x0028
0x002C
0x0030
0x0034
0x0038
0x003C
I_159
RD_ID
RD_TRACK
GDXSEL
RD_J3B
RD_ID
RD_TRACK
I_156
GSEL0
GSEL1
40
32
I_155
I_154
GDX_S0
GDX_S1
31
12
17
10
I_57
I_56
I_55
I_100
RD_MAP0
RD_MAP1
RD_MAP2
RD_MAP3
Read Stat0 Map Register
Read Stat1 Map Register
Read Stat2 Map Register
Read Stat3 Map Register
I_157
34
I_158
RD0_4_18
I_215
8
I_151
RD_ADC
Inverted read enable for ADC0808 OE
15
I_97
RD_DIAG
Read Diagnostic Control Register
26
I_96
RD_STAT
Read Fanout Status Register
VCC
9
I_189
EF_REN1
RD_EFIFO
routed to FIFO_CTL ISP using "reroute 1"
Read Error FIFO Register
RD_EFIFO
74
I_230
REROUTE1
Read Error FIFO Register
to FIFO_CTL ISP
RD's enabled when VME_WRITE == 1
READ_EN*
NVRAM_CYC
I_174
75
I_161
RD_ERRORS
Read direct error bit status
30
I_103
RD_NVRAM
REROUTING PINs to ispGDX
80
I_187
REROUTE3
LAD2
LAD3
LAD4
I_104
WRITE_PULSE
I_182
76
I_119
WRT_MAP0
Write Stat0 Map Register
11
I_118
WRT_MAP1
Write Stat1 Map Register
18
I_117
WRT_MAP2
Write Stat2 Map Register
47
I_116
WRT_MAP3
Write Stat3 Map Register
The TEST FIFO has two addresses: 0x001C and 0x0030
0x001C
0x0030
I_191
58
I_114
WRT_TFIFO
Write Test FIFO Register
78
I_113
WRT_DIAG
Write Diagnostic Control Register
WRT_ox0020
ADDRCOMP
AS
AD31
AD30
AD29
AD28
AD27
GA4
GA3
GA2
GA1
GA0
52
51
50
49
48
7
6
5
4
3
I_29
I_28
I_27
I_26
I_25
I_24
I_23
I_22
I_21
I_20
I_19
ITS_ME
I_38
LOCAL_CLK
POR
LOCAL_CLOCK
POWER_ON_RESET
79
I_231
REROUTE2
not used on GDX, test only.
pin 14 "reroute0" is used for ADC0808 START signal
Used to stop the TEST FIFO
from looping if the board
is accessed by VME
Used to stop loop mode of Test FIFO
29
I_147
STOP_LOOP
POR
I_203
VME_WRITE
77
I_60
0 = write cycle
1 = read cycle
D
P
Q
I_199
LATCH_VMERW
used to latch the status of the VME_WRITE signal
I_229
DS1
DS0
53
54
I_47
I_46
I_44
I_43
I_39
D32_CYCLE
L_LWORD
LWORD
57
I_7
I_89
AS*
C
I_88
POR
I_205
LWORD* is latched at the falling edge of AS*.
Upon power-up, L_LWORD* is low.
If LWORD* is low at AS(d), then L_LWORD is high, allowing cycle.
NVRAM_WRITE_PULSE
NVRAM_CYC
I_173
28
I_109
WRT_NVRAM
Also used to enable DTACK driver.
16
I_83
SLV_LED
OEAB low if addressed and VME_WRITE == 1.
VWRITE
I_232
39
I_73
OEAB
OEBA low if addressed and VME_WRITE == 0.
I_233
36
I_74
OEBA
I_234
I_81
37
I_72
CE_543
CE_543 is connected
to both CEBA and CEAB
inputs of 543 latches
ITS_ME
I_201
LATCH_VMERW
I_183
NVRAM_WRITE_PULSE
100nS min
I_207
READ_EN*
>240ns
I_31
WRITE_PULSE
I_67
LATCH_WRITE_DATA
35
I_70
LEBA
LEBA latches data from VME on writes.
On writes, module latches data and then writes it one clock later.
On reads, module enables the internal device then latches the data prior to DTACK.
Module only responds if AM is ok and address matches.
VME cycle timer. Reads turn on for entire cycle; writes get one pulse in middle.
LATCH_READ_DATA
I_66
38
I_69
LEAB
LEAB latches data from module on reads.
74F543 enable controls.
A -> B is module driving VME.
B -> A is VME driving module.
I_222
I_223
I_224
I_225
I_226
I_227
I_228
I_200
I_37
I_36
I_35
I_34
I_33
I_175
I_179
I_180
I_181
I_213
I_212
I_211
I_210
I_209
I_208
I_214
POR
I_206
LOCAL_CLK
I_40
55
I_32
DTACK
81
83
I_185
I_184
XROUTE0
XROUTE1
XROUTE1 is used by FIFO_CTL and CLK_CTL. DO NOT USE.
Reserved pins for rerouting
The ADC808 will start a conversion each time
the diagnostic register is written to.
WRT_ox0020
I_152
LOCAL_CLK
POR
I_202
S
R
I_194
I_216
VCC
TTL161
D0
D1
D2
D3
EN1
EN2
CLK
LD
CD
CAO
Q0
Q1
Q2
Q3
I_193
I_192
72
I_150
ADC_ALE
active high ALE for ADC0808
Address Latch Enable
200nS min
14
I_198
REROUTE0
active high START for ADC0808
pin 14 "reroute0" is used for ADC808 START signal
START Conversion
200nS min delayed >50ns after ALE
I_197
I_196
I_195
I_204
Data I/O
10525 Willows RD NE
Redmond, WA 98073
Title: VME_INT
Name:
Date: 11/11/99
Sheet 01 of 01


from ERROR PIPE ISP
active low POWER_ON_RESET
84
I_240
active low REROUTE15
16
I_279
I_329
"RESET ERROR LATCHES" from clock controller ISP (diagnostic register bit21)
POR active low
MCLK
20
I_11
POR SRC_RST1
I_332
active low SRC RESET ERRORS
SRC_RESET_ERR active low
67
I_239
SRC_RST1
GLINK_STAT0
18
I_8
GLINK_STAT1
27
I_7
I_276
GLINK_IN_LOCK
I_218
I_220
LATCHX D CLK RESET Q I_281
71
I_27
EBIT0
GLINK Has/Had lock
LATCHX D CLK RESET Q I_170
39
I_26
EBIT1
GLINK had lock and lost it
GLINK_ERROR active high
59
I_6
LATCHX D CLK RESET Q I_169
4
I_25
EBIT2
Framing error as detected by GLINK chip
GLINK_LINKRDY active low
47
I_5
I_241
11
I_24
EBIT3
Status of whether GLINK is ready or not
0: GLINK READY (in lock), 1: GLINK NOT READY (not in lock)
GLINK_CAV active low
72
I_4
I_243
26
I_23
EBIT4
High if CAV asserted. Low indicates command frames being received.
GLINK_DAV active low
38
I_3
I_242
76
I_22
EBIT5
High if DAV asserted. Low indicates data frames (normal data) being received.
GLINK_FF active high
73
I_2
I_228
30
I_21
EBIT6
Asserted high if GLINK receiving fill frames.
DI_PAD2
2
I_263
I_275
DI_PAD19
19
I_262
I_280
28
I_272
XROUTE0
57
I_271
XROUTE1
XROUTE1 is used by FIFO_CTL and CLK_CTL. DO NOT USE.
81
I_335
XROUTE2
Excess pins (reroute reserves)
OPT_PWR_LOW active low
37
I_1
I_290
LATCHX D CLK RESET Q I_164
45
I_20
EBIT7
Goes high if optical power received by GLINK receiver is below threshold.
MODE_FAULT
53
I_194
I_256
7
I_217
EBIT8
Asserted high if clock controller machines are neither in RUN STATE or in IDLE STATE.
IDLE_STATE
49
I_193
I_255
68
I_213
EBIT9
Asserted high if clock controller machines in IDLE STATE.
FIB_CMD_OVERFLOW
56
I_192
I_320
I_293
I_294
I_295
I_296
I_328
I_321
LATCHX D CLK RESET Q I_161
70
I_212
EBIT10
Asserted high if FIB command fifo is overflowed.
FIB_FLOW_CTL
48
I_191
I_319
I_309
I_310
I_311
I_312
I_327
I_324
LATCHX D CLK RESET Q I_160
77
I_211
EBIT11
Asserted high if FIB command fifo has more then 7 commands in it.
FIB_TRUNCATE
33
I_190
I_318
I_305
I_306
I_307
I_308
I_326
I_323
LATCHX D CLK RESET Q I_159
6
I_210
EBIT12
Asserted high if FIB truncated an input channel
FIB_DEAD_CHANNEL
83
I_189
I_317
I_301
I_302
I_303
I_304
I_325
I_322
LATCHX D CLK RESET Q I_158
13
I_216
EBIT13
Asserted high if FIB had no data in a channel (probably no OBDV)
SYNC_ERR
5
I_188
POR SRC_RST1
I_331
LATCHX D CLK RESET Q I_157
8
I_215
EBIT14
Asserted high if error pipeline sees error in SYNC bit (GLINK bit 19)
PIPE_RD2_ERR
75
I_187
LATCHX D CLK RESET Q I_156
60
I_214
EBIT15
Asserted high if error pipeline sees error in GLINK bit 18
I_284
69
I_285
FIB_ERROR
IO_PAD69
wired to ERROR FIFO
LATCHX macro provides a way to have "capture and hold until reset" flip-flops while still using global clock pin
POR SRC_RST1
I_334
RDQ_ERR
15
I_186
RDQERR
BXING_ERR
12
I_185
BXERR
L1A_ERR
50
I_184
L1AERR
ADVP_ERR
9
I_183
ADVPERR
CXQT_ERR
29
I_182
CQXTERR
LATCHX D CLK RESET Q I_155
52
I_209
EBIT16
Asserted high if error pipeline sees error in GLINK bits 16..17
LATCHX D CLK RESET Q I_154
14
I_208
EBIT17
Asserted high if error pipeline sees error in GLINK bits 8..15
LATCHX D CLK RESET Q I_153
17
I_206
EBIT18
Asserted high if error pipeline sees error in GLINK bit 7
LATCHX D CLK RESET Q I_152
51
I_207
EBIT19
Asserted high if error pipeline sees error in GLINK bit 6
LATCHX D CLK RESET Q I_151
55
I_199
EBIT20
Asserted high if error pipeline sees error in GLINK bit 5
POR SRC_RST1
I_333
J3_DRIVER_ENABLE active low
10
I_180
58
I_205
EBIT21
Low if J3 CLOCK/SYNC drivers are enabled
MCLK_SOURCE
31
I_179
40
I_204
EBIT22
Low if GLINK is the source of the MASTER CLOCK
High if the FFO is the source of the MASTER CLOCK
SYNC_SOURCE
34
I_178
35
I_203
EBIT23
Low if GLINK is the source of SYNC
High if the FFO is the source of the SYNC
EFIFO_HAS_DATA
32
I_177
82
I_202
EBIT24
Asserted high if EFIFO has stored something
VT_TOO_LOW active low
80
I_176
I_289
VT_TOO_HIGH active low
41
I_175
I_288
VEE_TOO_LOW active low
74
I_174
I_287
VEE_TOO_HIGH active low
54
I_173
I_286
LATCHX D CLK RESET Q I_145
LATCHX D CLK RESET Q I_144
LATCHX D CLK RESET Q I_143
LATCHX D CLK RESET Q I_142
I_254
79
I_198
EBIT25
Vt out of range
Active high outputs of various voltage comparators
I_253
46
I_197
EBIT26
Vee out of range
SYSRESET_ASSERTED active high
78
I_172
3
I_195
EBIT27
Asserted high if SYSRESET is being driven low by Fanout
RDQERR
BXERR
L1AERR
I_233
ADVPERR
CQXTERR
I_257
I_234
36
I_237
SAVE_ERROR
Combination of errors which should trigger Error FIFO to FIFO_CTL
I_283
I_282
Data I/O
10525 Willows RD NE
Redmond, WA 98073
Title: ERRLATCH
Name:
Date: 10/7/99
Sheet 01 of 01


1
2
3
4
5
6
7
8
A
B
C
D
J3DAT17
J3DAT16
J3DAT18
J3DAT6
J3DAT7
CLOCK
POR_AH
T0
T1
T0/T6
T1/T0
T6/T5
T0/T6
T5/T4
T6/T5
T4/T3
T5/T4
I_436
I_437
I_438
I_439
I_440
I_441
I_442
I_443
I_444
I_446
I_447
I_448
I_553
I_554
I_555
I_556
I_557
I_358
I_361
I_362
I_363
I_364
I_397
I_411
I_414
I_415
I_417
I_418
I_419
I_424
I_427
I_428
I_430
I_431
I_432
RDQ_ERR_INT
ERR
POR_AHDEL
SYNC1
I_542
PD2_ERR_INT
I_543
ADVP_ERR_INT
I_529
I_526
L1A_ERR_INT
I_527
I_525
20-bit data driven on J3 backplane,
either from GLINK or Test FIFO.
J3B_DATA19
J3B_DATA18
J3B_DATA17
J3B_DATA16
J3B_DATA15
J3B_DATA14
J3B_DATA13
J3B_DATA12
J3B_DATA11
J3B_DATA10
J3B_DATA9
J3B_DATA8
J3B_DATA7
J3B_DATA6
J3B_DATA5
J3B_DATA4
J3B_DATA3
J3B_DATA2
J3B_DATA1
J3B_DATA0
SYNCBIT
J3DAT18
J3DAT17
J3DAT16
J3DAT15
J3DAT14
J3DAT13
J3DAT12
J3DAT11
J3DAT10
J3DAT9
J3DAT8
J3DAT7
J3DAT6
J3DAT5
J3DAT4
J3DAT3
J3DAT2
J3DAT1
J3DAT0
I_21
I_20
I_19
I_18
I_17
I_16
I_15
I_14
I_13
I_12
I_10
I_11
I_9
I_8
I_7
I_6
I_5
I_4
I_3
I_2
I_484
I_483
I_482
I_481
I_480
I_497
I_498
I_495
I_496
I_493
I_494
I_491
I_492
I_286
I_487
I_486
I_485
I_503
I_504
I_501
I_502
I_499
I_500
I_489
I_490
I_510
I_505
I_285
T5/T4
T6/T5
T4/T3
T5/T4
Modified to mask SRC protocol error.
November 2000
I_554
I_536
BC_ERR_INT
I_537
PD2_ERR_INT
RDQ_ERR_INT
BC_ERR_INT
L1A_ERR_INT
ADVP_ERR_INT
CMDXQT_ERR_INT
SYNC_ERR_INT
8
I_129
PD2_ERR
7
I_130
RDQ_ERR
73
I_131
BC_ERR
5
I_132
L1A_ERR
10
I_133
ADVP_ERR
80
I_184
CMDXQT_ERR
26
I_135
SYNC_ERR
ERRENCD
PD2_ERR
RDQ_ERR
BC_ERR
L1A_ERR
ADVP_ERR
CXQT_ERR
SYNC_ERR
I_140
ERROR ENCODER
ERROR2
ERROR1
ERROR0
12
I_141
ERROR2
11
I_143
ERROR1
9
I_142
ERROR0
VCC
I_390
I_391
I_392
6
I_388
ANY_ERROR
ANY_ERROR_INT
I_563
I_564
I_566
I_567
I_568
I_569
I_570
I_565
Disable the error logic output for 7 clocks after a reset
DX05
DX04
DX03
DX02
DX01
DX00
I_456
I_455
I_454
I_457
I_453
I_452
I_338
I_278
I_467
I_468
I_465
I_466
I_463
I_464
I_469
I_470
I_461
I_462
I_459
I_460
I_479
I_471
I_475
I_474
I_548
I_552
CMDXQT_ERR_INT
I_549
XROUTE1
XROUTE0
REROUTE9
REROUTE10
REROUTE8
XROUTE2
28
I_239
4
I_238
15
I_258
33
I_257
58
I_386
38
I_240
XROUTE1 used by FIFO_CTL and
CLK_CTL. DO NOT USE.
Reserved pins for rerouting
PIPE_CLK
63
I_188
Pipeline clock.
CLOCK
Gated clock as controlled by CLK_CTL programmable logic.
TF_DUMPING
69
I_1
High if Test FIFO dumping.
unused
J3D19_COPY
20
I_186
J3B_D19_COPY
GLINK_DAT_ENBL
active low
3
I_127
I_122
RUN_STATE
Generated by CLOCK_CTL, is high when
the state machines are in "RUN STATE".
TEST OUTPUTS
27
I_256
J82
29
I_255
J83
36
I_254
J100
37
I_253
J99
41
I_252
J98
54
I_251
J129
56
I_250
J128
60
I_249
J127
70
I_248
J124
71
I_247
J125
75
I_246
J113
78
I_245
J111
79
I_244
J110
82
I_243
J109
83
I_242
J107
16
I_241
J80
SYNC1
SYNC2
SYNC3
SYNC4
SYNC5
SYNC6
SYNC7
I_337
I_336
I_335
I_334
I_333
I_332
I_331
TTL174
D0
D1
D2
D3
D4
D5
CLK
CD
Q0
Q1
Q2
Q3
Q4
Q5
I_163
D_Latches
I_560
TTL138
A0
A1
A2
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
ox38
ox39
ox3A
ox3B
ox3C
ox3D
ox3E
ox3F
I_166
Decoder
ANY_ERROR_INT
POR
I_561
I_174
I_562
I_216
46
I_172
SRC_SYSRESET
Goes low if SRC sends command 0x38
49
I_571
SRC_FPOUTPUT
Goes low if SRC sends command 0x39
J3B_D19_COPY
I_277
I_269
I_276
I_270
S
R
I_384 SR_FF1
I_383 SR_FF2
52
I_170
SRC_FORCE_STAT_ON
Is set high by SRC sending command 0x3A
Cleared by SRC command 0x3B or 0x3C
47
I_169
SRC_FORCE_STAT_OFF
Is set high by SRC sending command 0x3B
Cleared by SRC command 0x3A or 0x3C
SRC command 0x3C clears the effects of SRC commands 0x3A and 0x3B
SRC command 0x3D requests that the Fanout return to Init mode.
CMD_x3D
59
I_183
SRC_REQ_INIT_MODE
Command 0x3E resets the error latches.
30
I_224
SRC_RESET_ERRORS
Reserved, currently unused SRC command.
50
I_223
SRC_CMD_3F
SYNC_ERR
SYNC_CK
I_339
SYNC_ERR_INT
I_422
RESET_EFIFO
14
I_222
POR_AH
I_385
POR
POWER_ON_RESET
68
I_137
I_387
Low during power on reset.
Commands decoding is enabled only
when no error occurrs and the
clock controller state machines are in "RUN STATE"
Commands from TEST FIFO are not recognized.
Data I/O
10525 Willows RD NE
Redmond, WA 98073
Title: ERR_PIPE
Name: FIB FANOUT ERROR PIPE
Date: 11/10/00
Sheet 01 of 01

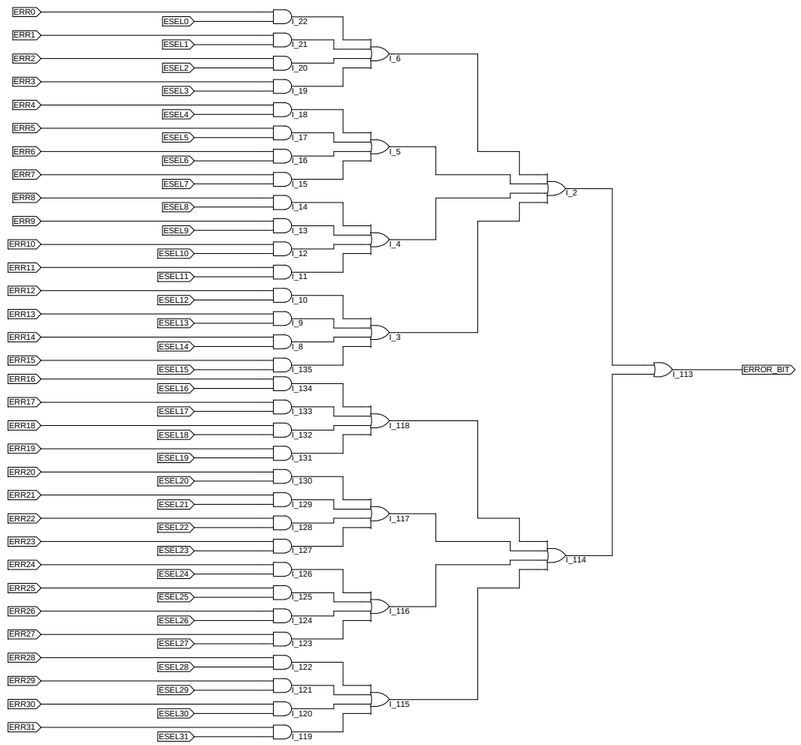


Test Fifo Write
WRT_TFIFO
Low True
delay and inversion
LOCAL_CLK
LowSelect 53Mhz Local Clock (loop mode enabled)
High Select VME Write Clock
MUX2
TF_WCLK
Write into Test Fifo
One clock pulse if writing from VME
Local clock when /TFIFO_LOOPING=0
TF_WEN1
Enable Write to Test Fifo
Low True
RESET_TF
The FIFO Writing is disabled during the FIFO Reset
TF_WEN2
High True
Not used for this design, only used when using the programmable flag option.
Enable/Disable Loop Mode
1=Loop Mode Enabled
0=Loop Mode Disabled
LOOP_EN
SINGLE_READ
DB26
(bit26 of Diag Register)
ENABLE LOOP MODE High True
SEND TEST DATA High True
(bit25 of Diag Register)
DB25
1=SEND TEST DATA true
0=SEND TEST DATA false
/POWER_ON_RESET
POR
WRT_0020
DB28_IN
STOP_LOOP
Low True
(from VME Interface)
LOOP_START
START LOOP High True
(bit21 of TFIFO data out)
latching of LOOP START signal
SYNC Delays for the TFIFO State Machine use
LOCAL_SYNC
LSYNC_D1
LSYNC_D2
resync of the local sync with the local clock.
TEST_FIFO_EMPTY
TF_EMPTY
TFIFO
SINGLE_READ
LOOP_EN
RESET
SEND_TEST_DATA
STOP_LOOP
START_LOOP
LOCAL_CLOCK
LSYNC_D1
LSYNC_D2
RUN_MODE
TEST_FIFO_EMPTY
TF_WEN
TF_LOOPING
TF_REN
TF_DUMPING
S3
S2
S1
S0
FORCE_RESET_TFIFO
RUN MODE force the TEST FIFO LOGIC to reset state.
(to VME Interface, enable reading of J3 Monitor Register)
TFIFO_LOOPING
Low if TFIFO in loop mode
The TFIFO goes in "loop mode" when the loop mode is enabled (bit 26 of DIAG Register) and there is a START_LOOP request(bit 21 of TFIFO output data).
The FIFO Reading is disabled during the FIFO Reset
When low Test Fifo is read enabled
Read enabled is latched with the Test FIFO read clock (inverted local clock)
TF_REN
Low True
(to GDX and TFIFO)
TF_DUMPING_INT
TF_DUMPING
TF_S3
TF_S2
TF_S1
TF_S0
RESET_TFIFO
Low True
EFFF
EF_FULL
(active low)
PIPE_CLK_INT
Error FIFO Almost Full Flag
J67
EFAFF
(active low)
J50
from pin23 of U20 (/GLINK SYNC=TTL not(GLDB19))
XROUTE1
to CLK_CTL
GLINK SYNC=TTL GLDB19
EN_TEST_DATA
active low
(to GDX for STATUS REGISTER)
REROUTE11
XROUTE0
XROUTE2
Extra pins reserved for reroutes
LOCAL_CLOCK
LOCAL_CLK
EFIFO REN1 driven low by VME INT
UNUSED_1
UNUSED_0
active low
from VME INTERFACE ISP
goes also to the ERROR FIFO chips
J3_TTL BUS BLANKING
RUN_MODE
REROUTE12
EN_TEST_DATA
Low True
from CLK_CTL
RUN_STATE signal, active low.
Is used as Output Enable for the TFIFO and as direction selection for 861s bidirectional buffer.
The 861s are used to blank the J3 Backplane TTL bus when the GLINK in not driving it.
In order to do this the TEST FIFO must had be resetted or the last word clocked out must be all 0s
J59
RD_0020
EF_ERRORD_MODE
SET_EDL_LATCH
ENABLE ERROR DETECTION MODE
(bit23 of Diag Register)
RESET_EF0
SET_ETM_LATCH
RESET_LATCHES
DB17
EF_TEST_MODE
SET_ETM_LATCH
ENABLE EF TEST MODE
(bit17 of Diag Register)
SET_EDL_LATCH
J55
Inverted CLOCK to TEST FIFO (Read CLOCK)
TEST OUTPUTS
EFS0
EFS1
EFS2
J46
J47
J49
TRIGGER
REROUTE14
active high
SAVE_ERROR
SV_ERR
from ERROR LATCH ISP
Is active when one of the following error conditions occurred:
-protocol error
Pin 20 and 19 are shorted on the outside the chip.
SAVE_ERROR2
The ERROR FIFO to SAVE the data if:
1) ERROR DETECTION MODE signal is true and the signal SAVE ERROR is received.
2) ERROR FIFO TEST MODE is set, the TEST FIFO is dumping data.
3) Trigger is received from VME (Diagnostic Register bit 15).
ERROR Logic Trigger
TFIFO Trigger
VME TRIGGER
DB15
VME TRIGGER
(bit15 Diag Register)
from CLK CONTROLLER
is either the local 53MHz clock or the GLINK clock. It is used as the clock for the protocol error detection logic
PIPE_CLK
EFIFO
RESET_LATCHES
EFOE_EN
EF_RCLK_SEL
EF_WEN
EF_REN
EF_HAS_DATA
S0
S1
S2
FORCE_RESET_EF
TRIGGER
EF_TEST_MODE
PIPE_CLK
EFAFF
EFEF
RESET
EFOE_EN active low
if EDL or ETM latches are set the EFIFO logic is reset.
REROUTE13
active low
RD_EFIFO signal
from VME INTERFACE ISP
Error Fifo Read
VME_RD_EFIFO
S0=0 -> READ CLK=PIPE CLK
S0=1 -> READ CLK=VME READ
LowSelect 53Mhz PIPE Clock (Error Detection Logic enabled)
High Select VME Read Clock
EFRCLK
VME can READ only when READ CLK=VME READ
Write Enabled is latched by the EFIFO write clock.
(Inverted PIPE_CLOCK)
EFWEN1
Low True
EFREN2
active low
Enable Read to Error FIFO
The FIFO reading is disabled during the FIFO reset.
EFOE
active low
Error FIFO output enable
EFOE_INT
Inverted to adjust the clock timing for the Error FIFO Write
EFIFO_HAS_DATA
active high
to ERROR LATCH ISP
EFWCLK
Unused inputs from CLOCK_CTL
1=Local Clock
0=G-LINK Clock
(from CLOCK_CTL)
MCLK_SEL
J3_DRIVER_EN
(from Clock Control)
EFWEN2
High True
Not used for this design, only used when using the programmable flag option.
RD_0024
(status register)
TFFF
TEST FIFO FULL FLAG
(active low)
TF_EMPTY
(active low)
EF_FULL
(active low)
EF_EMPTY
(active low)
DB3
DB4
DB5
DB6
DB28
DB30
DB31
READ_DIAG
Low True
READ_STATUS
Low True
(diagnostic register)
WRT_DIAG
Low True
POWER_ON_RESET
/POWER_ON_RESET
POR
DB29
RD_0020
RD_0024
VME_RD_EFIFO
RESET_EF0
EFOE_INT
EF_EMPTY
EFEF
RESET_EFIFO
Low True
to FIFOs and to ERROR PIPE ISP
Data I/O
10525 Willows RD NE
Redmond, WA 98073
Title: FIFOCTL
Name:
Date: 11/15/99
Sheet 01 of 01



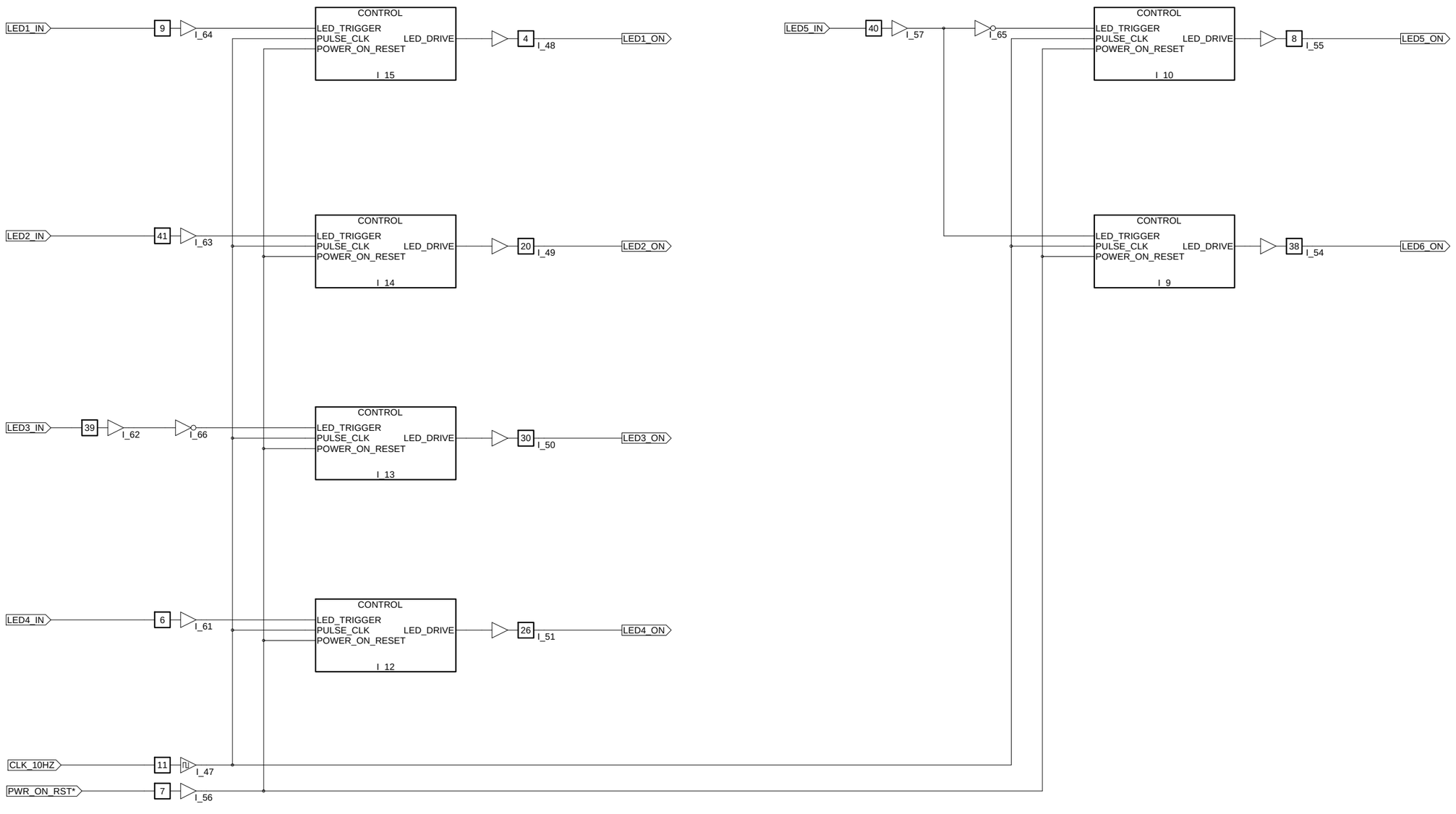
READ ERRORS	READ_REG1	READ_REG0	SEL1	SEL0 (XSEL)	OUT
1	1	0	0	0	REG0
1	0	1	0	1	REG1
1	0 (1)	1 (0)	1	1	0
0	1 (0)	1 (0)	1	0	ERRORS

Data I/O 10525 Willows RD NE Redmond, WA 98073	Title: ERSEL2 Name: Date: 9/23/99 Sheet 01 of 01



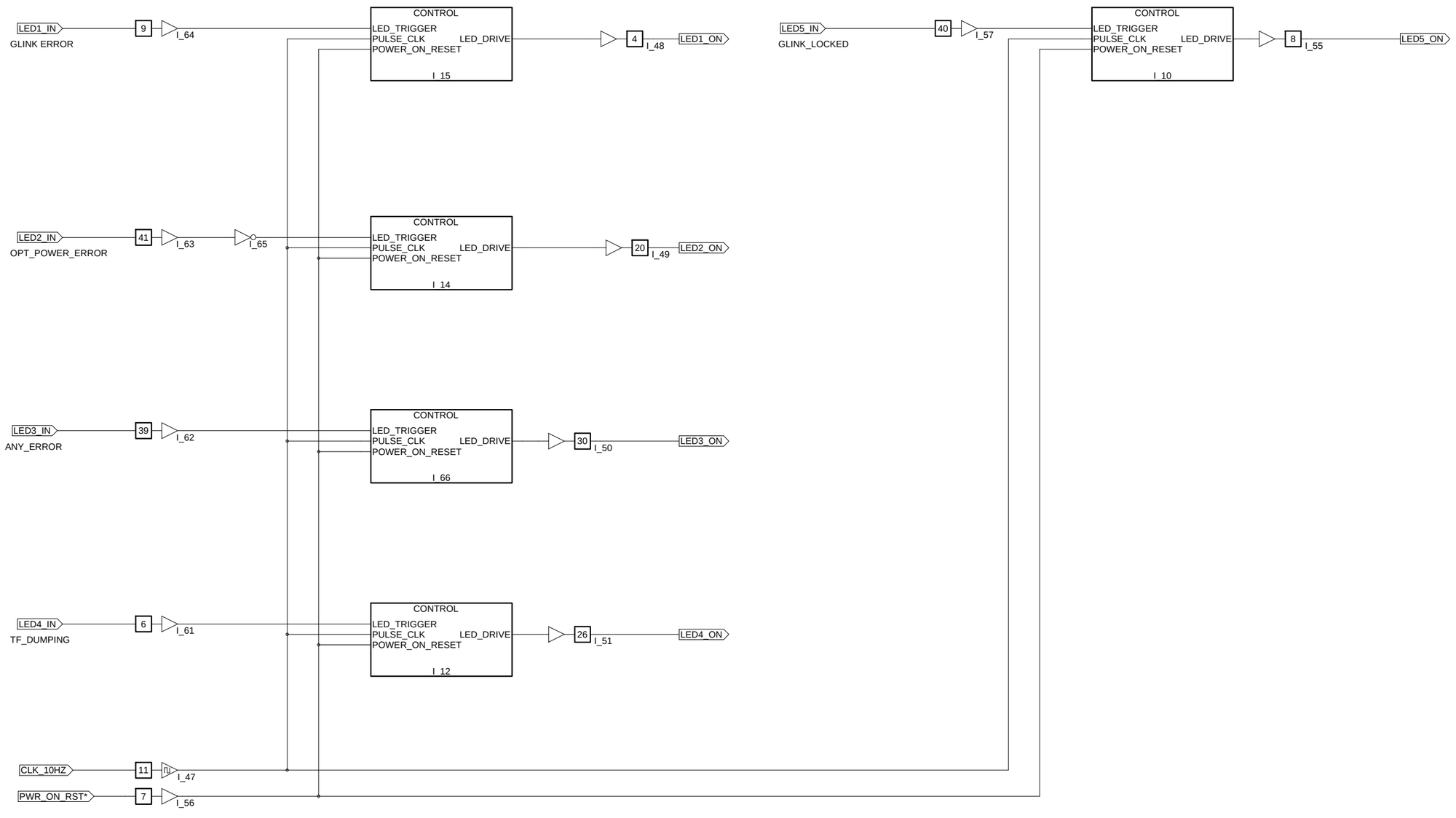
Data I/O 10525 Willows RD NE Redmond, WA 98073	Title: ERROUT Name: Date: 9/23/99 Sheet 01 of 01

Fib Fanout Module Led Control 1



"ON" outputs of logic blocks
connect to cathodes of led's

Fib Fanout Module Led Control 2



"ON" outputs of logic blocks
connect to cathodes of led's