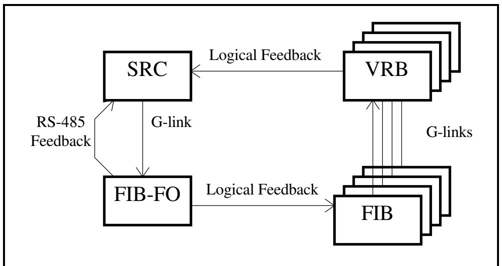
Using the G-link in the SVX system.

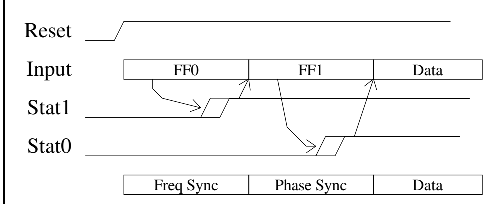
For a unidirectional link, HP recommends that 3 handshake signals be used to gain and maintain synchronization on its G-link chips. In the SVX design, we have chosen to use a single signal (in the SRC to FIB link) or a logical feedback path (in the FIB to VRB links). This document describes how G-links can be used in this manner.



Synchronization at the receiver:

Synchronization on the G-link receiver is a three state process. After a reset, it enters the frequency-sync state, where the PLL locks onto the frequency of the incoming signal. During this time, the transmitter should be sending fill frames of the type FF0. Lock is attained after about 2.5 ms, and the receiver asserts STAT1. The tranmitter should then begin tranmitting FF1 while the receiver gets a more accurate phase lock on the incoming signal. Finally, after the receiver gains phase lock and asserts STAT0, the transmitter can send data.

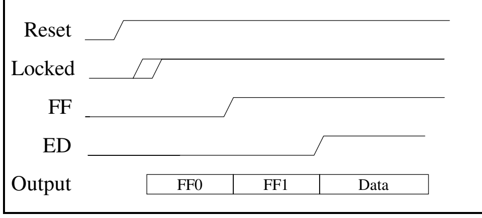
Receiver synchronization:



Synchronization at the transmitter:

Synchronization at the transmitter is similar. The transmitter locks onto the local clock first. Then the control signals FF (Fill Frame) and ED (Enable Data) control the transmitter operation. In the recommended handshake configuration, the transmitter LOCKED signal drives the receiver RESET pin; STAT1 drives FF; and STAT0 drives ED.

Transmitter synchronization:



In theory, it's possible to synchronize a G-link without handshake signals. If the proper sequence is followed, allowing plenty of time (about 5ms) at each state to gain lock, then the link can be operated with only an error signal fed back to reset and re-start the sequence.

The circuit shown at right is an example (untested) circuit that could be used to implement synchronization. It is a 16V8 GAL. The state bits are driven by a 5ms (200Hz) oscillator. On power up or reset, all three state bits (RESET, FF, ED) are cleared.

The RESET signal lasts for 1 clock pulse and is removed (driven high).

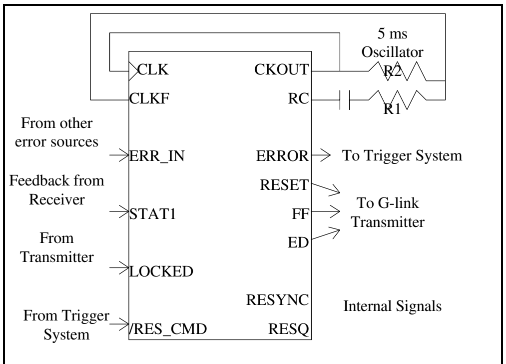
When STAT1 becomes true, and the trigger system has issued a reset command, FF is asserted to enter the phase-sync state. After 1 clock pulse, ED is asserted to enter the data transmission state. At this point, if the trigger system issues a reset command, the circuit goes back into the phase-sync state. The frequency-sync (reset) state is only entered if sync is lost by the transmitter (LOCKED=0) or receiver (STAT1=0).

The ERROR signal is sent to the trigger supervisor to report error conditions. This signal is held until the phase-sync state is entered. The phase-sync state will be entered when the trigger system responds to an ERROR by asserting RES_CMD.

In the SRC-to-FIB link, the STAT1 signal is fed back via an RS-485 wire. In the FIB-to-VRB link, no STAT1 signal is available, so STAT1 should be driven by RES_CMD from the trigger system. This will cause the transmitter to do a complete re-synchronization each time a reset command is issued.

Note that the GAL has several spare inputs that could be used for other error sources.

Recommended values for the oscillator circuit are R1=10K, R2=15K, and C=.22uF




```
#--------- PAL Equations -----------
CKOUT = /RC;         # Simple R/C clock
RC=CLKF;

# Assert Error and hold till we enter phase-sync state.
ERROR =    /FF + ERR_IN  +  ERROR * /(FF*/ED);

# Re-synchronize on some errors (only when FF=1)
# This signal clears the state bits: ED, FF, and RESET
RESYNC=   FF * (/STAT1 +/LOCKED + RESYNC);

/RESET:=    1;          # Reset pulse lasts one 5ms clock

# Go to phase-sync only when STAT1 and Trigger has
# issued a reset.
FF:=       /RESET*STAT1*RESQ  + FF;

# Stay in phase sync for one clock, then send data till
# reset or error.
ED:=       FF * /RESQ;

# Hold a reset command till we enter phase-sync state.
RESQ =  (RES_CMD + RESQ) * /(FF*/ED);
```