# Evolution of the Elefant chip from prototype version to production version.

## By


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# Modifications of the Elefant prototype version:

## SRAM

Problem: Corruption of data in the memory cell.

Error: The write bit-lines coupled to the read bit-lines.

Fix: The read and write bit-lines were swapped.

Simulation: Problem seen on detailed simulation with nearest neighbor parasitics in Hspice. Resolution of problem and modifications of layout resimulated okay, with excellent margins.



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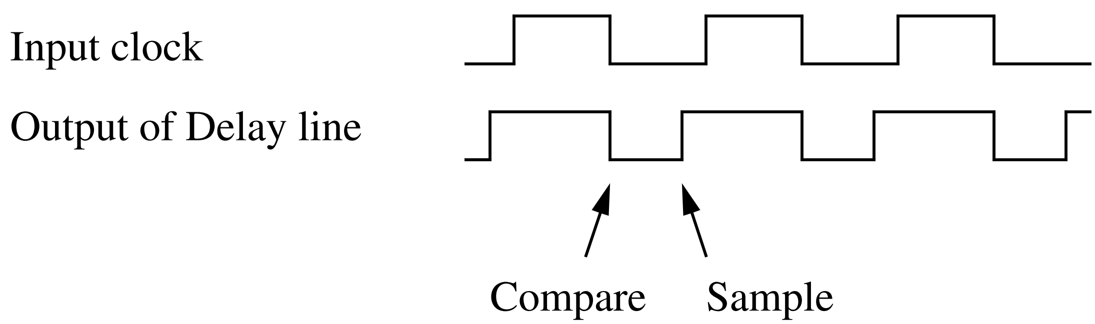
# TDC

Problem: Missing Code 0.

Error: Phase detector sensed falling edge of clock signal while rising edge was used to sample data. Leading edge versus falling edge dispersion ~ 1ns.

Fix: The input to the phase detector were inverted.

Simulation: Error was seen in simulation once dispersion simulated.



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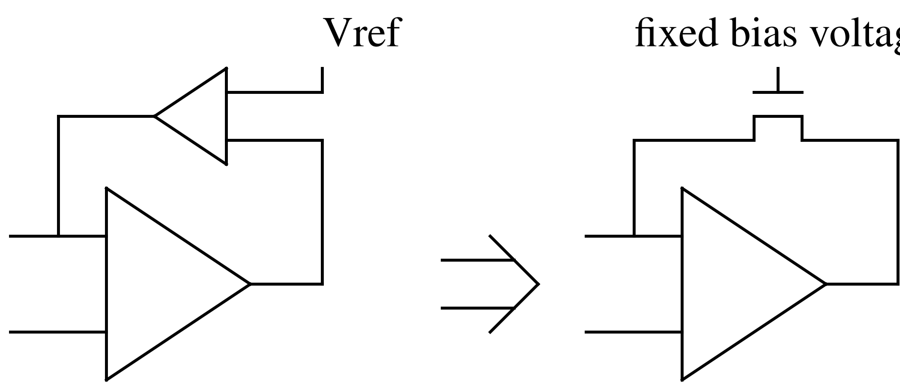
## Analog Receiver

Problem: Analog receiver had poor yield (15%).

Error: Incorrect bias of the reset amplifier, due to sensitivity to process variations.

Fix: Active reset amplifier substituted with a NMOS as feedback resistor.



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## Reliability Improvements

Problem1: IR drop on reference voltage to the FADC. 0.2V per line (4 LSB).

Fix: Wire dimension increased the layout. IR drop < 1 LSB

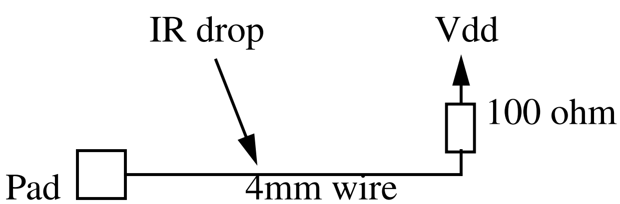
Problem2: Current handling power lines

Fix: Wire dimension increased in layout

Problem 3: Width of resistor in ladder in FADC to small.

Fix: Wire dimension increased in layout. Resistance increased from 3k ohm to 6k ohm.

Problem 4: Location of digital input pullups.




Fix: Resistor moved to pad.



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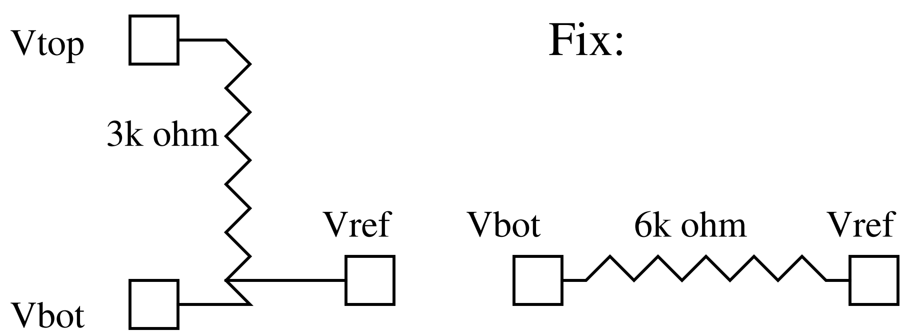
Problem 5: Pullups on digital inputs too large.

Fix: Pullup reduced from 200 ohm to 100 ohm. Concerns over long RC time constant, $C_{board}$ $+C_{chip}$~10pF, to set adequate signal rise time.

Problem 6: Lock indicator showed out of lock when in lock.

Fix: Name changed to Not Lock indication.

Problem 7: Vref ladder could have current density limitation during test.




Problem 8: Input pins did not match the output pins on the Amplifier IC.

Fix: Input pins moved on layout to match the output pins on the Amplifier IC



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Problem 9: Uncertainty about driver strength on the write lines going into the SRAM

Fix: Added extra buffers with increased drive strength

Problem 10: Noise on power lines.

Fix: Added decoupling caps on power. ~2pF

Problem 11: Control voltage for the TDC not centered.

Fix: Size of delay elements reduced and control voltage was centered.

Problem 12: Moved Not Lock pin to pin 98.



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# Only detected 3 problems in preproduction version.

Problem1: 0.5 V offset in Analog Receiver.

Problem 2: FADC timing margin.

Problem 3: Kickback on digital and analog inputs (The kickback on the analog inputs is not visible in LBL's test setup due to 20 pF capacitance between the differential input lines on the test board).

Tested 2 groups of chips:

1st. group: original group of 50 from MOSIS

2nd. group: Additional 84 die MOSIS had on hand.



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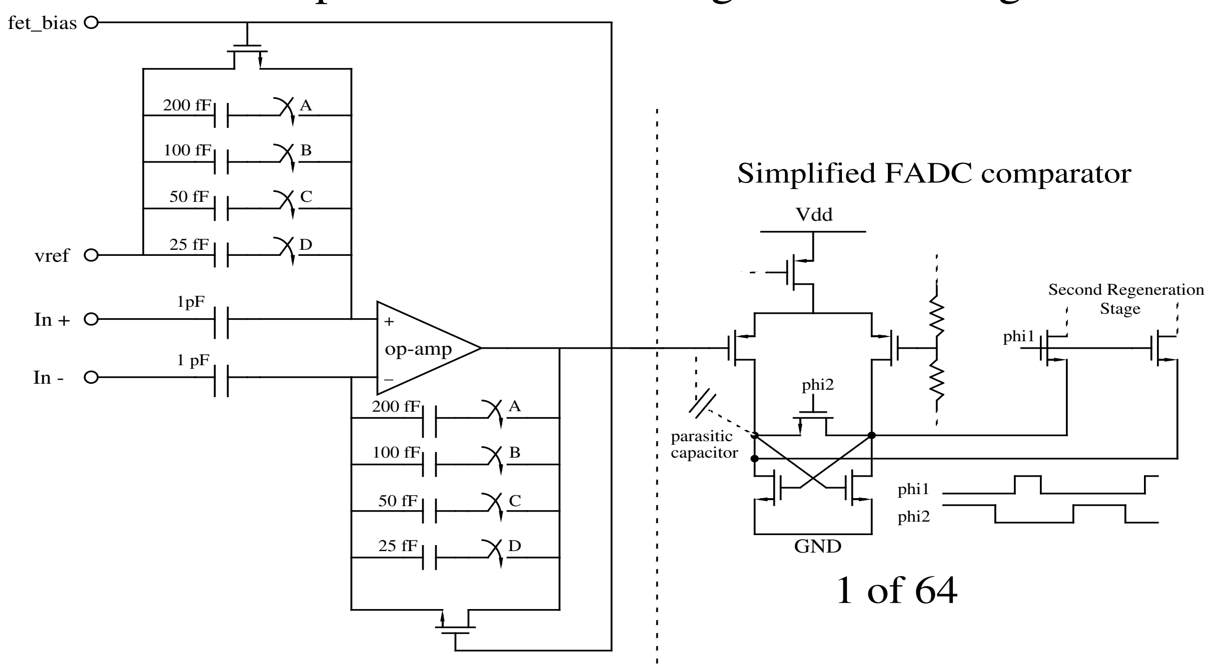
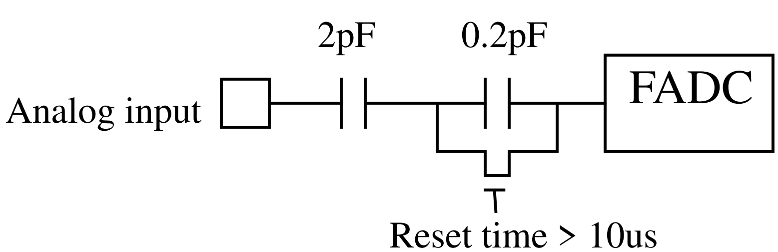
# Modifications of the Elefant preproduction version:

## Analog receiver

Problem: 0.5 V offset.

Error: Kickback from the FADC comparator. Output impedance of the analog receiver to high.



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include figure 5 from

Scotts document

use tape

Simulation of the offset caused by noise injection into the Analog Receiver.



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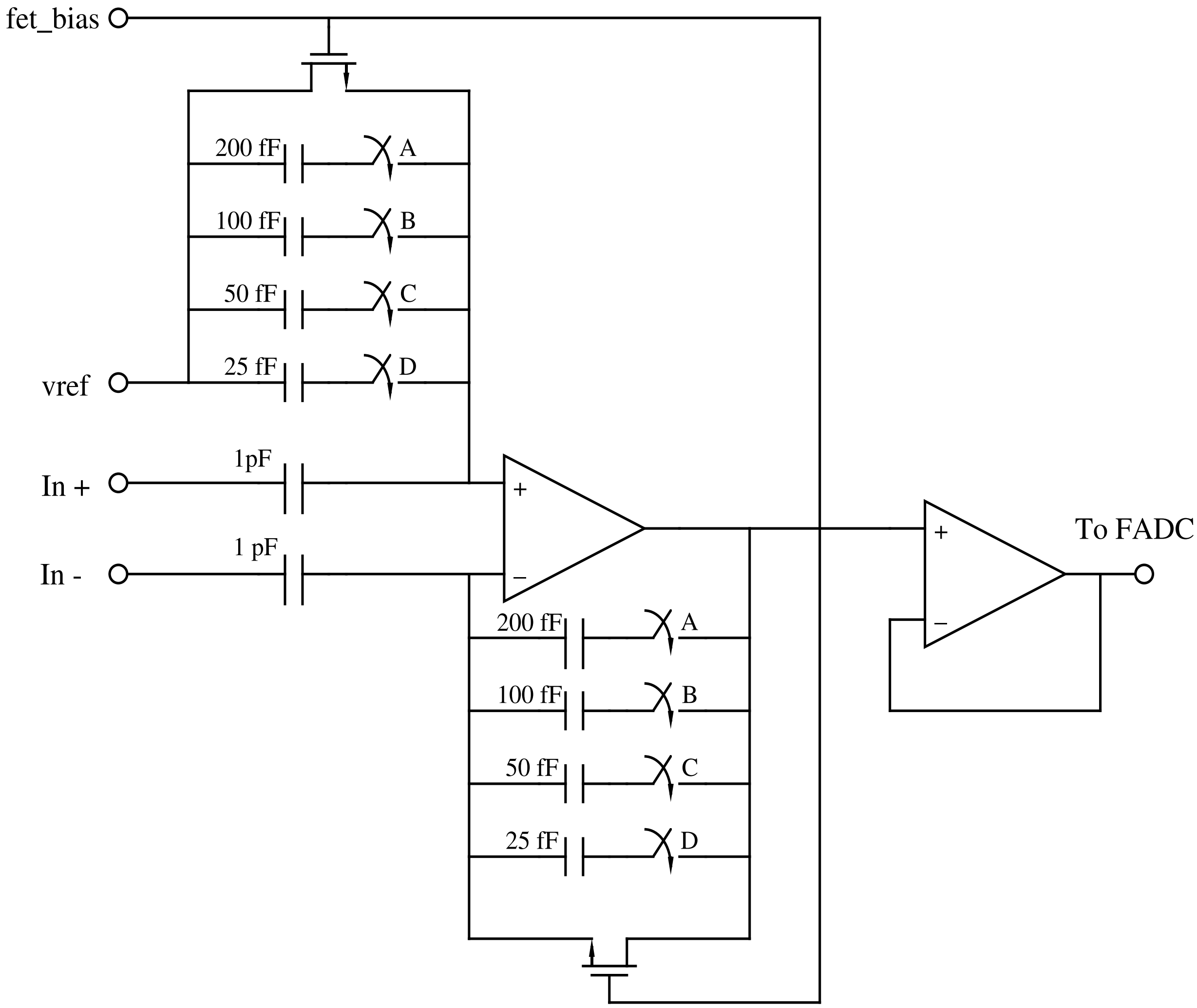
Simulation of the offset with an ideal op-amp replacing the forward amplifier.

Fix1: Include a unity gain buffer in-between the Analog Receiver and the FADC. Decreased the output impedance of the op-amp. Reduced response time of op-amp. The buffer isolates the analog input from the noisy FADC.



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Simulation of noise injection with the voltage buffer between the Analog Receiver and the FADC.



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Linearity for the Analog Receiver simulated over all 4 corners for the hp process.



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Linearity of the Analog Receiver simulated with nominal parameters for the hp process. Node 7 is the bias node for the amplifier.



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Fix 2: An additional 1pF capacitor is added to the output of the buffer to reduce the amplitude of the kickback noise from the FADC.

Fix 3: Timing of the FADC is changed so the output of the buffer is stable when the FADC samples the data. This also solves the problem with timing margin in the FADC.



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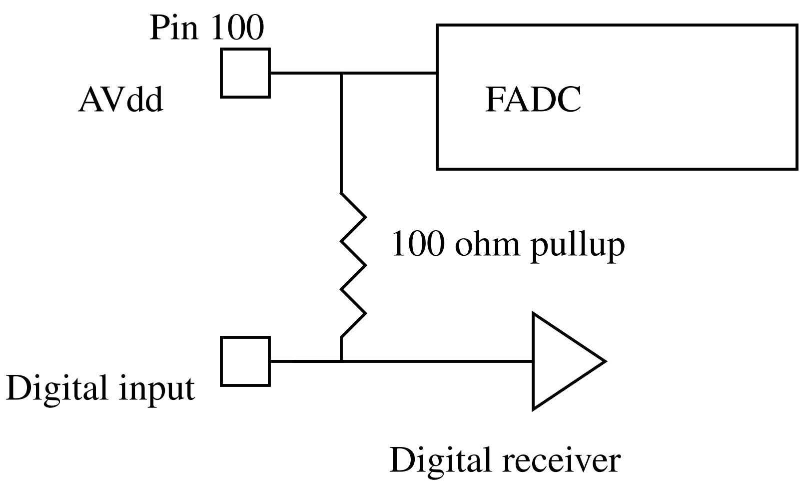
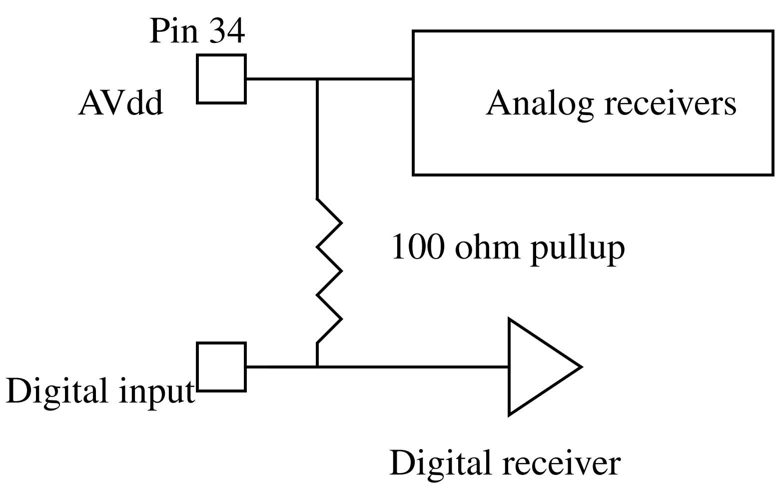
# Kickback on digital input lines.

Problem: Analog VDD supporting the FADC and the 100 pullup resistors is noisy.




Fix:



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# Conclusion

With the tools we have, we have not seen any new problems with the current design. We have improved the extraction capabilities to cover parasitic capacitance and resistance.

The new Analog Input Converter is simulated after extraction of layout. The new Analog Input Converter is simulated together with the input stage of the FADC (extracted netlist). Simulation shows that the offset problem is not present in the new design.

The op-amp used in the new Analog Input Converter is the same as the one which is in the Analog Receiver in the preproduction version. This is done to reduce the risk. The only difference between the op-amp in the Analog Receiver and the buffer is the compensation.



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