Test Report:

Single Event Testing of the TSS901E 1355 Controller

Mark Walter, Moses McCall, Christian Poivey,
and Stephen Buchner

Code 561
GSFC-NASA

16th March 2004

Texas A&M Cyclotron Facility

1. Introduction

Single event effects (SEE) testing of the Atmel Triple Point-to-Point IEEE 1355 controller ASIC (TSS901E) was performed with heavy ions at Texas A&M Cyclotron Facility on 16th March 2004. The ASIC was previously tested in October 2003 using a clock frequency of 6 MHz, which is much lower than the frequency (100 MHz) that will be used in the actual application. Because the upset rates in other data transmission devices have been shown experimentally to be dependent on clock frequency, it was deemed necessary to retest the ASIC at higher frequency to determine whether, in fact, clock frequency is a factor determining upset rate in this part. Except for higher clock frequencies and slight modifications to software, the same procedure was used.

2. Device

The device tested (TSS901E) is an ASIC with 0.6 µm CMOS triple-metal "Sea of Gates" technology that can be operated at both 5 V and 3.3 V. For these tests 5 V was used. There is no information about the date and lot codes for this part. The testing was done at room temperature (20 C).

3. Testing Configuration

a. Hardware.

The TSS901E ASIC was mounted on a 4LINKS board that could be plugged into a slot on a computer's motherboard. For SEE testing, a 1355 communications link was established between two computers. Each computer had a 4LINKS board. The metal lid covering the ASIC on one of the boards was removed to provide the beam of heavy ions access to the chip. The delidded ASIC is the DUT. Figure 1 shows the DUT board positioned in front of the accelerator port. The ASIC is located at the top of the board. Because the ASIC permits communications across three separate channels, the two computers were connected via three cables, one for each channel. The cables were approximately a meter in length. The 4LINKS card containing the DUT was plugged

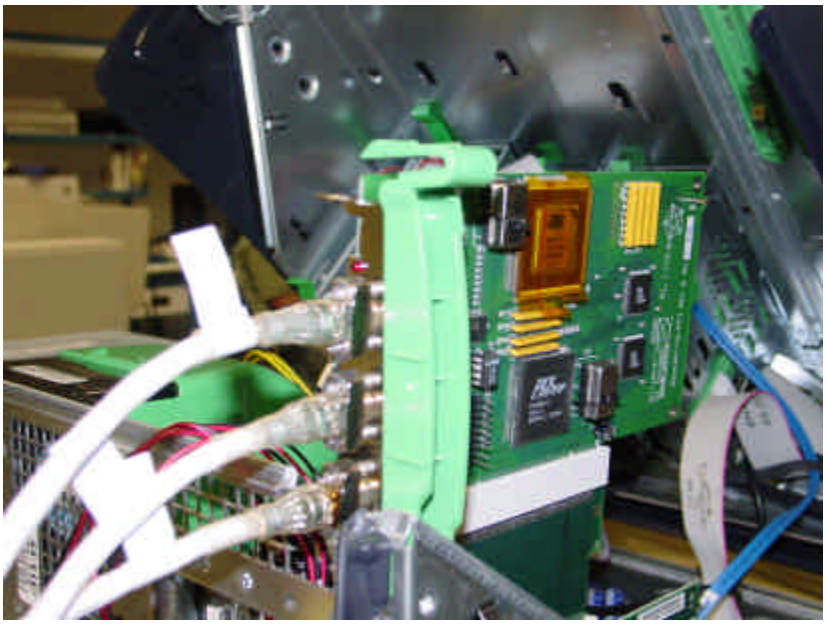

Figure 1. Picture showing the 4LINKS card containing the DUT positioned in front of the accelerator port. An extender card was used to raise the 4LINKS board above the computer chassis so that the accelerator ions would be able to reach the DUT unimpeded. The DUT is at the top of the card. The three cables connecting the two computers together are seen on the left.

into an extender card that was, in turn, plugged into a slot on the computer's motherboard. The extender card raised the 4LINKS card above the computer chassis so that the chassis did not block the accelerator ions from reaching the ASIC. Irradiations could not be done at non-normal incidence because the cables were too short to permit the computer with the DUT to rotate. Both computers were controlled from outside the test area using a single keyboard/mouse/monitor extender and a 100-ft cable. The extender card also had a connection for monitoring board current in order to detect sudden increases in current resulting from latchup.

b. Software.

Before communications could start it was necessary to designate which computer was the Master and which was the Slave by driving a specific pin on each ASIC to high voltage for the Master and to low voltage for the Slave. To establish proper communications required that the Master be started before the Slave. Each ASIC supports three separate communications channels operating independently of one another. The Master in each channel sends a "flow control character" to the Slave, requesting the Slave to send one byte of data. The Slave generates a packet consisting of a "Header" containing flow control characters followed by one byte of data (A5). Parity bits are added to flag any errors that may arise in the Header or data parts of the packet. The packet is transmitted over the IEEE 1355 cable to the Master, which checks for parity errors. Errors in the Header are likely to lead to "Link Drops" (recorded in a log file) that lead to a halt in communications. Errors in the data part of the packet are recorded as "Link Errors." The part of the ASIC where the Header and data in a packet are most likely to be upset is the FIFO, because that is where the data spends most of its time. The

ASIC contains 96 registers, with each register able to hold a 32-bit word. Forty of the registers are static making it possible to check for SEUs by comparing the contents of the registers before and after irradiation. The remaining 56 registers are dynamic. SEUs in those registers could disrupt communications, but there was no way to detect them in this test. An error in any one of the registers could lead to a "Link Drop."

4. Test Procedure

The 4LINKS card containing the DUT was configured as either the Master or the Slave. The clock frequency was set to 80 MHz, 100 MHz, or 140 MHz. Communications were started by having the Master send a flow control character to the Slave, requesting it to send a packet with 1 Byte of data. Once communications were established, the ion beam was turned on and the ASIC irradiated. During irradiation the supply current to the board was monitored. When communications stopped, the beam was turned off and the fluence noted. A file with all the pertinent information regarding number of errors and which links went down was recorded. Communications could be restarted either by software or by a hard power cycle. Ions with various LETs were used for producing single event effects so that the cross-section as a function of ion LET could be calculated, information that is needed for calculating error rates in space.

5. Results

The results of the SEE testing are summarized in Tables I and II. Table I contains data obtained when the DUT was the Master and Table II contains data when the DUT was the Slave. A summary of the results is as follows:

- ?? No latchups were observed, even at the highest LETs (87.4 MeV.cm^2/mg.)
- ?? All errors appeared only in the Master independent of whether the DUT was configured to be the Master or the Slave. This is because only the Master detected errors while the Slave acted as a "dumb" terminal.
- ?? Communications were halted when one, two or three links were dropped.
- ?? Only 40 of the 96 registers could be monitored for SEUs. The SEU threshold for those registers was greater than 29.3 MeV.cm^2/mg, whereas the SEU cross-section for Link drops and Link errors is below 20 MeV.cm^2/mg.
- ?? The SEU cross-section appeared to be independent of clock frequency when the DUT was either the master or the slave.
- ?? It was never necessary to restart communications by cycling power.

Table I.
Results obtained when the DUT was the Master.

Run#	DUT Config	freq	SN#	LET	Fluence	link1 master link error	link1 link drop	link1 slave link error	link 2 master link error	link 2 link drop	link 2 slave link error	link 3 master link error	link 3 link drop	link 3 slave link error	Total links master link error	Total links link drop	Register miscompares master	Xsection link err cm2/link	link drop cm2/link	reg mis cm2
1	master	140	74	87.4	1.59E+05		1	0	1	0	0	2	1	0			10			
2	master	140	74	87.4	3.18E+04	1	1	0		1	0	1	0	0			4			
3	master	140	74	87.4	4.50E+04	1	1	0	1	1	0	2	0	0			4			
4	master	140	74	87.4	2.74E+04		1	0	1	1	0		0	0			4			
1to4	**master**	**140**	**74**	**87.4**	**2.63E+05**	**2**	**4**		**3**	**3**		**5**	**1**		**10**	**8**	**22**	**1.27E-05**	**1.01E-05**	**8.36E-05**
11	master	100	74	87.4	3.32E+04	0		0	1		0	0	1	0			1			
12	master	100	74	87.4	3.80E+04	0	1	0	0	1	0	1		0			0			
13	master	100	74	87.4	2.91E+04	1		0	2		0	0	1	0			2			
11to13	**master**	**100**	**74**	**87.4**	**1.00E+05**	**1**	**1**		**3**	**1**		**1**	**2**		**5**	**4**	**3**	**1.66E-05**	**1.33E-05**	**2.99E-05**
14	master	80	74	87.4	5.85E+04	1		0	0	1	0	0	1	0			8			
15	master	80	74	87.4	2.55E+04	1	1	0	0	1	0	0	1	0			7			
16	master	80	74	87.4	7.71E+04	0	1	0	0	1	0	1		0			10			
14to16	**master**	**80**	**74**	**87.4**	**1.61E+05**	**2**	**2**		**0**	**3**		**1**	**2**		**3**	**7**	**25**	**6.21E-06**	**1.45E-05**	**1.55E-04**
23	master	80	74	53.9	3.23E+04	2		0	0	1	0	0	1	0			5			
24	master	80	74	53.9	1.96E+04	0	1	0	0	0	0	0	0	0			1			
25	master	80	74	53.9	2.80E+04	0		0	2	0	0	1	1	0			1			
23to 25	**master**	**80**	**74**	**53.9**	**7.99E+04**	**2**	**1**		**2**	**1**		**1**	**2**		**5**	**4**	**7**	**2.09E-05**	**1.67E-05**	**8.76E-05**
26	master	100	74	53.9	1.11E+04	0		0	0	1	0	1	0	0			4			
27	master	100	74	53.9	2.19E+04	0	1	0	1	1	0	0	0	0			0			
28	master	100	74	53.9	1.46E+04	0		0	0	1	0	0	0	0			3			
26to28	**master**	**100**	**74**	**53.9**	**4.76E+04**	**0**	**1**		**1**	**3**		**1**	**0**		**2**	**4**	**7**	**1.40E-05**	**2.80E-05**	**1.47E-04**
35	master	140	74	53.9	1.86E+04	2		0	1	1	0	1	0	0			1			
36	master	140	74	53.9	1.53E+04	0		0	0	1	0	0	0	0			2			
37	master	140	74	53.9	1.82E+04	0		0	0	1	0	0	1	0			2			
35to37	**master**	**140**	**74**	**53.9**	**5.21E+04**	**2**	**0**		**1**	**3**		**1**	**1**		**4**	**4**	**5**	**2.56E-05**	**2.56E-05**	**9.60E-05**
38	master	140	74	29.3	3.97E+04	14		0	0	1	0	1	0	0			0			
39	master	140	74	29.3	5.98E+04	14		0	0	1	0	2	0	0			0			
40	master	140	74	29.3	1.00E+05	0		0	0	1	0	0	0	0			0			
38to40	**master**	**140**	**74**	**29.3**	**2.00E+05**	**28**	**0**		**0**	**3**		**3**	**0**		**31**	**3**	**0**	**5.18E-05**	**5.01E-06**	**0.00E+00**
47	master	100	74	29.3		0	1		0	1		82763676	0				0			
48	master	100	74	29.3	3.37E+04	14			0	1		0	0				0			
49	master	100	74	29.3	2.25E+05	1			3	1		3	1				0			
47to49	**master**	**100**	**74**	**29.3**	**2.59E+05**	**15**	**1**		**3**	**3**		**82763679**	**1**		**18**	**5**	**0**	**3.48E-05**	**6.44E-06**	**0.00E+00**
50	master	80	74	29.3	2.76E+04	14		0	0	0	0	0	1	0			0			
51	master	80	74	29.3	5.97E+04	0	1		0	1		0	1				0			
52	master	80	74	29.3	1.07E+05	15		0	0	0	0	0	1	0						
50to52	**master**	**80**	**74**	**29.3**	**1.94E+05**	**29**	**1**		**0**	**1**		**0**	**3**		**29**	**5**	**0**	**4.98E-05**	**8.58E-06**	**0.00E+00**
60	master	80	74	20.7	3.34E+06	0			0	0		0	0				0			
61	master	80	74	20.7	2.69E+06	0	1		0	0	0	0	1				0			
62	master	80	74	20.7	3.82E+06	0			0	1		0	0				0			
60to62	**master**	**80**	**74**	**20.7**	**9.85E+06**	**0**	**1**		**0**	**1**		**0**	**1**		**0**	**3**	**0**	**0.00E+00**	**1.02E-07**	**0.00E+00**
63	master	100	74	20.7	3.25E+06	0			0	0		0	0				0			
64	master	100	74	20.7	2.02E+06	14			0	0		0	1				0			
65	master	100	74	20.7	3.17E+06	14			0	0		0	0				0			
63to65	**master**	**100**	**74**	**20.7**	**8.44E+06**	**28**	**0**		**0**	**0**		**0**	**1**		**28**	**1**	**0**	**1.11E-06**	**3.95E-08**	**0.00E+00**
72	master	140	74	20.7	3.15E+06	0			0	0		0	0				0			
73	master	140	74	20.7	3.10E+06	0			0	0		0	0				0			
74	master	140	74	20.7	6.24E+05	0			0	1		0	0				0			
72to74	**master**	**140**	**74**	**20.7**	**6.87E+06**	**0**	**0**		**0**	**1**		**0**	**0**		**0**	**1**	**0**	**0.00E+00**	**4.85E-08**	**0.00E+00**

Table I shows the number of SEUs in each of the three links and in the registers following a SEFI. There are three runs for every condition, and the results of those three runs are summed and entered into the table in the next row. The Table also shows that on two occasions there were over 80 million link errors. Such a large number of upsets might be due to a slip in synchronization in the phase lock loop (PLL). It took a while for the software to stop, during which time the large number of errors was accumulated. In some cases, communications were halted as a result of drops in one, two, or three Links.

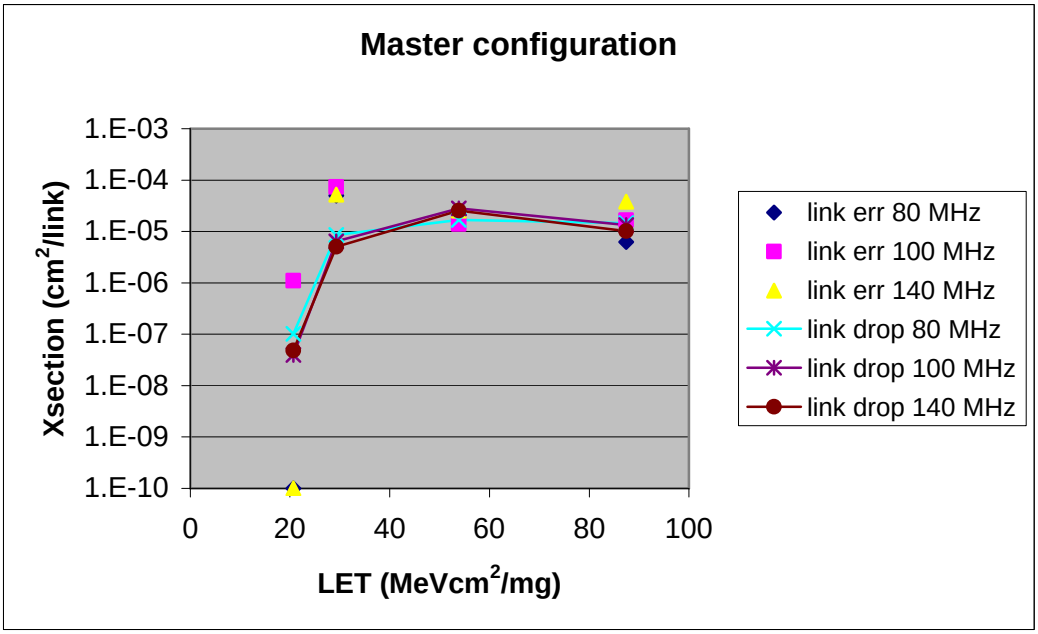

Figure 2. Cross-section as a function of ion LET for Link errors and Link drops when the DUT was configured as Master. Data are for three different frequencies.

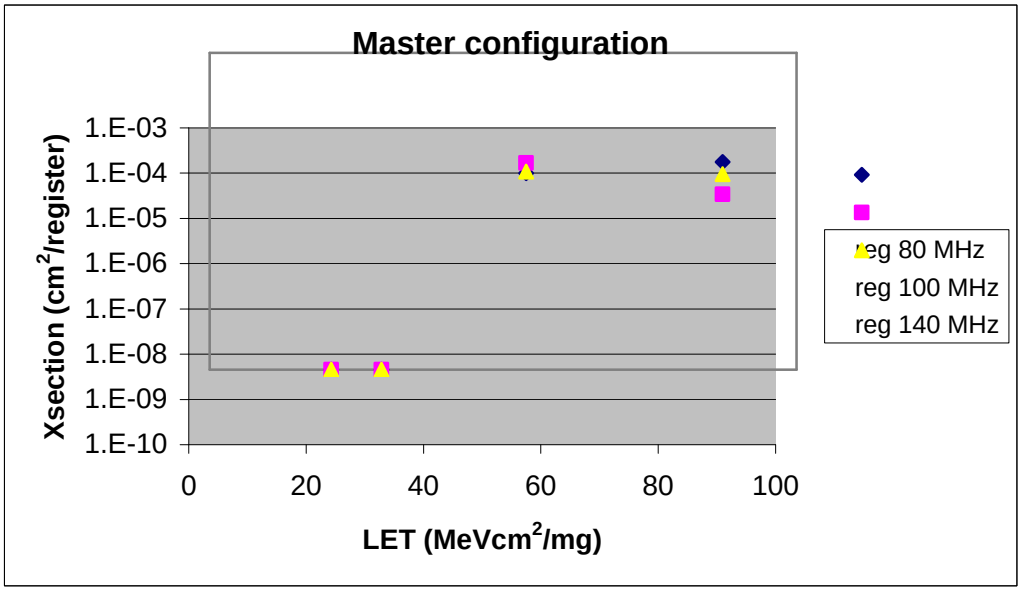

Figure 3. SEU cross-section as a function of ion LET for the registers when the DUT was configured as the Master. The data are for three different frequencies. Since no upsets were observed at the two lowest LETs, the data points represent the maximum possible cross-section.

Table II.
Results obtained when the DUT was the Slave

				link1 master		slave	link 2 master		slave	link 3 master		slave		total link master		Cross section link err	link drop	reg mis
Run#	Freq	LET	Fluence	link error	link drop	link error	link error	link drop	link error	link error	link drop	link error	Register Miscompares	link error	link drop	cm²/link	cm²/link	cm²
5	140	87.4	1.45E+05	7	1	0	3	?	0	4	?	0	7					
6	140	87.4	1.80E+04	431	1	0	982	?	0	0	1	0	5					
7	140	87.4	3.43E+04	0	1	0	0	1	0	853		0	2					
5to7	140	87.4	1.97E+05	438	3		985	1		857	1		14	2280	5	3.85E-03	2.53E-05	7.10E-05
8	100	87.4	3.67E+04	0	1	0	0	1	0	4		0	5					
9	100	87.4	3.28E+04	1	0	0	110	1	0	101	0	0	2					
10	100	87.4	3.02E+04	12	0	0	0	1	0	1	0	0	5					
8to10	100	87.4	9.97E+04	13	1		110	3		106	0		12	229	4	7.66E-04	4.01E-05	1.20E-04
17	80	87.4	5.12E+04	1	1	0	7		0	0	1	0	6					
18	80	87.4	3.70E+04	0	1	0	1		0	91	1	0	7					
19	80	87.4	2.40E+04	1	1	0	5	1	0	13163771		0	2					
17to19	80	87.4	1.12E+05	2	3		13	1		13163862	2		15	13163877	6	3.91E+01	1.78E-05	1.34E-04
20	80	53.9	4.55E+04	12	1	0	2	1	0	3		0	1					
21	80	53.9	3.73E+04	5		0	30	1	0	0	1	0	2					
22	80	53.9	3.75E+04	3		0	5	1	0	3		0	7					
20to22	80	53.9	1.20E+05	20	1		37	3		6	1		10	63	5	1.75E-04	1.39E-05	8.31E-05
29	100	53.9	2.57E+04	2		0	3	1	0	0	1	0	1					
30	100	53.9	1.65E+04	0	1	0	1	1	0	0	1	0	3					
31	100	53.9	1.64E+04	1	1	0	3	1	0	0	1	0	2					
29to31	100	53.9	5.86E+04	3	2		7	3		0	3		6	10	8	5.69E-05	4.55E-05	1.02E-04
32	140	53.9	2.93E+04	1	1	0	1	1	0	2	0	0	4					
33	140	53.9	2.45E+04	1	1	0	1	0	0	4	1	0	1					
34	140	53.9	1.91E+04	0	1	0	4	0	0	1	1	0	0					
32to34	140	53.9	7.29E+04	2	3		6	1		7	2		5	15	6	6.86E-05	2.74E-05	6.86E-05
41	140	29.3	2.78E+04	0		0	0	1	0	1	1	0	0					
42	140	29.3	5.26E+04	1		0	0	0	0	32061258	1	0	0					
43	140	29.3	2.94E+04	2		0	1	1	0	2	0	0	0					
41to43	140	29.3	1.10E+05	3	0		1	2		32061261	2		0	32061265	4	9.73E+01	1.21E-05	0.00E+00
44	100	29.3	6.27E+04	6			3	0		4	1							
45	100	29.3	9.93E+04	4	1		4	0		5	0							
46	100	29.3	2.77E+05	10			16	0		12	1							
44to46	100	29.3	4.39E+05	20	1		23	0		21	2		0	64	3	4.86E-05	2.28E-06	0.00E+00
54	80	29.3	2.80E+05	16		0	14	0	0	4178	1	0						
55	80	29.3	1.04E+05	1645115568		0	5	0	0	4	1	0						
56	80	29.3	3.54E+04	1346		0	1	0	0	0	1	0						
54to56	80	29.3	4.19E+05	1645116930	0		20	0		4182	3		0	1645121132	3	1.31E+03	2.38E-06	0.00E+00
57	80	20.7	1.05E+06	0		0	1	0	0	0	0	0	0					
58	80	20.7	1.02E+06	0			1	0		0	0							
59	80	20.7	3.40E+06	0			1	0		0	0							
57to59	80	20.7	5.47E+06	0	0		3	0		0	0		0	3	0	1.83E-07	0.00E+00	0.00E+00
66	100	20.7	3.28E+06	1			1	0		1	0							
67	100	20.7	3.16E+06	1			1	0		0	0							
68	100	20.7	1.45E+06	0			1	1		1	0							
66to68	100	20.7	7.89E+06	2	0		3	1		2	0		0	7	1	2.96E-07	4.22E-08	0.00E+00
69	140	20.7	1.78E+06	0			0	1		0	0							
70	140	20.7	3.09E+06	0			0	0		0	0							
71	140	20.7	5.50E+05	0	1		0	0		0	0							
69to71	140	20.7	5.42E+06	0	1		0	1		0	0		0	0	2	0.00E+00	1.23E-07	0.00E+00

The data in Table II show that no upsets were detected in the slave when the latter was irradiated. This is not surprising because only the master was monitored for errors. In addition, there were five occasions when a large number of errors appeared, most likely as a result of a single ion hit to the phase lock loop. Therefore, the burst of errors is counted as a single event.

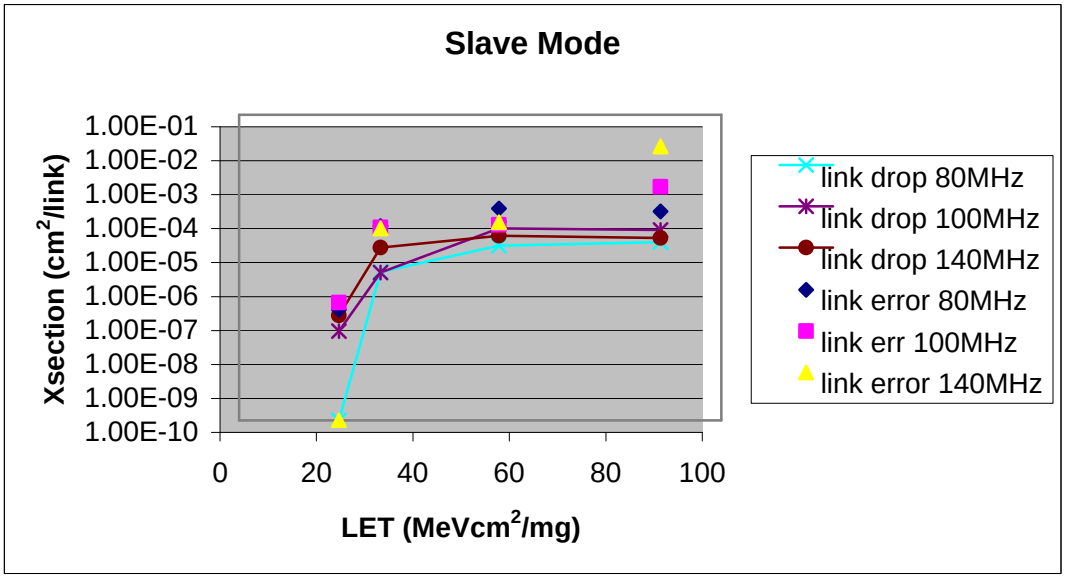

Figure 4. Cross-section as a function of ion LET for Link drops and Link errors with the DUT configured to operate in the Slave mode. Data for three different frequencies are included.

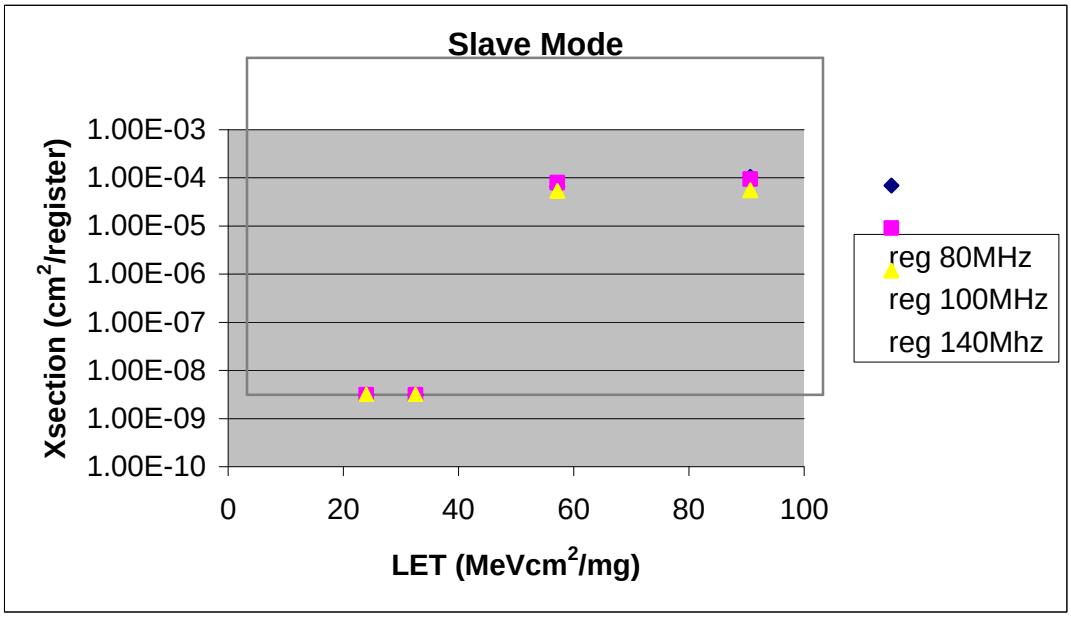

Figure 5. Cross-section as a function of ion LET for register errors with the DUT configured to operate in the slave mode. Data are for three different frequencies.

6. Conclusions

The salient results obtained from this testing are:

- The SEU cross-section is independent of clock frequency.
- The SEU cross-sections are consistent with those previously measured, which means the rate expected in space (1 in three years) should be unchanged.
- The registers have a higher LET threshold than other parts of the device, indicating that they are less SEU sensitive.
- No SELs were observed.
- It was never necessary to cycle power in order to restart communications after a Link drop.