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The ASDQ ASIC for the Front End electronics of the COT

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Abstract

The ASDQ ASIC provides eight channels of preamplifier, shaper, dE/dx and discriminator circuitry for the Run II COT front end electronics. It fulfills the competing requirements of short measurement times ($8--10$ ns), good double pulse resolution ($20--30$ ns), low power (≈ 40 mW/ch) and low operational threshold ($2--3$ fC) by implementing a fully differential circuit. Baseline Restoration is implemented to allow fast performance in a typical Run II conditions. In addition, Ion tail compensation is provided using the pole-zero cancellation technique. The measurement of the charge (dE/dx) is encoded into the width of the discriminator output. The ASDQ ASIC has been implemented on a 5.4 mm $\times$ 3.9 mm silicon substrate using a radiation tolerant analog bipolar process.

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1 Overview

The ASDQ ASIC provides eight channels of preamplifier, shaping, baseline restoration, dE/dx and discriminator circuitry for the Run II COT front end electronics. The purpose of this note is to present the necessary documentation for the ASDQ's design, performance and usage. The note is divided into two major parts. The first part comprises sections 2, 3 and 4, and provides an overview of the COT relevant for this document. The second part, consisting of section 5 provides the details of the ASDQ. Simulations of the ASDQ performance are presented in section 6.

2 The Central Outer Tracker

The Colliding Detector at Fermilab (CDF) is being upgraded to accommodate a 7.6 MHz beam crossing rate (132 ns bunch spacing time) that is planned for Run II [1]. The new Central Outer Tracker (COT) is designed to operate with a maximum drift time of 100 ns compared to 706 ns for the Run I Central Tracking Chamber (CTC). This reduction in drift time is achieved by reducing the maximum drift distance of electrons to $l_{drift} = 0.9$ cm ($\sim$ 25% of the CTC drift distance) and by using a 50:35:15 Ar-Ethane-CF_4 gas mixture with a drift velocity of 90 μm/ns. In 36 bunch mode of operation, Run II luminosities will be approximately eight times higher than typical Run I luminosities. The performance of the COT is expected to be similar to that of CTC under these conditions. Similarly, in 108 bunch operation with luminosities of $\sim 4 \times 10^{32}$ cm^{-1}s^{-1} ($\sim$ 20 times the luminosities of Run I), the COT is expected to maintain its performance. These performance requirements are primarily achieved by a larger number (factor of four relative to the CTC) of cells and with faster electronics and a modified geometry of the COT cells to allow a more uniform collection of charge.

Each COT cell is approximately 1 cm^2 in cross section and 3.1 meters in length. A cell consists of alternating potential and sense wires (13 potential and 12 sense wires respectively) enclosed by cathode field panels consisting of gold plated Mylar sheets. Each sense wire along the length of the cell attaches to the high voltage supply through a 550 pF decoupling capacitance with a resistance of 300 Ω to ground on one end. The high voltage supply connection to the wire is through a 100 kΩ resistor. The COT wire connection

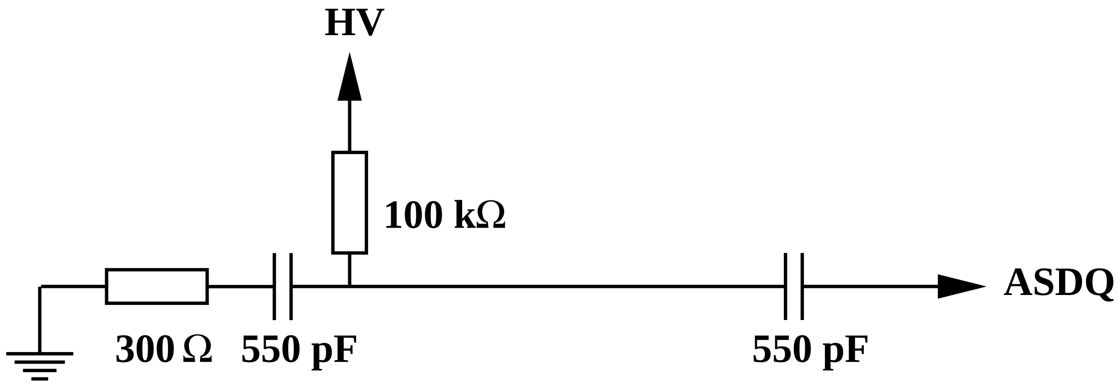

Figure 1: *The COT wire connection diagram.*

scheme is shown in Fig. 1. The resistance of the sense wire is 180 Ω, the total impedance of the COT cell is 300 Ω, and the stray capacitance is estimated to be 10 pF. The field panels are the equivalent of the field wires of the CTC, and allow for a higher and a more uniform drift field in a COT cell compared to the CTC. With a higher drift field, the Lorentz angle for the COT is deg 35 compared to deg 45 for the CTC. The ends of the cells are mechanically and electrostatically sealed by additional Mylar strips called Shaper Panels. The precise range of values of the potentials that the potential and sense wires will be held at will be determined during the operation of the CDF detector in Run II. The expected values are ~ 1.9 kV for the potential wires and ~ 2.9 kV for the sense wires. The cathode field panel will be grounded. With these expected values, the drift field in the cell is ~ 2.5 kV/cm.

The general scheme of the COT front end electronics is shown in Fig. 2. One side of the COT sense wire connects to the ASDQ daughter-board. Each daughter-board houses three ASDQ ASIC's. The signals from the daughter-board (24 channels) are carried off in micro-coaxial cables to the TDC. Each TDC receives the output of three ASDQ daughter-boards (96 channels). The repeater boards that sit between the daughter-boards and the TDC in the electronics chain compensate for the shaping of the signal through the micro-coaxial cables. The ASDQ ASIC's provide full analog signal processing between the COT chamber and the TDC.

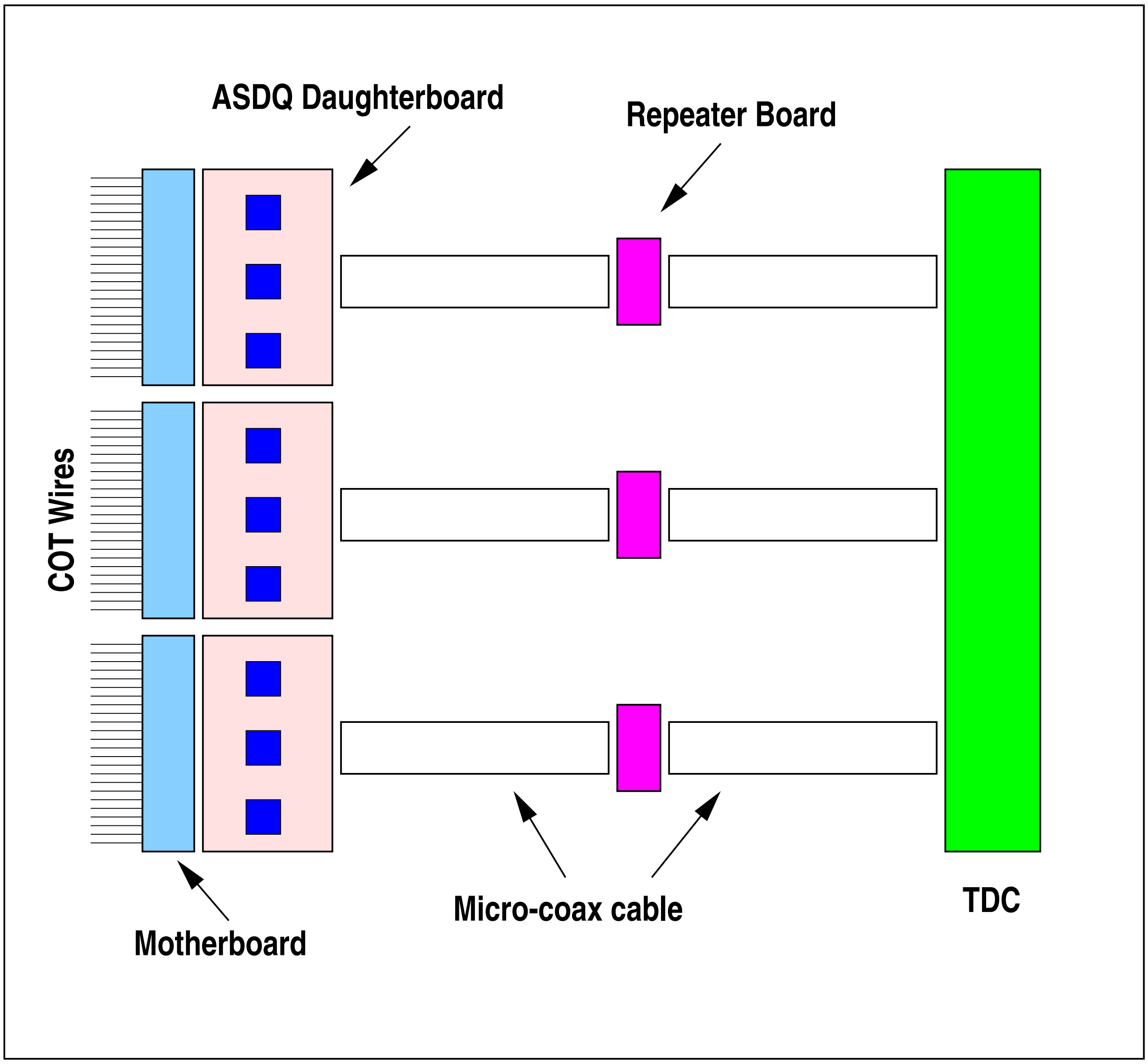

Figure 2: *The COT front end electronics scheme.*

3 ASDQ Requirements

High luminosity operation requires good double-pulse resolution for the electronics. Since the gas gain for the COT has a limited range for stable operation and the signal collection time is limited by the double-pulse resolution requirement, the noise in the electronics needs to be kept at a low level. In addition, to ensure that the double-pulse resolution is not degraded by the electronics, the discriminator is required to have a sub-nanosecond timing accuracy. All these requirements result in a high bandwidth and low threshold circuit that is susceptible to noise pickup from RF sources. To minimize the RF pickup the electronics are mounted on the COT itself. This presents an additional constraint of low power requirement of the circuit in order to minimize heat dissipation in the tracking volume of the CDF-II detector.

4 COT Signal

When a charged particle traverses a cell in 50:35:15 Ar-Ethane-CF_4, it leaves an ionization trail in its wake. From experimental data[2], there are ~ 28 clusters per cm for a minimum ionizing particle in Ar. The cluster size distribution in terms of the number of electrons (N_e) is also determined from experimental data, and is shown in Fig. 3. About 85% of the clusters have three or fewer electrons in them. The distribution has a long tail, which has been truncated at $N_e = 100$, and the mean of the distribution[1] is about 3.

The electrons in the ionization trail move towards a sense wire of the cell with the gas drift velocity of $v_{drift} \sim 90$ μm/ns. Within a few diameters of the sense wire, the large gradient of the logarithmically increasing electric field accelerates the electrons and they initiate a limited avalanche through secondary ionizations. The average number of secondary ionizations produced per primary electron, or the *Gas Gain*, is determined by the potential of the sense wire and is approximately $G \sim 2 \times 10^4$ for the COT chamber. A high gas gain results in rapid aging of the wires, and may also deteriorate the signal. Therefore, the gas gain of the chamber has a limited range for stable operation.

The typical distance traveled by a minimum ionizing particle in the gas is 3 mm. In order to determine the total number of electrons (N_i) that

[1] If the distribution is not truncated then the mean can be arbitrarily large.

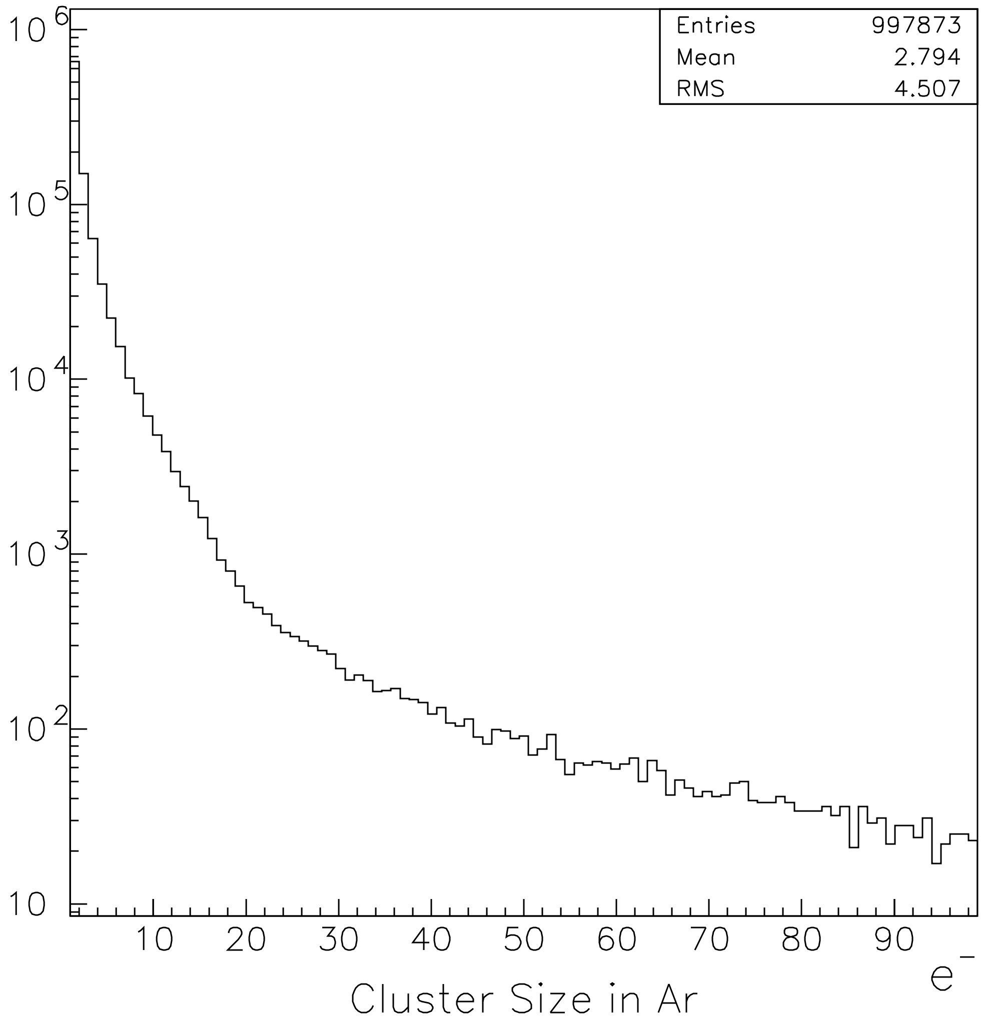

Figure 3: *Cluster size distribution for minimum ionizing tracks in Argon.*

drift to the sense wire (in the absence of Gas Gain), the mean number of clusters produced per cm (28/cm) is Poisson fluctuated and then combined with the individual cluster sizes. The resulting distribution is shown in Fig. 4. On average about 20 electrons drift to the sense wire. For an operational threshold of 5 (10) electrons, approx. 95% (80%) of the ionization signal is accepted. The Fig. also shows the distribution for a 5 mm path of a minimum ionizing particle. In that case the average number is about 30.

The total amount of charge deposited by a typical minimum ionizing track is given by $Q \sim N_i \cdot G$. This corresponds to a charge of 4×10^5 electrons or 64 fC[2]. However, not all of this charge is available for signal processing to the front end electronics.

Electrons produced by secondary ionization drift immediately to the sense wire. Since they are already close to the potential of the sense wire, they do not contribute significantly to the total signal. The positive ions produced in the avalanche move away from the sense wire and induce the signal on the wire that is detected by the readout electronics. Since the drift velocity of the relatively massive ions is much smaller than that for the electrons, they produce a measurable signal, referred to as the *ion tail*, on the wire that lasts for several microseconds. For good double-pulse resolution it is essential that both the charge collection time, and the inherent noise in the measurement (which is favored by a long charge collection time) be minimized. The strategy chosen is to collect enough charge to efficiently detect the signal avalanche charge while rejecting the remaining long tail.

The time evolution of the signal can be determined by analyzing the drift of charge in the electric field surrounding the sense wire. For the case of a proportional tube, this is done in detail elsewhere[2]. Here we only present the qualitative arguments.

In the case when the input signal rise times are shorter than the typical time scales ($\tau = CR$) of the capacitances and resistances connecting to the sense wire, the potential of the sense wire is re-established quickly. The readout electronics then act as a current source, and the signal manifests itself as a current that flows in the readout circuit. In terms of the wire radius (a), the tube radius (b), the radial electric field of the wire ($E(r)$), the ion mobility (μ_0) and the deposited charge (q), the time evolution of the current is described by:

[2] 1fC= 6250 electrons

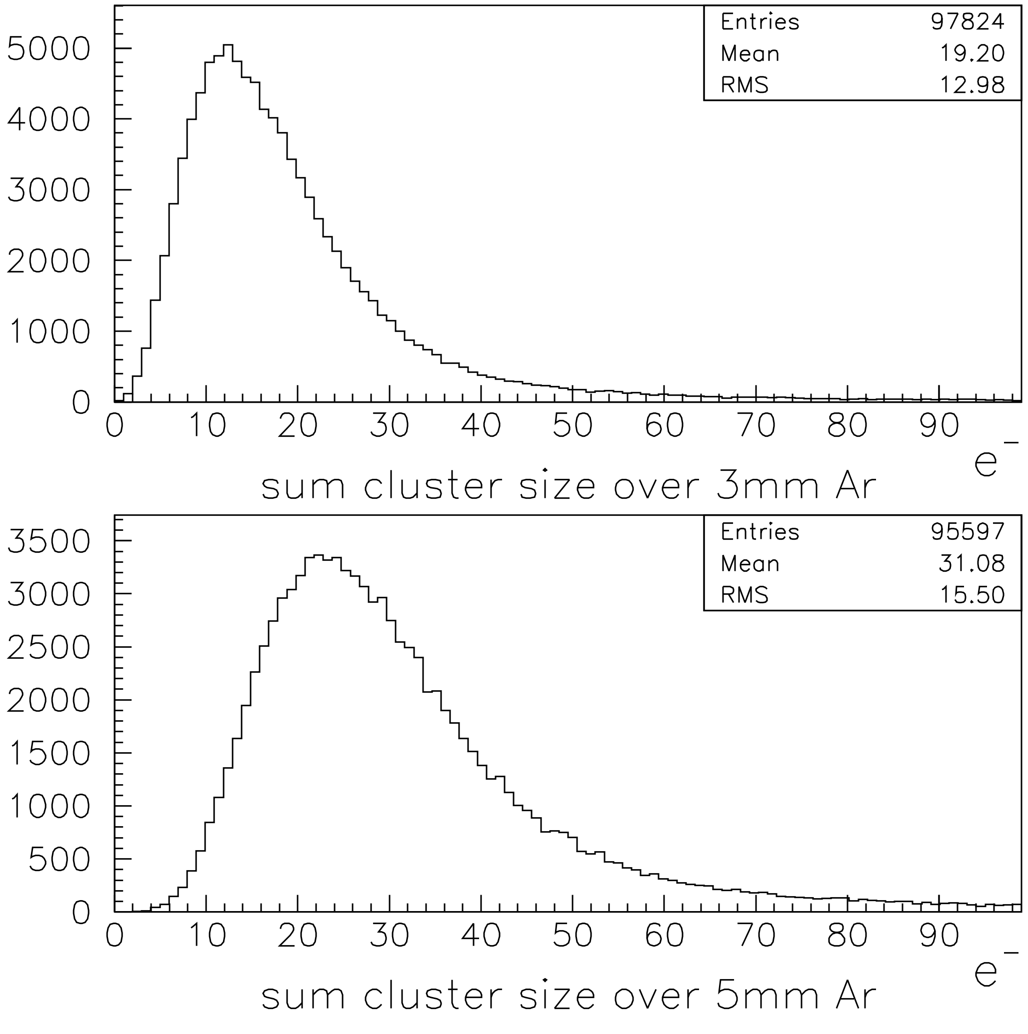

Figure 4: *Total number of electrons produced by a minimum ionizing particle that drift to the sense wire.*

$$I(t) = \frac{q}{ln(b/a)} \frac{1}{t + t_0}$$

Here $t_0 = a/2\mu_0 E(a)$ is the characteristic time for the sense wire in a given gas mixture. The current distribution in time is very narrowly peaked at zero, with a width t_0. The remainder of the signal is a factor b^2/a^2 wider than t_0. This $1/(t + t_0)$ behavior is characteristic of the signal induced by the ions. Strictly, this holds only in the case of perfect radial symmetry of the system, and neglects the effect of the electron contribution to the signal.

The electrons arrive almost instantaneously on the wire, and their contribution, is not negligible during time periods equal to the measurement time of the circuit. The electron component of the signal is incorporated by adding to the $1/(t + t_0)$ term a delta function at time $t = 0$ whose contribution to the charge is one-tenth of the charge collected in the measurement time of the circuit (8 ns). The COT signal is then parameterized as:

$$I(t) = \frac{k}{t + t_0} + \delta(0) \cdot \frac{1}{10} \int_0^8 I(t)dt \qquad (1)$$

Here $k = -0.8$ fC and $t_0 = 3$ ns have been determined using previous studies of drift chambers with similar properties[3].

Fig. 5 shows the characteristic shape of this signal as produced by a circuit that mimics the electron spike and the ion tail. It should be noted that this is the signal of one electron-ion pair on the wire. The actual signal on the sense wire is the sum of all the individual point ionizations and is shown in Fig. 6. This figure has been produced using GARFIELD[5]. More details about GARFIELD simulations are presented in Section 6.

The measurement time of 8 ns for the circuit has been chosen by studying digitized signals from a prototype COT chamber that have been fed into a SPICE simulations[6]. In addition, a longer integration time also decreases the bandwidth, and therefore improves the signal to noise ratio by lowering the noise.

In order to determine the fraction of total deposited charge that is available in the first 8 ns, one should integrate equation 1. Since the ion-tail extends for several microseconds, the fraction is normalized relative to the charge collected in $t_{1/2} = 1.5\mu s$. It is seen that only $\approx 18\%$ of the total deposited charge is available in the first 8 ns.

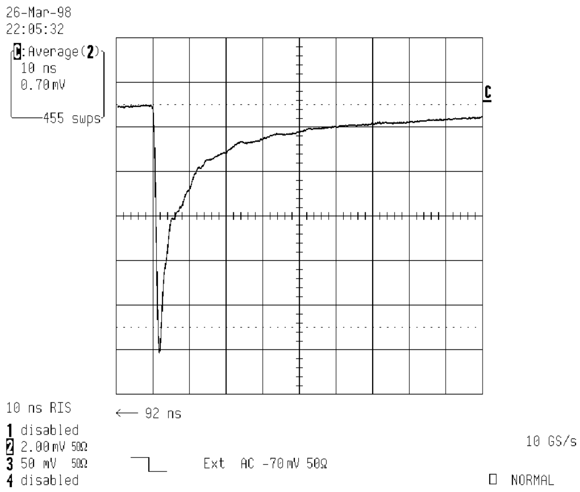

Figure 5: *The signal shape of a point ionization.*

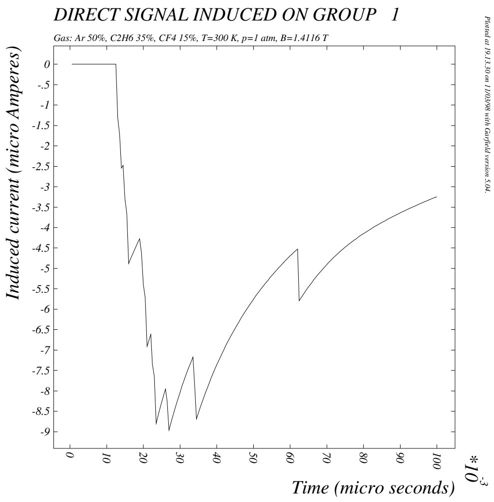

Figure 6: *The total signal from multiple point ionizations.*

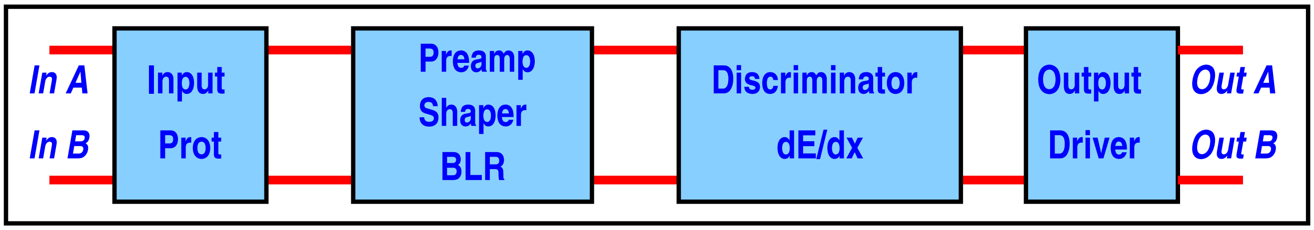

Figure 7: *ASDQ single channel block diagram.*

In addition, only 37.5% of the charge available during the first 8 ns makes its way into the circuit due to two effects. First, since the signal propagates in both directions, only 50% of the charge available comes into the circuit. In addition, the stray capacitance of the system results in further loss of charge equal to $C_{stray}V_{sense}$. This Fig. of 37.5% does not include the effects of a further loss of charge due to the attenuation of the signal as it travels down the sense wire which acts as a transmission line. Therefore, the total amount to "usable" charge for signal processing is about 18% × 37.5% = 7% of the charge deposited on the wire.

As a benchmark, a minimum ionizing particle deposits about 7 fC of usable charge into the circuit.

5 The ASDQ ASIC

5.1 Overview

The ASDQ ASIC has been implemented on a monolithic 5.4 $mm \times 3.9$ mm silicon substrate using an analog bipolar process. The block diagram of an individual ASDQ channel is shown in Figure 7. An incoming signal from the chamber goes through the following components of an individual channel:

1. Input Protection
2. Preamplifier
3. Tail Cancellation
4. Baseline Restorer

5. Discriminator
6. Width Encoder (dE/dx)
7. Output Driver

The signal from the wire goes into an *input protection* circuit designed to buffer the *preamplifier* from large external positive and negative spikes. The preamplifier amplifies the signal and converts the charge input into a voltage output while minimizing the noise added to the signal.

The presence of the ion tail inhibits efficient high rate operation. Fortunately, the time development of this signal is well understood and can be cancelled by introducing a circuit element whose impulse response produces a mirror image of the ion tail. This is referred to as *Ion Tail Cancellation* and is implemented in the ASDQ. After the preamplifier, a pole-zero cancellation network is used to eliminate the ion-tail in the signal. An additional pole-zero element removes the tail introduced by the preamplifier.

After the tail cancellation, the signal is fed into the *Baseline restorer* (BLR) which brings the signal back to nominal zero. A large signal in the chamber can introduce a significant shift in the baseline of the pulse. This can artificially cause the signal to stay above threshold for a long time, inhibiting fast performance in a busy environment.

After the BLR, the shaped signal is then DC coupled to a three stage *discriminator*. If an above-threshold signal is detected, a charge measurement is performed using the dE/dx element.

Due to the energy of the colliding beams, crude particle identification is possible using a pulse height information from several cells. Specifically, the number of primary ions produced in the gas by electron tracks is significantly (up to 40%) larger than those produced by heavier particles due to the highly relativistic nature of the electron in comparison to other heavier particles. This charge information can be crudely encoded into the comparator width but would be far too ambiguous if simply treated as the time spent by the signal over threshold. In the ASDQ, once an above-threshold signal is detected, a long time-constant signal integration is used to keep the comparator from returning to baseline before the signal from several primary ions can be integrated. This feature is often referred to as dE/dx. This feature can be turned off which is of utility for inner COT cells that are expected to operate at high rates, .

Finally, the discriminator output is fed into a differential open collector *output driver*. The evolution of the signal after the various stages of an individual ASDQ channel is shown in figure 8.

Various controls are also provided in the circuit. A selectable *attenuator*, when enabled, reduces the amplitude of the signal into the baseline restorer by a factor of 2. The leading and trailing edge thresholds of the discriminator can be adjusted externally. This impacts the triggering threshold for the discriminator and the width of its output pulse. The width of the discriminator output can also be adjusted by varying the drain current in the integrating capacitors in the width encoder. A larger drain current corresponds to a faster return to the trailing edge threshold of the discriminator and therefore a smaller discriminator output pulse width. In addition, the output width may also be changed by changing the a trailing edge threshold.

Two calibration circuits housed on the ASDQ provide COT-like pulses to the even and odd numbered channels respectively. The pulses are programmable in the range of zero to ≈ 30 fC. The calibration circuits provide an *in situ* capability to determine the absolute delay in the response (t_0) and a check of the output width uniformity (for different charges) for every channel.

A monitor circuit, if enabled, allows the user to examine the "analog" portion of the signal in the circuit. Specifically, the output of the BLR can be studied for the eighth channel of every ASDQ for debugging purposes.

The CTC readout electronics were fabricated using a mixture of discrete components and commercial Integrated Circuits. The ASDQ borrows from past experience with wire chamber ASIC's (ASD8[3] and ASDBLR[4]) and the original CTC charge encoding scheme. In this design we have modified the Baseline Restorer used in the ASDBLR, replacing it with a controlled current bridge diode array described later. The Preamp, Tail Cancellation and Shaper circuit is based on previous designs used in the ASD8 and later in the ASDBLR.

The specifications of the ASDQ are documented in Table 1. They have been studied using SPICE and GARFIELD[5] simulations, and a prototype COT chamber using Cosmic Ray and Fe^{55} data[6]. In the following subsections, the different components of the circuit are described in more detail. Interested readers are strongly encouraged to get the technical details from [3].

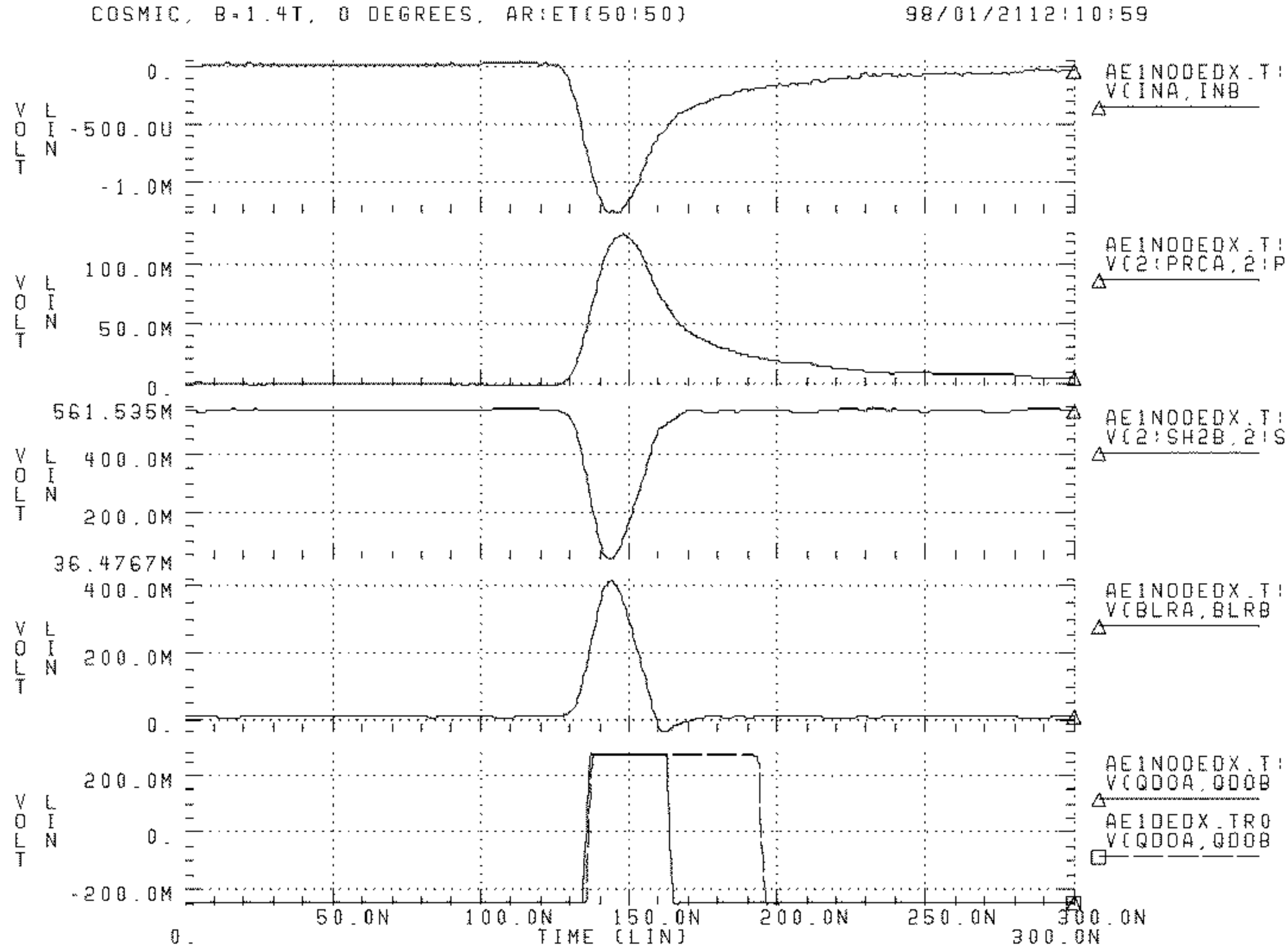

Figure 8: *Signal evolution for a Cosmic ray track which deposits 80 fC into the Preamplifier. From top to bottom the input into the Preamplifier, the output of the Preamplifier, the output of the Shaper, the Output of the Baseline Restorer and the output of the Discriminator (dE/dx on and off) are shown.*

In summary, the design of the ASDQ has been driven primarily by the following considerations:

- Good position resolution ($\sim$200μm)
- Good double-pulse resolution of the circuit with and without dE/dx enabled ($\sim$20 ns).
- Good charge measurement by the Width Encoder (dE/dx) over a large range (5 fC to 150 fC).
- Low operating thresholds ($2 - 3$ fC)
- Uniformity of response (channel/chip)
- Good stability of the circuit to temperature and process variations.

5.2 Technology

The ASDQ chip is fabricated using the inherently radiation-tolerant bipolar technology. This technology offers low intrinsic noise, low intrinsic capacitance and high speeds. Bipolar transistors offer the highest transistor gains, g_m, per unit of quiescent current of all commercially available technologies. This particular combination of properties makes it ideal for fast designs with low power requirements and low intrinsic noise. The typical noise level is 2000 ENC. This process offers excellent device matching and well characterized SPICE models. Two micron layout rules for the two metal layers allow close packing of devices. The active devices used in this circuit are vertical npn transistors. The passive components include Active Base (AB) and P+ resistors. The passive components also include CMOS capacitors. Most of the filtering capacitors used in the circuit are provided by the **Cpi** libraries supplied by Maxim. Other custom devices are constructed during the layout using the basic models contained in the process libraries. For detailed characteristics of the different devices, the reader is referred to the MAXIM technical manual.

The layout of the ASDQ was performed using **Quickic8**. Figure 9 shows the layout of the ASDQ chip. The eight individual channels in the chip are visible. The signal enters from the input pads at the bottom of the chip. After passing through the input protection circuitry, it is fed into the preamplifier.

The layout of each channel is sub-divided into two areas. The lower half of the chip comprises of the "analog" portion, which includes the preamplifier, shaping and baseline restoration stages. The output of baseline restoration is then sent into the upper half of the chip which contains the "digital" parts of the chip -the discriminator and the width encoder. The smallest rules in the layout are $1.8\mu m$ in width. Along the sides of the chip, the protective decoupling capacitors and the calibration circuitry are visible.

In order to ensure low channel-to-channel cross-talk, good isolation has been implemented in the layout. In addition, in order to maximize the yield, certain "in-house" layout rules have been followed. These rules involve the spacing between the active and passive components, proximity of components to major power and ground buses and shielding of the sensitive areas of the circuit from sources of potential noise pickup. Finally, in order to allow circuit changes through metal mask changes only, extra components have been strategically placed throughout the critical sections of the layout. Metal mask changes are cheaper and faster than more involved changes in the layout.

The ASDQ has been fabricated at MAXIM. Each wafer has been contains about 250 ASDQ sites. The chip is housed in a 64 lead thinned Quad flat pack TQFP package. A thorough characterization of each wafer has been provided by the manufacturer.

5.3 Input Protection

The sense wire of the COT attaches through a 550pF capacitor to the ASDQ. The sense wire is held at a potential of 3 kV, which implies that the capacitor has a stored energy of about $1.5mJ$. In the case of a breakdown of a wire, all that energy would be dumped into the ASDQ. Therefore an input protection is necessary. In addition to the input protection provided on the chip, a diode will be present on the ASDQ daughter-board. Fig. 10 shows the schematic of the input protection circuit.

Following previous designs, the buried layer is used to form a low value resistor, and P+ resistor bodies are used to provide anodes for a large area multi-contact diode. The incoming signal is fed in parallel to several rake like fingers with multiple epitub contacts to provide a conduction path through the buried layer. The resistance of each leg is approximately 6Ω. Near the second row of epitub contacts that connect to the preamplifier input,

Overall Specifications	
Size	$5.4\ mm\ \times\ 3.9\ mm$
Technology	Radiation-tolerant Analog Bipolar
Channels	8
Pins	64
Package	Quad flat pack
Required power (stability)	±3V DC (±5%)
Power Dissipation (channel)	$40\ mW$
Channel Crosstalk	$\leq\ 1\%$
Threshold Temperature Sensitivity	$0.1\ fC/10\deg C$
Saturation (Tail Cancellation)	Linear to 600 fC
Saturation (dE/dx, no attenuation)	120 fC (Impulse on wire)
Saturation (dE/dx, attenuation)	240 fC (reduced resolution)

Table 1: ASDQ Specifications: Overall.

HV Protection (Negative Spike)	$350\ \mu m \times 400 \mu m$ epi-resistance and epi-P+ resistor diode
HV Protection (Fast Neg. Spike)	$32\times$ transistor, diode-wired
HV Protection (Positive Spike)	$100\ \mu m \times 250\ \mu m$ P+ epi-wired

Table 2: Input Protection Specifications.

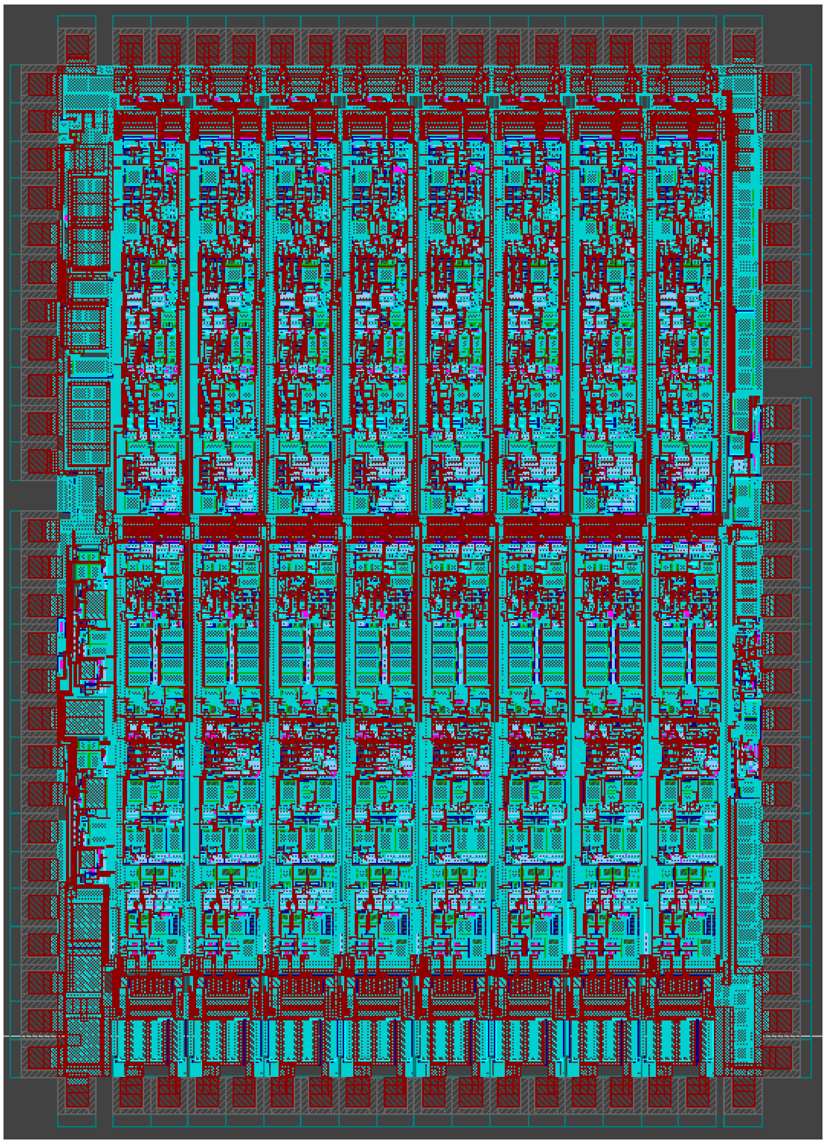

Figure 9: *The layout of the ASDQ chip.*

a row of P+ resistors, shorted to ground, provide the contacts for diode protection. The common emitter preamplifier keeps the input voltage at V_{be} above ground. Under normal operating conditions, the P+ resistor bodies do not conduct a signal current. Since the turn-on time for this kind of diode has not been characterized in sufficient detail, a standard large area transistor is included. The base and the emitter of the transistor are connected to ground, and the collector is connected to the signal to help catch the initial parts of a breakdown pulse.

In order to dissipate the energy from an inductive spike in the positive direction, the signal is attached to several resistors in a smaller epitub. The epitub contacts attach to a separate supply held at 1.2V.

The performance of this configuration has been tested in fabricated ASDQ's. A 560pF coupling capacitor, charged to 3 kV is discharged into the input of the ASDQ through an external 24 Ω resistor. No performance change is observed in the ASDQ.

The specifics of the input protection circuit are summarized in table 2.

5.4 Preamplifier

The preamplifier consists of a three transistor cascoded common emitter configuration. Although the input from the chamber is single ended, two identical preamplifiers are implemented for each channel. This pseudo-differential configuration provides a DC balanced input to the differential shaper and allows good common mode noise rejection. Inputs to each Preamplifier at the package level allow the exploitation of differential noise pickup rejection methods. A simplified schematic for each of the Preamplifiers is shown in Fig. 11.

Fig. 8 shows the response of the preamplifier to an input signal from a Cosmic ray track. Fig. 12 shows the evolution of the signal through the preamplifier. The signal enters from the left and is sent to the shaper on the right. The gain of the preamp is 1.5 mV/fC and it is linear for charges up to 2 pC. The preamp has a fast shaping time, 1.5 ns, and adds an 8 ns tail to the impulse input.

The preamp input impedance is controlled by balancing the capacitive and resistive feedback in the circuit. At low frequencies it is matched to the 260 Ω characteristic impedance of the COT. In order to maximize charge collection with the expected input stray capacitance of 10 pF, the input

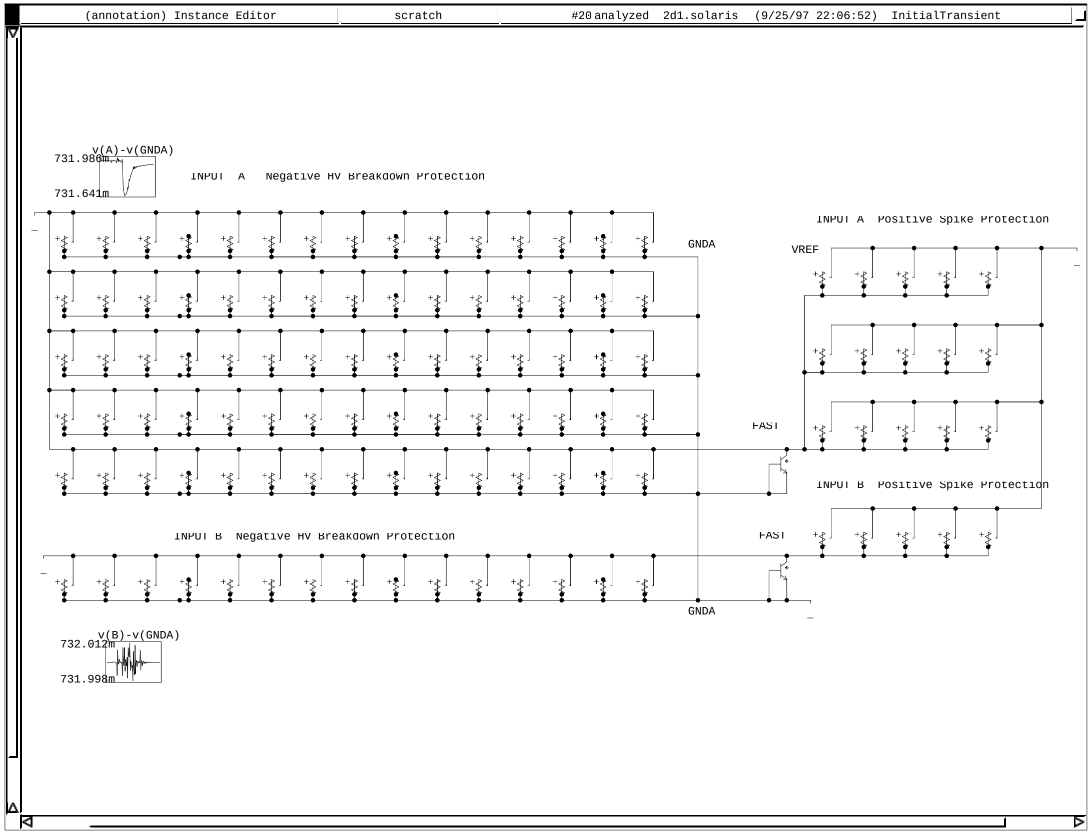

Figure 10: *The schematic of the input protection.*

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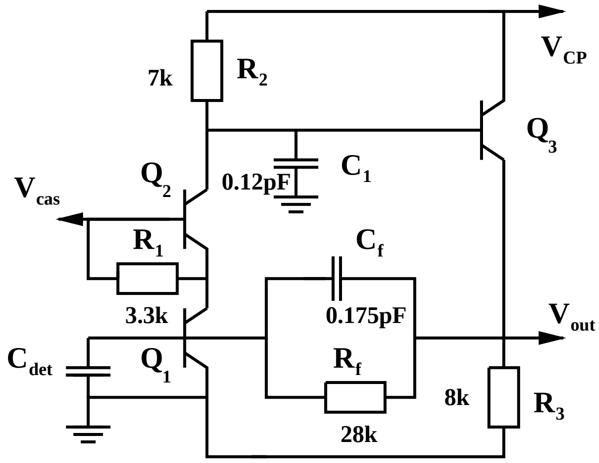

Figure 11: *The Preamplifier Schematic.*

impedance has been designed to roll off at high frequency. The roll off is about 30% at 30 MHz. Figure 13 shows a SPICE simulation of the input impedance of the ASDQ as a function of frequency for three different values of the stray capacitance, 0 pF, 10 pF and 20 pF, where the realistic value is estimated to be 10 pF.

The intrinsic noise of the preamplifier, referred to the input, is determined from SPICE simulations and measured by a count rate technique in fabricated ASDQ's to be 2100 electrons. The termination resistance of the wire introduces an additional noise of about 1800 electrons making the intrinsic noise of the system of the order of 4000 electrons. For efficient triggering, we require a signal to noise ratio in the preamplifier to be about 5 to 1. For a Gas Gain of 2×10^4, this corresponds to $\frac{5\times4000}{0.375\times20000\times0.15} \sim 18$ electrons or 6 clusters as the minimum amount of primary ionization in the chamber.

The details of input impedance, noise and the preamplifier are summarized in tables 3 and 4 respectively.

The Preamplifiers are inter-weaved in the layout in order to reduce imbalanced noise pickup. In addition, the input transistors of the Preamps are laid out in a *cross-quad* formation which ensure good geometric and thermal matching, and protect against systematic process variations.

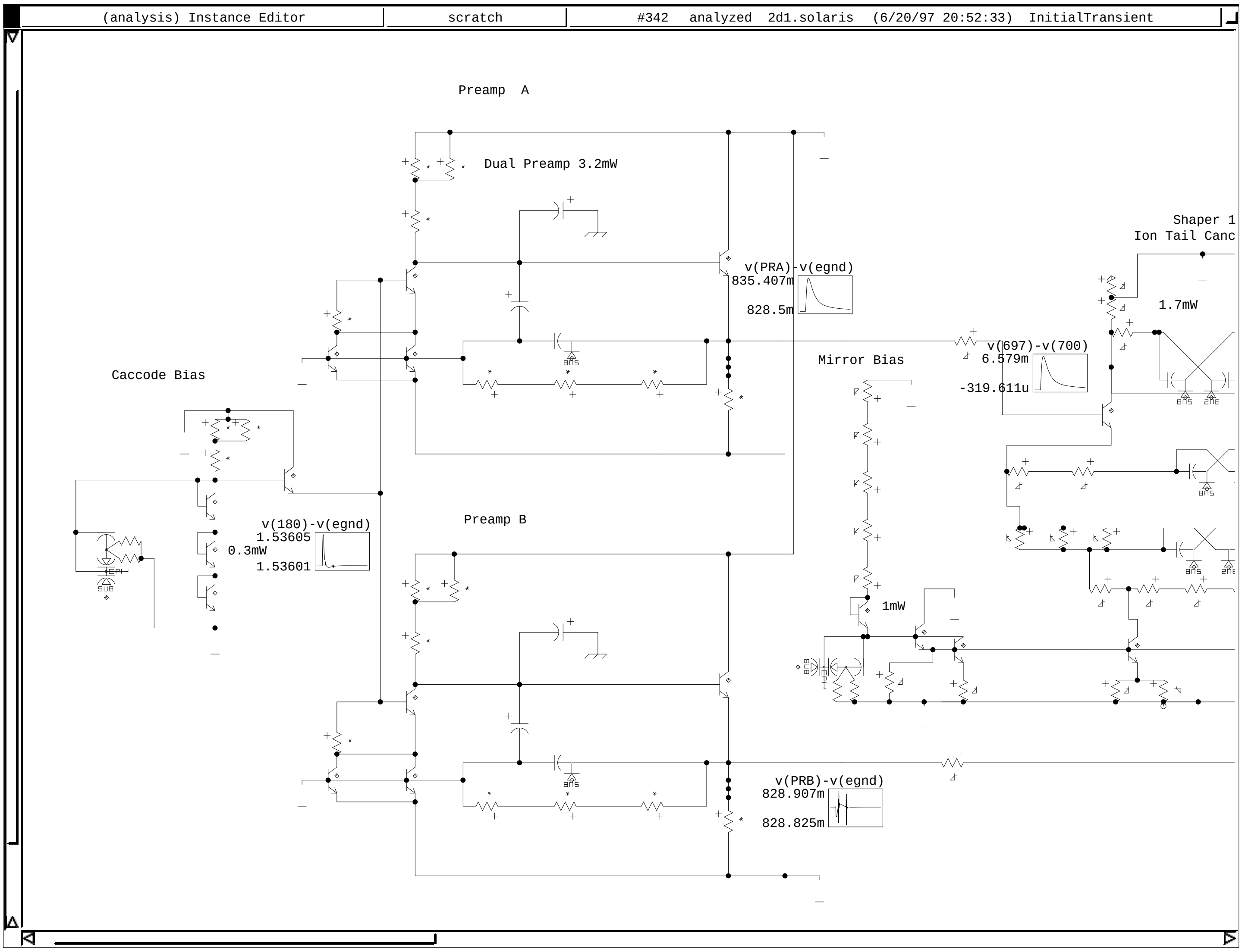

Figure 12: *Signal evolution through the Preamplifier.*

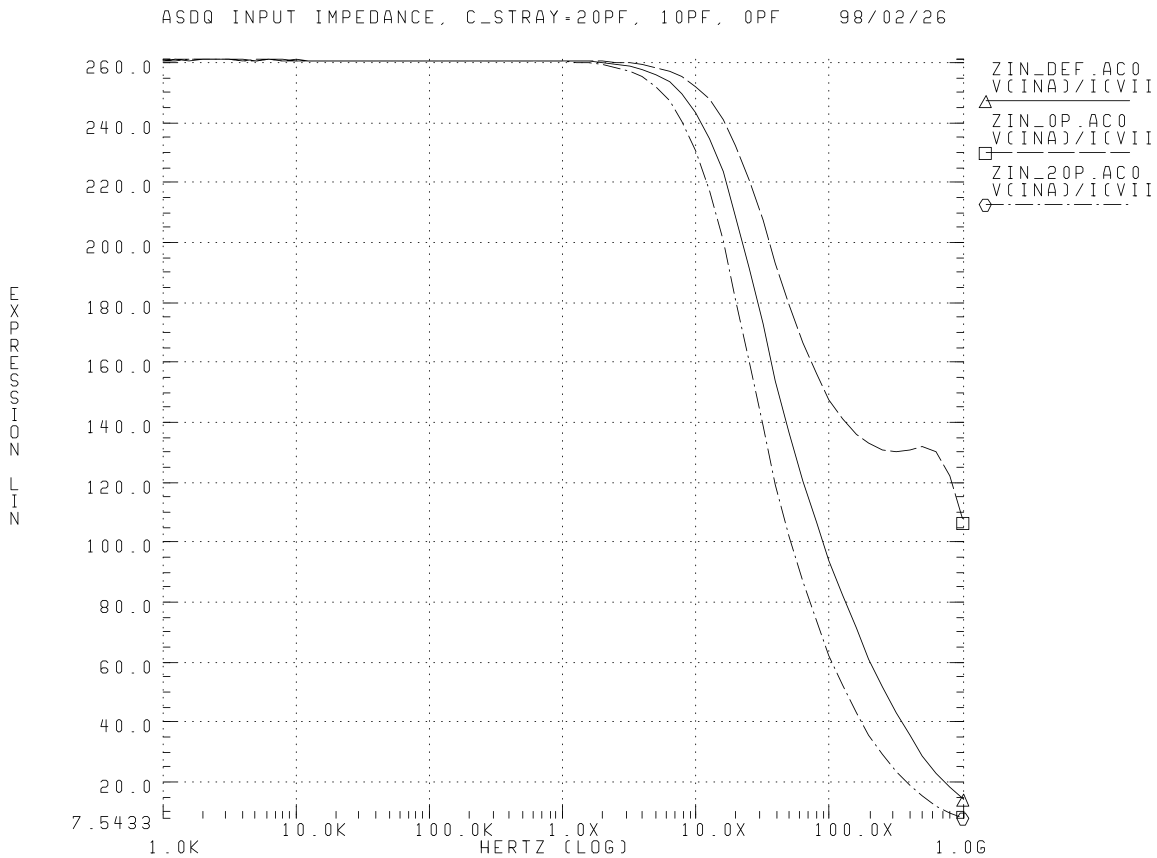

Figure 13: *ASDQ input impedance as a function of frequency. The three curves are for stray capacitance of 0, 10 and 20 pF. The realistic estimate for the stray capacitance is 10 pF (middle curve).*

Signal Input	
ASDQ Impedance (Low Freq.)	260Ω
ASDQ Impedance (High Freq.)	Roll-off by 30% at 30 MHz
Noise (10pF inp. cap)	$\sim$ 2100e (measured)
Noise (10pF+COT+Term. Res)	$\sim$ 3800e (calculated)

Table 3: ASDQ input impedance and noise

Preamplifier	
Gain	1.5mV/fC
Range	linear to 2 pC
Shaping	1.5ns rise

Table 4: Preamp Specifications

5.5 Shaping and Tail Cancellation

The ASDQ has a two stage fully differential multipole shaper. The goal of the first shaping stage is to eliminate the ion tail using the technique of pole-zero cancellation. In the second stage the tail induced by the preamp is also eliminated. In addition, the shaper provides a limited and fully differential signal to the BLR.

Fig. 14 shows the schematic of the shaping stage. The signal processed by the preamp enters from the left and after the shaping stage is sent to the BLR on the right.

Equivalent pole shaping results in an almost symmetric impulse response. This is good for double pulse resolution and does not impact the noise levels in the circuit. RC integrations in the collectors of each of the shaper stages in combination with the poles in the ion and preamp tail cancellation yield the almost symmetric impulse response. To minimize slew and optimize signal to noise, we have targeted a peaking time of 6 ns for the ion-tail compensated signal at the input to the Baseline Restorer. Additional shaping following the BLR increases the final peaking time to 8ns preceding the discriminator.

Ion tail cancellation depends on linear amplification of the input signal

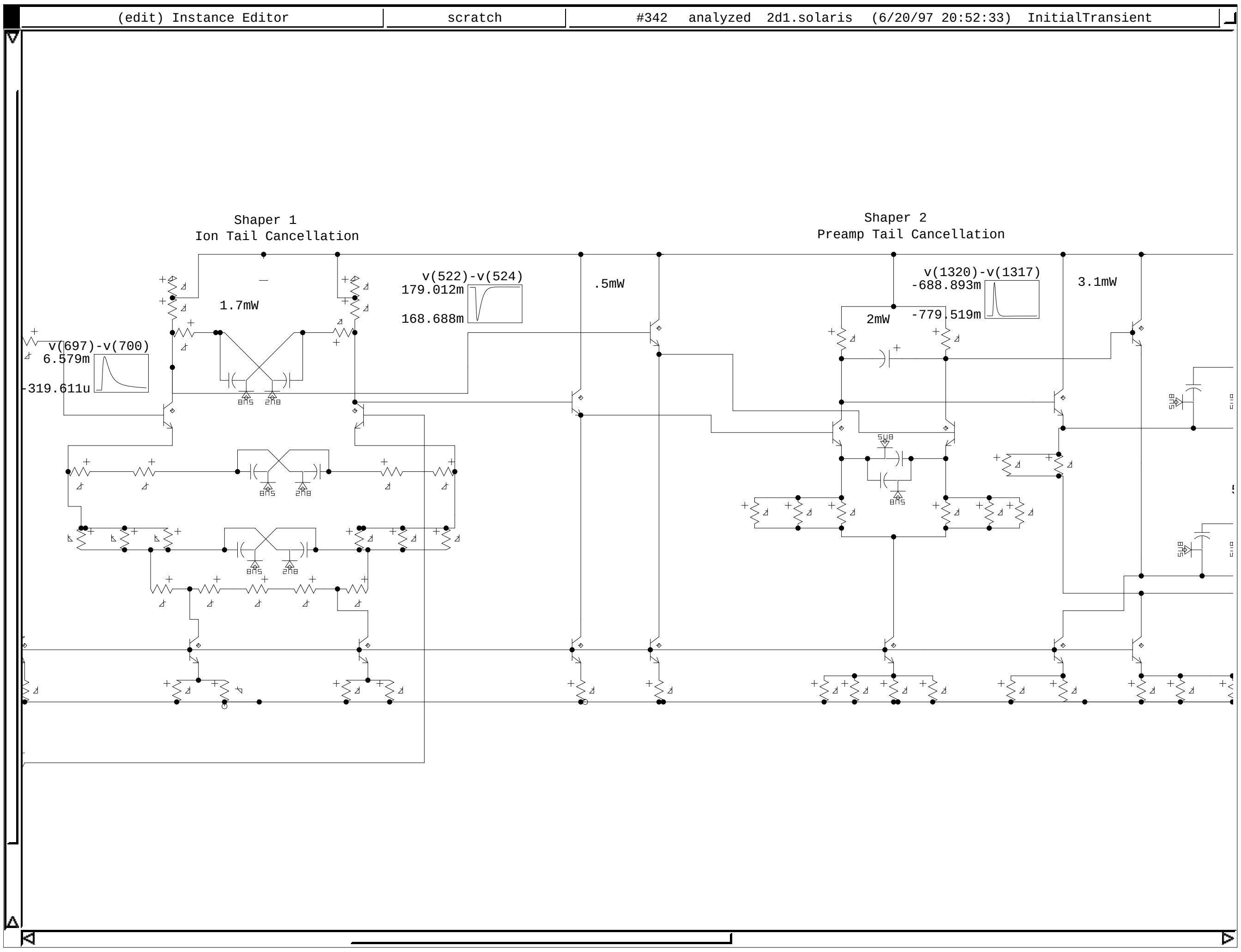

Figure 14: *Schematic of the shaper.*

and is performed early (in stage one) of the shaper where the largest dynamical range exists. The first shaper stage consists of a cascoded differential pair with a pole zero network in the emitters. Although the signal is not differential at the bases of the first stage shaper, it becomes differential in the collectors where the first integration occurs. Fig. 14 shows the output of the first stage of the shaper. It is seen that the ion tail contained in the input signal (on the left) has been eliminated at this stage.

The zero in the second stage of the shaper is intended to cancel the lowest frequency pole in the preamplifier. Fig. 14 also shows the output of the second shaper stage where now the tail has been completely eliminated. It is also seen that the output from the shaper is quite narrow.

The specifications of the shaper are summarized in table 5. A signal of 2 fC into the preamp results in a 45 mV signal with a 6 mV overshoot at the BLR output. The first stage of the shaper is linear to about 600 fC and the second stage begins to limit for an impulse (single ion) signal of 120 fC on the wire. Looking at the same charge split into 4 equal ion depositions over a period of 10 ns, the FS range increases to greater than 250 fC. A plot of width vs charge, which is sensitive to area and not the peak of the voltage profile shows a very linear relationship to about 60 fC. The relationship is nearly linear to about 120 fC and begins an obvious rollover out beyond 300 fC.

Shaper Specs	
Gain	25 mV/fC
Range (Ion Tail)	$\leq$600 fC
Range (Preamp Tail)	$\leq$120 fC
Shaping	6 ns 0-Peak at BLR input
Undershoot	$\leq$2%

Table 5: Shaper Specifications

5.5.1 Attenuator

A level selectable times-two resistor-based attenuator (as shown in Fig. 14) has been added after the emitter followers attached to the first differential pair in the Shaper. A 4K resistor is added in series with the output of each emitter follower and the input to the next differential pair. Attenuation is accomplished by supplying current to two diode-connected transistors which are attached to each other by an 8k resistance. When enabled, this provides a shunt resistance across the outputs, cutting the voltage input to the next differential pair stage by a factor of nearly 2.

5.6 Baseline Restoration (BLR)

The ASDQ has a fully differential BLR. The BLR offers several attractive advantages in signal processing. Its AC coupling removes DC process variations before the discriminator. It provides insensitivity to small offsets in the preamp arising mainly from differences in the base currents in the input transistors of the matched dual preamps. By breaking the DC path from input to output, it reduces the number of components that affect the DC offset, thus making it more feasible to consider a chip-wide threshold. In addition, its short time constant provides insensitivity to imperfections in the tail cancellation circuits. Since one cannot control $\tau = RC$ in integrated circuits to better than 30%, the accuracy of tail cancellation is compromised. This is especially helpful in recovery from very large signals that saturate the shaper. In DC coupled circuits for comparison, several microseconds of unstable behavior can accompany an input pulse that is large enough to fully saturate the tail compensation network. Recharge at high rate introduces a DC offset which is eliminated by the BLR. Thus the BLR significantly improves high rate performance and allows earlier re-triggering and eliminates multiple triggers when tail cancellation is saturated.

The BLR circuit schematic is shown in Fig. 15. Note that a 40K resistance, not shown in this schematic, has been added between the 8pF capacitors on the BLR side to set a known high impedance time constant.

The BLR implemented in the ASDQ has been designed to have minimal impact on the dE/dx capabilities. The initially proposed a baseline restorer consisted of a 10 pF integrating capacitor on each of the differential shaper outputs, followed by a single diode shunt that set the quiescent operating point of the other terminal of the capacitors. This arrangement provided satisfactory performance, maintaining a stable baseline, and introducing non-linear overshoot with minimal excursions. Examining the performance as an integrator, significant losses in integrated charge were found for signals spread

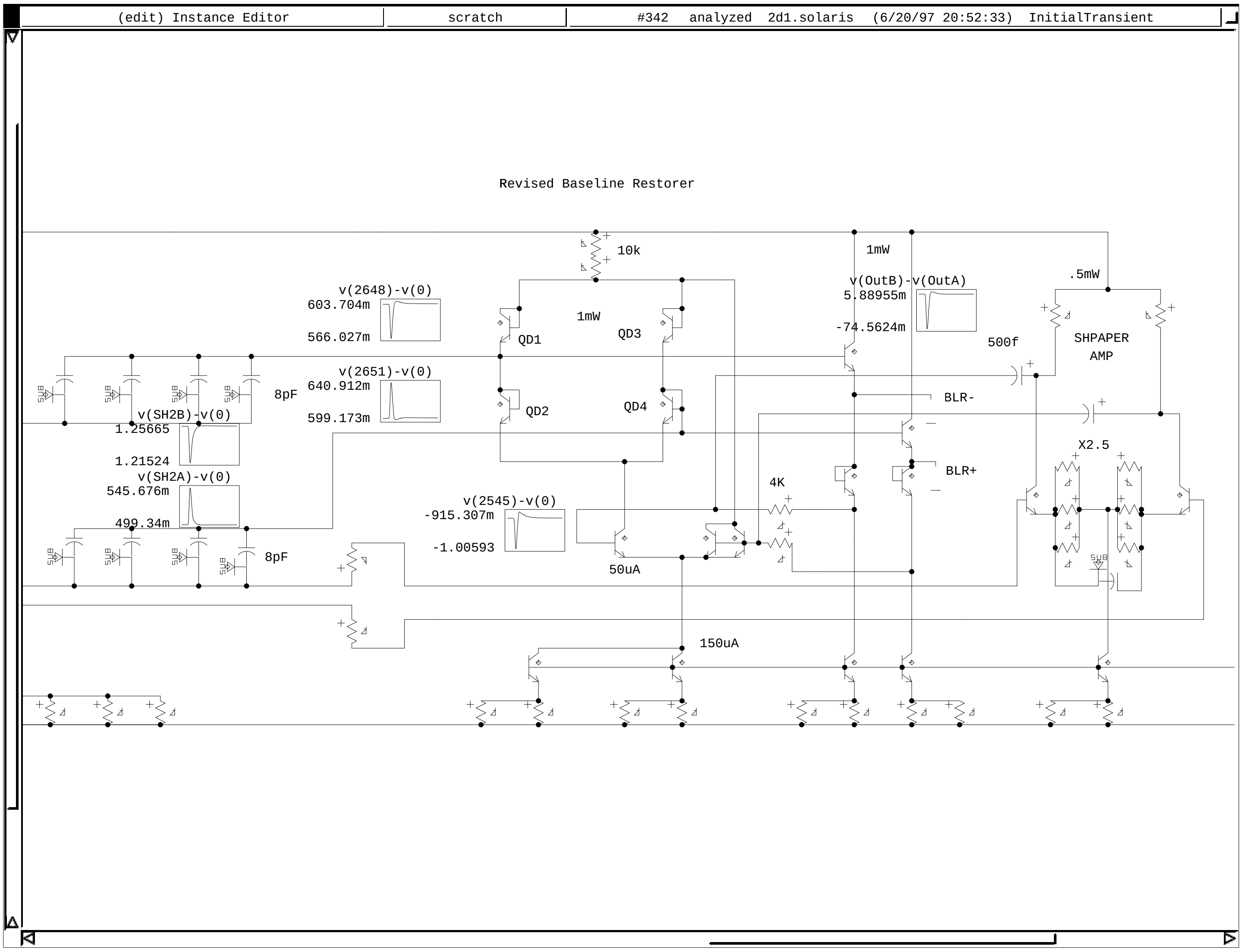

Figure 15: *The BLR Schematic.*

out in time over periods of up to 20 ns. Feeling that this would result in an unpredictable dE/dx width encoding, alternative designs were explored.

The alternative design significantly improves the integration function and improves the baseline recovery. Refer to Fig. 15. In this design, the shaper output is coupled to the BLR with two 8 pF capacitors. A four diode bridge offers a shunt path between the capacitors and holds each to the same potential. The current in the bridge is maintained by a differential pair biased to provide one third of the available current through the bridge in quiescent operation. The current available to this stage will be externally adjustable using a chip wide control by about $\pm 50\%$ to allow optimization after fabrication. The current in the bridge sets the shunt impedance between the outputs which is controlled directly by the BLR output level. The impedance goes to high values when the signal is of the desired polarity and goes to very low values when the output polarity is below baseline. Fig. 16 shows the response at the BLR output for signals ranging between 5 and 45 fC. The response of the BLR is seen to be linear over this charge range.

The 800 mV lobe of the 45 fC pulse is followed by a 33 mV excursion below baseline that is largely gone in 15 ns. The recovery time is shown in Fig. 17 where the discriminator response is plotted for a series of simulations with two 15 fC input pulses followed by a 2 fC pulse varied from 25 to 55 ns following the first 15 fC pulse. Both the single diode BLR and the new BLR retrigger within 35 ns of first pulse with the discriminator set to 1.5 fC. To improve the sensitivity to low level signals, the shaper output is used to drive a $2.5\times$ gain stage which is capacitively coupled to the diode bridge current regulator.

Also, it should be noted that the negative undershoot, as a fraction of the positive lobe of the signal, is progressively smaller for larger signals.

The response to a 1 fC chamber-like input signal at the shaper and BLR outputs for BLR circuits is plotted in Figure 18. While the signal attenuation is not large for this minimum size signal, the most striking feature is that the overshoot is significantly smaller than found using a simple diode clamp. This behavior continues to much larger pulseheight as can be seen in Figure 19.

Fig. 20 shows the response at the shaper and BLR outputs for a 20 fC chamber like pulse split into three equal 6.7 fC depositions that are 5 ns apart. As is seen in the plot, the effect in the BLR output signal is minimal. This effectively demonstrates that the BLR has a minimal impact on the

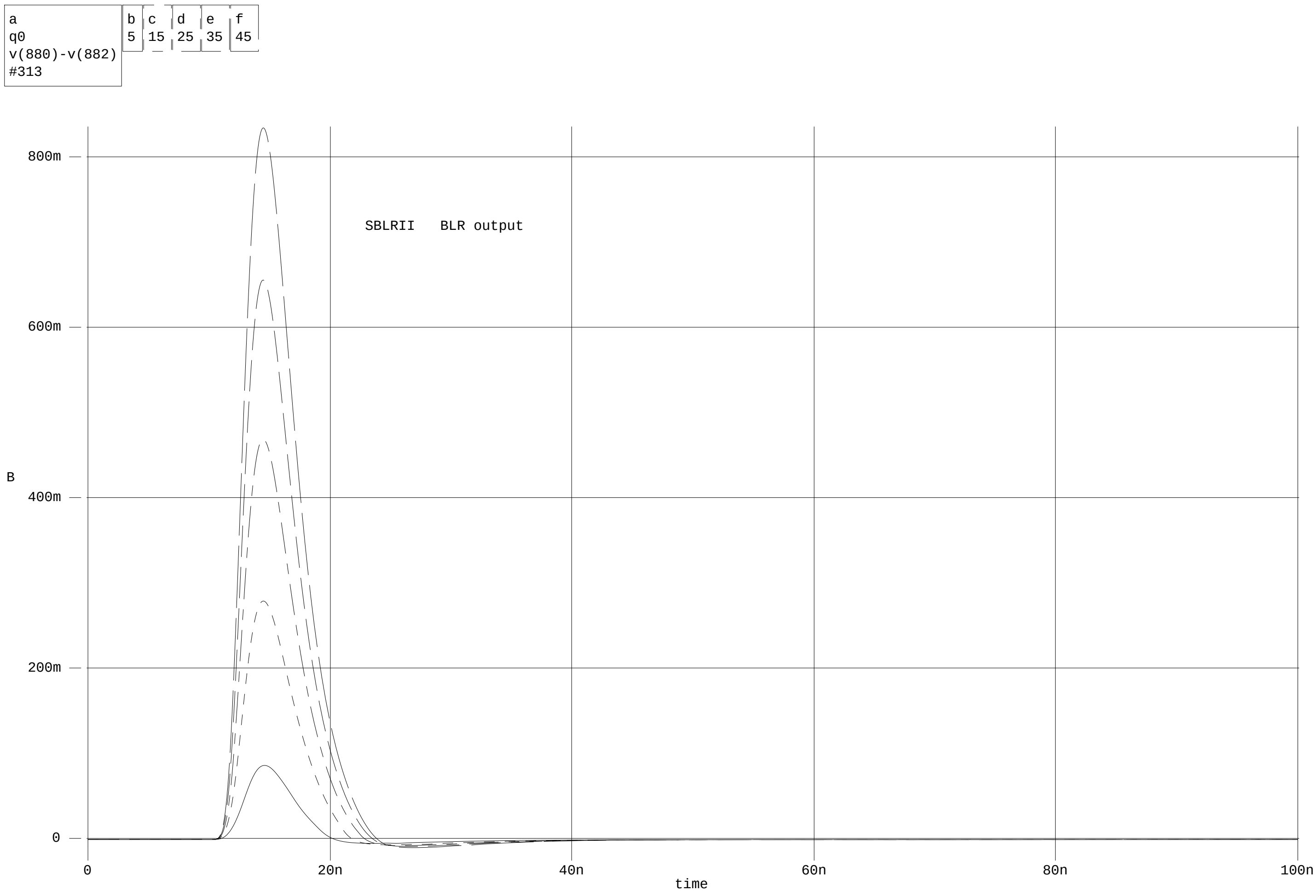

Figure 16: *Response at the BLR output for signals ranging between 5 and 45 fC.*

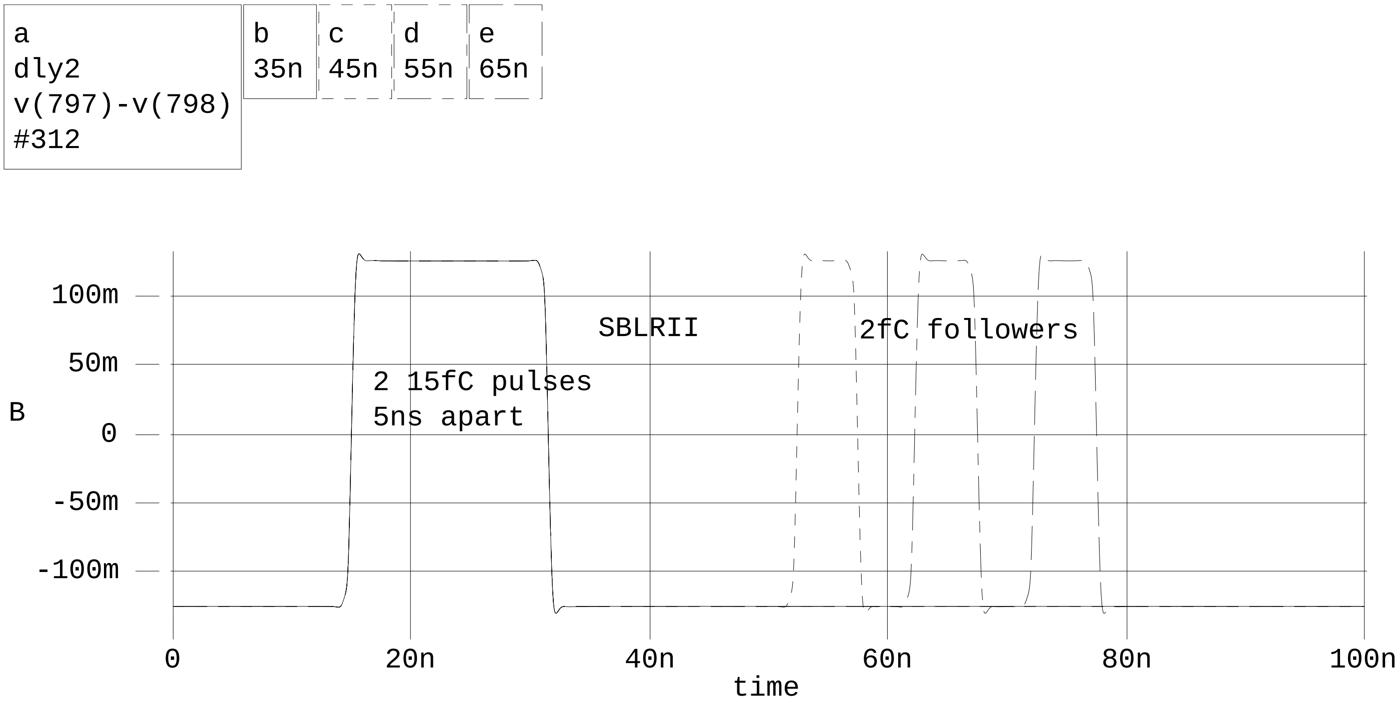

Figure 17: *Discriminator response is plotted for a series of simulations with two 15 fC input pulses followed by a 2 fC pulse varied from 25 to 55 ns following the first 15 fC pulse.*

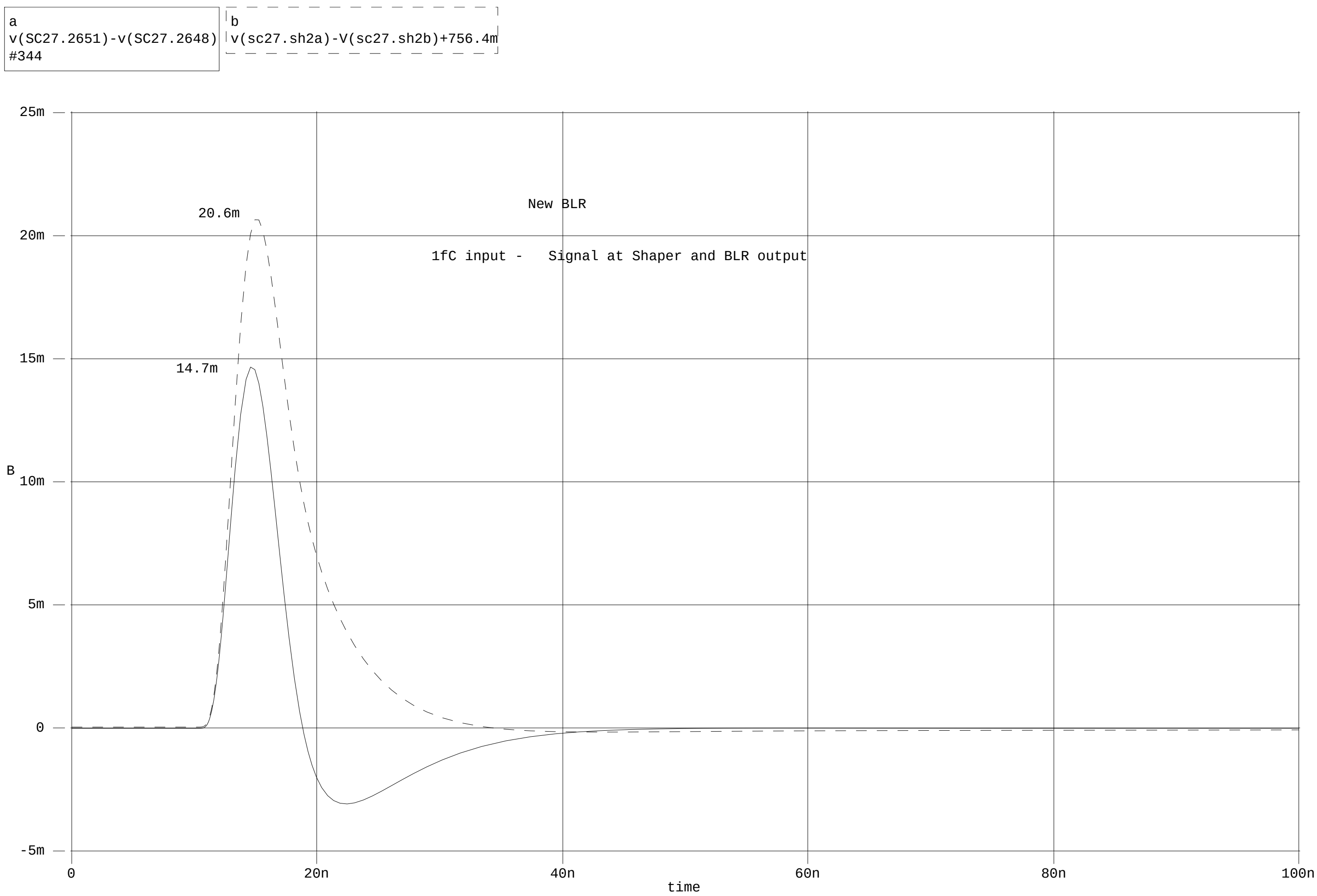

Figure 18: *Response to 1 fC pulse. Shaper and BLR outputs.*

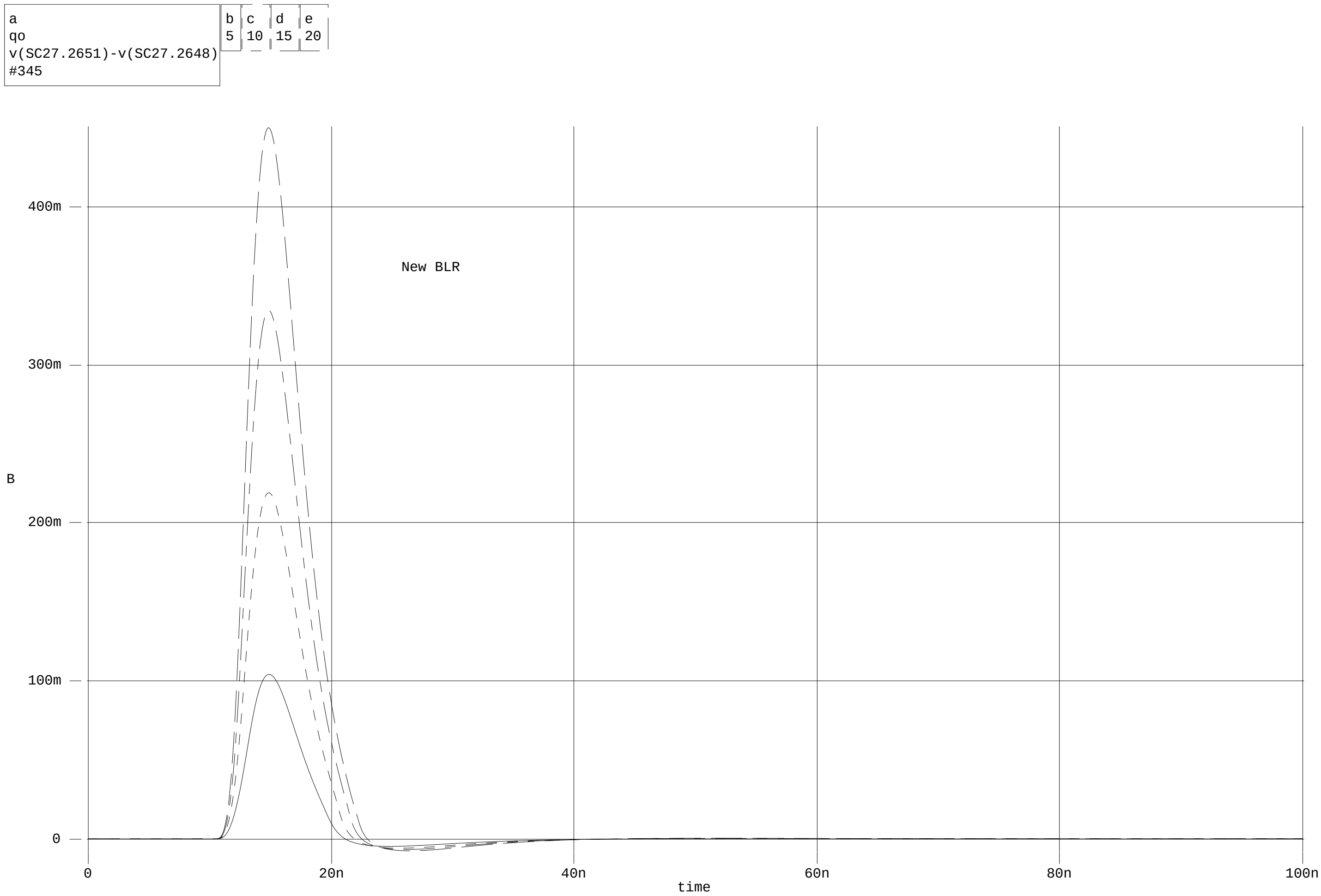

Figure 19: *Response at BLR output for 5 to 20fC input signals.*

dE/dx capabilities of the ASDQ.

Finally, the specifications of the BLR are summarized in table 6.

BLR	
Gain	$\geq$66% (3fC), 90% (> 30fC)
Range	120 fC
Shaping	No significant additional shaping for large pulses
Undershoot	$\leq$ 3 fC (Signals $\leq$100fC)

Table 6: BLR Specifications

5.6.1 Monitor Circuit

The monitor circuit allows the user to see the "analog" signal after the BLR for the eighth channel of every ASDQ. The gain of the circuit is 1.5 mV/fC on a terminated wire (with 6 ns integration time) and a maximum range slightly greater than 100fC without attenuator. With the attenuator, the range is effectively doubled.

5.7 Discriminator and dE/dx

The ASDQ has a three stage differential discriminator, similar in design to the one used in [3]. The full schematic of the discriminator and the dE/dx portion of the circuit, along with the evolution of the input signals is shown in figures 21, 22, 23 and 24. The discriminator has a programmable *leading edge* threshold. Once a signal is detected that exceeds the leading edge threshold, the discriminator triggers and remains on until the signal falls below the trailing edge threshold.

As mentioned earlier, since the arrival of ions at the wire is spread out in time in a non-deterministic way, it is necessary to integrate the charge for a relatively time to achieve the desired electronics resolution. To satisfy the requirement for leading edge timing precision and to minimize the number of cables coming out of the super conducting volume, we have chosen a switching technique based on the previous CTC readout that, when enabled,

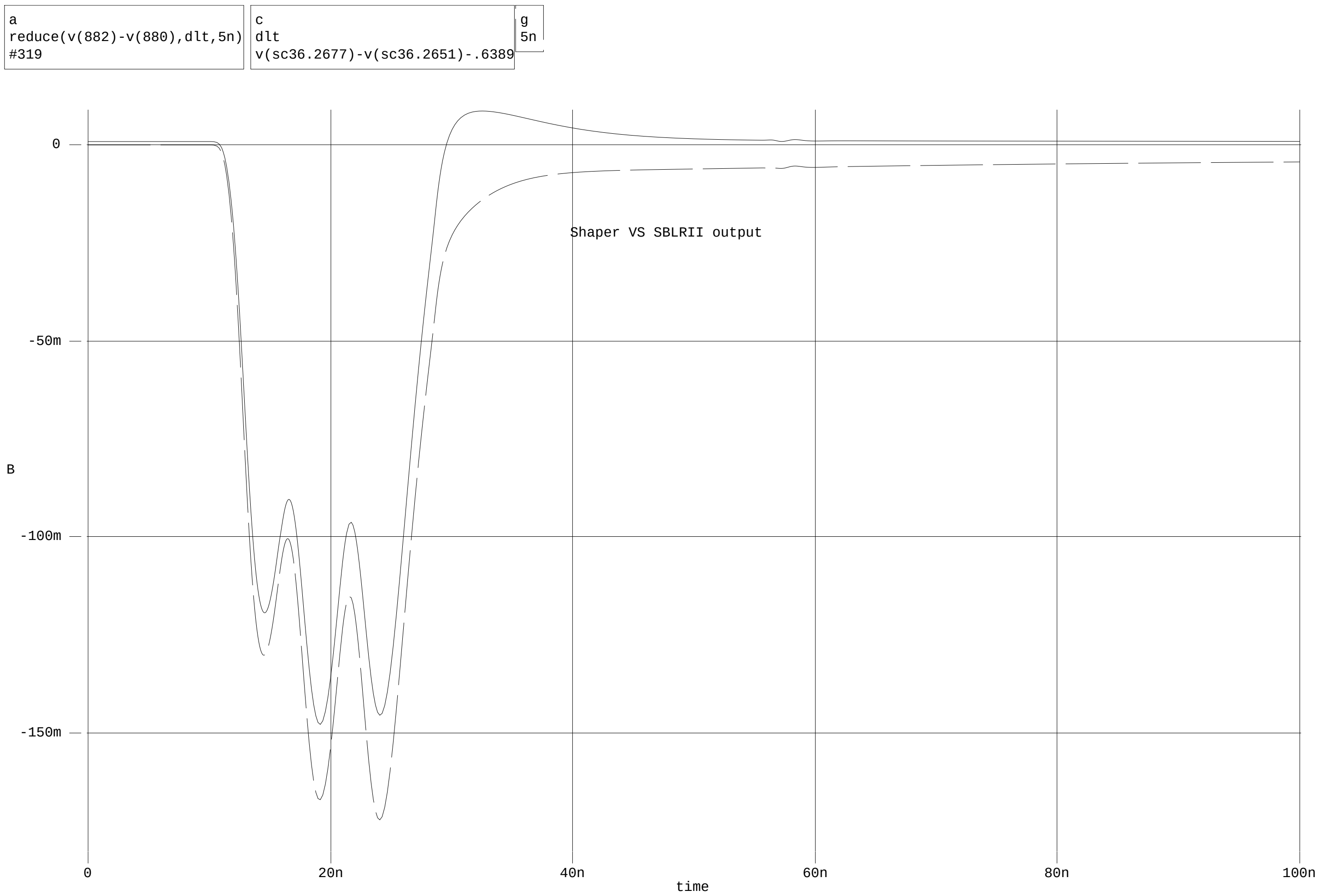

Figure 20: *Response of shaper and BLR to three 6.7 fC pulses separated by 5 ns.*

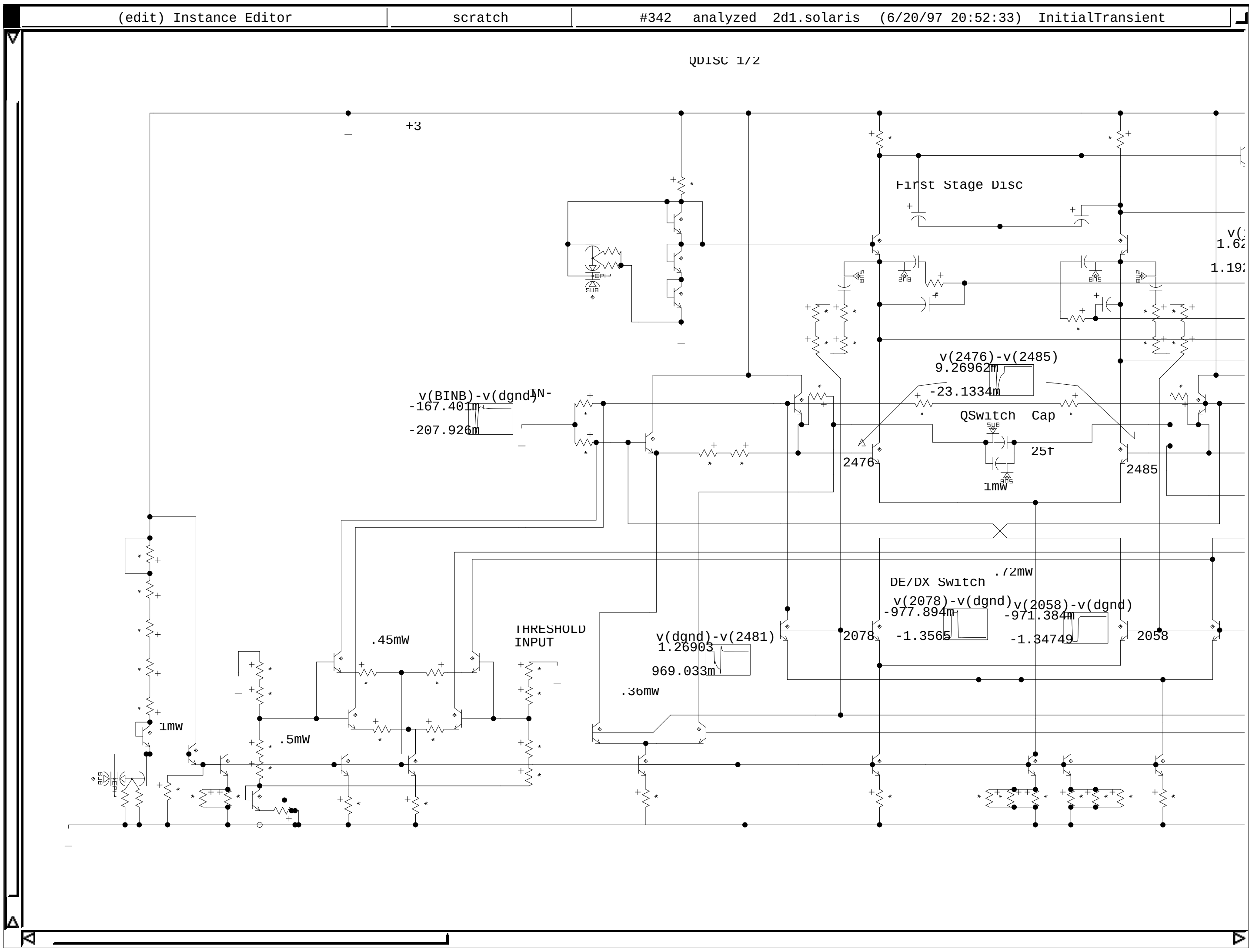

Figure 21: *Discriminator and dE/dx schematic (Part 1).*

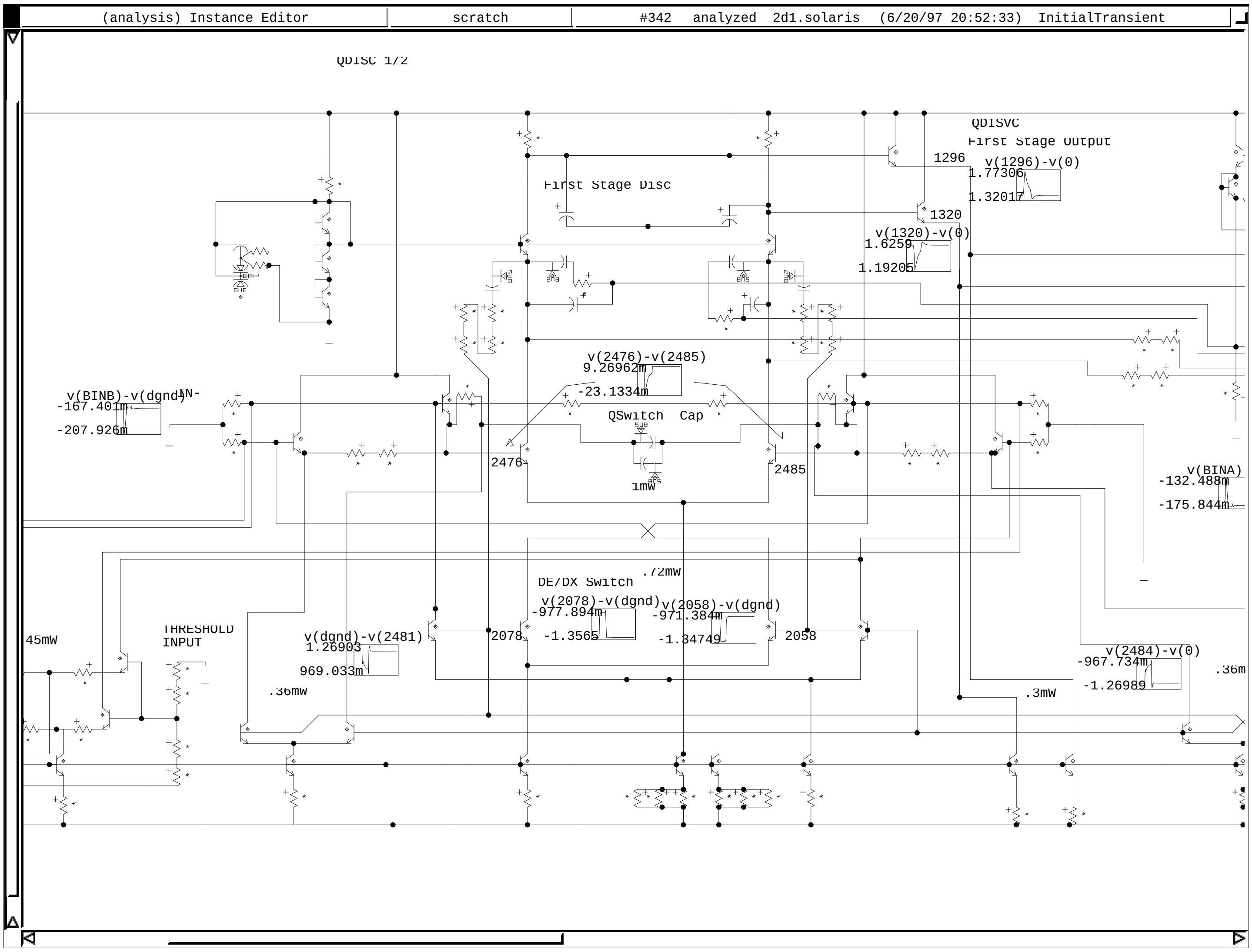

Figure 22: *Discriminator and dE/dx schematic (Part 2).*

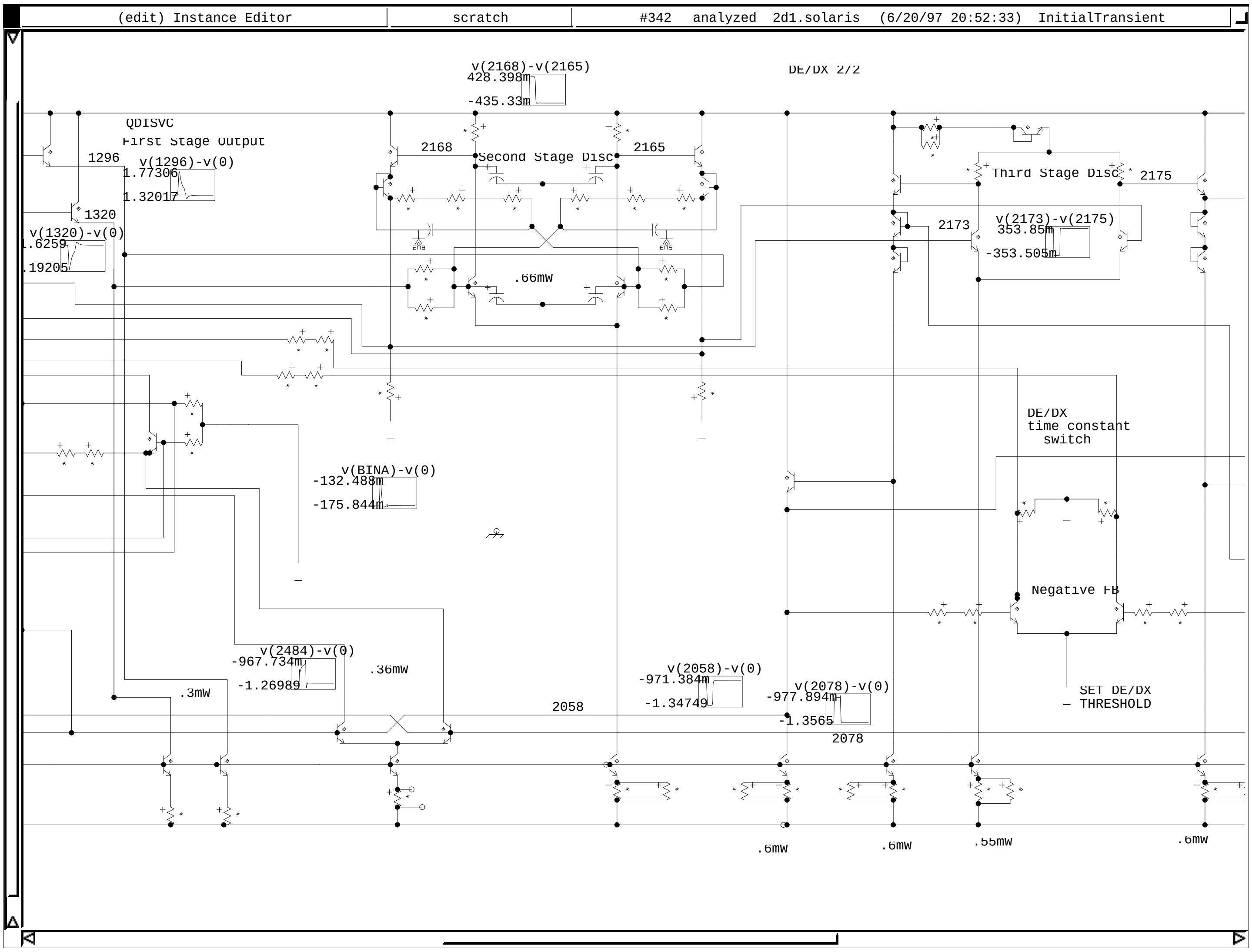

Figure 23: *Discriminator and dE/dx schematic (Part 3).*

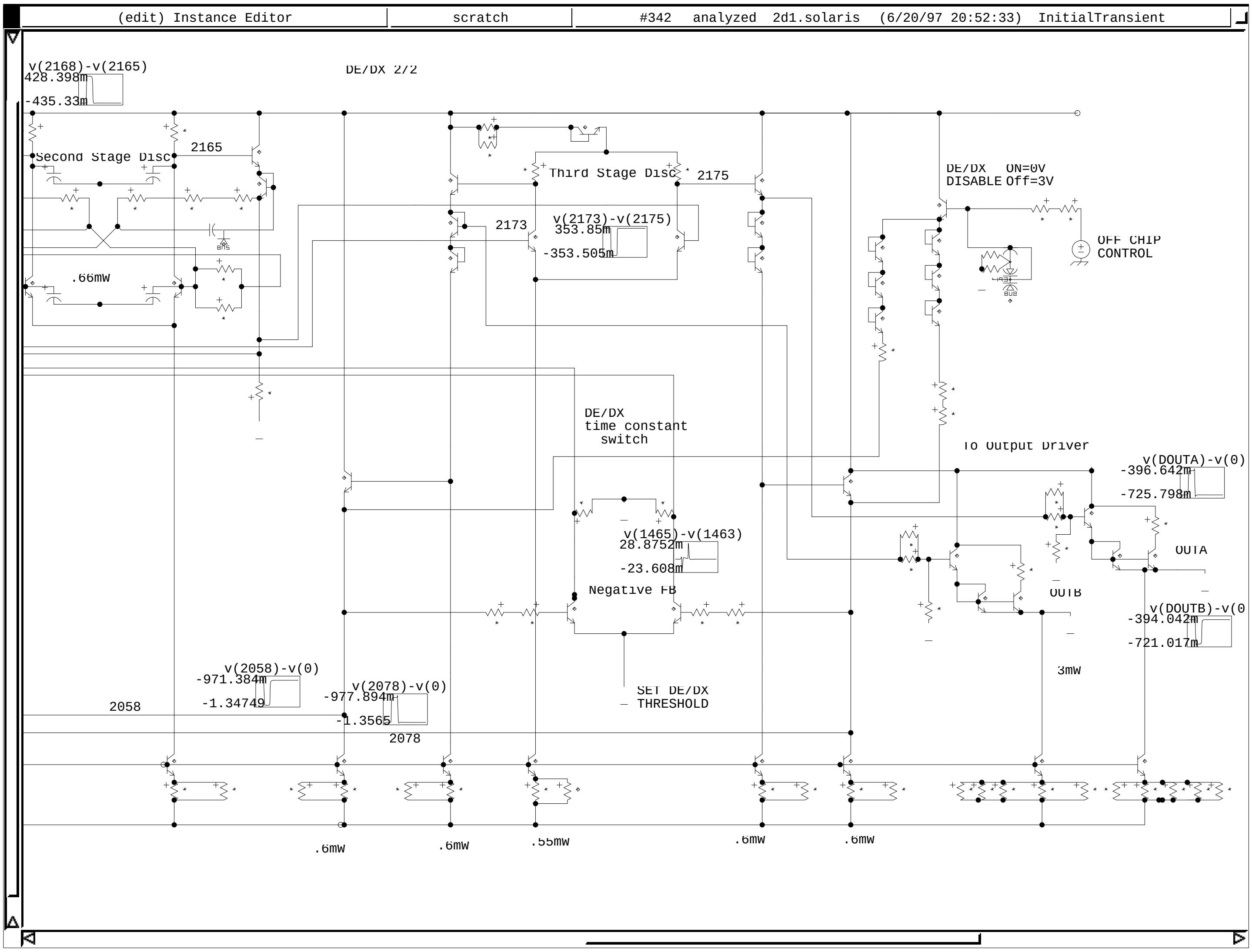

Figure 24: *Discriminator and dE/dx schematic (Part 4).*

allows a longer time constant integration to be switched in, once a signal over threshold is detected. In the present implementation, the 6 ns peaking time at the BLR output is increased to 8 ns using two additional poles in the front stage of the discriminator circuit. This provides the *fast* shaping for leading edge detection. Once triggered, a 28 ns shaping is invoked to smooth out statistical fluctuations in the arrival of the charge at the wire.

A simplified schematic of the **dE/dx** time constant switch is shown in Fig. 25. The schematic is not current and does not include the part which sets the drain current, but has been included to demonstrate the working of the dE/dx.

The differential output of the BLR is presented to the circuit at the nodes labeled SH+ and SH−. The signals Disc+ and Disc− are derived from the discriminator output and should be interpreted to be digital signals with a differential swing in excess of 250 mV. In quiescent mode the Disc− is high. This presents the current from I1 and I2 across R1 and R2 thru QCLS and QCRS lowering the voltage at the base of QLS and QRS. The current in I3 and I4 flows into QLF and QRF which are used as voltage followers. RD and C plus the emitter impedance of QLF and QRF add a short integration to the input signal shape from SH+, SH− of $\sim$ 1K×1.5 pF. This signal then steers the current in the differential pair QA and QB which operate in the linear region for signals up to about 100 mV. We expect to tune the shaping time of the overall circuit so that the signal at the bases of QA and QB has a peaking time of approximately 6 ns. The current in the collectors of QA and QB is input to the current summing node of a comparator similar to the one used in the ASD8.

When an input over threshold is detected, positive feedback in the form of charge injected into the current summing node is supplied from the transition of the discriminator outputs. Simultaneously the DC threshold is raised by several hundred mV. The current path of I1 and I2 is switched, the bases of QLF and QRF drop 300 mV and the current from I3 and I4 now flows through QLS and QRS. Since there are no resistors across the base of QLS and QRS, the signal is only attenuated by the long time constant given by (R7+R9)×2C. The result is a signal with a longer rise time, $\sim$28 ns, and an effective voltage boost of about 50% at the bases of QA and QB. The DC threshold is boosted when the discriminator triggers to about 25% the size of the peak expected from a typical input, typical signals will fall below threshold within one time constant after peaking. The value for this threshold is

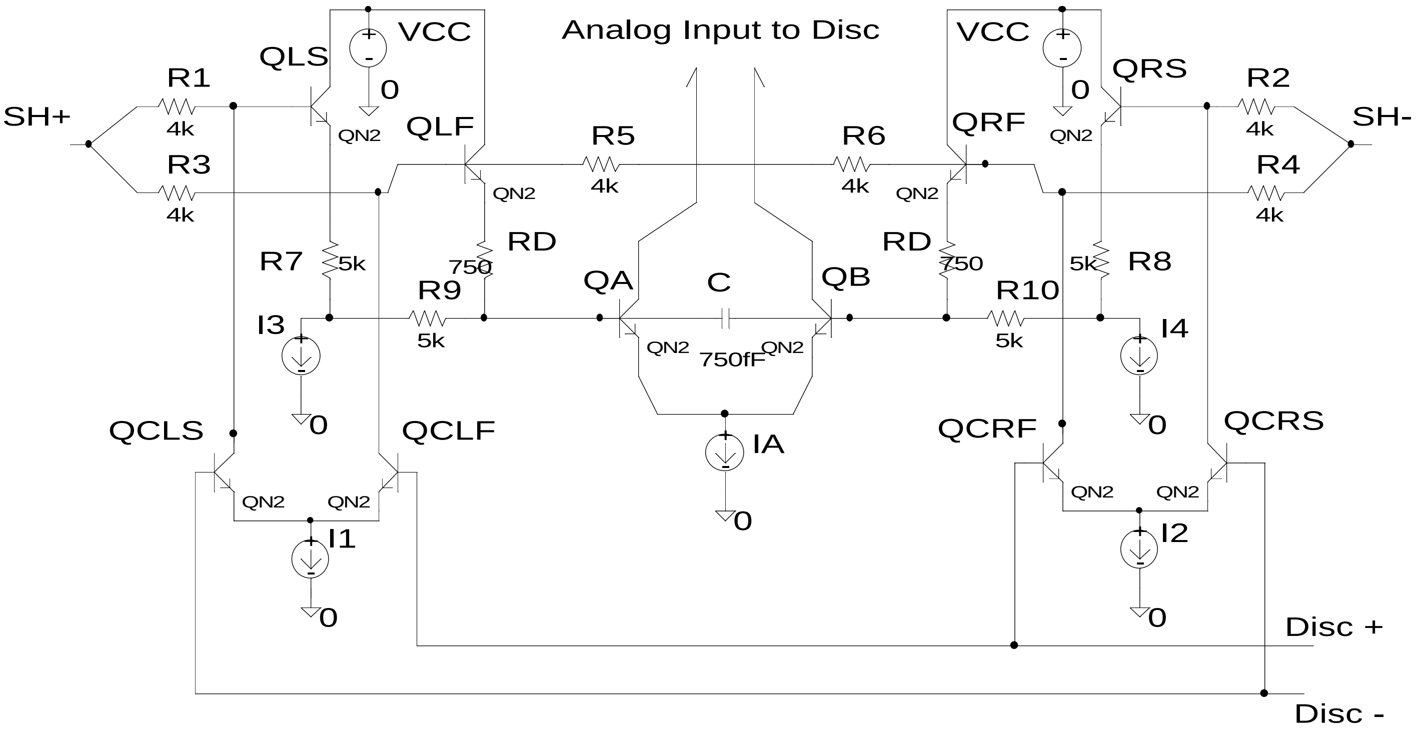

Figure 25: *dE/dx PSPICE schematic.*

programmable in the implemented design. As the signal goes below threshold, the comparator switches off, injecting charge into the current summing node, lowering the DC threshold and switching back the currents I1 and I2 across R1 and R2. The capacitor, C is quickly discharged by QLF and QRF and the circuit is ready to retrigger. Since the switching off point is determined by a fixed threshold, the recharge time should not be sensitive to the size of the input signal.

Along with a programmable *back edge* threshold, we have added programmable *drain current* (controlled by a level applied to QDR) that is switched in with the longer time constant to speed up the rate of discharge of the dE/dx capacitors. The qualitative effect of the back edge threshold and drain current controls is shown in figures 26 and 27 respectively.

Fig. 28 (not current values, but descriptive) shows input (lower trace) and signal at the bases of QA, QB (upper trace) for a signal below threshold followed 40 ns later by a signal over threshold. The shape of the signal at the bases of QA and QB is the same as for the input, attenuated by 1/2, for the input pulse below threshold, but is quite different for the over threshold pulse where the longer time constant shaping is evident. Three settings of the programmable trailing edge threshold adjustment are shown.

The specifications of the discriminator and the dE/dx circuit are summarized in table 7.

5.8 Output Driver

Both discriminator outputs have emitter follower buffers that are directly coupled to the output driver differential pairs. The switching currents for each pair and a constant current for each output node can be programmed at the chip level by adjusting the current source reference voltages. This allows the ASDQ to be compatible with a variety of cable and receiver configurations.

5.9 Calibration Circuit

The calibration circuit is shown in Fig. 29. Provision has been made for two calibration reference lines to be brought onto the ASDQ daughter-boards through the low voltage power distribution bus (±3V) that runs along the detector. These two reference voltages allow separate control of odd and even

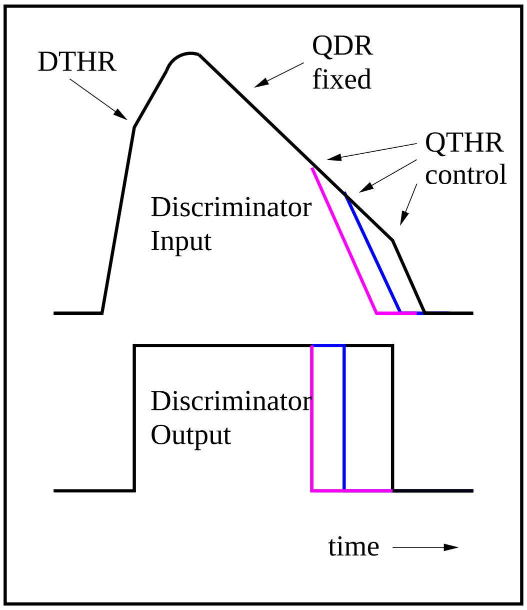

Figure 26: *The effect of the back edge threshold control.*

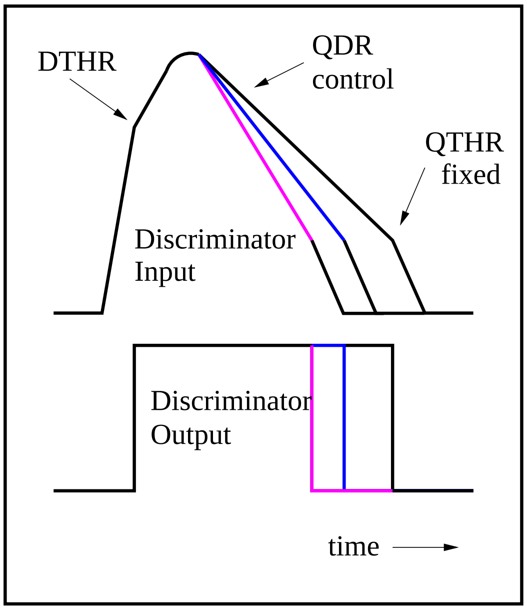

Figure 27: *The effect of the drain current control.*

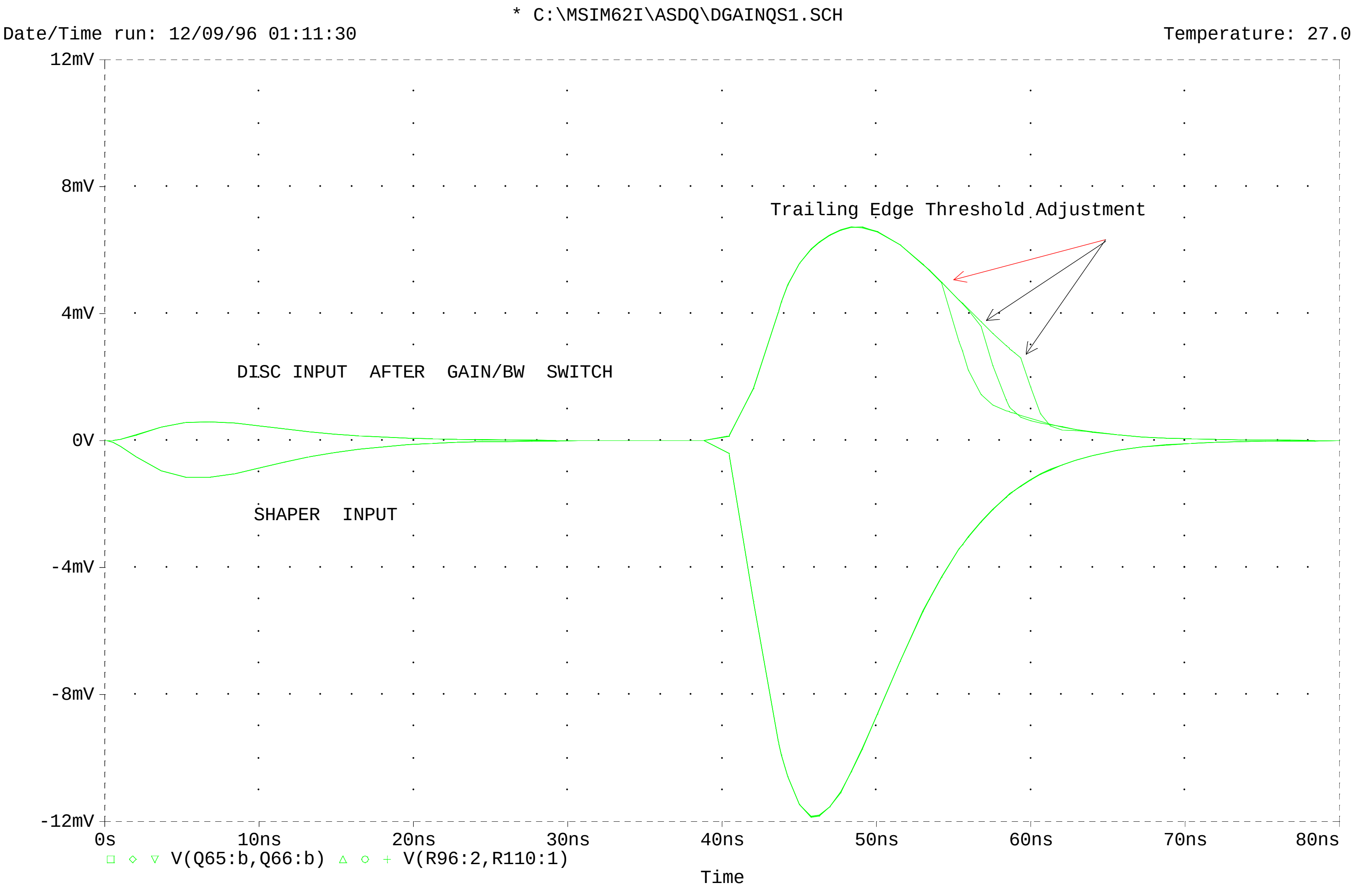

Figure 28: *dE/dx signal at QA and QB.*

dE/dx Specs	
Shaping	Peaking time 28 ns
Pedestal	5 ns
Encoding	$\Delta t \propto \log(Q)$
Saturation	120 fC
Mean pulse width	10-15ns beyond width of shaped pulse (40-50ns)
Discriminator Specs	
Power dissipation	7 mW
Time slewing	<1 ns/decade of overdrive
Minimum width	5 ns
Internal offset	≤1mV (0.05fC)
Threshold range	10fC
Threshold uniformity	Δ(thresh)/thresh < 10% (chip-to-chip)
Output	Bi-level

Table 7: Discriminator and dE/dx Specifications

channels. These lines provide a voltage reference to adjust the magnitude of the calibration pulse signal. The calibration timing pulse originates in the TDC crate and is sent to the daughter board on the same cables as the ASDQ outputs.

Two calibration blocks are included on the ASDQ ASIC to allow independent control of simultaneous signal injection to all 'odd' or all 'even' channels. The circuit is shown in Fig. 29. The reference input, "TREF" is a voltage between 0 V (max) and -3 V (off) which sets the current in the differential pair used as the calibration pulse receiver. A passive network between the inputs and the bases of the differential pair provides compensation for the non-ideal rise time of the signal received from the TDC crate. The insets near IN- and IN+ show the anticipated signal shape. The ASDQ daughter board will require a pair of coupling capacitors and a resistive biasing network to receive the calibration pulse, which will then be bussed to each ASDQ chip on the card. The pulse width may be fixed or variable between 5 and 15 ns.

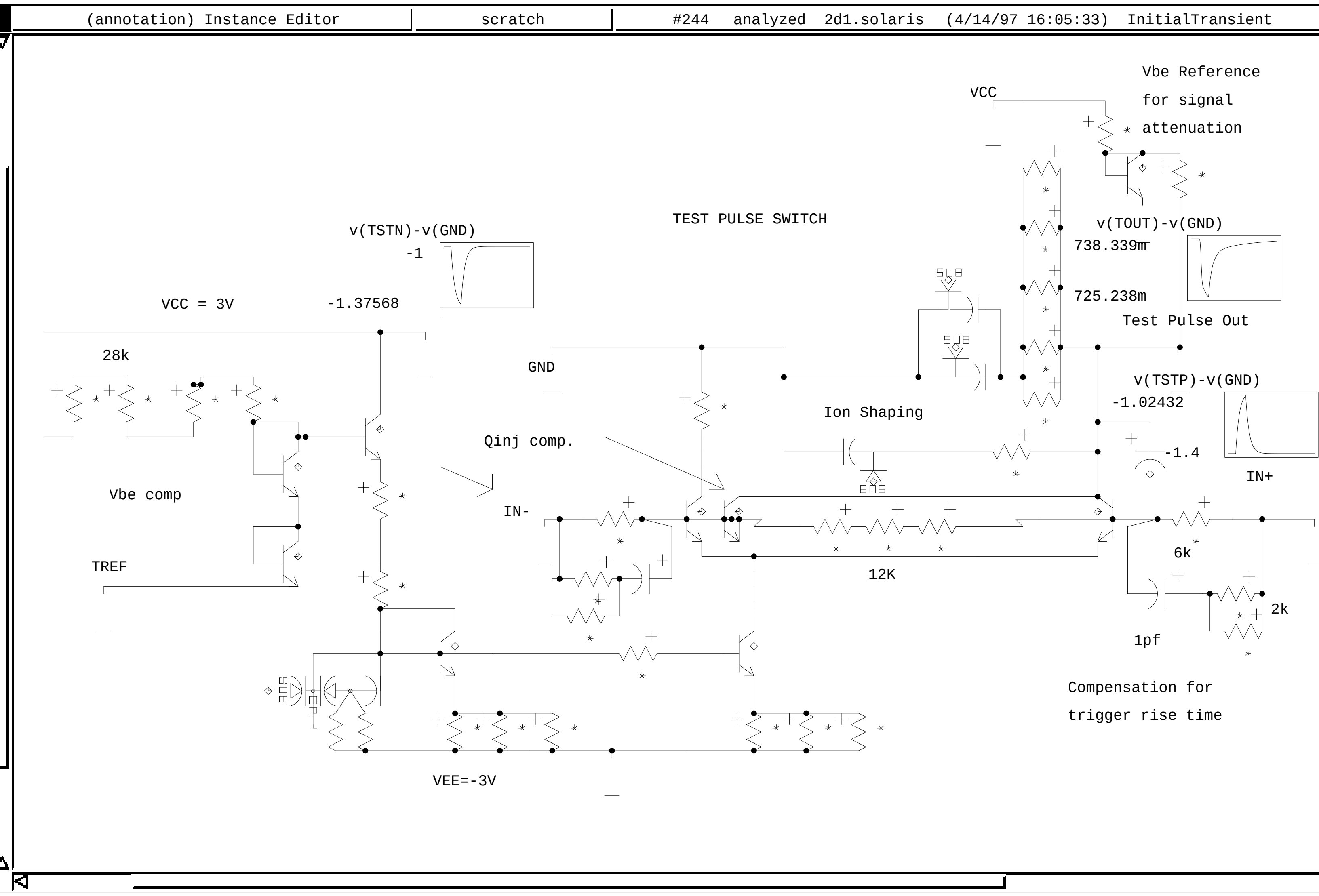

Figure 29: *The calibration circuit schematic.*

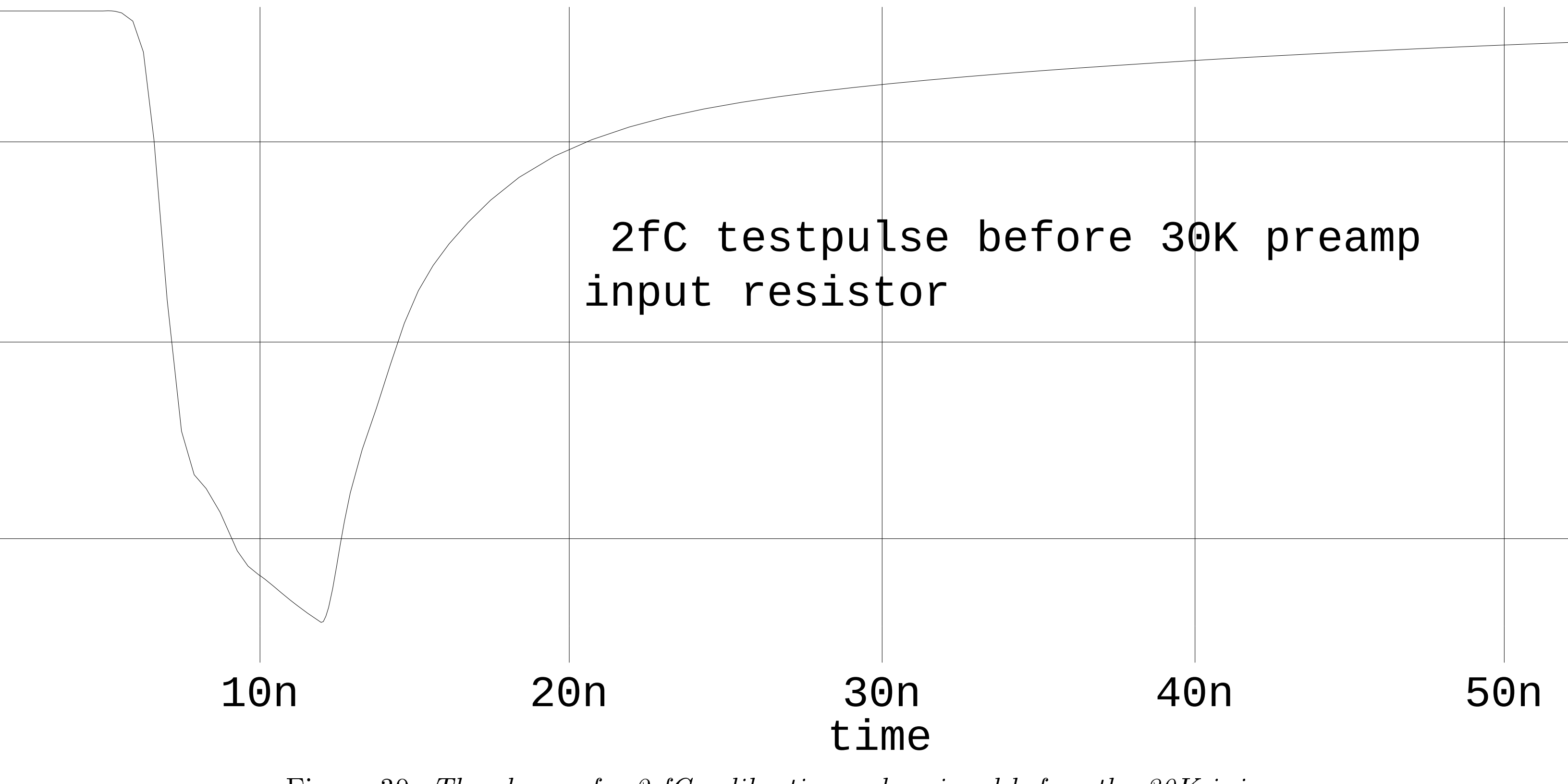

Figure 30: *The shape of a 2 fC calibration pulse signal before the 30K injection resistor.*

In quiescent mode the differential pair is switched to pass the current set by "TREF" to GND through a small resistor. A calibration pulse shifts this current into a pulse shaping network that adds a tail similar to the "ION" tail characteristic of a real chamber pulse; see the inset in the upper right side of Fig. 29 to see the final injected pulse shape. This signal is then bussed to four channels connecting to the input of each with individual 30K resistors. A fixed, 7 ns wide, calibration pulse can provide an input signal of up to 30 fC by adjustment of 'TREF'. The shape of a 2 fC calibration pulse signal before the 30K injection resistor is shown in figure 30.

By including the calibration pulse network on the ASDQ ASIC, we take advantage of the high ft SHpi process transistors. The switching time for the differential pair is less than 1 ns when the current is set for a near threshold signal; we therefore expect the channel-to-channel and chip-to-chip time variation to be much less than 1 ns. When not in use, each calibration block uses less than 0.5 mW of power.

Finally, the specifications of the calibration circuit are summarized in table 8.

Calibration	
Test Pulse Minimum input width	Transition board Input 5ns
Input amplitude	Differential ECL
Test Pulse Minimum input width	ASDQ input 5 ns
Minimum input amplitude	250 mV differential
Test Pulse Reference	0V (max out), -3V (zero out)
Output Type	Differential, switched constant-current
Output Range	< 30fC

Table 8: Calibration circuit Specifications

5.10 Power

The power consumption for each channel is as follows: The preamp, shaper and BLR consume 14 mW per channel, the dE/dx and discriminator consume

17 mW per channel, the output driver consumes 9 mW per channel and each chip has a drive-current control circuit that consumes 5 mW per chip. This translates into a total power consumption of about 40 mW per channel. The total chip consumption is about 0.33 W.

5.11 Pin and Pad List

The Pin/Pad list of the ASDQ is summarized in table 9. There are a total of 64 pins in a TQFP package. There are 7 extra pads to allow for bonding flexibility. The table shows the names of the individual inputs and output of the ASDQ, the number of pads assigned to them, their nominal operating voltages, and their ranges of operation. A brief description is also given of each of the pins.

6 Simulations of the ASDQ performance

In order to demonstrate some of the properties of the COT signals and the ASDQ, fast simulations have been performed. The goal of the simulations is to realistically model the COT signal by taking into account the following effects:

- Velocity dependent dE/dx
- Track position and angle in a COT cell
- The number of clusters and the size of the individual clusters
- The arrival times of the clusters
- The effect of Gas Gain
- The effect of gain in the electronics and the discriminator threshold
- The effect of shaping in the electronics for both dE/dx enabled and disabled
- The effect of gas composition and wire voltages

Name	Number	Extra	Nominal	Low	High	Description
AGND	4		0V			Preamp & Calib Chamber Ref
SUBA	2	2	-3V			Substrate Analog Ref
VPP	2		1.2V			Inp. Prot, Rail Preamp & Calib Power
VCP	1	1	+3V			Preamp & Calib Supply
VCS	2		+3V			Shaper & BLR
VES	1	1	-3V			Shaper & BLR
VCD	2		+3V			Discriminator, dE/dx & Driver
VED	2		-3V			Discriminator & dE/dx
SUBD	1	1	-3V			Chip-wide Digital Substrate (SUBA off-chip)
VEDR	2		-3V			Driver Supply
DGND	1	1	0V			Discriminator & dE/dx Gnd
VCATCH	1	1	0V			Output driver catch (1 diode drop below gnd)
TSTN	1		-0.25V	-0.8V	-0.2V	Neg going calib pulse edge
TSTP	1		-0.5V	-0.6V	-0.4V	Pos going calib pulse edge
TREFE	1			-3V	+3V	Calib ref for even channels (–3V=off)
TREFO	1			-3V	+3V	Calib ref for odd channels (–3V=off)
ATTN	1		0V	0V	+3V	Attenuate input by 2× (0V = no atten)
DTHR	1		0.08V	0V	+1V	Tracking Disc Threshold
QTHR	1		1V	-3V	+3V	Trailing edge tracking control
IBLR	1		2V	-3V	+3V	BLR current reference
QDR	1		2V	-3V	+3V	dE/dx cap drain ref (–3V = off)
QEN	1			0V	+3V	dE/dx enable (3V = dE/dx OFF)
ID	1		+3V			Output Current Ref
InA	8					Negative going channel input
InB	8					Positive going channel input
DnA	8					Channel driver output (Trigger on rising edge)
DnB	8					Channel driver output (Trigger on falling edge)
TOTAL	64	7				Extra pads for bonding flexibility

Table 9: ASDQ Pin/Pad list.

The larger goal of this effort is to provide code for CDF Run II simulation which will allow the users to select the ASDQ parameters that optimize the dE/dx and double pulse resolution requirements.

It should however be kept in mind that these simulations only demonstrate general features which are only as reliable as the assumptions made for them. They are not intended to provide a rigorous quantitative guideline. Rigorous statements can only be made in the presence of experimental data from an instrumented and operational COT.

6.1 The Simulation Algorithm

The single wire simulation algorithm proceeds in the following steps:

1. Select the number of produced clusters (n_{cl}) from the appropriate Poisson distribution. This number depends on the gas composition, the geometry of the configuration and the velocity of the ionizing particle.

2. Position the n_{cl} clusters on the track within the acceptance region of the sense wire.

3. Look up the total drift time to the sense wire for each cluster.

4. Select the number of electrons in each cluster from the cluster size distribution.

5. Simulate the gas gain for each cluster, including the effect of statistical fluctuations.

6. Form an input signal for the ASDQ.

7. Simulate the response of the ASDQ to obtain the ASDQ output pulse start times and widths.

The cluster size distribution is taken from experimental data, and is shown in Fig. 3. As discussed in section 4, it is known from experimental data that there are ~ 28 clusters per cm in Ar. The average size of these clusters is 3 electrons.

The effect of the velocity of the particle is considered by using the Bethe-Bloch equation to determine the velocity dependent correction factors for the

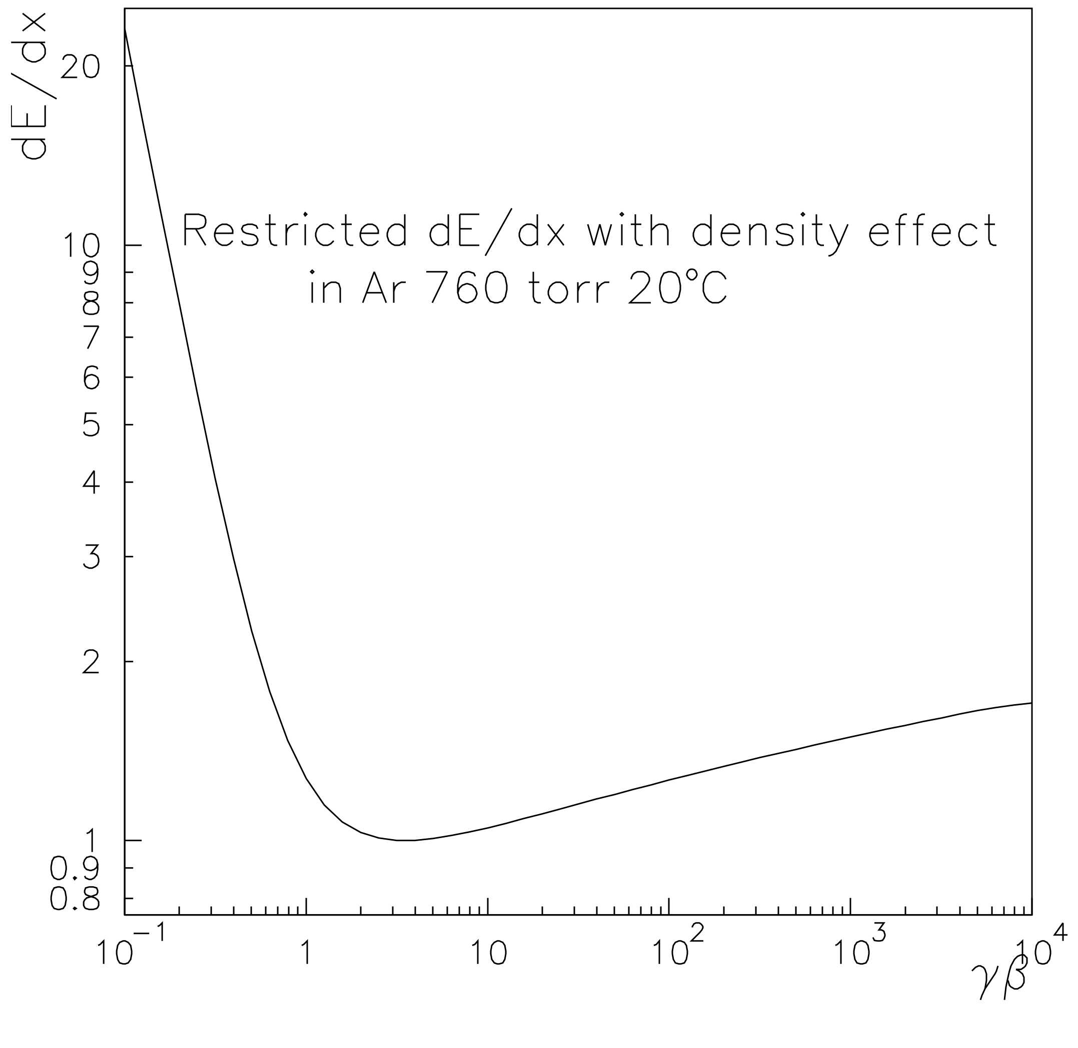

Figure 31: *dE/dx relative to minimum ionizing particles for pions in Ar. Restricted energy loss ($T_{max} = 1.0$ MeV) includes the effect of density.*

ionization. This depends on the gas composition, temperature and pressure. In the algorithms, electrons are treated separately from all the other tracks that use the same curve. Fig. 31 shows the dE/dx relative to minimum ionizing particles for pions in Ar. The dE/dx has been calculated using the GEANT routine GDRELX. The effect of density is included.

As mentioned in section 4, the typical distance traveled by a minimum ionizing particle in the gas is 3 mm. In order to determine the total number of electrons (N_i) that drift to the sense wire (in the absence of Gas Gain), the mean number of clusters produced per cm (28/cm) is Poisson fluctuated and then combined with the individual cluster sizes. The resulting distribution is shown in Fig. 4. On average about 20 electrons drift to the sense wire. For an operational threshold of 5 (10) electrons, approx. 95% (80%) of the ionization signal is accepted. The Fig. also shows the distribution for a 5 mm path of a minimum ionizing particle. In that case the average number is about 30.

The statistical fluctuation in the gas gain, the number of electrons (n) produced in an avalanche by one electron, is given by the Polya distribution, where the parameter b depends on the details of the gas used. The mean number of produced electrons is $\overline{n}$.

$$P(n) = \frac{1}{b\overline{n}\Gamma(\frac{1}{b})}\left(\frac{n}{b\overline{n}}\right)^{\frac{1}{b}-1} e^{-\frac{n}{b\overline{n}}}$$

For the COT, b is taken to be 0.4. Fig. 32 shows the statistical fluctuation in gas gain for single incident electron (top) and 10 incident electrons (bottom) for gas with $b = 0.4$. The 10 electron response is the convolution of 10 one electron response distributions. Whereas in the single electron case, the gas gain fluctuations can be substantial, in the case of 10 electrons the fluctuations are relatively small.

A realistic track produces many primary ionizations and the arrival times of the ionization electrons are staggered in time. The signal seen in the chamber is thus the sum of the individual signals. Using previous experience with drift chambers, and with tests done using Cosmic ray and Fe^{55} sources, the effect of geometry can be taken into account to simulate the expected signal from a track.

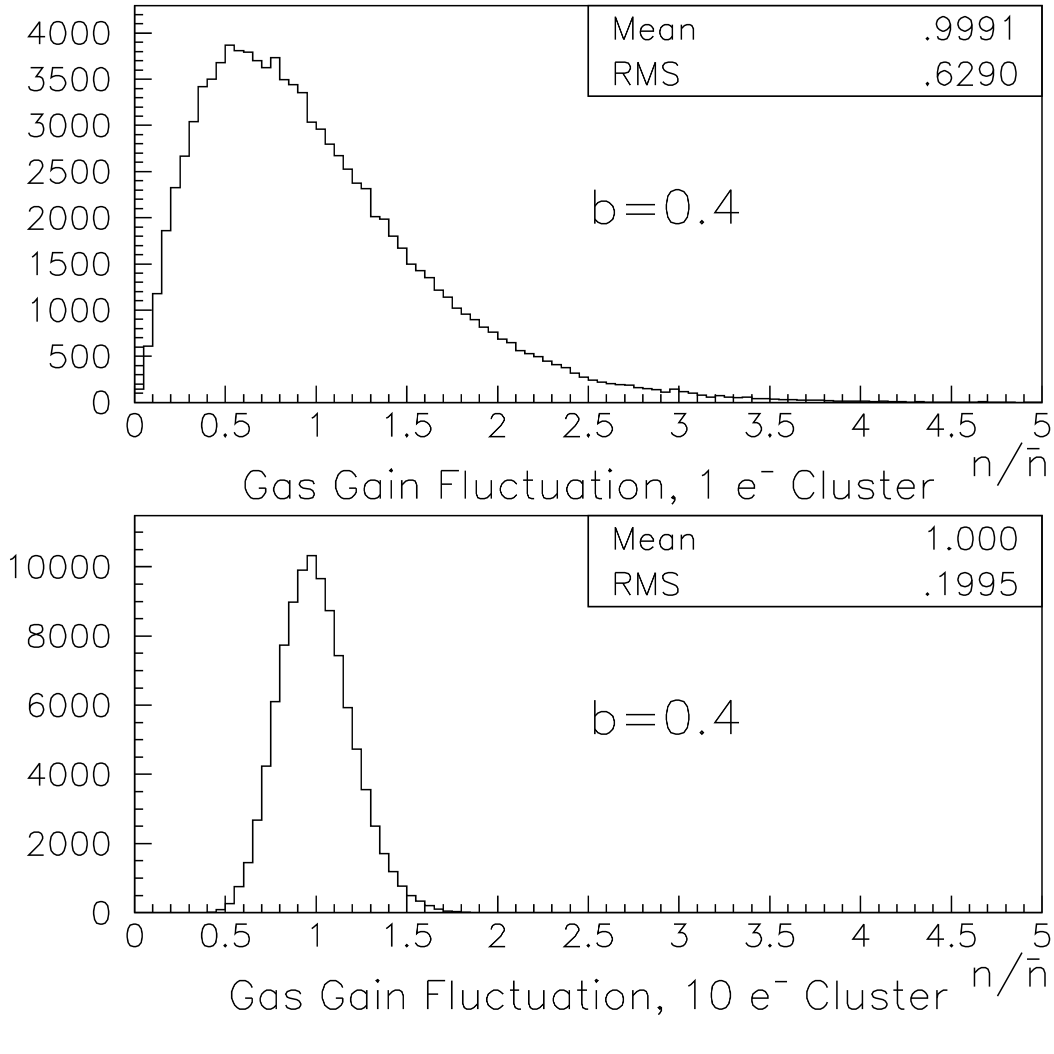

Figure 32: *Statistical fluctuation in gas gain for single incident electron (top) and 10 incident electrons (bottom) for gas with* $b = 0.4$. *The 10 electron response is the convolution of 10 one electron response distributions.*

6.2 Track signal simulation using GARFIELD

The time characteristics of the signal are modeled using GARFIELD[5]. Using the specifications of a COT cell and the active gas, a track is simulated. The effect of a full avalanche is then modeled -the electrons are drifted towards and the ions are drifted away from the sense wire respectively. Fig. 33 shows the COT cell simulated by GARFIELD, along with the alternating potential and sense wires. The electron drift lines are also shown. Fig. 34 shows the ion drift lines for the same cell. The induced signal in the sense wires is shown in Fig. 35. As mentioned earlier, the total signal is the sum of all the individual signals. The directly induced signal in the sense wire, also induces a mirror signal in the neighboring sense wires that is smaller in magnitude and opposite in sign. Figure 36 shows the effect of the cross-induced charge.

6.3 Drift times

The drift lines and drift times are calculated by GARFIELD for specified gas composition and parameters, wire potentials and the magnetic field. Fig. 37 shows the drift lines and the equal time contours for a simulated COT cell. The time contours are at 10 ns intervals, and the location of a "typical" track is also shown. The simulation takes the drift times reported by GARFIELD and interpolates between them. Fig. 38 shows the cluster drift time as a function of the cluster position on the track. The typical drift times to the sense wire are 70 to 100 ns. It is also seen that there are regions close to the sense wire where the drift times can be substantially longer. These long drift times correspond to the long drift trajectories that can be seen at the top and the bottom of the sense wire.

The same information is also contained in Fig. 39 which shows the drift time distribution for electron clusters distributed along a segment of the "typical" track. The top plot shows that the charge arrival time has a long tail associated to it, that continues for up to 60 ns for this track configuration. The same plot is also shown on a logarithmic scale (bottom), where it is seen that the drift time of few clusters can be substantially longer.

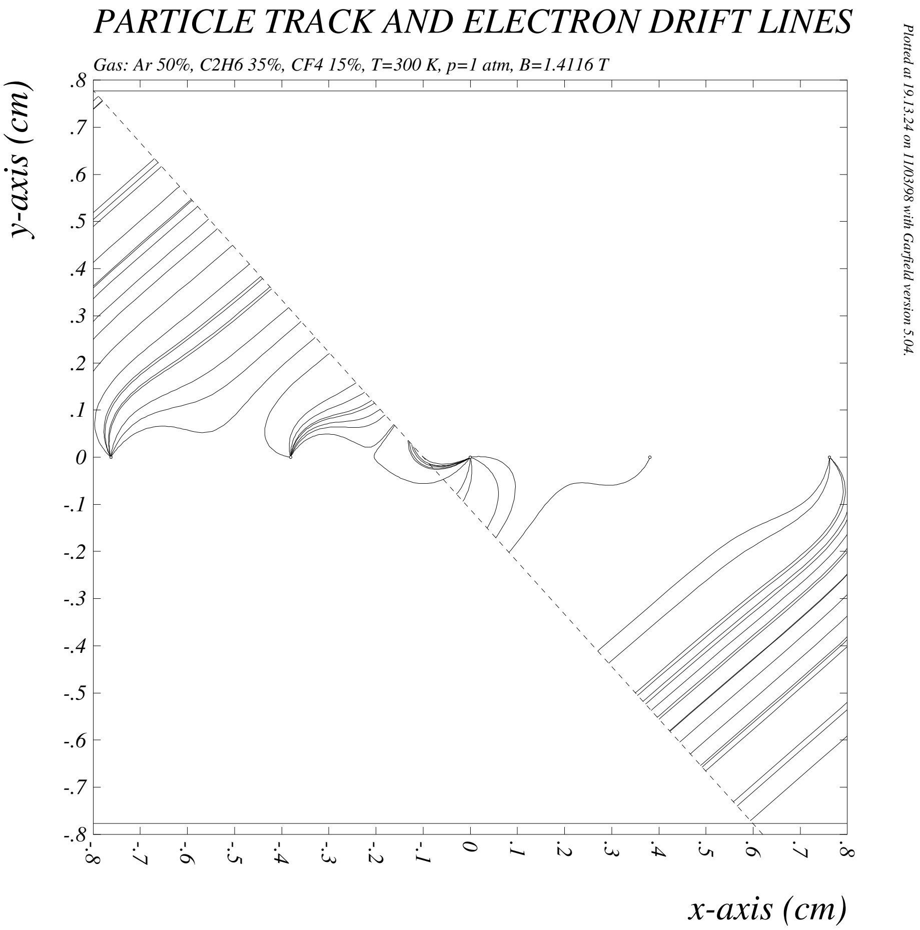

Figure 33: *GARFIELD simulation of a track and the electron drift lines in a COT cell.*

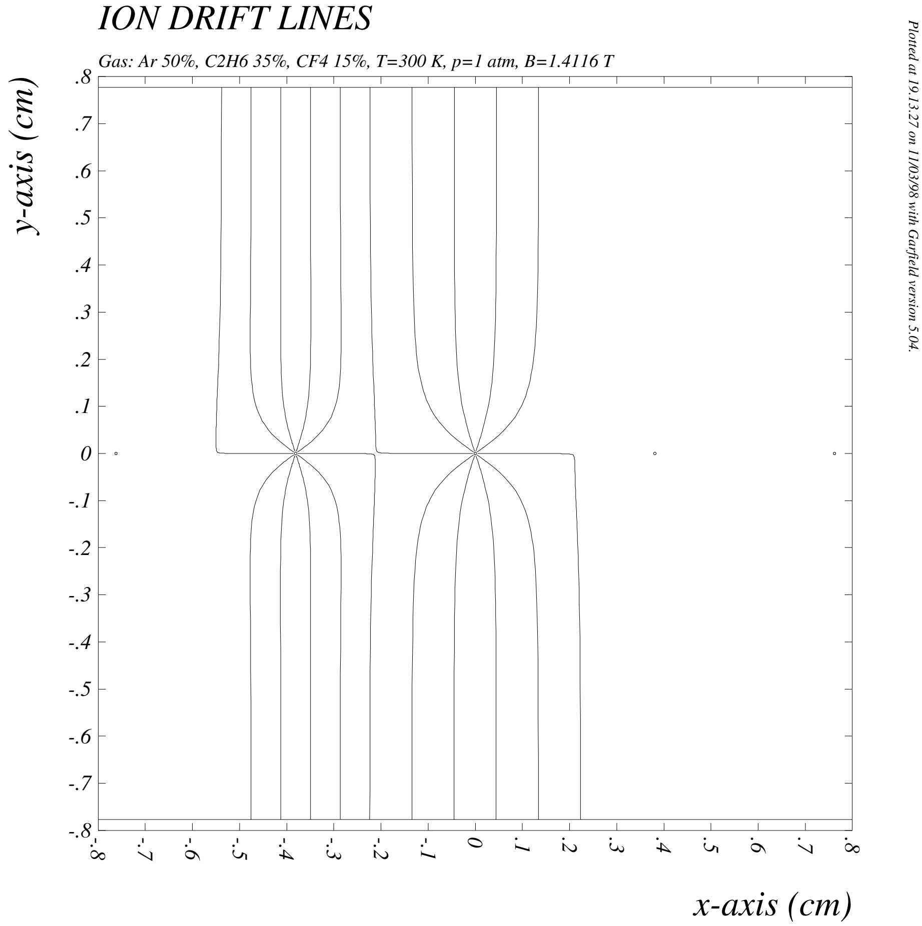

Figure 34: *GARFIELD simulation of ion drift lines in a COT cell.*

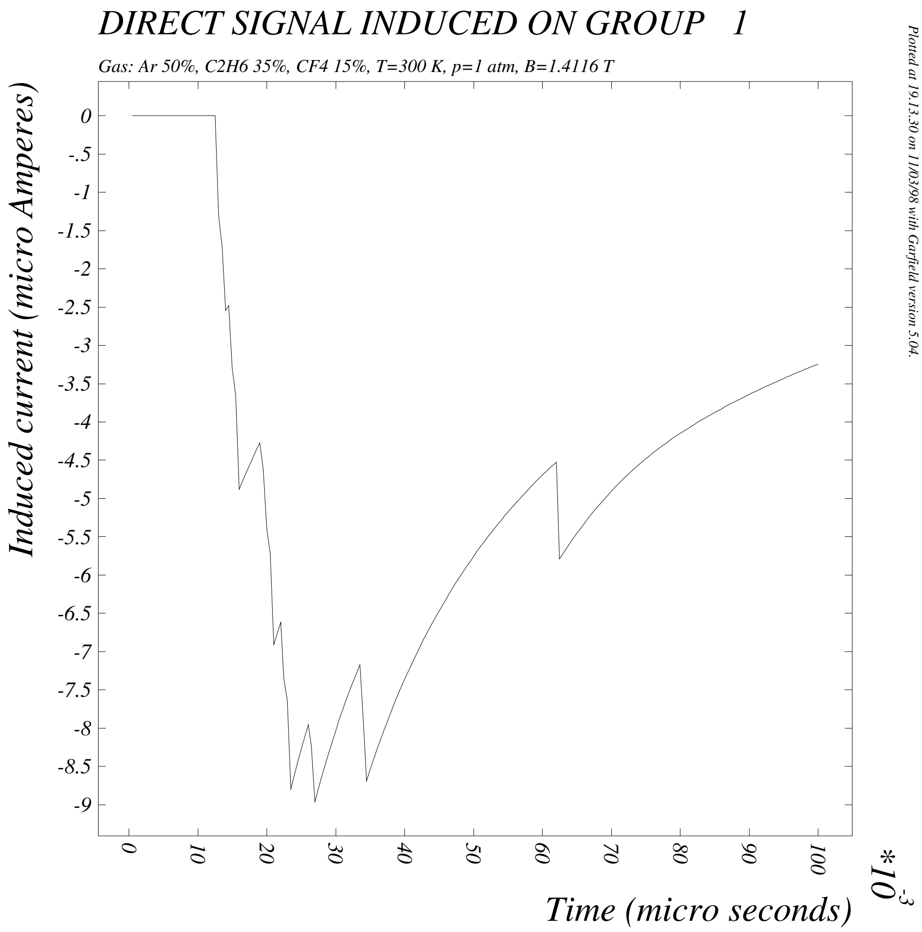

Figure 35: *The induced signal in a COT wire.*

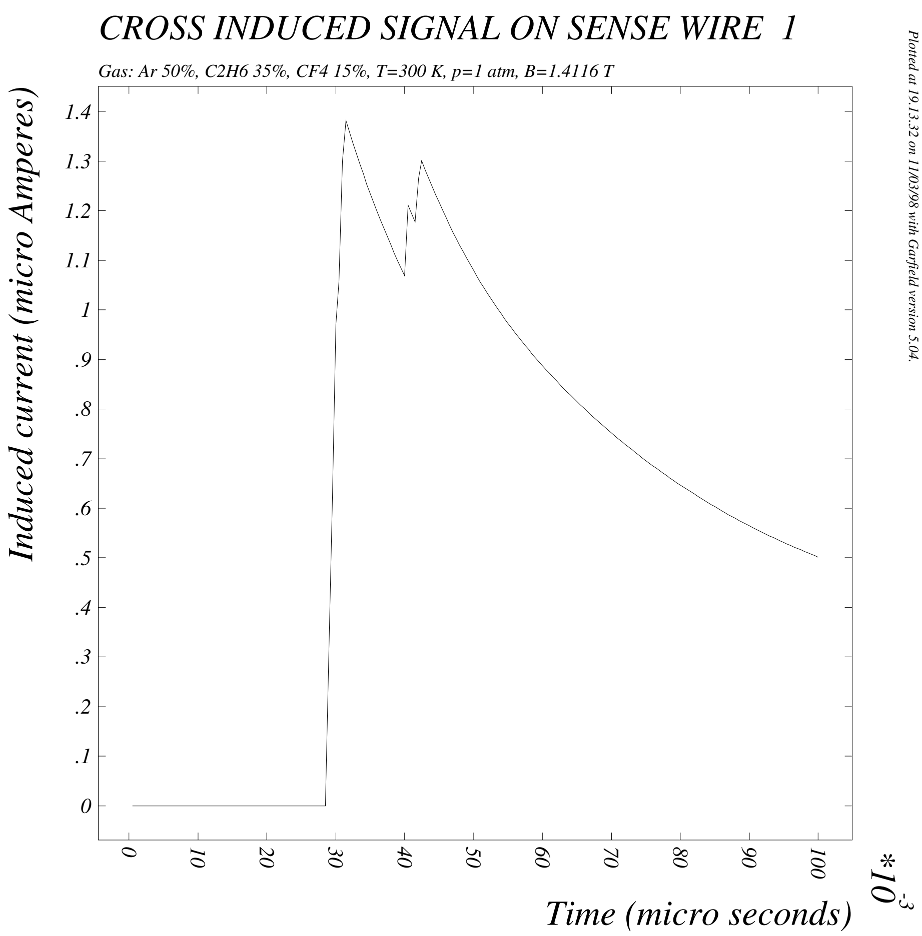

Figure 36: *The cross induced signal in a COT wire.*

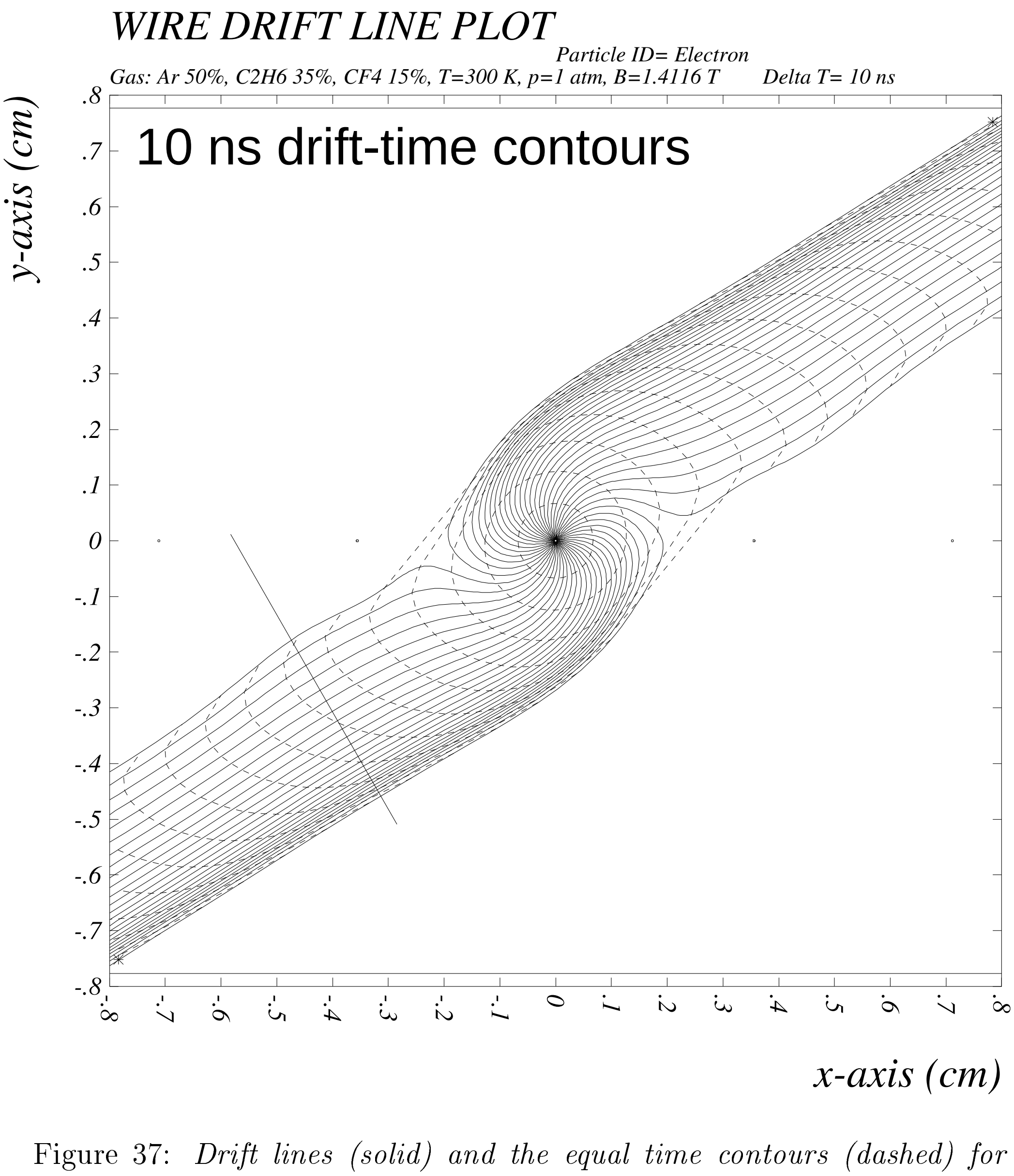

Figure 37: *Drift lines (solid) and the equal time contours (dashed) for a GARFIELD simulated COT cell. The time contours are at 10 ns intervals. The location of a "typical" track is also shown.*

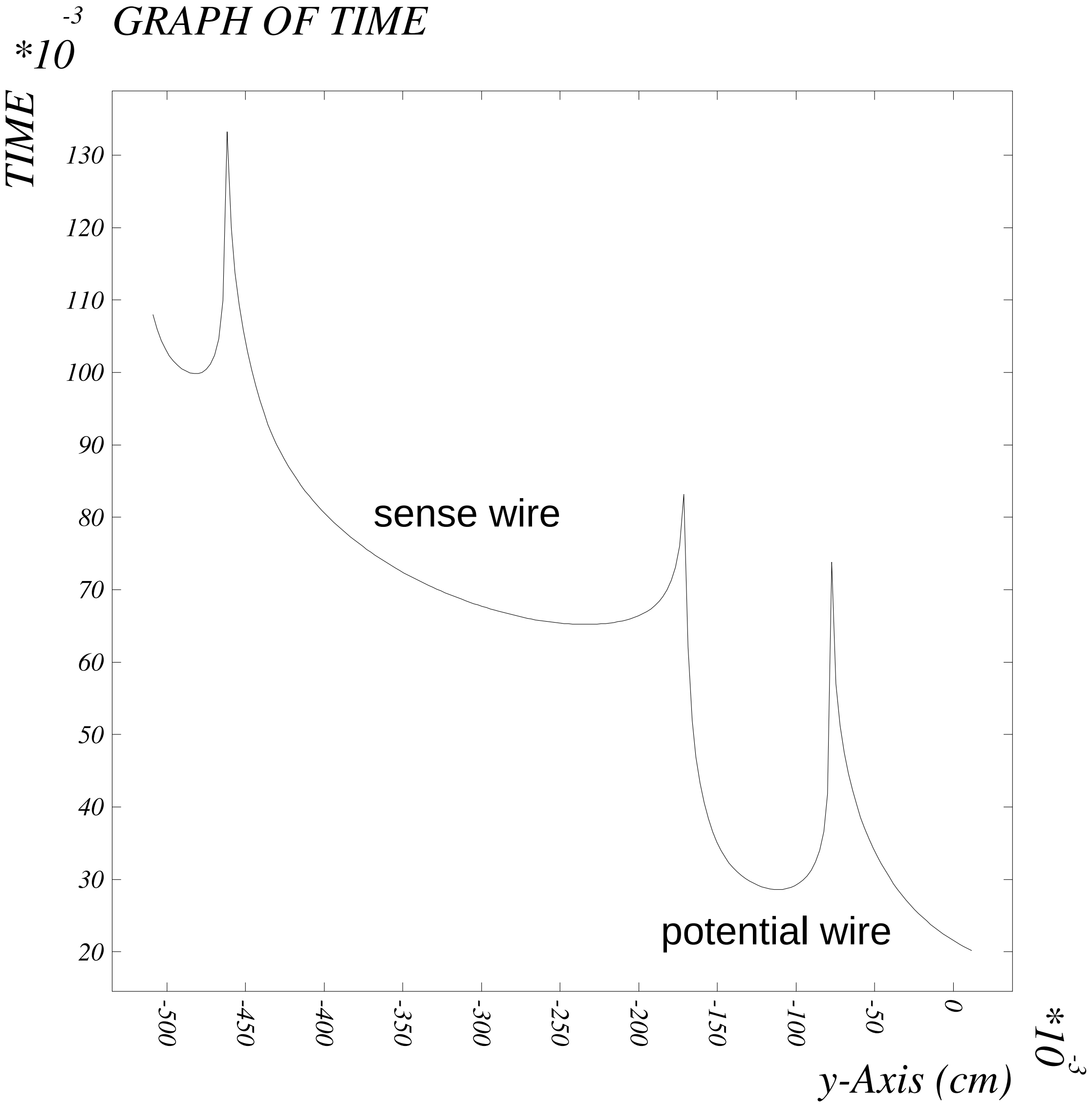

Figure 38: *Drift times (in ns) for electron clusters distributed along a segment of a "typical" COT track.*

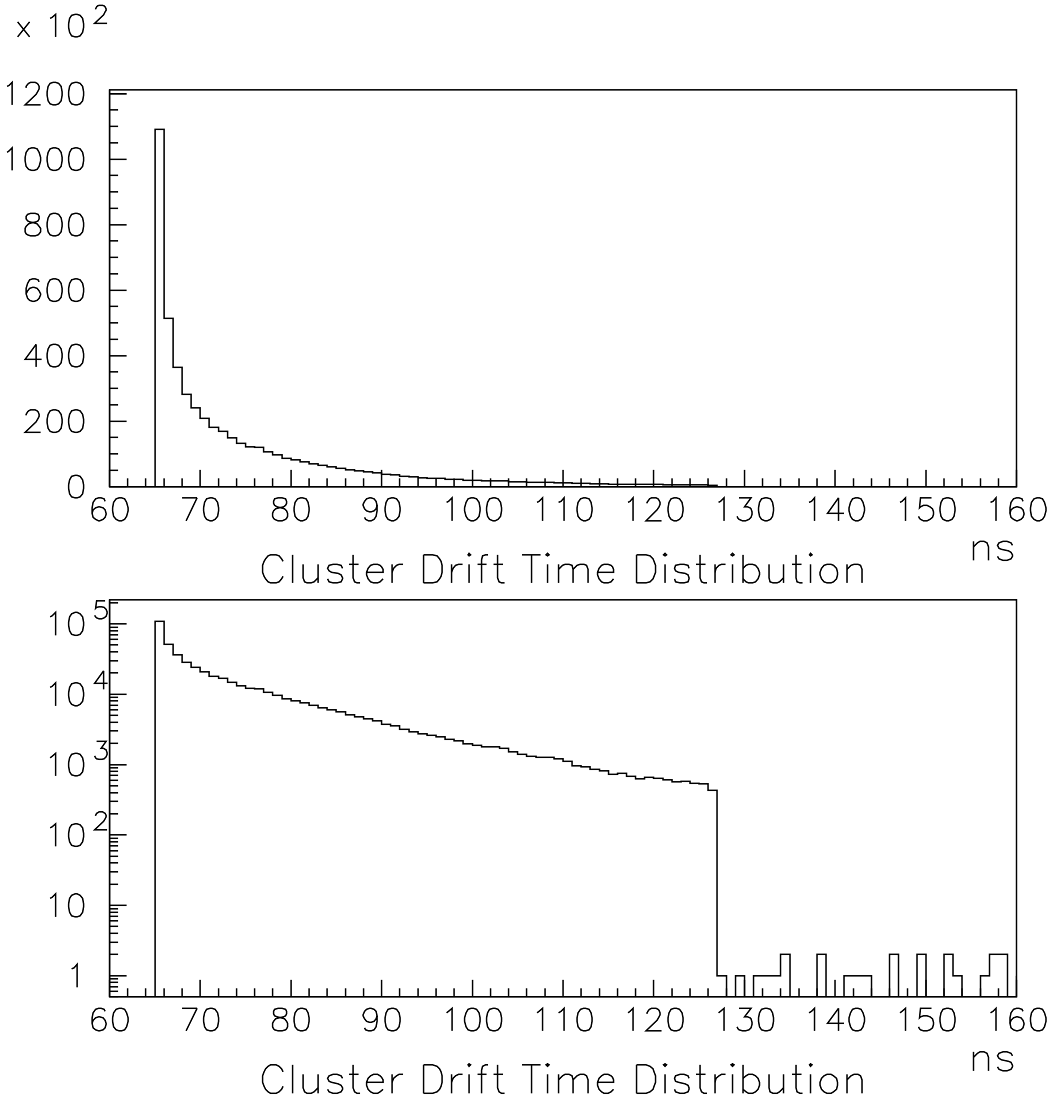

Figure 39: *Drift time distribution for electron clusters distributed along a segment of a "typical" COT track.*

6.4 Simulation of the ASDQ response

In order to model the response of the ASDQ, only the electron component of the signal is considered. It is assumed that the tail cancellation networks completely eliminate the tails in the signal. The electron component is therefore modeled as impulse signals that are staggered in time.

The simulation of the ASDQ response is broken down into three components:

- Response of the shaping stage:

  The impulse response for an ideal multipole shaper is given by:

  $$V(t) = \left(\frac{t}{nt_i}\right)^n e^{n-t/t_i}$$

  Here t_i are the time constants for the integrations in each of the shaping stages and n refers to the number of shaping stages when all other uncanceled poles have been set to significantly higher frequency. The response is normalized to unity at its peak when $t = nt_i$ (the measurement time).

- Non-linear response of the BLR

  The BLR response is modeled by four coupled ODE's that model the response of the components within the BLR. The ODE's are solved using the Runge-Kutta method.

- Response of the dE/dx

  The impulse response of the dE/dx, in terms of the dE/dx time constant, τ_D, is given by:

  $$V(t) = \frac{1}{\tau_D} e^{-\frac{t}{\tau_D}}$$

  The threshold is modeled simply by looking for a signal that exceeds a given value.

The simulation assumes that the discriminator threshold is set to $DTHR =$ 15 mV, the shaping time to 8 ns and the dE/dx integration time to 20 ns.

Fig. 40 shows the simulation of the arrival of the electron charge on the sense wire and the simulated signals at three different stages within the ASDQ. The earliest arriving charge is at time $t = 0$ ns. This Fig. also illustrates the effect of the presence of late arriving charge, which is primarily to extend the tail of the signal going into the BLR. The effect of the BLR is also seen, where the tail in the signal is quickly brought back to zero.

In order to study the effect of drift times, the “typical” track shown in Fig. 37, is generated 200K times and the pulse start time from the discrimination of the leading edge is noted. Fig. 41 shows the start-time (t_{start}) distribution for the clusters from this track for different number of clusters, $n_{cl} \leq 5$ and $n_{cl} \geq 16$. The top plot shows the effect of cluster drift time straggling when the number of clusters is small. When the number of clusters is larger, they arrive less staggered in time. It is also seen that with a larger number of clusters, the discriminator tends to trigger earlier -the effect of discriminator walk. This is clear in the bottom plot which shows the t_{start} for different charges, again the effect of the discriminator walk is clearly seen.

The total charge versus pulse width relation is shown in figure 42. The Fig. also shows the charge versus width relation for the same track. The effect of the charge on the output width (for the particular settings of the control voltages) is clearly seen.

In order to study the resolution of charge measurement, the charge versus output width distribution is fit to a cubic polynomial. Defining $\Delta q = (q - q_{meas})$, where q_meas is the “measured” charge from the fit, and q is the actual charge, the resolution is given by $\Delta q/q$.

Fig. 43 shows the charge versus output width and the resolution distribution. The top plot is the contour plot (the contours are logarithmic) of the distribution shown in Fig. 42, with the cubic fit overlaid. The bottom Fig. shows the fit of the $\Delta q/q$ distribution to a Gaussian and a linear background in the vicinity of the peak. The $\Delta q/q$ distribution is asymmetric but has a core with $\sigma \approx 10\%$ that is approximately Gaussian.

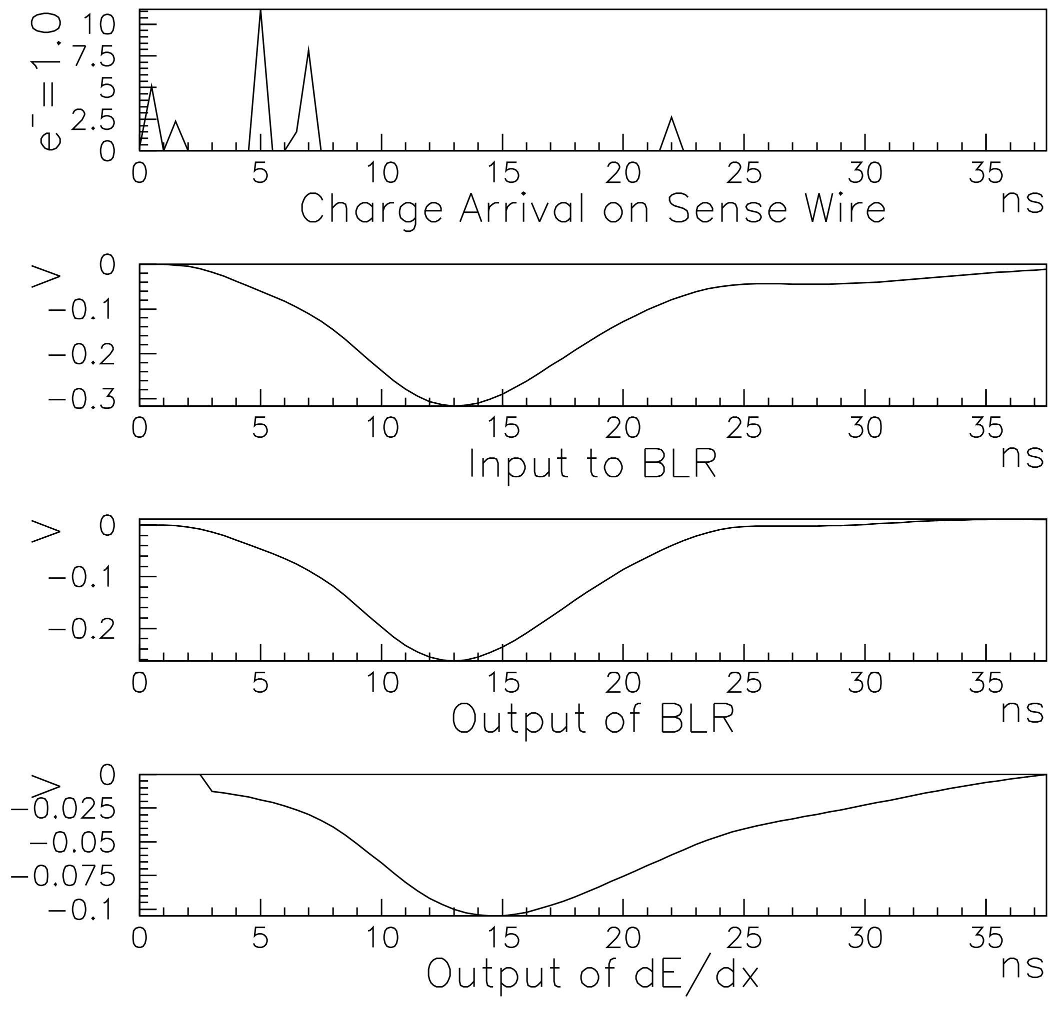

Figure 40: *Charge arrival at the sense wire and simulated waveforms at three stages in the ASDQ.*

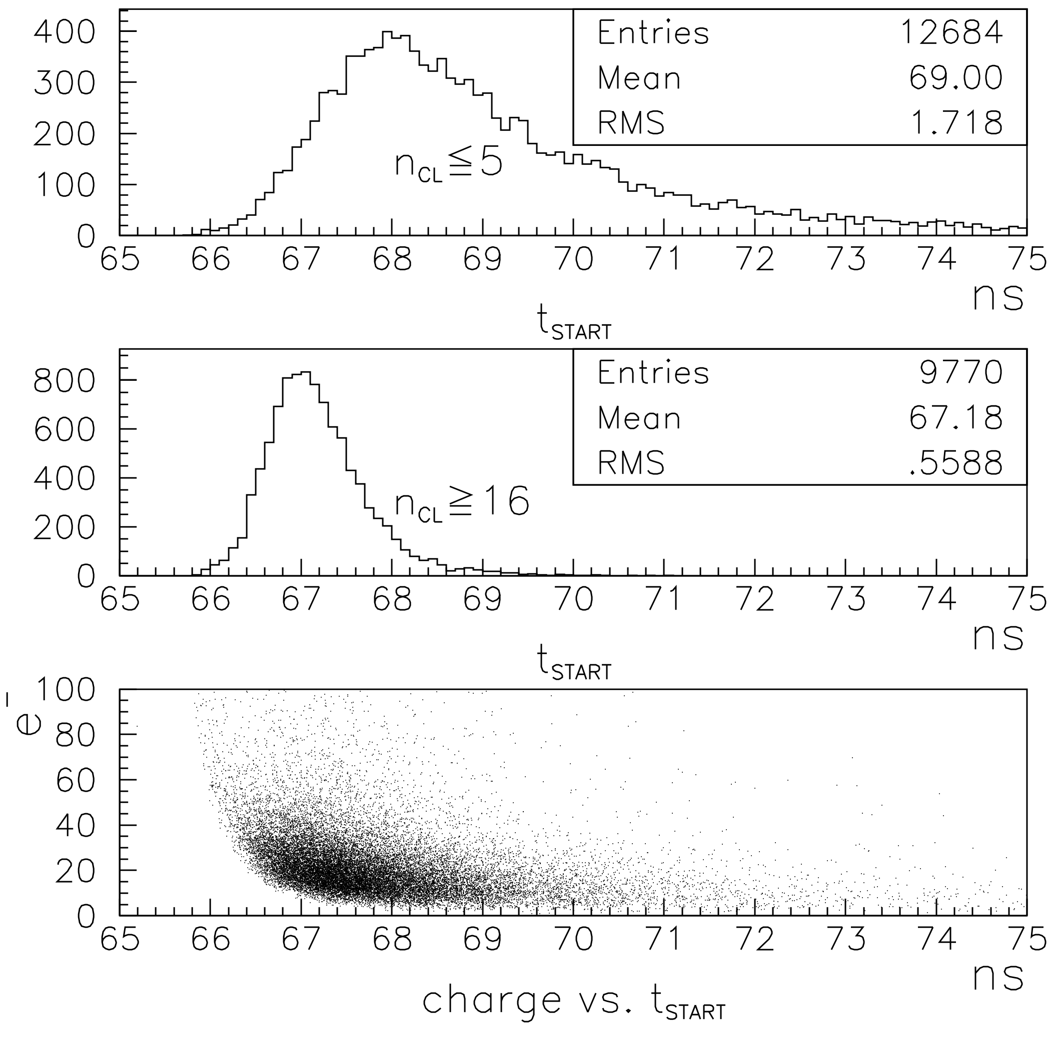

Figure 41: *Pulse start-time and charge versus start-time distribution for minimum ionizing tracks. The top plot shows the start-time when the number of clusters is* ≤ 5*. The middle plot shows the start-time when the number of clusters is* ≥ 16*. The bottom plot shows the charge versus start-time distribution.*

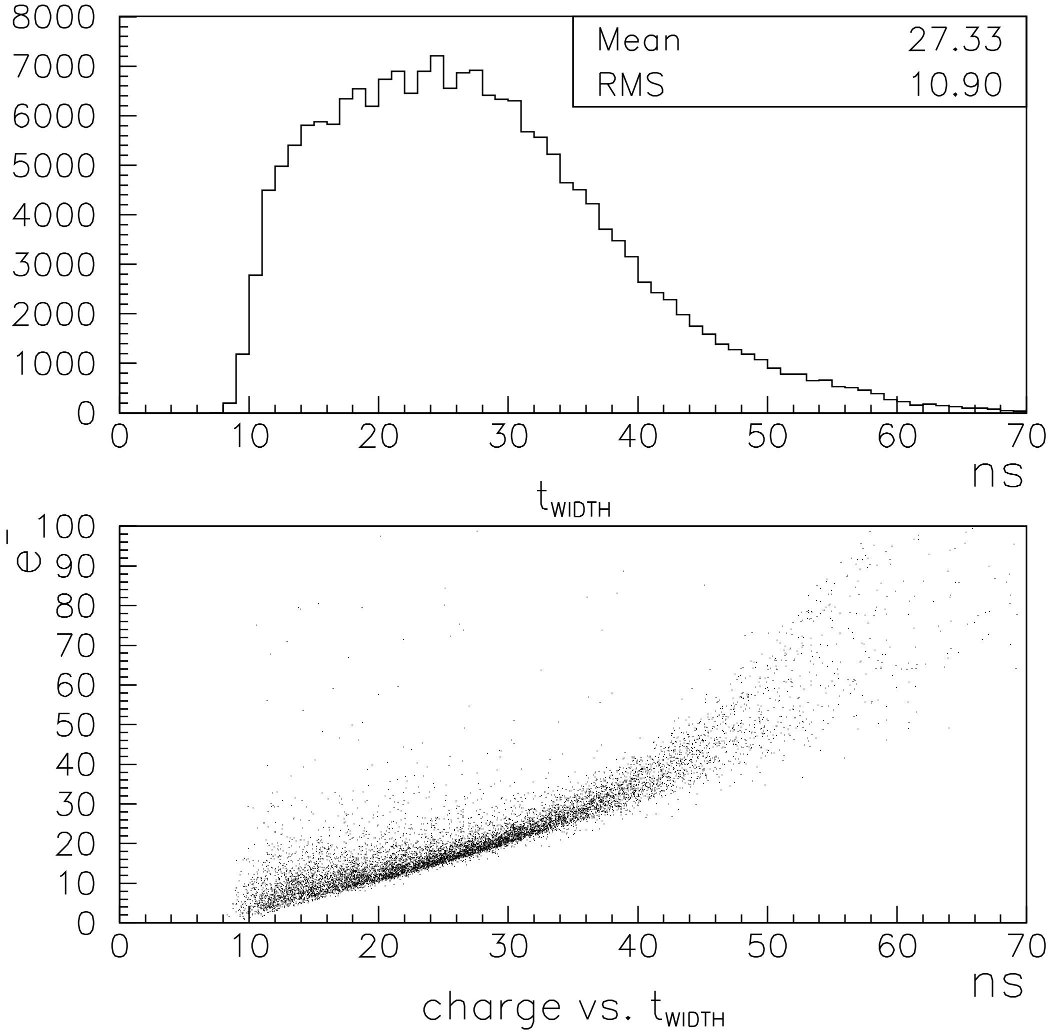

Figure 42: *Top: The output width distribution for a "typical" minimum ionizing track. Bottom: Charge versus width relation for the same track.*

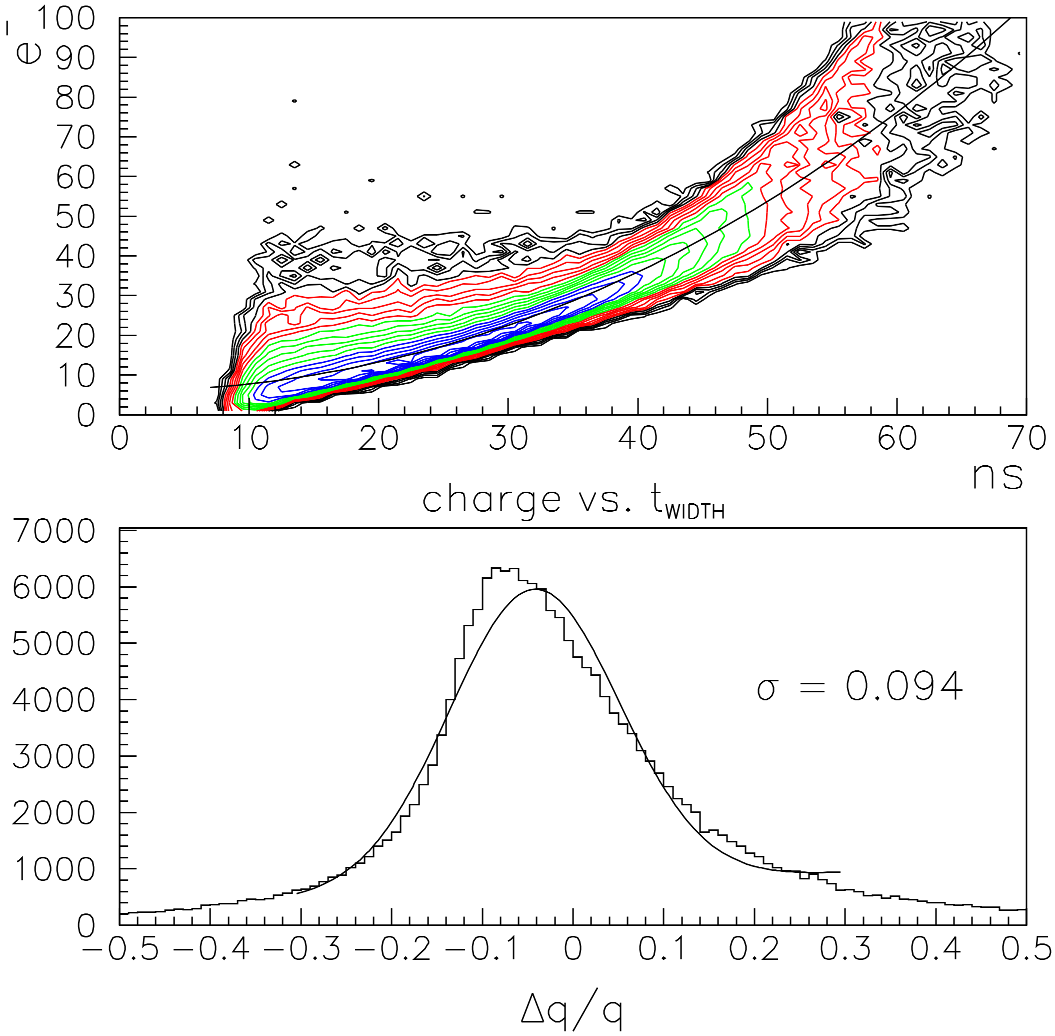

Figure 43: *Top: The charge versus output width distribution for a "typical" minimum ionizing track. The cubic polynomial fit to charge as a function of output width is shown. The contours are logarithmic. Bottom: Fit of the* $\Delta q/q$ *distribution to a Gaussian and a linear background in the vicinity of the peak.*

7 Conclusions

The expected signals from the COT have been discussed and the essential features of the ASDQ have been described. The note also presents the specifications of the ASDQ, and the necessary details for its usage. Latest information about the ASDQ tests and status are available on the ASDQ web-site, **http://dept.physics.upenn.edu/~wasiq/asdq.html**.

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[3] A Fast, Low Power, Amplifier-Shaper-Discriminator for High Rate Straw Tracking Systems, IEEE trans on Nuc. Sci. V 40. No. 4, August 1993, p 630.

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[5] Garfield.

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