CDF/DOC/TRIGGER/CDFR/DRAFT

Run II XFT Linker Design Specification

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1 Overview

The Linker is the second stage of the eXtremely Fast Tracker (XFT). It has the responsibility of linking pixels *between* the axial superlayers of the COT. The pixels themselves are found by the Finder, the first stage of the XFT, which is documented elsewhere [1, 2]. The Linker is separated into 288 ϕ slices of $1.25°$. Each slice has a dedicated chip with the task of finding tracks within the slice. The results of the Linker are passed to the XTRP for extrapolation to other portions of the detector and used in the Level 1 trigger decision. The chips will be commercially available programmable logic devices (PLD's). These provide the benefit of being relatively inexpensive and readily available. The programmability adds a tremendous amount of flexibility to the system. This will allow a change of the Level 1 tracking algorithm during the run if necessary and increase our ability to respond to unforseen problems.

This document is the design specification for the Linker portion of the XFT. The Linker system will consist of 24 identical 9U VME cards which reside in three Linker crates (8 cards in each crate). The Linker crates will be located below the Finder crates in the three XFT racks in the first floor counting room. Figure 1 shows the Finder and Linker crates in a single XFT rack. Also, shown are the interconnects between the Finder and Linker.

2 Linker Board

The input to the Linker cards is through four cables entering the front panel. Each Linker card contains receivers for the input data, input FIFOs, 12 Linker PLD chips, 2 output formatting chips, a VME interface, PLD loading circuits, clock circuits, and LVDS drivers for the output to the XTRP. The Linker output signals will pass through the J3 backplane to a passive transition card with 2 60 conductor cables connected to the XTRP.

A block diagram of the Linker Card is shown in Figure 2. The input to the Linker card is via four cables from the Finder. Two of the cables are 25 pair cables and the other two cables are 17 pair cables. (This assumes the use of 28 bit channel links). The data is received by National's 28 bit Channel Links. The channel links demux the data from 7:1. Twenty-eight bits of Finder data are presented at the output of the channel links to a block of FIFO's (Cypress CY7C42X1) with the write clock supplied by the channel links. The FIFO's are read/write accessible from VME. This provides a means to load and unload the FIFO's for diagnostic purposes. The pixel information is routed to 12 Linker chips (Altera 10K70RC240-3) for processing. The function of the Linker chips is described in Section 5. The output of the 12 Linker chips is routed to two Formatter Chips (Altera 10K20RC240-4). The function of the Formatter chips is discussed in Section 6. The Formatter chips include the implementation of output FIFO's which are accessible through VME. The output of the Formatter chip is routed to LVDS drivers (National DS90C031). The output of the LVDS drivers is sent through the J3 backplane to a passive transition card with 2 60 conductor cables connected to the XTRP.

In addition, the Linker Board contains circuitry to perform a number of support functions. The first is a VME interface (Altera 10K20RC240). The VME interface is discussed in detail in Section 3.1. The second section is for the programming of the Linker and Formatter chips. This consists of a controller (actually part of the same chip used for the VME interface) and FlashRam memory which is deep enough to store a separate program for each Linker and Formatter chip. More details are given below. The third section is the clock generation and distribution. This takes as input the CDF clock and generates three clocks in phase with one another. The three clocks are 132ns, 66ns, and 33ns. Finally, for diagnostic purposes we have a JTAG controller which allows a boundary scan of all Linker chips, both Formatter chips, and the VME interface chip. The access to the JTAG circuitry is via a connector on the front panel.

3 Control

The control logic consists of 3 main pieces: the VME slave interface, the response to trigger and diagnostic commands, and the loading of the programmable logic devices. In addition, there is the need for the Linker to be synchronized with the rest of the trigger system. Each of these are described below.

3.1 VME Slave Interface

The Linker board will implement a modified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may either be single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. We have implemented and tested a version of this interface using an Altera 10K50 device (note that the the interface uses less than 10% of the resources of this device).

The readout of the Level 2 buffers is accomplished by performing block reads of memory mapped address space. The memory map is detailed in Appendix A.

3.2 Synchronization

There will be an 8-bit bunch counter on each Linker board, following the specification set in CDF Note 3145[5]. This counter will be used to time stamp the data relative to the Bunch Zero signal. The counter output will be latched and stored in the pipeline along with the Linker input and output signal described above. An offset is applied to this counter which indicates the number of crossings used by systems prior to data receipt at the Linker Board (this includes the Finder Board). This offset will be loadable via VME.

3.3 Response to Control Signals

The Linker is designed to continually process data at input, provide outputs, respond to L1/L2 accepts, etc. The exception to this is at power-up, or after an error, when the HALT-RECOVER-RUN control sequence is issued.

The response to the HALT-RECOVER-RUN sequence follows guidelines described in reference [3].

- HALT
  - The clocking of the pipeline FIFOs will halt.
- RECOVER
  - Input FIFOs are reset.
  - Pipeline is reset. This means the following stages of each Linker chip (each described in 5.4) are reset:
    - RPIX output
    - ROAD_FIND output
    - OR output
    - BEST_TRACK output
  - Formatter chip output and its pipline are reset
  - Bunch counter is reset.
- RUN
  - RPIX output is held at reset until first B0 is seen.

The above response will be implemented using a state machine.

3.4 Loading of Linker Chips

The Linker board will contain the following Altera devices:

- 12 Linker chips implemented using 10K70 chips
- 1 VME Interface + control implemented using a 10K20 chip
- 2 Formatter chips implemented using 10K20 chips

Each of these chips needs to be configured at system power-up. They can also be reconfigured in circuit by resetting the device and loading new data. Reconfiguration takes typically 200ms per device.

We plan to load the devices in the following way. The VME/control chip will be a fixed program and will be loaded using a configuration EPROM. If there are errors or changes needed to the VME/control , the EPROM can be removed and reprogrammed. This needs to be done, since this chip will then provide control for the loading of the remaining 14 chips.

The remaining 14 chips (the 12 linker chips and the 2 formatter chips) will be loaded using a passive serial scheme. A 10K70 device needs 881,000 bits loaded serially, while a 10K20 device needs 225,000 bits loaded serially. The total number of bits required to load these 14 chips is then 13MB. These will be stored in a 16MB FlashRAM.

Logic in the VME/control chip will toggle the control lines and serialize the data from the Flash RAMs for distribution to the Altera chips.

The procedure for loading the Altera chips on a Linker board will be:

- at power up the VME/control is loaded from the EPROM
- the FLASH rams will be loaded from VME
- the configuration command is given from VME and the remaining Altera chips are loaded.
- if there is a power failure, the chips will reload automatically from EPROM, and then FLASH ram.

4 Input

4.1 Finder to Linker Data Transmission

At present we assume (as does the Finder board design) that we will use National's Channel Link Driver/Receiver pair for the Finder to Linker communication. The plan is to use 1 28 bit channel link per two Finders (utilizing only 26 of the available 28 bits). The total number of channels links required per Linker Board is 14.

4.2 Input FIFOs

The 26 bits of output from each channel link will feed three 9 bit FIFOs. The FIFOs in turn will feed the Linker chips. Use of the FIFOs will allow for alignment of data from different Finders (from the same Finder Board as well as different Finder boards). In addition, these FIFOs can be loaded separately from VME which allows an important path for diagnostic tests.

4.3 Input Mapping

Each Linker receives input from 8, 9, or 10 Finder chips. The Finder information is then routed to each of the 12 Linker chips on the board. Appendix B lists the Finders for each Linker board, as well as which subset of Finders feed each Linker chip on each board. Note that all boards are identical, but that the inputs for each Linker chip vary for each chip. (This implies that the Altera programming for each Linker chip is different, for the input sections only.)

5 Linker Chip Design

Each Linker chip will be responsible for finding tracks within a 1.25° slice of the azimuthal angle phi. Each chip will locate the subset of tracks that pass through superlayer 6 (the third axial superlayer) within the slice.

5.1 Linker Chip Implementation in PLD

The Linker algorithm will be implemented in a programmable logic device (PLD). The targeted device is the 10K70RC240-3 from ALTERA's FLEX10K series. The device has logic elements that consists of 4 inputs and 1 output. The chip also contains "embedded array blocks" (EAB's) which can act as on-board RAM. The chip comes in several packages. We plan to use the quad-flat pack 240-pin package.

Using ALTERA's MAX-PLUS-II software we have implemented a version of the Linker onto a smaller device - the 10K50. To fit into this device the part of the algorithm for linking 3 layer tracks was removed. We found the follow use of resources:

- 2391 Logic Elements used, 83% of available elements.
- 11520 bits of Memory (EAB's), 56% of available memory.

The limiting factor in the above resources is Logic Elements. Although 17% of the Logic Elements are left in the above case, in practice it is difficult to utilise more than 85% of the available Logic Elements, since routing becomes extremely complicated. The above design in a 10K70 uses only 64% of the available Logic Elements. (Including the 3 layer linking requires an additional 500 Logic Elements, which puts resource usage at less than 80%.)

We have simulated test vectors in the ALTERA software. We have successfully produced output from test vector input. These studies are continuing.

5.2 Linker Chip Inputs

The inputs to the Linker chip are the pixels from the Finder chips. This information is routed from the input FIFO's to the each individual Linker chip. Each Linker chip requires either 8, 9, or 10 Finder chips worth of pixel information. Many pixels are shared among several Linker chips. The mapping of the Finder pixels to the Linker inputs is described in Section 2. Table 1 gives the pin assignment for the inputs to the Linker chip. The Finder pixels enter the Linker chip every 33ns and the information is an exact copy of the information output by the Finders every 33ns. The input data is latched in the Linker chips on the rising edge of the 33ns clock.

In addition to the pixel input, there is also VME address and data buses, trigger controls (L1/L2 accepts and buffer addresses), output enables for the VME data lines, 132ns, 66ns, and 33ns clock signals, chip configuration controls, and JTAG boundary scan controls. These are also summarized in Table 1.

5.3 Linker Chip Outputs

There are two types of outputs from the Linker chip. The primary output, which is passed onto the Formatter chip, consists of the track information for the Linker. Note that the output P_t word is 8 bits. The eight bits are 3 bits of mini-P_t and 5 bits of section P_t. Only 7 bits are required to uniquely specify a P_t, but for space reasons this conversion is done in the Formatter chip (the conversion is actually from 8 bits to a number from 0-95). Table 2 summarizes the output words and pin assignments for the Linker Chip. The second type of output is used for diagnostic purposes only. The diagnostic information consists of the core pixels for the Linker. The information is stored in the Level 1 pipeline and Level 2 buffers. Both are stored in RAM (EAB's : Embedded Array Blocks) on board the chip. The information is initially stored in the Level 1 pipeline. A copy of the this information is stored in one of four Level 2 buffers upon a Level 1 accept. The Level 2 buffers can be read out upon request via the VME interface.

Input	Pin Number	Note
Finder[1][0-11]		
Finder[2][0-11]		Finder[i][0-11] input occurs every 33ns. The Data is Latched on the rising edge of clk33.
Finder[3][0-11]		
Finder[4][0-11]		
Finder[5][0-11]		
Finder[6][0-11]		
Finder[7][0-11]		The Definition of Finder[i][] (i=1,10) is given in the mapping described in section 4.3
Finder[8][0-11]		
Finder[9][0-11]		
Finder[10][0-11]		
VME Data[0-31]		Data Lines are Bidirectional.
L1_Acc		Level 1 accept
L2_Buff[0-1]		Level 2 buffer address bits
L2_Acc		Level 2 enable (1 means L2 accept)
L2_DBuff[0-1]		Level 2 decision buffer address bits
Pipe_word		Indicates which of two 32-bit Level 2 words will be read out
Chip_sel		Enable for VME Data output
Reset		Resets internal registers, counters, FIFOs
clk132 clk66 clk33		

Table 1: Linker Chip Input Pin definition. Power, ground, and configuration pins are not user definable and are specified on the schematic diagrams.

Output	Pin Number	Note
Trk_Pt[0-7]		
Trk_Phi[0-2]		
Tfnd4		
Tfnd3		
B0 Marker		

Table 2: Linker Chip Output Input Pin. Note: VME databus is bidirectional and pins are defined in Table 1.

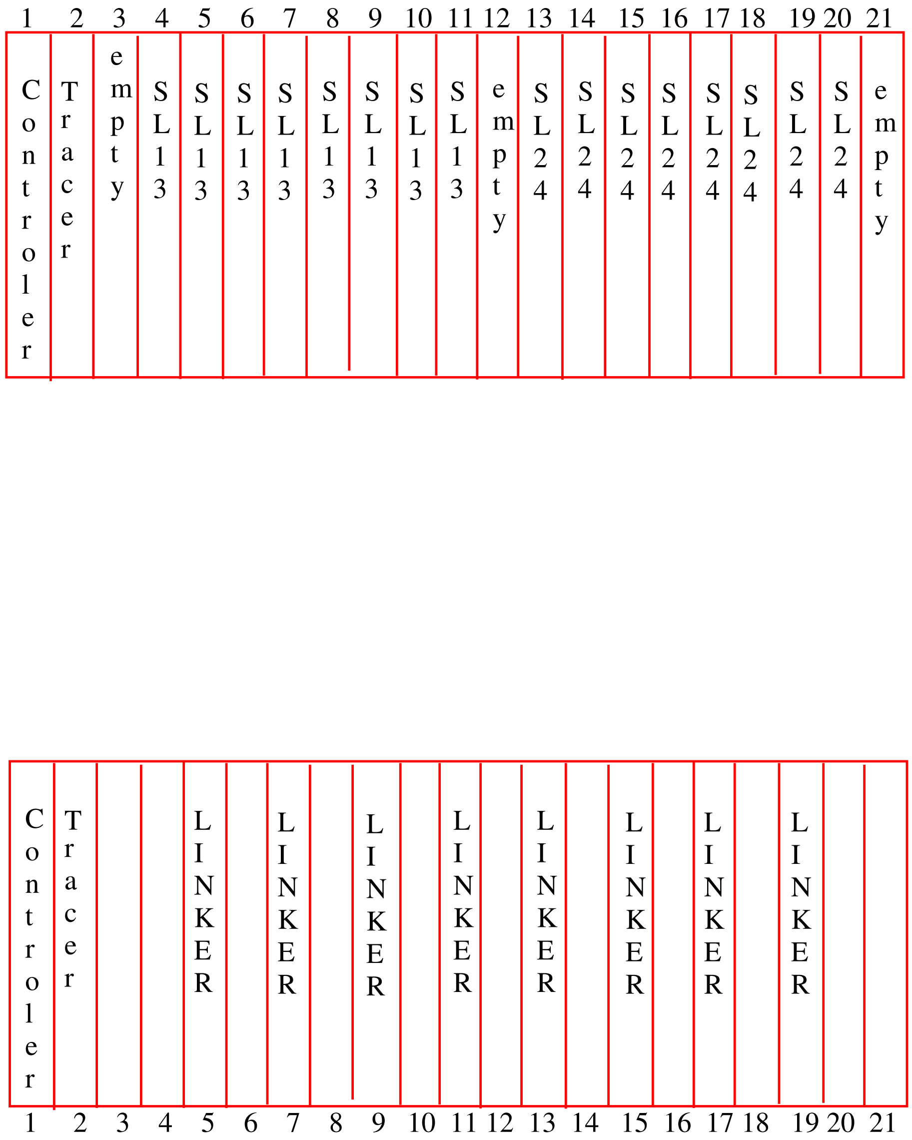

Figure 1: Finder and Linker Crate.

Figure 2: Linker Board Block Diagram.

5.4 Linker Chip Block Diagram

Figure 3 shows a block diagram of the functionality of the Linker chip. Each of the major blocks is implemented as a single routine written in AHDL (Altera's High Definition Language). The functionality of each block is described in broad terms below.

5.4.1 RPIX

Each finder sends the information from the 4 COT cells it processes to the Linker in 4 12-bit words, 1 word every 33nsec. These words then have to be time-demultiplexed so the linker can look at all cells in parallel, for all 4 superlayers (Altera routine RPIX2.TDF). There is a two-fold symmetry in the Linker, which allows the number of stored roads to be cut in half. Effectively, each Linker is then arranged as two sub-linkers, which we call A and B. To take advantage of this, RPIX must latch the pixels which are used as input to the two sub-linkers. The following tasks are then performed:

- Latches the input data on the rising edge of 33ns clock
- Reformatts the pixels into sublinkers A and B. Each sublinker covers one half of the $1.25°$ slice.
- Outputs the pixels for linker A on rising edge of 66ns clock
- Outputs the pixels for linker B on the falling edge of 66ns clock.

5.4.2 ROAD_FIND(4 and 3 layer)

The pixels for Linker A and B are passed on to the road finding logic (Altera routine RD48SL4.TDF and RDSL3.TDF). As mentioned above, by taking advantage of a two-fold symmetry in the Linker, only half the roads need to be implemented in the logic. Only 1229 4-layer Roads and 204 3-layer Roads are implemented in the chip logic. Each road is stored as the "AND" of 4 (or 3) pixels, one from each layer. Four-layer and three-layer roads are found in parallel. The four-layer road finding outputs a 96 bit P_t word every 66 ns. Each bit in this word corresponds to a valid track found with a given P_t bin. The three-layer road finding outputs a 32 bit Pt word every 66 ns. The number of output bits is smaller because the P_t resolution is worse using only 3 layers rather than 4. The bits are organized so that bits 0,1,2,....42,43,...93.94,95 correspond to P_t bins -1.5,-1.55,... -infinite,+infinite,...+1.55,+1.50. A similar arrangement is used for the 32 bit word from 3 layer tracks.

5.4.3 OR (4 and 3 layer)

The P_t words for sublinker A and B are "OR'ed" together.

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XFT Linker Chip Block Diagram (V2.0)

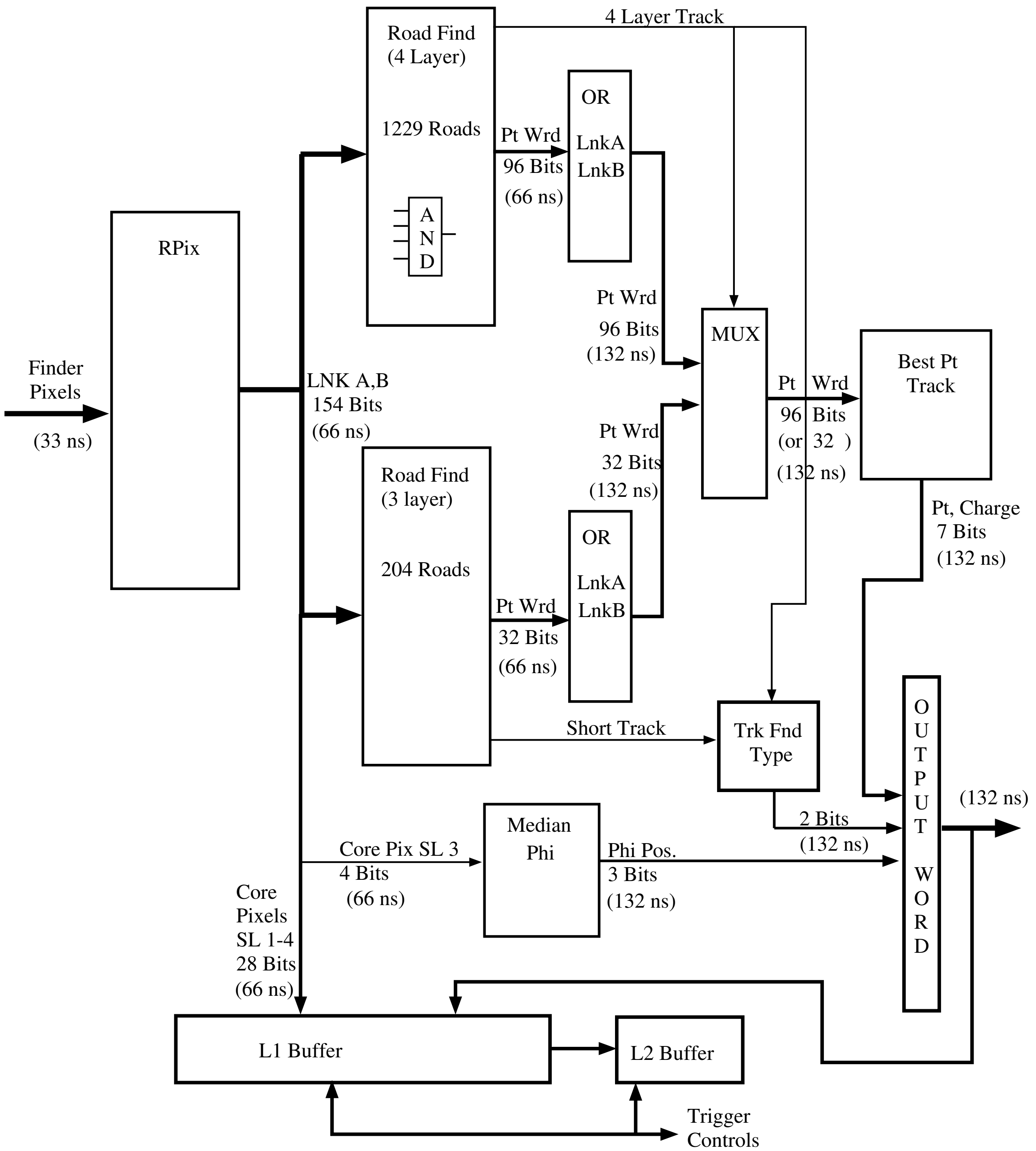

Figure 3: Linker chip block diagram.

5.4.4 MUX

The inputs to this section are the 96 bit word from the 4 layer track finding and the 32 bit word from the 3 layer track finding. If a 4 layer track is found, then it is output from the multiplexor, otherwise the 3 layer track word is output.

5.4.5 BEST_PT

Either the 96 (4 layer) or 32 (3 layer) bit P_t word is presented to the "Best P_t Track" logic (Altera routine LPOUT48.TDF) which determines what P_t to report. Its output is a 8 bit word with Pt and charge information: 3 bits of mini-P_t and 5 bits of section P_t. This set of logic is fairly complicated. It must of course handle the simplest case, where 1 track has passed through a given linker chip. Since the FINDER tends to report re than one pixel per layer even for isolated tracks, the Linker will tend to find multiple tracks (all neighboring in P_t bins). The BEST_PT logic is designed to report the median P_t bin of this cluster of P_t bins. In addition, the BEST_PT logic must handle the case where more than one track has passes through a given Linker chip. The bias at present when this occurs is to select the cluster of P_t bins which is higher in P_t and then report the median of this cluster.

5.4.6 MEDIAN_PHI

This section looks at the 8 pixels reported from the FINDER for superlayer 3 and determines a simple median of the pixels, outputing a 3 bit word. Remember that tracks are found in sub-linkers A and B. If no track is found in a given sub-linker, the pixels for superlayer 3 for that sub-linker are masked out. Beyond this, the correlation between the phi position and the reported P_t is lost (note that this is on average a 1 pixel shift).

5.4.7 L1 Pipeline/L2 Buffers

This section of logic (Altera routine LNK_PIPE.TDF) stores the core pixels (a total of 56 for all 4 layers) presented to each Linker chip. The Level 1 pipeline is implemented using a programmable-depth FIFO (up to 128 deep). Two 32 bit words are written into the FIFO each 132 nsec. The FIFO feeds 4 Level 2 buffers.

5.5 Linker Chip Timing Diagram

Figure 4 shows the timing diagram for the Linker chips processes. From input to output, the total number of 132nsec clock ticks needed by the Linker chip is 4.

6 The Formatter Chip

The role of the Formatter chip is to prepare the tracking data out of the XFT for input to the extrapolating unit (XTRP). First, the Formatter chip receives a new list of tracks from a set of Linker chips every 132ns. Next, duplicate tracks near the boundaries of the region covered by each Linker chip are removed. Finally, the tracking information is multiplexed into 4 data words that are sent on sequentially (every 33ns) to the XTRP.

6.1 Format Chip Input

Every Linker board contains 12 Linker and 2 Formatter chips. The 12 Linkers are segregated into two sets of 6. Each Formatter chip takes in the tracking information from one of two sets of 6 Linkers. Because a Linker chip puts out track information as a 14 bit word every 132ns, each Formatter chip receives one 84 bit word (6×14 bits) every 132ns. The 14 bit Linker word (the format is described in detail above) includes 8 bits of P_T and 3 bits of ϕ information. Within the 84 bit word, the 6 Linker words are ordered in increasing ϕ with increasing Linker number. Since each Linker covers an angular region of $1.25°$ in ϕ, the total coverage for each Formatter chip is $7.5°$Ṫable 3 lists the input pin specification for a given Formatter chip.

6.1.1 Formatter chip L1 Pipeline/L2 Buffers

This section of logic stores the Linker Chip output data (a total of 84 bits for all 6 Linker chips/formatter chip). The Level 1 pipeline is implemented using a programmable-depth FIFO (up to 128 deep). Two 32 bit words and one 20 bit word are written into the FIFO each 132 nsec. The FIFO feeds 4 Level 2 buffers.

6.2 P_T word compression

As mentioned in the Linker chip section above, each Linker presents the Formatter chip with an 8-bit P_T word. The 8 bits actually correspond to 96 separate P_T bins, so only 7 bits are needed to specify the P_T. This is a simple shift and add operation, but due to timing and space considerations this is easier to implement in the Formatter rather than in each Linker chip.

6.3 Duplicate Track Removal

Often, a track near the edge of the region covered by a Linker chip will also be found by the neighboring Linker. Keeping both tracks may cause problems with the trigger. This situation is resolved by keeping only one of the *duplicate* tracks. Within a Linker board, duplicate track removal is performed by the Formatter chip. The XTRP will remove duplicate tracks for Linkers at the board boundaries.

Figure 4: A simple timing diagram for the linker chip processing.

Input	Pin Number	Note
Linker[1][0-12]		
Linker[2][0-12]		
Linker[3][0-12]		
Linker[4][0-12]		
Linker[5][0-12]		
Linker[6][0-12]		
Address[0-7]		
VME Data[0-31]		
L1_Acc		Level 1 accept
L2_Buff[0-1]		Level 2 buffer address bits
L2_Acc		Level 2 enable (1 means L2 accept)
L2_DBuff[0-1]		Level 2 decision buffer address bits
Pipe_word		Indicates which of two 32-bit Level 2 words will be read out
Chip_sel		Enable for VME Data output
clk132		
clk66		
clk33		

Table 3: Formatter Chip Input Pin definition. Power, ground, and configuration pins are not user definable and are specified on the schematic diagrams.

	Linker(N+1)	Linker(N)	Linker(N-1)
ϕ bin position	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0

Table 4: Arrangement of phi bins for adjacent Linker chips. Note: the direction of increasing ϕ is the direction of increasing Linker number.

The duplicate track removal algorithm begins by checking the ϕ bits for each Linker word to determine the angular position of the track. The 3 ϕ bits in the 14 bit Linker word give 8 bin positions (0 - 7) spanning 1.25°.The ϕ bin arrangement of adjacent Linker chips is illustrated in Table 4. Duplicate tracks are identified by comparing phi bin (0-7) on Linker N to Linker N-1. If Linker N-1 has a phi position within 2 bins of Linker N, the two tracks are considered to be duplicates. To remove the duplicate, the P_T of the track of Linker N-1 is set to zero. For example, if Linker-6 has phi-bin 0 registered and Linker-5 has phi-bin 7 registered, the P_T for Linker 5 is set to zero.

6.4 Formatter Chip Output

After duplicate tracks are removed, the Linker information is reformatted before it is sent to the XTRP. The data out of the format chip will consist of 4, 30 bit words, each clocked out at 33ns. The format of the output words is given below (Subsections of the output word is separated by a '/', and the number of bits for each subsection are in parentheses).

- word 1: Mk(2) / Ph0,S,I,X,Pt0(7) / Ph1,S,I,X,Pt1(7) / SP(2)
- word 2: Mk(2) / Ph4,S,I,X,Pt4(7) / Ph5,S,I,X,Pt5(7) / SP(2)
- word 3: Mk(2) / Ph2,S,I,X,Pt2(7) / Ph3,S,I,X,Pt3(7) / SP(2)
- word 4: Mk(2) / B0(1) / SP(27)

Mk(2) is the word marker count (1 - 4), B0(1) is the beam zero marker, SP indicates spare bits (2 in the first 3 words and 27 in the last word), Ph# is the 3-bit phi word, S is the short track bit, I is the isolated track bit, X is an extra bit left over for future use. The order of the output words is important so that enough time is permitted for the XTRP to remove duplicate tracks at board boundaries. Table 5 lists the output pin designation for a given formatter chip.

6.5 Formatter Chip Implementation and Simulation

We plan on implementing the Formatter algorithm using the Altera 10K20RC240-4, which is a 20,000 gate device. The footprint of the chip contains 84 inputs, 30 outputs,

Output	Pin Number
Formatter[0-29]	139 141 142 143 144 146 147 148 149 151
	152 153 154 156 157 158 159 161 162 163
	164 166 167 168 169 171 172 173 174 175

Table 5: Formatter Chip Output Pin definition.

32 + 8 bi-directional pins for VME addressing and control. After compiling the text design file, we find that the formatter chip requires less than 25% of the logic elements available. The simulation was performed on the formatter chip consisted of sending the chip a 84-bit long word that contained the pt+phi words for 6 Linkers. The output of the 1st word occurs 47 ns after the 84 bit Linker word arrives, and so the Formatter adds one-half of a 132nsec clock tick to the Linker board timing.. The timing diagram shown in Figure 6 illustrates the performance of the formatter chip.

7 Linker Board Output

The output of each formatter chip is sent to a National DS90C031 LVDS differential driver. Each driver sends the data on to the XTRP over a 60 conductor flat cable. Each signal of the 30 bit output is paired a separate ground conductor. The drivers will be located on the Linker board, and will send the information to the Linker transition card, which at present is a passive card with connectors only. The data format on the two cables is described in the Formatter chip section above.

Each Linker board sends (57 bits/formatter chip $\times$ 2 Formatters per 132 nsec) for a bandwidth of 8.64×10^8 bits/second

8 Linker Board Clock

The Linker chip expects 3 clocks on input: 132nsec, 66nsec, and 33 nsec. The Finder data is clocked in at 33nsec, and the linker data is clocked to the XTRP module on output (from the Formatter chips) at 33 nsec.

These clocks will be generated on each linker board using a Phase Locked Loop. A possible choice for this function is the Cypress Programmable Skew Clock Buffer CY7B991 (aka RoboClock). The reference clock in this case would be CDF_CLOCK, and we would divide down to produce a 33nsec and 66nsec clock, each with zero phase difference with the reference.

9 Linker Board Diagnostics

The primary method for implementing diagnostics on the Linker board relies on the input and output FIFOs. (Note that the output FIFOs will be implemented as part of the Formatter chip, and will be approximately 128 words deep.) The FIFOs will be read and write capable from VME. This will allow test patterns to be downloaded to the input FIFOs, which can then either be read back, or fed into the Linker chips. The output FIFOs can then be examined to verify that the proper tracks are found.

In addition, we plan to implement a JTAG controller which allows a boundary scan of all Linker chips, both Formatter chips, and the VME interface chip. The access to the JTAG circuitry is via a connector on the front panel.

Figure 5: Block diagram of the formatter chip

Figure 6: Timing diagram of the formatter chip

A APPENDIX: Memory Map

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The memory map follows the guidelines described in CDF Note 2388\cite{cdf2388}
and CDF Note 3145\cite{synch}.

Memory Map:

General:
  YY00 0000 Diagnostic register (32 bits) (R/W)

  YY00 0004 Control (R/W)
Bit  Function
 32  Reset


  YY00 0008 Pipeline Length (R/W)
  This equals 42 minus the number of stages before the Linker.
Bit     Function
24-31   Programmable pipeline depth

  YY00 000C Pipeline offset (R/W)
  This equals the number of pipeline stages in the Linker.

  YY00 0010

  YY00 0000

  YY00 0000


Linker Input Fifos

  YY50 XXXX FIFO 1 (bits


Linker Output Fifos

  YY50 XXXX FIFO 1 (bits


L2 buffers (Read only)
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```
  L2 buffers start at address YYZ0 0000, where
Z=8 for buffer 0
Z=9 for buffer 1
Z=A for buffer 2
Z=B for buffer 3
  YYZ0 0000 L2 Buffer Header word
Bit    Function
0-7    Bunch ID: 8 bit counter from Bunch Zero
8-12   Geographical address
13-22  Board Number
23-31  Board Type
  YYZ0 0004 Linker 0 Core pixel info a (bits 0-27)
  YYZ0 0008 Linker 0 Core pixel info b (bits 0-27)
  YYZ0 000C Linker 1 Core pixel info a (bits 0-27)
  YYZ0 0010 Linker 1 Core pixel info b (bits 0-27)
  YYZ0 0014 Linker 2 Core pixel info a (bits 0-27)
  YYZ0 0018 Linker 2 Core pixel info b (bits 0-27)
  YYZ0 001C Linker 3 Core pixel info a (bits 0-27)
  YYZ0 0020 Linker 3 Core pixel info b (bits 0-27)
  YYZ0 0024 Linker 4 Core pixel info a (bits 0-27)
  YYZ0 0028 Linker 4 Core pixel info b (bits 0-27)
  YYZ0 002C Linker 5 Core pixel info a (bits 0-27)
  YYZ0 0030 Linker 5 Core pixel info b (bits 0-27)
  YYZ0 0034 Linker 6 Core pixel info a (bits 0-27)
  YYZ0 0038 Linker 6 Core pixel info b (bits 0-27)
  YYZ0 003C Linker 7 Core pixel info a (bits 0-27)
  YYZ0 0040 Linker 7 Core pixel info b (bits 0-27)
  YYZ0 0044 Linker 8 Core pixel info a (bits 0-27)
  YYZ0 0048 Linker 8 Core pixel info b (bits 0-27)
  YYZ0 004C Linker 9 Core pixel info a (bits 0-27)
  YYZ0 0050 Linker 9 Core pixel info b (bits 0-27)
  YYZ0 0054 Linker 10 Core pixel info a (bits 0-27)
  YYZ0 0058 Linker 10 Core pixel info b (bits 0-27)
  YYZ0 005C Linker 11 Core pixel info a (bits 0-27)
  YYZ0 0060 Linker 11 Core pixel info b (bits 0-27)
  YYZ0 0064 Linker 0 and Linker 1 Output (bits 0-25)
  YYZ0 0068 Linker 2 and Linker 3 Output (bits 0-25)
  YYZ0 006C Linker 4 and Linker 5 Output (bits 0-25)
  YYZ0 0070 Linker 6 and Linker 7 Output (bits 0-25)
  YYZ0 0074 Linker 8 and Linker 9 Output (bits 0-25)
  YYZ0 0078 Linker 10 and Linker 11 Output (bits 0-25)
```

B APPENDIX: Finder to Linker Map

In the tables below, the 12 Linkers per board are labelled L1-L12. The layer 1 Finders are numbered from 0-47, the layer 2 Finders from 0-71, the layer 3 Finders from 0-95, and the layer 4 Finder from 0-119. X means that input Finder is not used.

Linker chip Finder Map, Board No. 1

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	47	47	47	0	0	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1	2	2	2
1	X	1	1	X	X	X	X	2	2	X	X	X
2	71	71	0	0	0	0	1	1	1	1	2	2
2	0	0	1	1	1	1	2	2	2	2	3	3
2	X	1	X	X	X	2	X	X	X	3	X	X
3	0	0	0	1	1	1	2	2	2	3	3	3
3	X	X	1	X	X	2	X	X	3	X	X	4
4	119	119	0	0	0	1	1	2	2	3	3	3
4	0	0	1	1	1	2	2	3	3	4	4	4
4	1	1	2	2	2	3	3	4	4	5	5	5
4	X	X	X	X	3	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 2

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	1	1	1	2	2	2	2	2	2	3	3	3
1	2	2	2	3	3	3	3	3	3	4	4	4
1	X	3	3	X	X	X	X	4	4	X	X	X
2	2	2	3	3	3	3	4	4	4	4	5	5
2	3	3	4	4	4	4	5	5	5	5	6	6
2	X	4	X	X	X	5	X	X	X	6	X	X
3	4	4	4	5	5	5	6	6	6	7	7	7
3	X	X	5	X	X	6	X	X	7	X	X	8
4	4	4	5	5	5	6	6	7	7	8	8	8
4	5	5	6	6	6	7	7	8	8	9	9	9
4	6	6	7	7	7	8	8	9	9	10	10	10
4	X	X	X	X	8	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 3

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	3	3	3	4	4	4	4	4	4	5	5	5
1	4	4	4	5	5	5	5	5	5	6	6	6
1	X	5	5	X	X	X	X	6	6	X	X	X
2	5	5	6	6	6	6	7	7	7	7	8	8
2	6	6	7	7	7	7	8	8	8	8	9	9
2	X	7	X	X	X	8	X	X	X	9	X	X
3	8	8	8	9	9	9	10	10	10	11	11	11
3	X	X	9	X	X	10	X	X	11	X	X	12
4	9	9	10	10	10	11	11	12	12	13	13	13
4	10	10	11	11	11	12	12	13	13	14	14	14
4	11	11	12	12	12	13	13	14	14	15	15	15
4	X	X	X	X	13	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 4

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	5	5	5	6	6	6	6	6	6	7	7	7
1	6	6	6	7	7	7	7	7	7	8	8	8
1	X	7	7	X	X	X	X	8	8	X	X	X
2	8	8	9	9	9	9	10	10	10	10	11	11
2	9	9	10	10	10	10	11	11	11	11	12	12
2	X	10	X	X	X	11	X	X	X	12	X	X
3	12	12	12	13	13	13	14	14	14	15	15	15
3	X	X	13	X	X	14	X	X	15	X	X	16
4	14	14	15	15	15	16	16	17	17	18	18	18
4	15	15	16	16	16	17	17	18	18	19	19	19
4	16	16	17	17	17	18	18	19	19	20	20	20
4	X	X	X	X	18	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 5

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	7	7	7	8	8	8	8	8	8	9	9	9
1	8	8	8	9	9	9	9	9	9	10	10	10
1	X	9	9	X	X	X	X	10	10	X	X	X
2	11	11	12	12	12	12	13	13	13	13	14	14
2	12	12	13	13	13	13	14	14	14	14	15	15
2	X	13	X	X	X	14	X	X	X	15	X	X
3	16	16	16	17	17	17	18	18	18	19	19	19
3	X	X	17	X	X	18	X	X	19	X	X	20
4	19	19	20	20	20	21	21	22	22	23	23	23
4	20	20	21	21	21	22	22	23	23	24	24	24
4	21	21	22	22	22	23	23	24	24	25	25	25
4	X	X	X	X	23	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 6

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	9	9	9	10	10	10	10	10	10	11	11	11
1	10	10	10	11	11	11	11	11	11	12	12	12
1	X	11	11	X	X	X	X	12	12	X	X	X
2	14	14	15	15	15	15	16	16	16	16	17	17
2	15	15	16	16	16	16	17	17	17	17	18	18
2	X	16	X	X	X	17	X	X	X	18	X	X
3	20	20	20	21	21	21	22	22	22	23	23	23
3	X	X	21	X	X	22	X	X	23	X	X	24
4	24	24	25	25	25	26	26	27	27	28	28	28
4	25	25	26	26	26	27	27	28	28	29	29	29
4	26	26	27	27	27	28	28	29	29	30	30	30
4	X	X	X	X	28	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 7

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	11	11	11	12	12	12	12	12	12	13	13	13
1	12	12	12	13	13	13	13	13	13	14	14	14
1	X	13	13	X	X	X	X	14	14	X	X	X
2	17	17	18	18	18	18	19	19	19	19	20	20
2	18	18	19	19	19	19	20	20	20	20	21	21
2	X	19	X	X	X	20	X	X	X	21	X	X
3	24	24	24	25	25	25	26	26	26	27	27	27
3	X	X	25	X	X	26	X	X	27	X	X	28
4	29	29	30	30	30	31	31	32	32	33	33	33
4	30	30	31	31	31	32	32	33	33	34	34	34
4	31	31	32	32	32	33	33	34	34	35	35	35
4	X	X	X	X	33	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 8

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	13	13	13	14	14	14	14	14	14	15	15	15
1	14	14	14	15	15	15	15	15	15	16	16	16
1	X	15	15	X	X	X	X	16	16	X	X	X
2	20	20	21	21	21	21	22	22	22	22	23	23
2	21	21	22	22	22	22	23	23	23	23	24	24
2	X	22	X	X	X	23	X	X	X	24	X	X
3	28	28	28	29	29	29	30	30	30	31	31	31
3	X	X	29	X	X	30	X	X	31	X	X	32
4	34	34	35	35	35	36	36	37	37	38	38	38
4	35	35	36	36	36	37	37	38	38	39	39	39
4	36	36	37	37	37	38	38	39	39	40	40	40
4	X	X	X	X	38	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 9

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	15	15	15	16	16	16	16	16	16	17	17	17
1	16	16	16	17	17	17	17	17	17	18	18	18
1	X	17	17	X	X	X	X	18	18	X	X	X
2	23	23	24	24	24	24	25	25	25	25	26	26
2	24	24	25	25	25	25	26	26	26	26	27	27
2	X	25	X	X	X	26	X	X	X	27	X	X
3	32	32	32	33	33	33	34	34	34	35	35	35
3	X	X	33	X	X	34	X	X	35	X	X	36
4	39	39	40	40	40	41	41	42	42	43	43	43
4	40	40	41	41	41	42	42	43	43	44	44	44
4	41	41	42	42	42	43	43	44	44	45	45	45
4	X	X	X	X	43	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 10

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	17	17	17	18	18	18	18	18	18	19	19	19
1	18	18	18	19	19	19	19	19	19	20	20	20
1	X	19	19	X	X	X	X	20	20	X	X	X
2	26	26	27	27	27	27	28	28	28	28	29	29
2	27	27	28	28	28	28	29	29	29	29	30	30
2	X	28	X	X	X	29	X	X	X	30	X	X
3	36	36	36	37	37	37	38	38	38	39	39	39
3	X	X	37	X	X	38	X	X	39	X	X	40
4	44	44	45	45	45	46	46	47	47	48	48	48
4	45	45	46	46	46	47	47	48	48	49	49	49
4	46	46	47	47	47	48	48	49	49	50	50	50
4	X	X	X	X	48	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 11

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	19	19	19	20	20	20	20	20	20	21	21	21
1	20	20	20	21	21	21	21	21	21	22	22	22
1	X	21	21	X	X	X	X	22	22	X	X	X
2	29	29	30	30	30	30	31	31	31	31	32	32
2	30	30	31	31	31	31	32	32	32	32	33	33
2	X	31	X	X	X	32	X	X	X	33	X	X
3	40	40	40	41	41	41	42	42	42	43	43	43
3	X	X	41	X	X	42	X	X	43	X	X	44
4	49	49	50	50	50	51	51	52	52	53	53	53
4	50	50	51	51	51	52	52	53	53	54	54	54
4	51	51	52	52	52	53	53	54	54	55	55	55
4	X	X	X	X	53	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 12

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	21	21	21	22	22	22	22	22	22	23	23	23
1	22	22	22	23	23	23	23	23	23	24	24	24
1	X	23	23	X	X	X	X	24	24	X	X	X
2	32	32	33	33	33	33	34	34	34	34	35	35
2	33	33	34	34	34	34	35	35	35	35	36	36
2	X	34	X	X	X	35	X	X	X	36	X	X
3	44	44	44	45	45	45	46	46	46	47	47	47
3	X	X	45	X	X	46	X	X	47	X	X	48
4	54	54	55	55	55	56	56	57	57	58	58	58
4	55	55	56	56	56	57	57	58	58	59	59	59
4	56	56	57	57	57	58	58	59	59	60	60	60
4	X	X	X	X	58	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 13

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	23	23	23	24	24	24	24	24	24	25	25	25
1	24	24	24	25	25	25	25	25	25	26	26	26
1	X	25	25	X	X	X	X	26	26	X	X	X
2	35	35	36	36	36	36	37	37	37	37	38	38
2	36	36	37	37	37	37	38	38	38	38	39	39
2	X	37	X	X	X	38	X	X	X	39	X	X
3	48	48	48	49	49	49	50	50	50	51	51	51
3	X	X	49	X	X	50	X	X	51	X	X	52
4	59	59	60	60	60	61	61	62	62	63	63	63
4	60	60	61	61	61	62	62	63	63	64	64	64
4	61	61	62	62	62	63	63	64	64	65	65	65
4	X	X	X	X	63	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 14

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	25	25	25	26	26	26	26	26	26	27	27	27
1	26	26	26	27	27	27	27	27	27	28	28	28
1	X	27	27	X	X	X	X	28	28	X	X	X
2	38	38	39	39	39	39	40	40	40	40	41	41
2	39	39	40	40	40	40	41	41	41	41	42	42
2	X	40	X	X	X	41	X	X	X	42	X	X
3	52	52	52	53	53	53	54	54	54	55	55	55
3	X	X	53	X	X	54	X	X	55	X	X	56
4	64	64	65	65	65	66	66	67	67	68	68	68
4	65	65	66	66	66	67	67	68	68	69	69	69
4	66	66	67	67	67	68	68	69	69	70	70	70
4	X	X	X	X	68	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 15

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	27	27	27	28	28	28	28	28	28	29	29	29
1	28	28	28	29	29	29	29	29	29	30	30	30
1	X	29	29	X	X	X	X	30	30	X	X	X
2	41	41	42	42	42	42	43	43	43	43	44	44
2	42	42	43	43	43	43	44	44	44	44	45	45
2	X	43	X	X	X	44	X	X	X	45	X	X
3	56	56	56	57	57	57	58	58	58	59	59	59
3	X	X	57	X	X	58	X	X	59	X	X	60
4	69	69	70	70	70	71	71	72	72	73	73	73
4	70	70	71	71	71	72	72	73	73	74	74	74
4	71	71	72	72	72	73	73	74	74	75	75	75
4	X	X	X	X	73	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 16

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	29	29	29	30	30	30	30	30	30	31	31	31
1	30	30	30	31	31	31	31	31	31	32	32	32
1	X	31	31	X	X	X	X	32	32	X	X	X
2	44	44	45	45	45	45	46	46	46	46	47	47
2	45	45	46	46	46	46	47	47	47	47	48	48
2	X	46	X	X	X	47	X	X	X	48	X	X
3	60	60	60	61	61	61	62	62	62	63	63	63
3	X	X	61	X	X	62	X	X	63	X	X	64
4	74	74	75	75	75	76	76	77	77	78	78	78
4	75	75	76	76	76	77	77	78	78	79	79	79
4	76	76	77	77	77	78	78	79	79	80	80	80
4	X	X	X	X	78	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 17

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	31	31	31	32	32	32	32	32	32	33	33	33
1	32	32	32	33	33	33	33	33	33	34	34	34
1	X	33	33	X	X	X	X	34	34	X	X	X
2	47	47	48	48	48	48	49	49	49	49	50	50
2	48	48	49	49	49	49	50	50	50	50	51	51
2	X	49	X	X	X	50	X	X	X	51	X	X
3	64	64	64	65	65	65	66	66	66	67	67	67
3	X	X	65	X	X	66	X	X	67	X	X	68
4	79	79	80	80	80	81	81	82	82	83	83	83
4	80	80	81	81	81	82	82	83	83	84	84	84
4	81	81	82	82	82	83	83	84	84	85	85	85
4	X	X	X	X	83	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 18

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	33	33	33	34	34	34	34	34	34	35	35	35
1	34	34	34	35	35	35	35	35	35	36	36	36
1	X	35	35	X	X	X	X	36	36	X	X	X
2	50	50	51	51	51	51	52	52	52	52	53	53
2	51	51	52	52	52	52	53	53	53	53	54	54
2	X	52	X	X	X	53	X	X	X	54	X	X
3	68	68	68	69	69	69	70	70	70	71	71	71
3	X	X	69	X	X	70	X	X	71	X	X	72
4	84	84	85	85	85	86	86	87	87	88	88	88
4	85	85	86	86	86	87	87	88	88	89	89	89
4	86	86	87	87	87	88	88	89	89	90	90	90
4	X	X	X	X	88	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 19

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	35	35	35	36	36	36	36	36	36	37	37	37
1	36	36	36	37	37	37	37	37	37	38	38	38
1	X	37	37	X	X	X	X	38	38	X	X	X
2	53	53	54	54	54	54	55	55	55	55	56	56
2	54	54	55	55	55	55	56	56	56	56	57	57
2	X	55	X	X	X	56	X	X	X	57	X	X
3	72	72	72	73	73	73	74	74	74	75	75	75
3	X	X	73	X	X	74	X	X	75	X	X	76
4	89	89	90	90	90	91	91	92	92	93	93	93
4	90	90	91	91	91	92	92	93	93	94	94	94
4	91	91	92	92	92	93	93	94	94	95	95	95
4	X	X	X	X	93	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 20

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	37	37	37	38	38	38	38	38	38	39	39	39
1	38	38	38	39	39	39	39	39	39	40	40	40
1	X	39	39	X	X	X	X	40	40	X	X	X
2	56	56	57	57	57	57	58	58	58	58	59	59
2	57	57	58	58	58	58	59	59	59	59	60	60
2	X	58	X	X	X	59	X	X	X	60	X	X
3	76	76	76	77	77	77	78	78	78	79	79	79
3	X	X	77	X	X	78	X	X	79	X	X	80
4	94	94	95	95	95	96	96	97	97	98	98	98
4	95	95	96	96	96	97	97	98	98	99	99	99
4	96	96	97	97	97	98	98	99	99	100	100	100
4	X	X	X	X	98	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 21

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	39	39	39	40	40	40	40	40	40	41	41	41
1	40	40	40	41	41	41	41	41	41	42	42	42
1	X	41	41	X	X	X	X	42	42	X	X	X
2	59	59	60	60	60	60	61	61	61	61	62	62
2	60	60	61	61	61	61	62	62	62	62	63	63
2	X	61	X	X	X	62	X	X	X	63	X	X
3	80	80	80	81	81	81	82	82	82	83	83	83
3	X	X	81	X	X	82	X	X	83	X	X	84
4	99	99	100	100	100	101	101	102	102	103	103	103
4	100	100	101	101	101	102	102	103	103	104	104	104
4	101	101	102	102	102	103	103	104	104	105	105	105
4	X	X	X	X	103	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 22

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	41	41	41	42	42	42	42	42	42	43	43	43
1	42	42	42	43	43	43	43	43	43	44	44	44
1	X	43	43	X	X	X	X	44	44	X	X	X
2	62	62	63	63	63	63	64	64	64	64	65	65
2	63	63	64	64	64	64	65	65	65	65	66	66
2	X	64	X	X	X	65	X	X	X	66	X	X
3	84	84	84	85	85	85	86	86	86	87	87	87
3	X	X	85	X	X	86	X	X	87	X	X	88
4	104	104	105	105	105	106	106	107	107	108	108	108
4	105	105	106	106	106	107	107	108	108	109	109	109
4	106	106	107	107	107	108	108	109	109	110	110	110
4	X	X	X	X	108	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 23

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	43	43	43	44	44	44	44	44	44	45	45	45
1	44	44	44	45	45	45	45	45	45	46	46	46
1	X	45	45	X	X	X	X	46	46	X	X	X
2	65	65	66	66	66	66	67	67	67	67	68	68
2	66	66	67	67	67	67	68	68	68	68	69	69
2	X	67	X	X	X	68	X	X	X	69	X	X
3	88	88	88	89	89	89	90	90	90	91	91	91
3	X	X	89	X	X	90	X	X	91	X	X	92
4	109	109	110	110	110	111	111	112	112	113	113	113
4	110	110	111	111	111	112	112	113	113	114	114	114
4	111	111	112	112	112	113	113	114	114	115	115	115
4	X	X	X	X	113	X	X	X	X	X	X	X

Linker chip Finder Map, Board No. 24

Layer	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
1	45	45	45	46	46	46	46	46	46	47	47	47
1	46	46	46	47	47	47	47	47	47	0	0	0
1	X	47	47	X	X	X	X	0	0	X	X	X
2	68	68	69	69	69	69	70	70	70	70	71	71
2	69	69	70	70	70	70	71	71	71	71	0	0
2	X	70	X	X	X	71	X	X	X	0	X	X
3	92	92	92	93	93	93	94	94	94	95	95	95
3	X	X	93	X	X	94	X	X	95	X	X	0
4	114	114	115	115	115	116	116	117	117	118	118	118
4	115	115	116	116	116	117	117	118	118	119	119	119
4	116	116	117	117	117	118	118	119	119	0	0	0
4	X	X	X	X	118	X	X	X	X	X	X	X

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