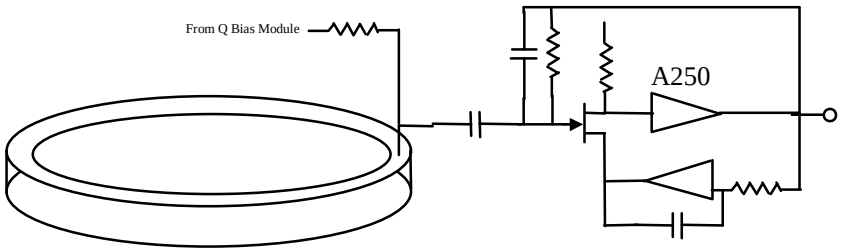
Created 1/29/98
Revised 11/23/98
Merle Haldeman

This file is located on the CO-OP PC (Merle-co-op)\\ D:\Cdms\Qamps\Qamp – A250\
qampA250_usr_man.doc

General Module Description

The **Q Amp Module** is used in conjunction with the front-end FET, to convert charge collected from the detector to a voltage which ultimately gets sent to the data acquisition system for digitization. The detector has a disk shape, approximately 7.5 centimeters(cm) in diameter, and 1cm thick. The Charge-collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.



A separate, individually controlled, DC bias voltage is provided for each of these two Charge-collecting electrodes, on the detector, by the **Q Bias Module.** The detector charge from each of these two Charge-collecting electrodes, is AC coupled to the two JFET-Gates through DC Bias blocking capacitors. Because the JFET-Gate is very sensitive to charge, it is important to minimize the noise charge at this node.

Charge on a capacitor is proportional to both capacitance and voltage; $Q = C * V$. The stray capacitance at the JFET-Gate to it's surroundings is difficult to control. Mechanical vibrations (microphonics), cause variations in the stray capacitance which produce corresponding variations in charge in the stray capacitance. The smaller we make the stray capacitance voltage, the smaller will be the variations in Q for a given variation in C_{stray} . Reducing V to zero would obviously make Q zero, and thus independent of variations in C_{stray}.

The simplified theory of operation of the Q Amp, is as follows. There are two feedback loops at work in this module, as illustrated above; a fast one(the upper path in the illustration) and a slow one, each having an individual separate purpose. The slow loop, which drives the JFET-Source, serves the purpose of keeping the DC output of the A250 at zero volts. This is important because the A250 output has a DC connection to the JFET-Gate. The slow loop also keeps the JFET at the correct operating point when the JFET-Gate is at essentially zero volts with respect to ground. There may be other reasons for keeping the JFET-Gate at zero volts, but the most fundamental reason is to prevent charge from coupling into the input due to the physical motions of grounded portions of the detector enclosure, as mentioned above. If the JFET-Gate is at the same voltage as the enclosure, the voltage across the stray capacity is zero, and changes in the stray capacity will not result in a flow of charge through the stray capacitance.

The operation of the slow loop is as follows; let's assume the JFET-Gate is at ground voltage and the, JFET-Source is at some positive voltage with-respect-to(wrt) the JFET-Gate, say ¾ of a volt, and the drain is at about 3 volts.. The A250 has a zero voltage output when the JFET drain (connected to the A250 input) is approximately +3 volts. Since the A250 is a non-inverting amplifier, an increase in the JFET-Drain voltage produces a positive voltage at the output of the A250. This positive output at the input of the, long time-constant, inverting, integrator begins driving the JFET-Source in a more negative direction, causing a larger current flow in the JFET and thus a decrease in the JFET-Drain voltage,

opposing the original increase. Thus the integrator's task is to keep the DC output of the A250 at zero volts.

The fast loop also keeps the JFET-Gate near zero volts by neutralizing the charge injected into the gate node by the detector through the JFET-Gate, DC blocking capacitor, situated between the Detector and the JFET-Gate. This neutralizing charge is supplied from the output of the A250 through a parallel combination of Resistance and Capacitance which we call the "**Feedback Network**". The amplitude of the A250 output pulse is determined by the capacitance in the feedback network and the quantity of charge from the detector.

So both loops essentially function to keep the JFET-Gate near zero volts.

Supplied Voltages

Power Control Circuitry
This module utilizes the following voltages available at the backplane:

FE+15, FE-15 and +5D.

When the Driver Module is plugged in, the circuitry voltages remain off for a period of approximately 1.3 seconds, after which IC24, pin 5 goes high, turning Q3, Q4, Q5, and Q6, on, connects the + & - 15 volt supplies to the rest of the module circuitry. Simultaneous with IC24, pin 5 going high, is pin 6 going low , which turns Q1 on connecting 5 Volt supply to the rest of the Module. Approximately 300 milliseconds after application of the 5 volts to the rest of the circuitry, IC 25 terminates it's "power-on" reset level.