Part VIII

Preliminary External Electrical Interfaces

Chapter 47

Preliminary External Interfaces

All information Part V is preliminary. This information concerns the three interfaces: (1) SVT Readout Electronics–Trigger, (2) SVT Readout Electronics–DAQ, and (3) SVT–Controls. The information contained in this section must be considered by the Interface Groups and incorporated appropriately.

47.1 SVT – Hardware Controls

Last Updated: 15 June 1995

The overview of **STAR Controls** is given in **The STAR On-line Controls Requirements Document**. This specifies that the EPICS system will be used for **Controls**. The selection of the EPICS environment predefines the hardware configuration of the Control System. The EPICS system runs on a UNIX-based workstation connected to VME crates operating under VxWorks, a real-time operating system. A variety of EPICS—supported hardware exists for conventional monitoring and control.

The HDLC protocol was chosen as the protocol for the Controls requirements associated with the Readout Electronics, and a Slow Control Daughter Board (HDLC Mezzanine Card) has been designed [**The STAR TPC FEE HDLC Link**, by Paul Barale, Fred Bieser, James Hunter, Susanna Jacobson, Spencer Klein, Chuck McParland, June 22, 1995]. This Daughter Board receives HDLC packets via the EPICS system, extracts the actions required, and initiates actions via 16 data lines and 23 address lines.

A summary of monitoring and control functions required of Controls is tabulated below. The column **Number** refers to the number of independent parameters of the given type. It does not necessarily mean the number of physical channels that must be provided because multiplexing may occur for some of the parameters. For example, for the electronics carriers and readout electronics, all controls information passes serially through the 24 HDLC links associated with the readout electronics.

Location	Number	Function	Accuracy	Interface
Electronics Carrier	144	Water Temp	0.1°C	HDLC
-	144	Displacement	10 μm	HDLC
-	144	Voltage Sum	1%	HDLC
-	144	High Voltage	0.1%	HDLC
-	72	Carrier Temp	0.1°C	HDLC
Readout Electronics	24	Voltage Sum	1%	HDLC
-	24	Temperature	1.0°C	HDLC
-	24	Current 1	1%	HDLC
-	24	Current 2	1%	HDLC
-	24	Current 3	1%	HDLC
-	24	Current 4	1%	HDLC
-	24	Current 5	1%	HDLC
Low Voltage (+8 V)	24	Voltage	1%	Allen Bradley
-	24	Current	1%	Allen Bradley
-	24	Status (on/off)	-	Allen Bradley
-	24	Control (on/off)	-	Allen Bradley
-	24	Reset	-	Allen Bradley
Low Voltage (-8 V)	24	Voltage	1%	Allen Bradley
-	24	Current	1%	Allen Bradley
-	24	Status (on/off)	-	Allen Bradley
-	24	Control (on/off)	-	Allen Bradley
-	24	Reset	-	Allen Bradley
Low Voltage (-100 V)	24	Voltage	1%	Allen Bradley
-	24	Current	1%	Allen Bradley
-	24	Status (on/off)	-	Allen Bradley
-	24	Control (on/off)	-	Allen Bradley
-	24	Reset	-	Allen Bradley
High Voltage (-2000 V)	72	Voltage	1%	LeCroy1440/1131
-	72	Current	1%	LeCroy1440/1131
-	72	Status (on/off)	-	LeCroy1440/1131
-	72	Control (up/down)	-	LeCroy1440/1131
-	72	Control (on/off)	-	LeCroy1440/1131
-	24	Reset	-	LeCroy1440/1131
Calibration Pulser	1	Control (on/off)	-	TBD
-	1	DC level	1%	TBD
-	1	Channel Mask	2 byte word	TBD
Air Conditioning	1	Control (on/off)	-	TBD

-	1	Setpoint	-	TBD
-	2	Temperature	1°C	TBD
-	1	Flowmeter	1%	TBD
-	1	Humidity	1%	TBD
Water System	1	Control (on/off)	-	TBD
-	1	Setpoint	-	TBD
-	4	Temperature	1°C	TBD
-	1	Flowmeter	1%	TBD
Position Monitor	144	TBD	-	TBD

47.1.1 EPICS

Requirement:
A VME crate with a Motorola 68040 processor. The crate must be located in the SVT racks area. The VME crate must be networked with similar systems for the other subsystems via ethernet. A SUN workstation, dedicated to the SVT, must be on the same subnet.

Note: The crate will contain other commercial interfaces to VME [e.g., Allen Bradley systems, LeCroy 1131, RS232, and GPIB].

Justification:
These hardware components are required becuase of the choice of the EPICS system and the decision to use HDLC between the readout electronics and Controls.

47.1.2 HDLC

Requirement:
An HDLC Controls interface (Controls HDLC Daughter Board) on each (24 total) SVT readout electronics' Power and Timing board. A total of 24 HDLC to VME interfaces are required in the SVT EPICS VME crate.

Justification:
An HDLC Controls interface on each readout electronics (24 total) must provide a path to Controls for readout of monitor data from the SVT and from the readout electronics. These data are associated with temperatures, voltages, currents, and positions. There are a total of 144 Carrier Interfaces, each of which has monitors for water temperature, control voltage (summed), high voltage, and relative position. In addition, each end of each ladder (72 total) will have a thermistor near the

carrier. Located on each of the 24 Readout Electronics stations will be monitors for temperature (1), Voltage (sum) (1), and currents (5).

Also, the HDLC Controls interface on each readout electronics (24 total) must provide a path to/from Controls for configuring the fixed part of the event header, selecting operation modes, and to provide an alternate data path for data acquisition and to provide a path for test data input.

47.1.3 Conventional Interfaces

Requirement:
EPICS supported Controls interfaces for monitor and/or control of all high voltage power supplies, low voltage power supplies, the water cooling system, the air cooling system, the air dehumidifier, the calibration system (pulser electronics), and SVT position monitoring system. For the power supplies essential functions to be included in Controls include: status (on/off), control (on/off), reset, voltage monitor(s), current monitor(s).

Justification:
All high/low voltage power supplies should be monitored to insure that they are operating properly. It should also be possible to check the status of the power supplies and to control the power supplies via slow control. Located in the Readout Electronics are power conditioners for generating the voltages required by both the Readout Electronics and the Carrier Interfaces. These voltages will be generated from (24) $\pm$ 8 VDC power supplied from the SVT racks. In addition, each (24) Readout Electronics will contain power conditioners for generating the shaping and focusing voltages required by the SDDs. These voltages will be generated from (24) -100 V power supplied from the SVT racks.

Each end of each ladder (72) receives high voltage from supplies (72) located in the SVT racks.

The Controls interface will be used to control a Pulser System for SDD calibration. The Pulser System will interface to the VME crate (method to be determined) and it will be controlled through the HDLC link between the Readout Electronics and Controls.

The Air Conditioning System and Water System most likely will be commercially designed and constructed turn-key systems for which Controls will dictate on/off control, issue setpoints, and provide independent monitors such as temperature, flow, and humidity.

The Position Monitor will monitor absolute position of the SVT with respect to the STAR coordinate system. This system is not designed yet, but it is expected that about 4 monitors/ladder (144 total) will be required. These lines will be routed with the cables to the readout electronics but will go directly to the position monitor electronics and then to a Controls interface.

47.1.4 HDLC Interface to EPICS

The HDLC link developed for the TPC Front End Electronics will also be used by the SVT Readout Electronics for the Readout Electronics – Slow Controls Interface. Details are provided in the document: **The STAR TPC FEE HDLC Link**, by Paul Barale, Fred Bieser, James Hunter, Susanna Jacobson, Spencer Klein, and Chuck McParland, 22 June, 1995.

The SVT readout electronics will have a 10 pin IDC connector on the PTB board to interface to the Controls system. The PTB routs these signals to the P2 connector of the Slow Control daughter board on the PTB. The interface connections are:

HDLC	S4 pin	SC-DB P2 pin Signal
1	32	RO+ (in)
2	33	RO- (in)
3	34	TD+ (in)
4	35	TD- (in)
5&7	36	CLK+(out)
6&8	37	CLK-(out)
9	NC	NC
10	NC	NC

Terminating resistors of 110 ohms are connected between pins 1 and 2 and 3 and 4.

47.1.5 Slow Control on RO Board

Given here is a discussion of what is being done for the SVT Prototype Readout Electronics to be used in the System Test Run. The Specifications will change based on what is learned from the Prototype.

The SC-DB interface to the RO electronics is memory mapped to 16 bit data, 24 bit address and two of the four pre-decoded strobes from the MC68302. PTB board uses strobe (2) and AMB boards use strobe (3) and address bits 1-4 and 16-21 to interface to control and status registers and to provide control functions on PTB and AMB through their ALTERA PLDs.

Slow control can read an 8 bit ID code gated from connector S2 on PTB.

Slow control can read 8 monitor channels from two 4 channel ADCs. A strobe ADC 1 or 2 is issued as a write address xxxxx. After 100 μs the data are read with four reads from address xxxxx and four reads from address xxxxx. Four of the channels are used for temperature input from remote AD590 temperature sensors through connector S2 on PTB. 8 pins are used for floating twisted pair connection. The other four channels are used (1) for on board temperature and (3) combinations of onboard supply voltages.

Slow control can read or write data to the 128k $\times$ 40 bit memory on either AMB by using a 40 bit of registered transceivers and an incrementing memory address reqister in the AMB Altera PLD. The 40 bits are addressed as 00-15, 16-31, and 32-39 with three reads or writes to addresses xxxxx0-2. Data is transferred between memory and the register with reads and writes to xxxxx. Addresses xxxxx write to the address counter. The Analog read and Optical out counters have reloadable 8 bit registers for bits 11-17 which are loaded by writing to addresses xxxxx and xxxxx.

Slow control will put static information in the header space of the memory during set up.

47.1.6 SVT High Voltage

A LeCroy 1131 VME-to-SIB Interface will be used to interface a LeCroy 1440 high voltage power supply which provides 72 high voltage lines to the SVT. Operating voltage will be less than -2000 V. The developoment of an EPICS driver for the 1131 module is required. Controls must allow turn on, turn off, reset, standby, read status of supply, set voltages, read voltages, and read currents. The 1440 is a multichannel, programmable high voltage system. The 1131 VME-to-SIB Interface is a VME module that connects the 1440 to the VME crate. SIB is a LeCroy Systems Interface Bus, a 16-bit wide parallel I/O bus with handshake.

47.1.7 SVT Low Voltage

The Controls interface to the (24) $\pm$ -8 VDC, and (24) -100 V low voltage power supplies will utilize commercially available Allen Bradley systems. The SVT will use the same system as used for the TPC low voltage supplies.

47.1.8 Calibration Pulser

To be specified

47.1.9 Air Conditioning

To be specified

47.1.10 Water System

To be specified

47.1.11 Air Conditioning

To be specified

47.1.12 Position Monitor

To be specified

47.2 Readout Electronics–Trigger

Last Updated: date
Last Updated: 15 June 1995

Preliminary STAR specific Readout Electronics –Trigger requirements are specified in the document **Trigger → Front-End Electronics Interface Specification** *Trigger/Clock Distribution Tree*, by V. Lindenstruth, P. Barale, R. Bellwied, F. Bieser, B. Bonner, M. Botlo, J. Cannon, H. Crawford, L. Greiner, J. Hoffmann, R. Jared, S. Klein, M. LeVine, T. Noggle, J. Schambach, and D. Underwood, 3 February 1995. Much of the material in this section has been taken from that document and reworded or changed as necessary to serve as preliminary specifications for the SVT Readout Electronics–Trigger interface.

47.2.1 Clock Distribution

Requirement:
Distribute the RHIC strobe to the SVT Readout Electronics. Allow to compensate for different propagation delays up to 100 ns in steps of 1 ns. The timing jitter with respect to the RHIC strobe input to the trigger distribution tree is limited to 1ns RMS.

Justification:
The RHIC strobe (110 ns clock period) defines the interaction time and is the heart beat of the whole detector. It will be used as timing reference for any state transitions in the SVT.

Three parameters are relevant for the SVT trigger/clock distribution tree:

- phase: average phase difference due to different propagation delays and cable lengths at the end points of the trigger/clock distribution tree, the readout boards.
- coherent jitter: the phase of all trigger/clock distribution receivers varies in phase with respect to the RHIC strobe on an event-by-event basis.
- incoherent jitter: the phase of all trigger /clock distribution receivers varies with respect to each other within an event. This number defines the timing resolution possible with signals derived from the trigger/clock distribution tree.

The maximum acceptable phase is 1 ns, the maximum jitter (coherent and incoherent) is 1 ns.

Note: The trigger/clock distribution tree logic will support both multi drop and point to point cabling scenarios. However in the case of a multi drop scenario it may not be possible, for example, due to cable delays, to adjust the relative phase of the various trigger/clock receivers down to 1 ns.

47.2.2 Trigger Command Word

Requirement:
Distribute a global 4 bit trigger command word to the SVT.

Justification:
Each Readout Board needs to know if for a given RHIC strobe certain actions are required. Generally the number of bits needed to be communicated per trigger or abort should be kept as small as possible because it corresponds to either transmission speed or the number of signals of the trigger distribution cable. Both affect the cost of the system. Sixteen different trigger commands are sufficient. This allows to encode them in a 4 bit binary word. To define a good timing reference these trigger command words must be sampled at the rising edge of the RHIC clock.

Note: There are three classes of Trigger Command Words.

- Commands that are not readout related
- Commands that are readout related and require an event to be produced in the front-end
- Commands that are readout related and accompanied by a valid trigger token but that do not result in any readout.

The first group are commands that have to be distributed synchronously to the RHIC strobe and are not related to readout. These commands are broadcast to the detectors. The trigger token and DAQ command word that will be distributed together with these trigger command words will be forced to zero. These commands will be distributed independent of the busy status of the detector.

The second group requires Trigger to produce and reserve a unique trigger token different from zero that is distributed together with the Trigger Command. Depending on the Trigger Command it also has to inform DAQ about the event as specified in the Trigger-DAQ interface.

The meaning of the different trigger commands for the SVT is as follows:

Group 1 Trigger Commands:

[0:] no-trigger

- This is the default symbol that will be transferred in the case of an idle link.

[1:] clear

- This command clears redundancy counters on the readout boards. The readout boards will have redundant counters counting the RHIC strobe. The value of these counters will be shipped together with the raw data allowing cross checks that each system received exactly the same number of clock pulses.

[2:] master-reset

- This command will perform a general reset of the whole front-end logic.

[3:] spare

- reserved

Group 2 Trigger Commands:

[4+n:] triggern

- There are four trigger commands available allowing four different kinds of readout in the front-end.

[4:] trigger0

- This is the default physics readout and has to be supported by all detector systems. This trigger results in physics readout.

[5:] trigger1

- reserved - executed as trigger0

[6:] trigger2

- reserved - executed as trigger0

[7:] trigger3

- executed as trigger0 but copy event also into local buffer

[8+n] pulsern

- There are four different test strobe commands available that will be used to fire test pulses for calibration and monitoring purposes.

  Note: The test pulse command produced by Trigger may be intercepted by the trigger/clock Driver module and result in a sequence of test pulse commands. This test pulse sequence will be protected by the detector dead time signal which will be asserted by the trigger/clock Driver module while performing that sequence. The trigger/clock Receiver modules can easily disendtangle a pulser command that shall just fire the specified pulser and the final test pulse command that requires also the read-out since only the latter will be accompanied by a non zero trigger token.

[8:] **pulser0**

- electrical pulser - calibration pulser

[9:] **pulser1**

- electronics test pulser

[10:] **pulser2**

- reserved - ignored

[11:] **pulser3**

- buffered readout - reproduce event stored by trigger3 command or by controls

[12:] **config**

- This is a house keeping trigger. It has to be supported by all detector systems and returns geographic information of the front-end boards allowing automatic configuration of the experiment.

Group 3 Trigger Commands

[13:] **abort**

- This command aborts and clears an active event. Which event must be cleared is defined with the accompanying unique trigger token.

[14:] **L1accept**

- This command informs the front-end that there was a level one (L1) accept of the event identified by the trigger token. It is usefull for detectors that perform level two (L2) analysis on their data. The L1 accept would define the event to be available for this L2 analysis preventing the L2 processors from wasting time on events that will be cleared by the trigger L1 logic. L1accept commands are always sent in the same order as the corresponding triggers were issued.

[15:] L2accept

- This command informs the front-end that the event identified with the trigger token was accepted by the trigger system and that DAQ was informed about the existence of that event. Fast detectors like EMC and TOF use this command to start the transmission of the event to DAQ. After receipt of a L2accept command aborts for that event are impossible. L2accept commands may be issued in any order.

47.2.2.1 Trigger Token

Requirement:
Generate a unique 12-bit trigger token for every trigger and distribute it with each trigger, accept and abort command.

Justification:
The STAR detector system will consist of many independent detector systems, which will have their individual dead time. Any combination of detectors is possible for coincident triggers. The readout time of the various systems varies greatly. Therefore it is possible that during the conversion of one detector another detector is already live and ready to take more data. The STAR trigger system supports to fire triggers to fast detectors even if their previously coincident event with a slow detector is still being processed. Therefore it is very important to have a mechanism that allows to uniquely identify to which event and detector any data buffer belongs. In order to uniquely identify a data buffer with a given event the trigger system will distribute a unique trigger token together with the trigger command itself. The L1/L2accept and abort commands identify the event with the trigger token as well.

One way to make the trigger token unique is to use enough bits to make sure that the same trigger token will never be used again. For example a 64 bit bunch crossing number would be a good example. However cost considerations require the number of bits transferred per trigger to be as small as possible. Another approach is to make sure that the same trigger token is not used again until the event is assembled. In this scenario the number of bits required for the trigger token is defined by the maximum number of outstanding triggers that are allowed by the data acquisition system. An upper limit for this number is defined by the highest accepted DAQ trigger rate (1000/sec) and the maximum DAQ latency (2s). Correspondingly a 12 bit trigger token would be sufficient. The trigger system will reuse a trigger token only if the corresponding event was readout and assembled by DAQ and the appropriate trigger structures were cleared by DAQ in the Trigger-DAQ interface (refer to the Trigger-DAQ interface specification).

47.2.2.2 DAQ Command Word

Requirement:
Distribute for every trigger a global 4 bit DAQ command word to all DAQ front end systems of all coincident detectors of a given event.

Justification:
There are event attributes that require the same handling on the front-end electronics level but different handling of the raw data on the DAQ front-end level. For example normal events and baseline events or scale-down events, that have to bypass the L3 filter, would all require exactly the same handling on the readout boards. However their handling on the receiver boards would be significantly different. Of course, it would be possible to fetch this information that is available in the Trigger-DAQ interface and distribute it to all DAQ front-end systems for each event. But considering that there will be 144 receiver boards for the TPC and 24 receiver boards for the SVT, this seems to be a clumsy approach. A much cleaner approach would be to distribute a descriptive bit pattern to DAQ together with the data that allows to disentangle different handling procedures in the front-end.

Four bits or 16 different commands are sufficient. The same DAQ command word is distributed to all coincident detectors.

Note: The DAQ Command Word will be produced together with the Trigger Command word in the trigger action word lookup table within the TCU.

47.2.2.3 Maximum Trigger Distribution Dead Time

Requirement:
The maximum time to distribute a complete trigger command is 5 RHIC strobes.

Justification:
The time required to distribute a trigger or clear command affects the dead time and correspondingly the detector performance. It defines also the minimum time between two successive trigger pulse commands. There detector system in STAR that requires triggers or test strobes faster than 5 RHIC strobes back-to-back.

47.2.3 Physical Signal Distribution

Requirement:
The physical trigger/clock signals are:

- differential, copper
- maximum cable length 30 m
- maximum ground potential difference (common mode suppression) 1 V
- highest frequency distributed: five times RHIC clock

Justification:
Given the number of trigger/clock distribution tree end nodes of about 1000 and given the moderate distance and clock rate a fiber optics based system could not be justified. The AC requirements need to be specified to allow the design of the trigger/clock distribution tree.

47.2.4 Accept Front-End Electronics Busy and DAQ Busy

Requirement:
Accept one individual busy signal from each detectors front-end electronics and one corresponding DAQ front-end busy (no common dead time). Support optional BUSY return from the end nodes of the Trigger/Clock distribution tree.

Justification:
STAR does not have a common dead time. There is dead time created by the front-end electronics during digitization of an event or while clearing an event. Another source of dead time is the DAQ front-end if all available elasticity buffers are allocated. The trigger control unit will use the logical OR of these signals of a given detector as the detector busy input and if asserted prohibit any further triggers to the given detector.

Some detectors like EMC may perform data compression at the readout module level. Therefore there may be a need for producing a BUSY signal to protect buffers from overflowing. All BUSY signals of the readout modules will be logically ORed in the Trigger/Clock distribution tree. In this scenario a slow controls interface is required to allow checking of the BUSY status of every board for maintenance.

47.2.5 Special Trigger Requests

Requirement:

Accept level sensitive special trigger requests as L0 requests. The latency between a L0 trigger request and the issue or reject of the given request has to be deterministic.

Justification:
Special or maintenance triggers such as pulser triggers have to be implemented so that they can be requested by a given detector.

47.2.6 Timing

Requirement:
Trigger must inform SVT of an event within 3 microseconds of the interaction.

Justification:
The SVT scrolls data onto an SCA which holds 4.5 microseconds of data. It takes some time to swatch the Readout System from aquire to digitize.

47.2.7 Trigger/Clock Distribution Tree

Figure 8 shows a sketch of the trigger/clock distribution tree as it is currently envisioned.

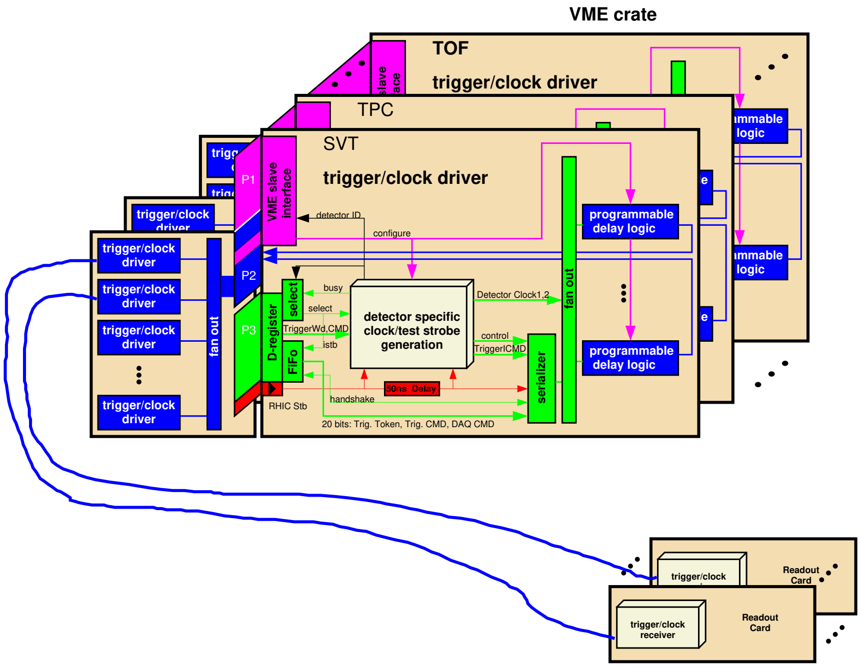

Figure 47.1: The major components of the trigger/clock distribution tree

There will be root driver modules for each individual detector. All root modules will sit in a VME crate and receive the 96 trigger bits and the RHIC strobe from the back plane. Each trigger root module will have a detector specific section that allows to customize the detector specific clock signals that must be distributed, and to add any detector calibration logic necessary to provide for calibration sequencing. The trigger distribution tree will be implemented as point-to-point connections with length adjusted cables due to the strong requirement of the clock phase. Therefore, there are 12 trigger/clock distribution cables per detector end cap of STAR going to the SVT readout systems, for a total of 24 cables.

It is planned to distribute additional SVT specific clock signals through these cables to the readout systems. This makes the system design very simple since these clocks will be produced at one well defined place and distributed to the front-end through the trigger clock distribution tree. These two clocks are used to drive the SCA's in the front-end, with one of the clocks running at the acquistion frequency (3 $\times$ RHIC clock), and the other clock running at the readout frequency (3/8 $\times$ RHIC clock).

47.2.8 Trigger/Clock Receiving Interface

The trigger/clock distribution tree will have 10 signal pairs as follows:

1	RHIC strobe
2...5	4 bit data word
6	data clock (2.5$\times$RHICclk; double edge transmission)
7	detector clock 1
8	detector clock 2
9	BUSY
10	STATUS

The first 8 signal pairs are PMECL signals sourced by the clock/trigger distribution system and should be received using AT&T receiver chips type 41MF with 110 ohms across each pair at the end of the cable. The "busy" and "status" pairs may be used to send "slow" signals back to the clock/trigger distribution system thru the use of optically coupled open-collector buffers.

There are five 4-bit entities that have to be distributed for each trigger (trigger CMD, DAQ CMD, Trigger token (12 bits)). Running the 4-bit word clock at 5 times the RHIC clock rate which is well within the capabilities of the distribution tree it is possible to distribute the full trigger information within one RHIC strobe. Consequently the trigger/clock distribution tree would be dead time free. The two last optional signals (BUSY and STATUS) are returned as wired OR to the Trigger/Clock driver Module.

The actual 4 bit word sequence within one RHIC strobe period is sketched in Figure 9.

The corresponding signals are underlined in light grey. The rising edge (dark) of the RHIC strobe defines the timing reference. The Trigger command is the most important word and needs to be available at the trigger time (rising edge of RHIC strobe). Consequently it is distributed first. The other words follow and are buffered in the trigger/clock receiver.

The actual logic of the trigger/clock receiver will be implemented in programmable logic in the readout system. Figure 10 shows a sketch how this will be implemented.

The programmable logic will essentially implement a FiFo to buffer the TriggerCMD, DAQ CMD and Trigger Token. This FiFo will have an 8 bit output allowing the data to be read out exactly in the header format as required by the fiber interface specification. The FiFo output has an individual output enable to allow the receiver module to be connected to a global data bus. The Trigger CMD always will be driven and guaranteed to have a stable value at the rising edge of the RHIC strobe.

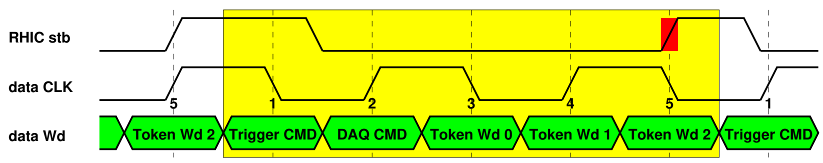

Figure 47.2: The word sequence within one RHIC strobe period

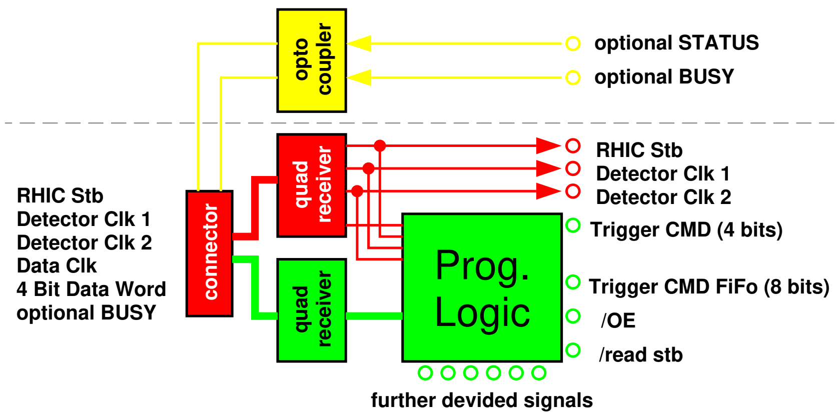

Figure 47.3: The components of the trigger/clock receiver logic

47.2.9 Trigger/Clock Driver Module

The trigger/clock driver module is the root of the trigger/clock distribution tree. Its major components are sketched in Figure 8. The trigger/clock driver module will be implemented as a 9U VME board. The use of this widely accepted standard bus allows easy configuration access using only standard components and interface chips. The trigger/clock Driver Module will be identical for all detector systems. However it will host a detector specific section that implements all the detector specific logic required to produce the clock signals and calibration trigger command sequences.

Therefore there are four major components on the trigger/clock Driver Module: the VME slave interface, the trigger decode logic, the detector specific trigger/clock generation section and the delay logic. The VME slave interface allows configuration of all parameters and CSR registers of the board. All resources will be memory mapped into the sub-address space of the trigger/clock Driver Module. The decode logic defines if a given trigger command includes the given detector. The most important component of the trigger/clock Driver Module is the detector specific section. It generates the detector specific clock signals and the special command sequences. The output of this section is serialized and forwarded to the fan-out modules. These 6U modules will be plugged in at the back side of the P2/P3 back plane. The signals of the P2 VSB bus will be used for passing through the trigger/clock signals. There are two sets of programmable delay line units. The actual delay used will be selected by writing to a CSR register.

47.2.10 Trigger Back-Plane

The P3 bus of the trigger/clock Driver Module will be used to distribute the actual Trigger L0 TCU output signals (Trigger backplane). The logical signal groups distributed at the trigger back plane are:

1	(1)	I	RHIC strobe
2	(8)	O	individual detector BUSY (one bit per detector, open collector, low active)
3	(8)	I	coincidence detectors (one bit per detector)
4	(4)	I	Trigger Command
5	(4)	I	DAQ Command
6	(12)	I	Trigger Token
7	(16)	I	Trigger Word

Note: Items 3 through 5 form the 16 bit Trigger Action Word.

All signals are latched with the rising edge of the RHIC strobe. The setup time is 10 ns and the hold time is 5 ns.

The individual detector busy signals are required for special trigger generation. The time required to process a special trigger command is not deterministic, it may result in several special triggers to be sent to the front-end. Therefore the special trigger sequencer on the trigger/clock detector specific mezzanine board has to be able to assert the detector specific dead time signal.

The Trigger Action Word is split into three logical fields as indicated in the above table. Each detector (up to eight) has its own bit indicating if it is involved in the given trigger command. The trigger command and DAQ command are global for any given event.

The trigger token is distributed in case of a trigger command that results in a read-out.

The Trigger Word is the 16 bit field that caused the trigger to be fired for the actual bunch crossing.

There has to be a back-plane that distributes these trigger signals. Most elegant would be the use of an existing back-plane avoiding the need of the design of a private back-plane. It is possible to use VME P1 for this purpose. The P3 signal-pin assignment of the Trigger back plane is shown below.

VME-P3 pin assignment of the Trigger back plane:

pin	signal(P3)	(P1)	pin	signal(P3)	(P1)
A10	RHIC_STB	SYSCLK			
A01	TRG_EMC	D00	B30	BSY_EMC	RQ1
A02	TRG_SVT	D01	B29	BSY_SVT	IRQ2
A03	TRG_TOF	D02	B28	BSY_TOF	IRQ3
A04	TRG_TPC	D03	B27	BSY_TPC	IRQ4
A05	TRG_XTPC	D04	B26	BSY_XTPC	IRQ5
A06	TRG_spare	D05	B25	BSY_spare	IRQ6
A07	TRG_spare	D06	B24	BSY_spare	IRQ7
A08	TRG_spare	D07	A20	BSY_spare	IACK
A25	TRG_CMD[0]	A06	C16	DAQ_CMD[0]	AM0
C25	TRG_CMD[1]	A13	C17	DAQ_CMD[1]	AM1
A24	TRG_CMD[2]	A07	C18	DAQ_CMD[2]	AM2
C24	TRG_CMD[3]	A14	C19	DAQ_CMD[3]	AM3
A30	TRG_TOKEN[0]	A01	C30	TRG_TOKEN[6]	A08
A29	TRG_TOKEN[1]	A02	C29	TRG_TOKEN[7]	A09
A28	TRG_TOKEN[2]	A03	C28	TRG_TOKEN[8]	A10
A27	TRG_TOKEN[3]	A04	C27	TRG_TOKEN[9]	A11
A26	TRG_TOKEN[4]	A05	C26	TRG_TOKEN[10]	A12
A25	TRG_TOKEN[5]	A06	C25	TRG_TOKEN[11]	A13
C23	TRG_WORD[0]	A15	C01	TRG_WORD[8]	D08
C22	TRG_WORD[1]	A16	C02	TRG_WORD[9]	D09
C21	TRG_WORD[2]	A17	C03	TRG_WORD[10]	D10
C20	TRG_WORD[3]	A18	C04	TRG_WORD[11]	D11
C19	TRG_WORD[4]	A19	C05	TRG_WORD[12]	D12
C18	TRG_WORD[5]	A20	C06	TRG_WORD[13]	D13
C17	TRG_WORD[6]	A21	C07	TRG_WORD[14]	D14
C16	TRG_WORD[7]	A22	C08	TRG_WORD[15]	D15

47.2.11 The Trigger/Clock SVT Section

This section of the Trigger/Clock distribution board is responsible for the generation of the appropriate readout sequences in response to a trigger command

and for the generation of the 2 SCA clocks (acquisition and readout clock). A programmable logic device will be used to accomplish these tasks.

47.2.12 The Trigger/Clock Fan-Out Back-Plane

The Trigger/Clock output of the programmable delay units will be fed through fan-out boards, which will be mounted from the back side of the 9U VME crate. The P2 VSB back-plane signals will be used for that purpose. All signals at this back-plane are 5V TTL signals. The choice of the VSB back-plane standard allows the use of this back-plane for more than one fan-out module per Trigger/Clock driver module (the SVT needs 4 fan-out modules, since each fan-out can drive 6 readout systems). The VSB back-plane will be mounted at the back side of the VME P2 back-plane. The pin definition of the Trigger/Clock VSB back-plane is defined below.

VME-P2 pin assignment of the Trigger/Clock fan-out

pin	signal (P3)	(VSB)	pin	signal (P3)	(VSB)
A01	C0RHIC	AD00	C01	C1RHIC	AD01
A02	C0D0	AD02	C02	C1D0	AD03
A03	C0D1	AD04	C03	C1D1	AD05
A04	C0D2	AD06	C04	C1D2	AD07
A05	C0D3	AD08	C05	C1D3	AD09
A06	C0DCLK	AD10	C06	C1DCLK	AD11
A07	C0CLK1	AD12	C07	C1CLK1	AD13
A08	C0CLK2	AD14	C08	C1CLK2	AD15
C28	C0BUSY	ASACK0	C27	C1BUSY	ASACK1
A32	C0STATUS	BREQ	C31	C1STATUS	BUSY
A09	C2RHIC	AD16	C09	C3RHIC	AD17
A10	C2D0	AD18	C10	C3D0	AD19
A11	C2D1	AD20	C11	C3D1	AD21
A12	C2D2	AD22	C12	C3D2	AD23
A13	C2D3	AD24	C13	C3D3	AD25
A14	C2DCLK	AD26	C14	C3CLK	AD27
A15	C2CLK1	AD28	C15	C3CLK1	AD29
A16	C2CLK2	AD30	C16	C3CLK2	AD31
C25	C2BUSY	ACK	A24	C3BUSY	ERR
C29	C2STATUS	CACHE	C30	C3STATUS	WAIT

The back side of the 9U VME board will have card guides supporting the 6U fan-out modules. These modules will sit behind the VME P2 and P3 back-plane because the VME power supply is typically mounted behind the P1 back-plane.

The fan-out boards have to support hot insertion because all trigger/clock driver modules will be in one crate and a power cycle of that crate would affect the whole experiment. The connectors on the back side of the VME P2 or VSB back plane are of male type. Bent pins may cause shorts, which are dangerous especially if power pins are involved. Therefore the power of the VME P2 and VSB back-plane will be decoupled from the P1 and P3 back-plane. The Trigger/Clock drivers are allowed to use only power from the P1 and P3 back-plane. The Trigger/Clock fan-out boards use only the P2 power pins. The P2 back-plane will have an individual fuse that will prevent the back-plane from burning upon a power shortcut due to bent connector pins. This is possible because the fan-out boards will not need a lot of power.

There has to be a commercial module in the crate that allows initialization of the Trigger/Clock drivers. This module may use both the P1 and P2 power pins. Therefore there will be two slots in the Trigger/Clock crate where the P1 and P2 power pins are connected. This crate will have correspondingly a 2 slot and a 19 slot P2 back-plane. These back-planes will be connected except for the power pins forming a virtual 21-slot VME P1/P2 back-plane. Such back-planes bridges with decoupled power pins are commercially available.

47.3 Readout Electronics–Data Acquisition

Last Updated: 15 June 1995

STAR specific Readout Electronics –Data Acquisition requirements are specified in the document **Front–End Electronics ←→ DAQ Reciever Board Fiber Optics Specification Version 1.0**, by V. Lindenstruth, P. Barale, R. Bellwied, F. Bieser, B. Bonner, M. Botlo, J. Cannon, H. Crawford, L. Greiner, J. Hoffmann, R. Jared, S. Klein, M. LeVine, T. Noggle, J. Schambach, and D. Underwood, 28 January 1995. Much of the material in this section has been taken from that document and reworded or changed as necessary to serve as preliminary specifications for the SVT Readout Electronics–DAQ interface.

47.3.1 Bandwidth

Requirement:
Support enough bandwidth to send the uncompressed 10-bit raw data of the SVT readout boards within 10 ms to the DAQ receiver boards in the counting house.

Justification:
The transmission speed defines the dead time per event and consequently the detector performance. The TPC and SVT digitization time is 10 ms. The uncompressed raw data volume of one Au+Au event is:

(9 Si detectors per readout board)
$\times$ (480 channels per detector)
$\times$ (128 time buckets per channel)
$\times$ (10-bit ADC value per time bucket)
$= 553 \times 10^3$ words (10-bit)

Note: The SVT and the TPC intend to use the same cluster finder ASIC. To ensure compatibility the SVT has to send 16 padding channels per Hybrid (for a total of 256 channels $\times$ 128 time-buckets per channel). Therefore, the bandwidth has to be increased to 590×10^3 words (10 bit) per event.

47.3.2 Fiber Commands

Requirement:
The fiber link has to support the command sequence as sketched in Figure 11.

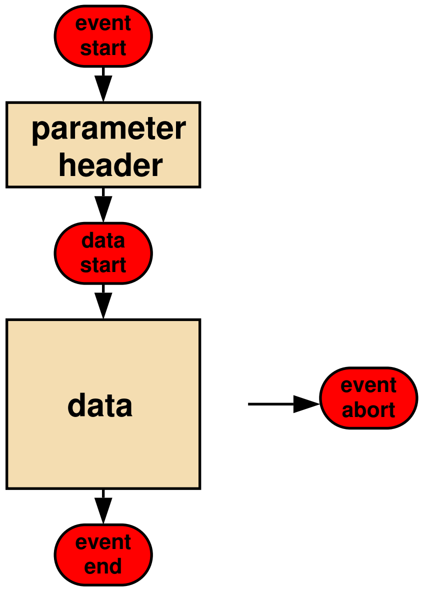

Figure 47.4: Sketch of the data format. The two data sections are encapsulated by command words

The four command codes (listed in brackets) follow:

[1] event-start

- This command starts the sequencer on the receiver boards. It will configure itself to be ready to accept the header data.

[2] data-start

- This command precedes the transmission of the raw data. If the sequencer on the receiver board detects this command before it receives exactly 64 header words, it will flag an appropriate sequencing error bit. During the raw data phase, event-abort commands are possible at any time.

[4] event-end

- This command defines the normal and complete transmission of an event. If the internal counters of the sequencer on the receiver board do not indicate that all header or data words have been received, then appropriate error bits have to be set indicating this sequencing error. Upon receipt of this command, the receiver boards will be busy for about 400 μs. After that time, the DAQ front-end busy will be released if there is at least another buffer available.

[8] event-abort

- An event may be aborted any time during the data phase. This command will be used for the SVT and TPC data transmissiion.

Justification:
Encapsulation of the header and data phase with command words to ensure data integrity and to steer the sequencer on the receiving end of the fiber link is very useful. Interrupting the transmission of the raw data at any time in case of a L1/L2 abort is also required.

Note: These command words are only intended to control the sequencer on the receiver board. They will not support any command transmission from the read-out board/trigger system to DAQ. The trigger command and DAQ command will be part of the header. Currently each command will be followed by the appropriate number of idles to make up for about 100 ns of wait states. The command sequence for the case of two aborted events followed by an accepted event would be: 1,2,8,1,2,8,1,2,4.

47.3.3 Header

Requirement:
Send fixed-length header information preceding the data such as the trigger/DAQ command, trigger token and status of the readout board, including local bunch crossing counters and geographic readout unit IDs. The length of the header is fixed for any detector and cannot exceed 512 bytes.

The first 16 words of the parameter header must comply with the format shown in Figure 12.

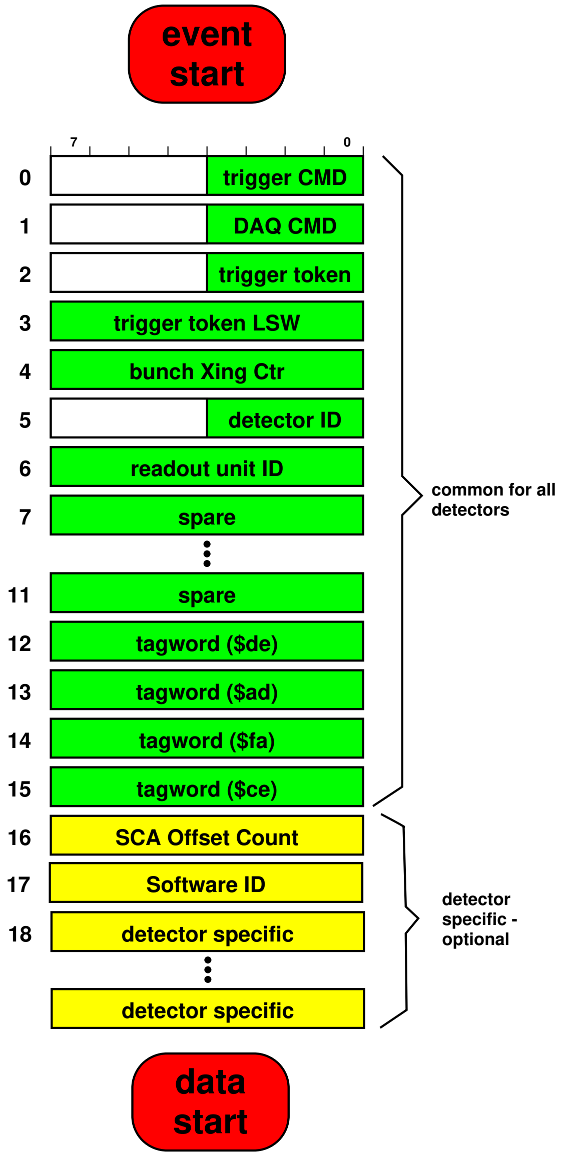

Figure 47.5: Layout of parameter header. The four tag words were implemented to have a redundancy check to insure that the header is transferred correctly. The number of valid bits in the readout unit ID field depends on the detector specified in the detector ID. Any insignificant leading bits have to be forced to zero in this data word. The number of significant bits for the SVT is 5.

Insert wait states depending on word clock rate to limit header word cycle time to a minimum of 30 ns.

Justification:
ID and maintenance information is required to accompany the raw data to allow identification of which detector and event the given buffer belongs. The trigger system will send a trigger command and a unique trigger token to each individual readout board. All readout boards will have a unique geographic ID that they send in the header together with the raw data. The readout boards will also count the bunch crossing number. This counter will ensure the integrity of the trigger distribution cabling. DAQ needs some handling information about the raw data buffer that may select different options in the code of the front end processors or L3. This information is distributed through the trigger tree together with the trigger command to all readout boards. They would forward that command to DAQ in the parameter header.

Currently there are two definitions for the detector specific data fields. The SCA offset count will be sent in word 16. Word 17 and 18 shall define 16-bits of program ID uniquely identifying the program version of the PLD source code on the readout board.

The header data may be stored in some extra memory or FiFo on the receiver cards. To reduce the implementation costs the cycle time of this header memory is defined not to exceed 30 ns. This will require one wait state for the TPC and SVT links running at about 60 MHz word rate (1.5 GBits/sec bit rate). Wait states may not be required if the fiber link is running at slower bit rates.

The detector ID for the SVT is defined to be "2".

47.3.4 Configuration Events

Requirement:
Support configuration events that define the mapping between physical detector channels, such as SDD and anode numbers and channels of the detector-daq interface. Only the lower 8 of the 10 data bits of each channel (high and low word of the 20-bit HP data bus) shall be valid during configuration events. The number of words transferred in the case of configuration events has to be exactly the same as in the case of the transmission of raw data.

Justification:
The concrete order of the channels transferred is detector specific. The mapping of channels of the readout board onto the SDD and anode numbers, depends on the geometric position of the readout board. However, this mapping will be fixed.

In order to determine the channel mapping, there will be special data formats responding to housekeeping triggers like the geographic readout. These events will contain ID information instead of raw data. This ID information defines which detector channels (ie., SDD and anode number) are mapped onto a given channel in the receiver board.

SVT raw data events comprise two 10-bit ADC values per 20-bit word. In the case of configuration events, only the lower 8-bits of the 10-bit word will be used. This restriction is required because SVT configuration events will be sent through the ASICs without pedestal correction and gain mapping. The back end bus of the ASIC is only 8-bits wide allowing the storage of only 8-bit values.

The number of words transmitted for configuration events will not differ from raw data to allow the same sequencer logic to handle both events. There are 128 configuration bytes (8-bit) per SDD anode in the case of an SVT configuration event. It is expected that only a very small fraction of that will be used.

47.3.5 Aborts

Requirement:
Support aborts during the data transmission due to aborts issued by the trigger system. These aborts are forwarded to DAQ on the fiber link.

Justification:
The trigger system may issue L1/L2 aborts any time up to 10 ms after a trigger command. In the case of slow detectors like the SVT aborts will (if at all) always happen before the event is completely transferred. Because the SVT readout boards will be located on the detector and hard to access and maintain, they shall be kept as simple as possible. There will be no elasticity buffers on the readout boards. They will send the data synchronously to the DAQ receiver boards as it is digitized using a state machine that is started with an incoming trigger request. Consequently aborts will have to be forwarded to the DAQ receiver boards.

47.3.6 ASIC Compatibility

Requirement:
The TPC and SVT raw data format has to be compatible with the final STAR ASIC implementation.

Justification:
The design of the STAR cluster-finder ASIC requires all channels of a given time bucket to arrive before the first channel of the next time bucket can be accepted. The number of channels per ASIC is fixed — 64 for the TPC mode and 256 for the SVT mode.

This requirement deals with the internal sequencer in the ASIC. Essentially, there is one slow running global time counter and a fast running channel counter. Every time the channel counter wraps, the time counter is incremented. Correspondingly, the readout board has to send all channels of a given time bucket before it can advance to send the next time bucket.

The ASIC does not have any elasticity input buffers. Therefore, it has to receive a data word every 150 ns in order to achieve 10 ms dead time in the case of the TPC (i.e., 1024 pixels times 64 channels per 10 ms). It cannot accept data at shorter time intervals than 150 ns. Strobing it slower would result in a dead time greater than 10 ms per event.

The header data mentioned earlier will bypass the ASIC.

All front-end electronics boards are required to send the same number of data words. Readout boards with fewer FEE channels shall zero fill the unused data channels. This allows one generic sequencer at both the readout and the receiver board.

In case of configuration events (trigger command 12...15), the raw data is restricted to having only 8 valid bits, because the buffers at the back-end of the ASIC are only 8-bits wide. Data words wider than 8-bits have to be split into several words. In order to use the same sequencer logic for raw data and configuration data, the configuration events shall have exactly the same size as a normal event. Therefore, there are 128 bytes of configuration data per SVT channel.

47.3.7 Wait States

Requirement:
Allow to insert padding or idle words after each command word and header word.

Allow to insert padding or idle words after each header word in order to limit the Header word rate.

Justification:
Both the sequencer on the readout and the receiver boards will need certain time to react to the various state changes of the system. For example, it may be required to delay the transmission of raw data after the parameter headers to give the sequencer on the DAQ receiver boards time to reconfigure for the data mode. The interface definition has to be able to accommodate this requirement.

Note: Currently, each command will be followed by the appropriate number of idles to make up for about 100 ns of wait states.

After each header data word, there has to be one wait state in fiber link to accommodate slow header buffers at the receiving end.

47.3.8 Channel Count

Requirement:
The number of raw data channels transferred from any readout board has to be fixed.

Justification:
All readout boards will send data as outlined earlier. The appropriate unused slots in the transmission sequence shall be filled with zeroes. (This is not a strong requirement because the front end processors can be programmed to ignore certain channels depending on some mapping that will be downloaded during the configuration phase.) This requirement for SVT and TPC allows exactly the same sequencer logic for both detectors on both the readout boards and receiver boards.

47.3.9 Fiber Connection

The connection between the SVT readout systems and the DAQ will be implemented using the HP Gigalink chip set.

There are two data phases: header and data. Both the header and data phase are encapsulated by command words. The HP transmitters allow to disentangle command words from data words (/DAV, /CAV in- and outputs). The command strobes will be used to transfer the command words. After each command strobe the sending readout board will insert a constant wait state of about 100 ns (6 transmission clocks). This can be accomplished by not strobing either /DAV or /CAV.

The headers are fixed length and 8-bits wide. The first 16 bytes of the header will be common for all detectors. The rest of the header (48 bytes in case of the SVT) is free to be defined detector specific. The header format was defined in the requirements section. Between the data start and event end commands, any number of words may be transmitted.

SVT raw data events contain two 10-bit ADC values per 20-bit fiber word. In the case of configuration events, only the lower 8-bits of the 10-bit word will be used. This restriction is required because configuration events shall be sent through the ASICs with pedestal correction and gain mapping switched off. The back end bus of the ASIC is only 8-bits wide allowing to store only 8-bit values.

Due to the nature of a collider experiment, all STAR detectors are symmetric with respect to the interaction vertex and consequently the end cap of the magnet. The definition of the readout unit IDs in the following are with respect to one end cap. The two end caps of STAR will be labelled left and right, where left means the left side of the detector as seen from the entrance of the wide angle hall. This corresponds to the 5:45 position if the beam enters the collider ring at the 6 o'clock position.

47.3.10 Data Formats

Each SVT detector has two Hybrids on its two opposite sides with 240 channels each. The sequence of SVT raw data channels is relatively unconstrained since one SVT Hybrid maps directly onto one ASIC with the upper 16 channels filled with padding data to make up for a total of 256 channels. Unlike the TPC system, there are no clusters overlapping between detectors/ASICs. It is relatively irrelevant which detector is mapped onto which ASIC or mezzanine board of the DAQ receiver board. Figure 13 shows a sketch of the SVT detector.

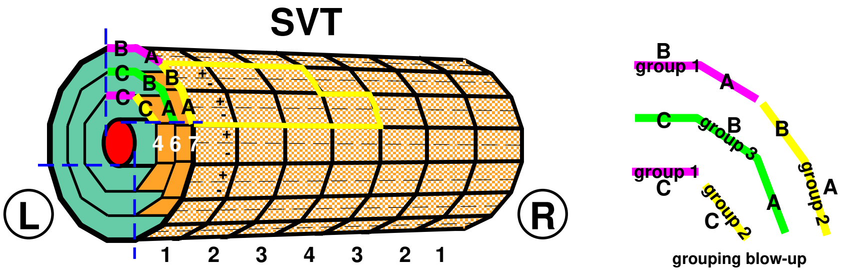

Figure 47.6: A sketch of the SVT detector geometry. There are three fiber links per octant as indicated with different colors. Each box in this figure represents a full silicon detector with two detector halfs.

Each box represents one detector with two Hybrids. The whole detector can be split into octants, four quadrants on each side. Each octant sends uncompressed raw data through three fibres. The grouping is indicated by different colors in Figure 13.

Each group consists of 9 silicon detectors or 18 Hybrids. Two of the three groups have the same mapping (group 1 and 2). They are shifted by $\pi/4$ in Φ. Due to the implementation constraints of the ASIC outlined in the requirements section of this document, the overall order of raw channels is defined as follows:

time bucket (0 ... 127)
detector channel (1...240, 16 padding zeroes)
detector (18 Hybrids)

There are 18 Hybrids sent per detector channel as indicated in the table above or 256 detector channels (including padding zeroes) times 18 Hybrids per time bucket. The Hybrid number index is running the fastest.

The 18 Hybrids in the two groups are assembled as follows: In group 1 ladder A contributes 8, ladder B 6, and ladder C 4 Hybrids. In group 2 all three ladders contribute 6 Hybrids each. The 18 Hybrids in each group are connected to 18 ADC's on the readout system. The distribution of Hybrids to ADC's is somewhat unconstrained, since each connection will deliver the time buckets of all 240 anodes. However, the sequencing of the ADC values onto the fiber link is fixed and is shown in the following table. The notation used in this table is as follows: an = ADC n (n=1,18), cn = channel (anode) n (n=1,256), tn = time bucket n (n=0,127). The "–' indicates 10-bit ADC values that are combined to 20-bit fiber link words.

Sequence Number	**High**		**Low**
0	a1c1t0	–	a2c1t0
1	a3c1t0	–	a4c1t0
2	a11c1t0	–	a12c1t0
3	a13c1t0	–	a14c1t0
4	a5c1t0	–	a6c1t0
5	a7c1t0	–	a8c1t0
6	a15c1t0	–	a16c1t0
7	a17c1t0	–	a18c1t0
8	a9c1t0	–	a10c1t0

47.3.10.1 Readout Unit IDs

The SVT has a total of 24 readout systems, 12 on each side of the STAR detector. Figure 14 shows a sketch of the position of the 12 SVT readout boards in the TPC wheel.

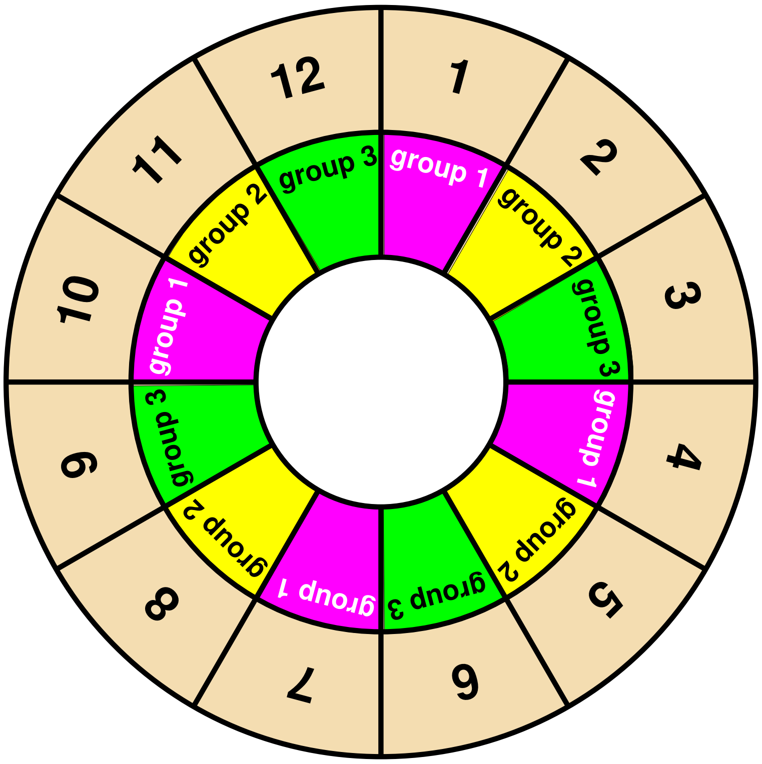

Figure 47.7: The position and readout sequence of the SVT readout boards in the TPC sector wheel.

There will be one SVT readout board per TPC sector. Which SVT detectors a given readout board in the TPC wheel reads is also indicated in Figure 14. The same nomenclature is used as in Figure 13. The TPC sector numbers are defined as seen from the outside of the magnet. Group 1 in Figure 15 would be SVT readout unit ID 1, group 2 ID 2, and group 3 would correspond to readout unit ID 3.

The corresponding (5-bit) SVT readout unit ID definition is as follows. The side of the detector is defined in bit 0 where a bit value 0 identifies the left and 1 the right side of the STAR detector. The SVT readout boards are numbered with respect to the corresponding TPC sector number from 1 to 12. This number makes up bits 1 through 4.