Aeroflex ECLIPSE Single Event Effects (SEE) High-Speed Test Results

Melanie Berg – Principle Investigator MEI
HAK Kim, Mark Friendlich, Anthony Phan: MEI
Ray Ladbury, Ken LaBel: NASA/GSFC
Steve Buchner: QSS

Test Date: 3/2006(IU), 5/2006(TAMU), 11/2006(TAMU), 1/2007(LBNL), 5/2007(TAMU), Report Date: 10/4/07

1. INTRODUCTION

This study was undertaken to determine the single event destructive and transient susceptibility of the Aeroflex Eclipse – UT6325. The devices were monitored for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing them to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility. The objective of the study was to determine Bit Error Rates (BER) per day within a synchronous design implemented within a hardened FPGA device and the BER's dependency on: Clock Frequency, Design Architecture (amount of combinatorial logic vs. Sequential logic), and Data pattern (Data Frequency).

2. DEVICES TESTED

There were 6 different architectures tested 2 parts each. The sample size per device (in this case) was not the focus since they are production- high speed parts with very little variation across the CMOS process. The emphasis was to test variations over the design state space. The devices were manufactured on an advanced 0.25um CMSOS Antifuse Process Technology with 5 layers of metal - Epi-substrate. The manufacturer is Aeroflex . The devices tested had a Lot Date Code of the following:

Aeroflex daughter board survey 8/22/2006 (TAMU)

Part Markings

WF01G QL1082

Daughter Board Design	Daughter Board ID
D2 REG 08	124
DL REG 00	151
D3 REG 88	194
D5 REG 1120	O87

Aeroflex daughter board survey 10/16/2006 (Berkey)

Part Markings

WF01G QL1059

Daughter Board Design	**Daughter Board ID**
1120	O29
1120	O34
1120	O28
88	O39
88 ?	(de-lidded)
88	O13

Aeroflex daughter board survey 11/6/06 (Berkey)

Part Markings

WF01G QL1059

Daughter Board Design	**Daughter Board ID**
1120	O29
1120	O34
1120	O28
88	O39
88 ?	(de-lidded)
88	O13

Aeroflex daughter board survey 10/16/2006 (TAMU)

Part Markings

WF01G QL1082

Daughter Board Design	**Daughter Board ID**
D3 REG 88 ?	194
D5 REG 1120	O87

Aeroflex daughter board survey 12/7/2006 (TAMU)

Part Markings

WF01G QL1059

Daughter Board Design	**Daughter Board ID**
88	O53
88	O51
1120	O56
1120	O58
1120	O30

Part Markings

WF01G QL1082

Daughter Board Design	**Daughter Board ID**
1400	O10

Part Markings

WF01G QL1059

Daughter Board Design	**Daughter Board ID**
1120	O29
1120	O34
1120	O28
88	O39
88 ?	(de-lidded)
88	O13

Part Markings

WF01G QL1082

Daughter Board Design	**Daughter Board ID**
1120	O87
88?	194

Purpose is to investigate SEU Frequency Data Pattern, and Architectural Dependencies. SEU testing targets speeds from 500 KHZ up to 100 MHZ.

2.1 DUT Architecture

The Principle Configuration is a shift register string (175 to 1125 DFF's) with varying levels of combinatorial logic (0, 4 or 8 inverters between DFF's – 3/2006 to 1/2007; including 20 inverters 7/2007) and Fanout options to the Enable inputs. A By-4 clock divider circuit is implemented to shift the last 4 bits of the Shift register string into a DFF window (SCAN_DATA). The window is output to the tester. A data clock (SHIFT_CLK) is also output to the tester for high speed synchronous data capture. Reset passes through an asynchronous assert – synchronous de-assert circuit and is supplied to every DFF.

The following is the reset circuit used within the DUT.

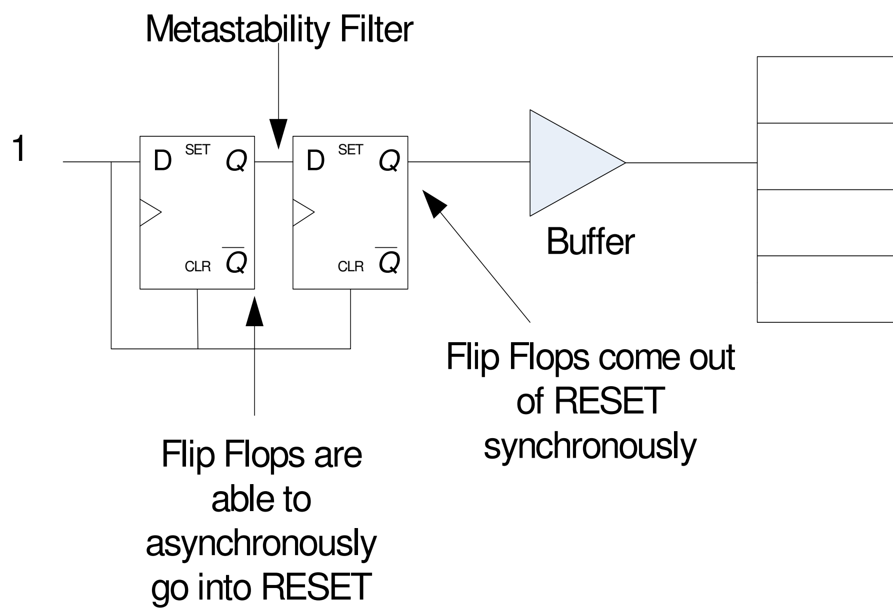

Figure 1: Asynchronous Assert - Synchronous De-assert

The following is the DUT configuration schematic:

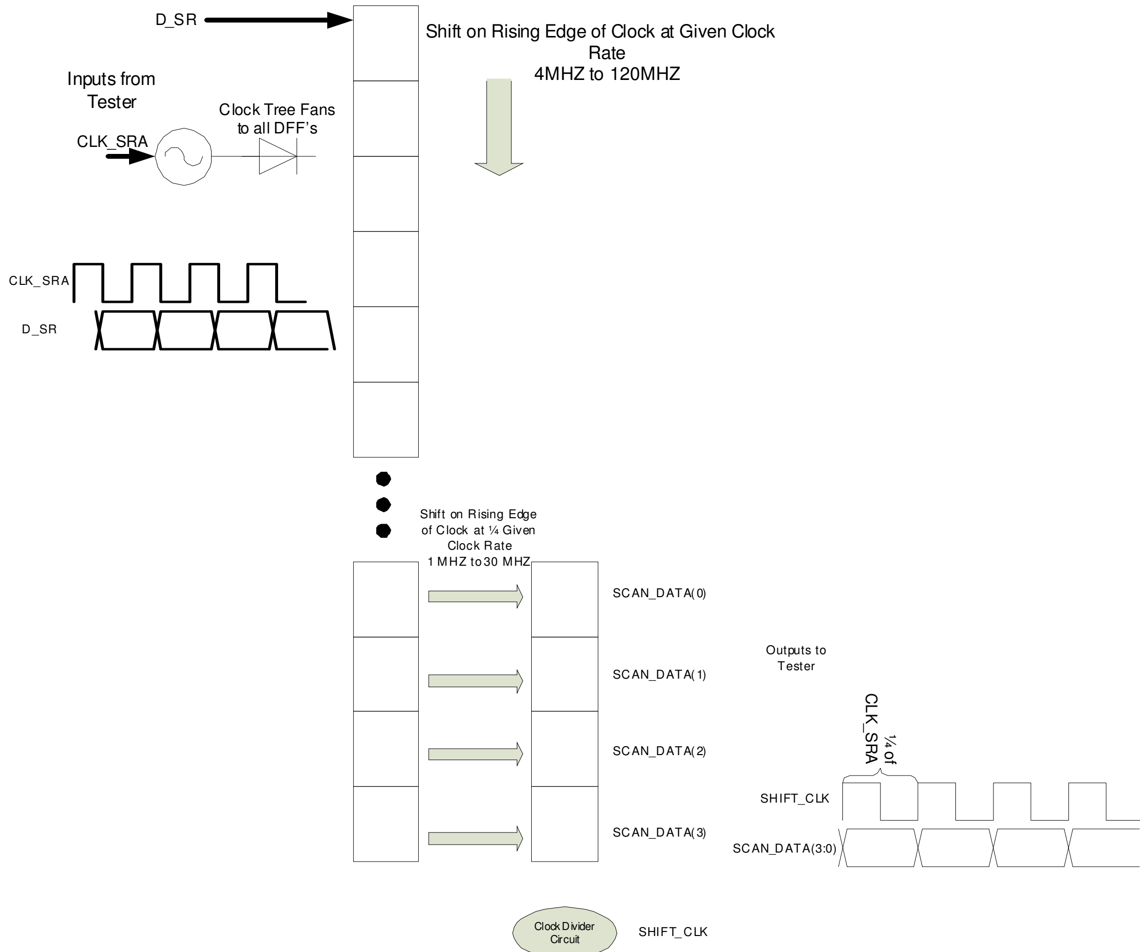

Figure 2: Device Under Test Top Level Architecture

The following demonstrates details of the shift register strings.

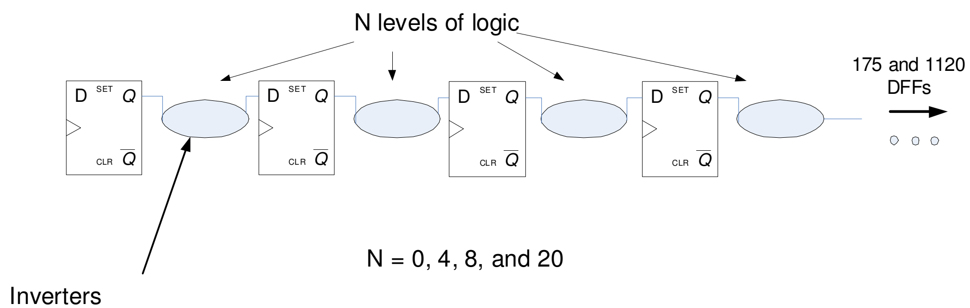

Figure 3: Shift Register String with Optional Combinatorial Logic

Various levels of combinatorial logic are used in order to measure possible transient susceptibility. If the Eclipse device is susceptible to transients, then faults will be frequency dependent. String lengths of 175 and 1120 are tested with and without the combinatorial logic. A string length of 1120 is tested without the combinatorial logic in order to insure that the additional faults are not from the larger area of the additional combinatorial logic.

3. TEST FACILITY

3.1 Heavy Ion.

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 15 MeV/amu tune).
Flux: 1.0E04 to 2.0E05 particles/cm^2/s
Fluence: All tests were run to 1 x 10^7 p/cm^2 or SEFI.

Table 1: LET Table

Ion	Energy (MEV/Nucleon)	LET (MEV/cm^2/mg) 0 deg	LET (MEV/cm^2/mg) 45 deg
Ar	15	8.5	12
Cu	15	20.7	
Kr	15	28.5	40.26
Xe	15	52.7	74.5

3.2 Proton

Tests were performed at two facilities.

Facility: Crocker Nuclear Laboratory (CNL) at the University of California at Davis (UCD)
Flux: 1.0E09 particles/cm^2/s
Fluence: All tests were run to 7.14E11 p/cm^2
Energy : 63 Mev-protons

Facility: Indiana University Cyclotron Facility (IUCF)
Flux: 3.0E9 particles/cm2/s
Fluence: All tests were run to 1.0E12 p/cm2
Energy : 195 MeV - incident

4. TEST CONDITIONS

Test Temperature: Room Temperature
Operating Frequency: 15 MHZ to 150MHZ
Power Supply Voltage: 3.3v I/O and 1.5V Core.

5. TEST METHODS

5.1 Tester Architectural Overview

The Eclipse controller/processor is instantiated as a sub component within the Low Cost Digital Tester (LCDT). The LCDT consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). There was a daughter board created for each DUT. The objective of this DUT Controller/processor is to supply inputs to the Eclipse Device and perform data processing on the outputs of the Eclipse. The LCDT communicates with a user controlled PC. The user interface is LAB-VIEW. It will send user specified commands to the mother board and receive information from the mother board. Please see Documents: "LCDT" and "General Tester" for further information concerning the LCDT functionality. The LCDT is connected to the Eclipse DUT as shown in the following Block Diagram.

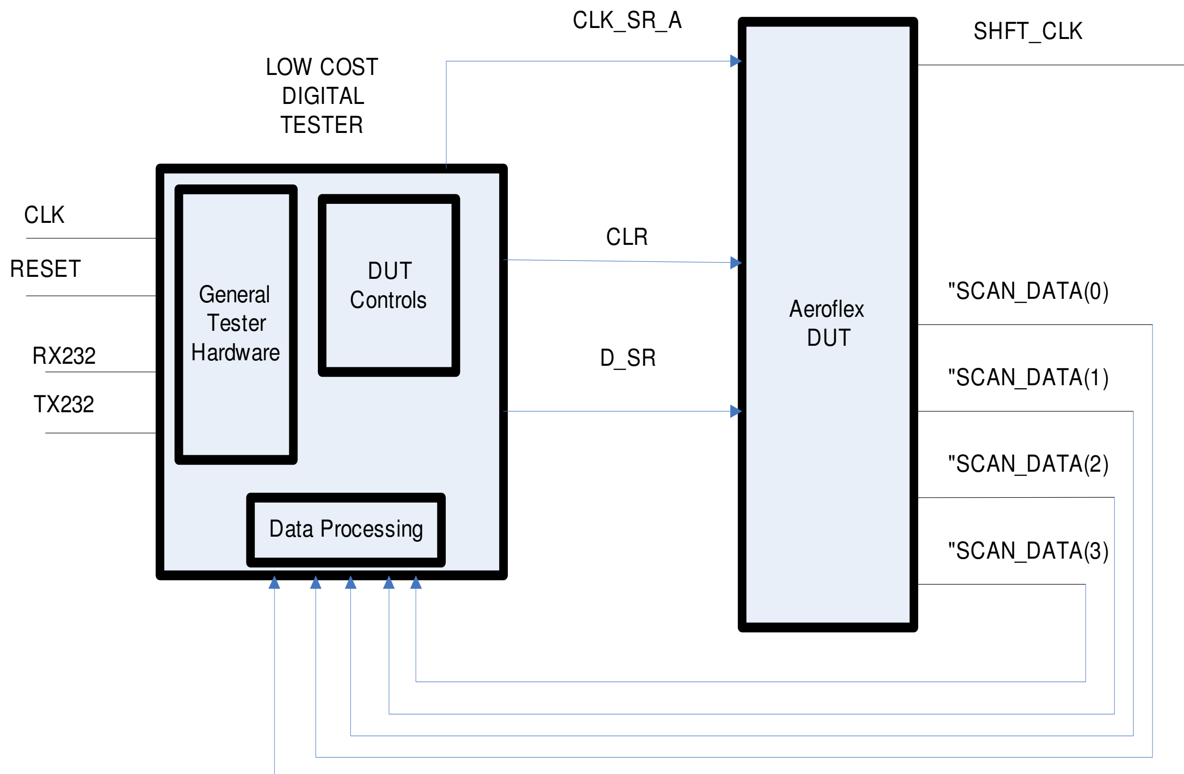

Figure 4: System Level Tester Architecture

5.1.1 I/O List and Definitions

Table 2: I/O Table

Input Name	Description	Direction	Synchronous	Slew	Pullup
CLK	System clock of the LCDT	Input	Clock		N
RESET	LCDT system reset	Input	A		N
RX232	Serial receive input	Input	A		N
SCAN_DATA(4:0)	Data window of Eclipse. Data is processed by LCDT and compared against expected value	Input	A		N
SHIFT_CLK	Output clock of ECLIPSE. Used to control SCAN_DATA capture. SHIFT_CLK is always ¼ the speed of CLK_SR_A. However it is not synchronous with CLK_SR_A	Input	A		N
CLK_SR_A	Input clock to ECLIPSE. Max speed is 150mhz	Output		FAST	N
CLR	Reset to the Eclipse	Output		FAST	N
D_SR	Data Input to the Eclipse	Output			N
TX232	Serial transmission line	Output			N

5.2 Requirements

The requirements for the Eclipse LCDT tester are listed in Table 3.

Table 3 – Requirements Table

Item	Requirement
1	Supply System Clock to the Eclipse DUT
2	Supply Reset to Eclipse
3	Supply Data Input to the Eclipse
4	Clock Frequency of Eclipse shall be variable
5	Maximum Eclipse input clock frequency shall be 150Mhz
6	0,1, and checker board data patterns shall be generated and placed on the ECLIPSE data lines
7	ECLIPSE reset shall be active low
8	ECLIPSE reset shall be active for at least 3 ECLIPSE system clocks
9	ECLIPSE Data Inputs shall be stable at the Rising Edge of the ECLIPSE system clock with a set-up time of 3ns and a hold time of 3ns
10	ECLIPSE data inputs shall be captured by the LCDT data processing module once detecting the rising edge of the data clock (SHIFT_CLK)
11	SHIFT_CLK rising edge detection must include a metastability filter because the SHIFT_CLK input is asynchronous.
12	Input Data must be registered before the data processing block implements the compares – protects against radiation induced I/O transients.
13	Data processing block shall report every error to the FIFO block
14	Tester must be able to adjust supplied clock frequency to DUT – command driven from user PC
15	Tester must be able to adjust data pattern (and frequency) to DUT – command Driven from user PC

The tester supplies inputs as follows: Data (D_SR) changes at the falling edge of the input clock (CLK_SR) so that it is stable and can be captured at the rising edge. CLK_SR and D_SR will be at the user specified frequency. The user will also supply (by command) the preferred data pattern. Data patterns range from all 0's , all 1's, and alternating 1's and 0's.

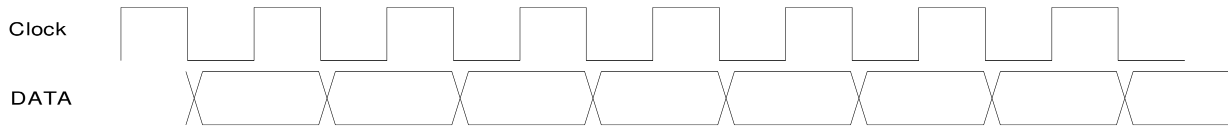

Figure 5: Clock and Data Input to DUT

5.3 User Interface and Control

The User controls the tests via a LABVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

Table 4 : Summary of Commands Used in Eclipse Tester

Command #HEX	Command	D0	D1	D2	Description
01	Reset DUT	n	n	n	Resets ECLIPSE
02	Start Test	n	n	n	Starts ECLIPSE clock and data generation
90	Pattern Number	y	n	n	0,1,or checker board
A0	Clock Frequency	y	n	n	Clock frequency divider of 150mhz

The following is a detailed description of commands and their associated functionality.

5.3.1 RESET DUT:

The RESET DUT command is decoded as x01. The following represents the command as noted in Table 4:

x01	xx	xx	xx

Figure 6: Reset Command Format – Command Number, D0, D1, and D2

Once decoded, all DUT inputs will go into reset mode (Reset, CLK_SR and D_SR are low)

5.3.2 START TEST:

START TEST is decoded as x02. The following represents the command as noted in Table 4:

x02	xx	xx	xx

Figure 7: Start Command Format

All other commands should be supplied before start test. I.e. the user should define the pattern and clock frequency before administering a start. This command activates the CLK_SR and D_SR DUT inputs.

5.3.3 PATTERN NUMBER:

There are three data patterns that can be generated by the tester. Data can be a static 0, a static 1, or alternate every ECLIPSE clock cycle (checker board). The command number is x90. The first byte of data (D0) is also decoded (all other bytes are ignored but must be supplied – i.e. all commands must be 4 bytes of data).

x90	x00	xx	xx

x90	x01	xx	xx

x90	x02	xx	xx

Figure 8: Pattern Command Format

D0 decode is as follows:

X00: Static 0
X01: Static 1
X02: Checkerboard Pattern

5.3.4 CLOCK FREQUECY:

The clock frequency command is decoded as xA0 and D0. The following represents the command as noted in Figure 9:

xA0	xnn	xx	xx

Figure 9: Clock Frequency Command Format

Upon the receipt of this command, D0 is used as a clock frequency divider. This command must be sent after a RESET DUT and before a START TEST. D0 must be an even number and must be greater than or equal to 2. The associated output is CLOCK_FREQ. See the LCDT General Tester for more information concerning the processing of CLOCK_FREQ.

5.4 Running a Test

The following is a flow diagram of running a single test. Clock Frequency default is set at 100MHz and pattern default is set at checker board. If the user decides to set different parameters (other than default), then the corresponding command must be sent (see section 5.3 for a list of user commands).

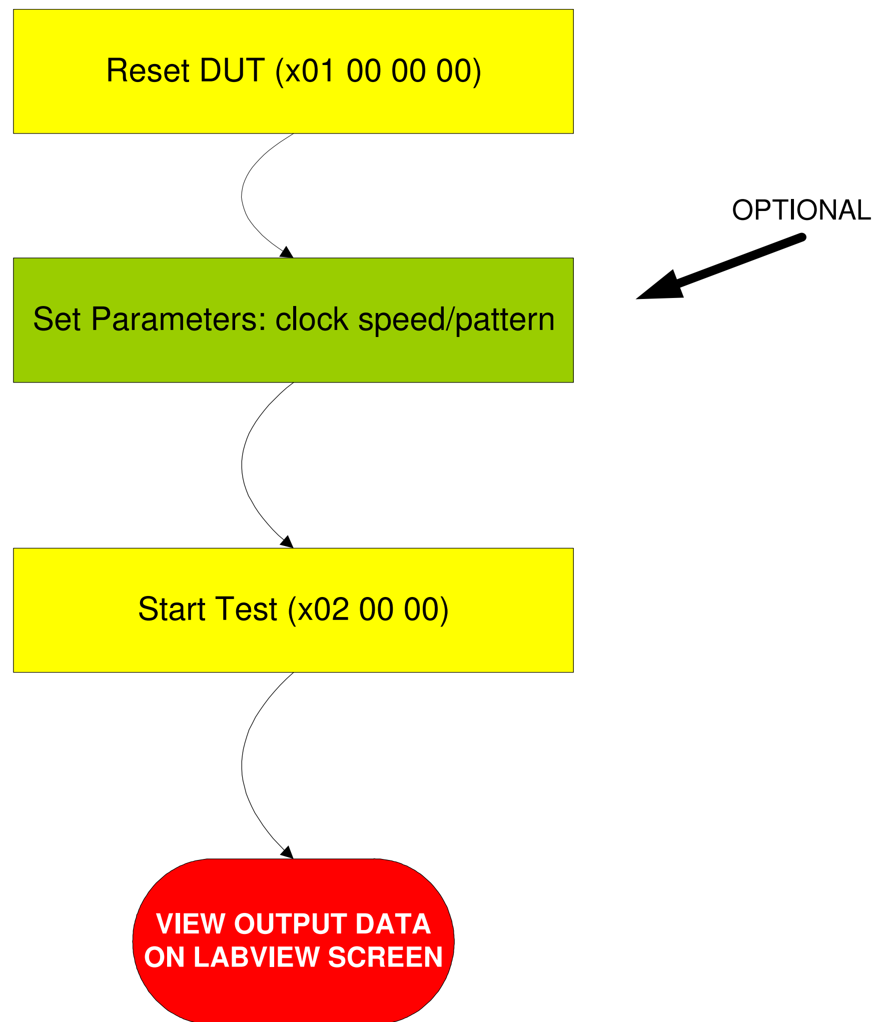

Figure 10: Flow Diagram: Running a Test

5.5 Processing the DUT Outputs

The outputs of the DUT are fed to the tester for data processing. The objective of the data processing is to synchronously capture data using SHFT_CLK (as a data enable) and SCAN_DATA (as a 4 bit window of DUT Data). SHIFT_CLK has a maximum frequency of 37.5MHZ (150 MHZ divided by 4). It is a control signal indicating new data. It is considered

asynchronous to the tester and is sampled using the tester's system clock (max 150 MHZ). Thus, the tester's sampling clock will always be 4 times as fast as SHIFT_CLK. The SHFT_CLK is fed into a metastability filter and an edge detect. This process takes 1 to 2 clock cycles of the sampling clock (detection will be delayed by 1 to 2 sampling clock cycles of the actual edge). Once the edge is detected, data is then sampled and registered. The data is then registered again. The comparison is made against the second registered data and if there is a mismatch, the error is reported.

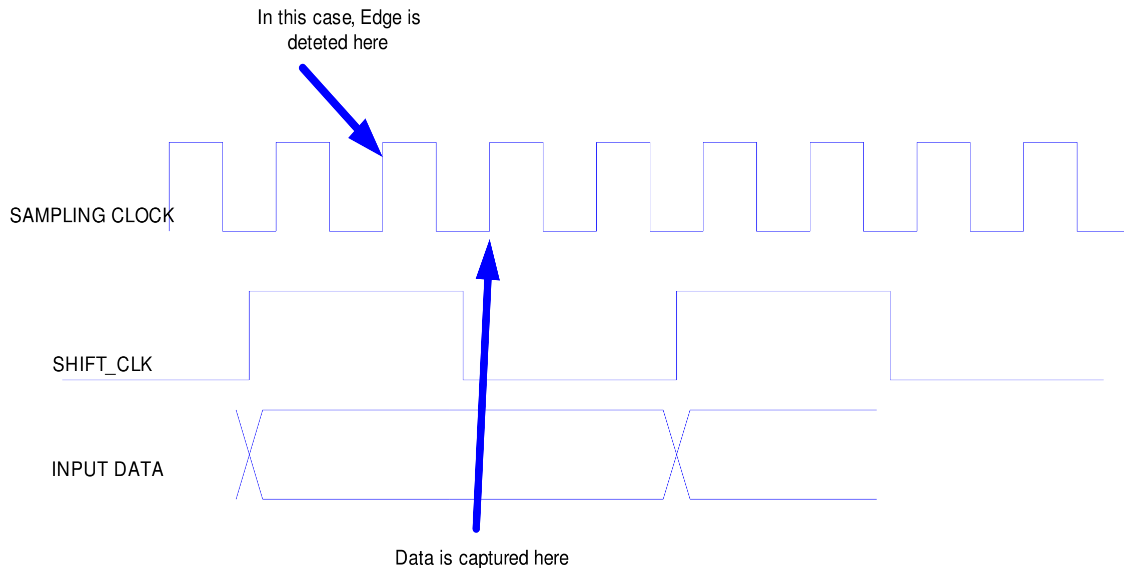

Figure 11: Timing Diagram of Expected DUT Outputs

6. HEAVY ION RESULTS: TEXAS A&M UNIVERSITY

The ECLIPSE devices were irradiated with Argon, Copper, Krypton, and Xenon beams at normal incidence, 0 and 45 degrees (yielding effective LETs of approximately 8.5, 12, 28.5, 40.26, 52.7, 74.5 MeV•cm^2/mg) at the Texas A&M University Cyclotron Single Event Effects Test Facility (please refer to Section 3 Test Facility). Faults from the ECLIPSE devices were encountered at all LETs operating at 100 MHZ. However, the number of SEUs was very low at Argon.

The ECLIPSE devices were tested to measure the Single Event latchup cross section under the above conditions. Each part was placed in the beam until 10^7 ions/cm^2 – the beam fluence was then recorded. During our experiment, no Single Event latchup events occurred, yielding a threshold SEL LET for latchup of > 74.5 MeV•cm^2/mg.

The ECLIPSE devices were also tested to measure the error cross section under the above conditions. Each part was placed in the beam until 10^7 ions/cm^2 was reached. An average cross section per bit was determined for a given LET as the number of fault events observed divided by the total fluence of the associated run at that LET.

6.1 Cross Section with respect to LET

As the LET value increases, so does the transient width. The error cross section is directly proportional to the LET. Most runs at an LET of 8.5Mev*cm^2/mg yielded no error. However, there were a small number of runs with error. LET threshold is approximately at this point of 8.5Mev*cm^2/mg.

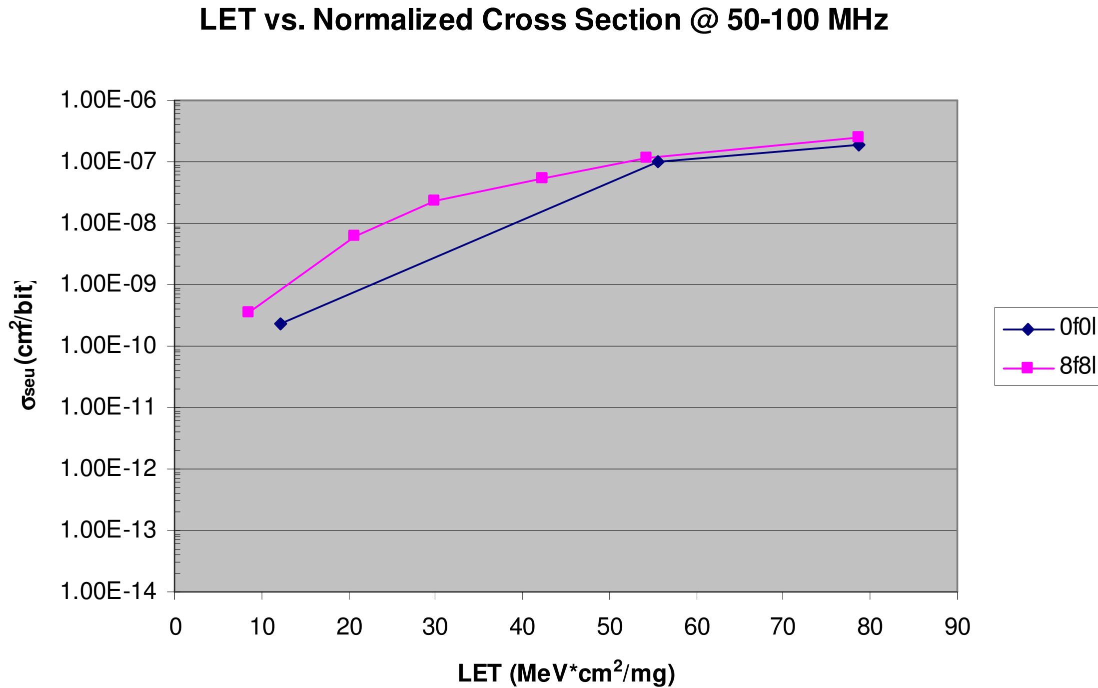

Figure 12: Comparison of two Architectures: Cross Section and LET @ 50-100MHZ – Data Pattern = Alternating

6.2 Bit Error Rate Calculations

Using the **CREME96** at worst case GEO, the errors-bit/day were:

- 50 to 100 MHZ and no extra level of combinatorial logic (0F0L) : < 5E-9

6.3 Architectural and Frequency Effects

At each LET, several tests were performed at various frequencies on all of the shift register string types. The DFF primitive within the ECLIPSE series contains combinatorial logic and contains shared input Data and Clock signals. Theoretically, there should be a linear increase of cross section corresponding to frequency. However, this was not the case, as the frequency increased, the cross-section did not increase. .

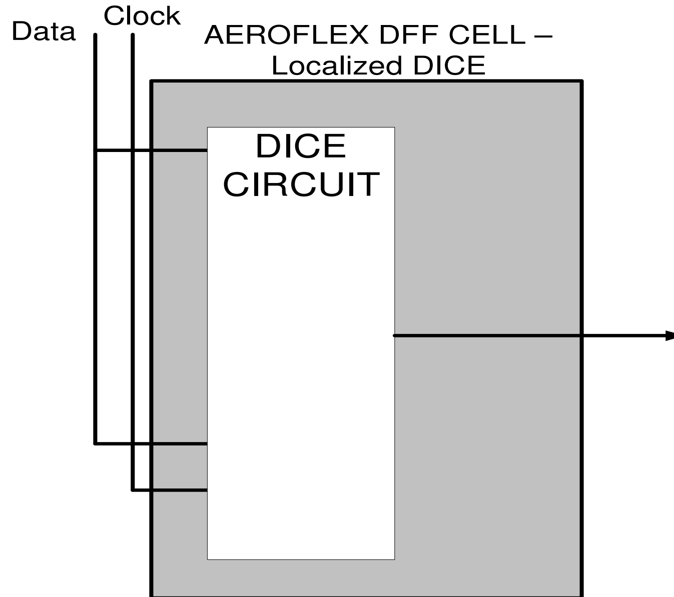

Figure 13 : Aeroflex DFF Primitive: DICE Redundant Flip Flops

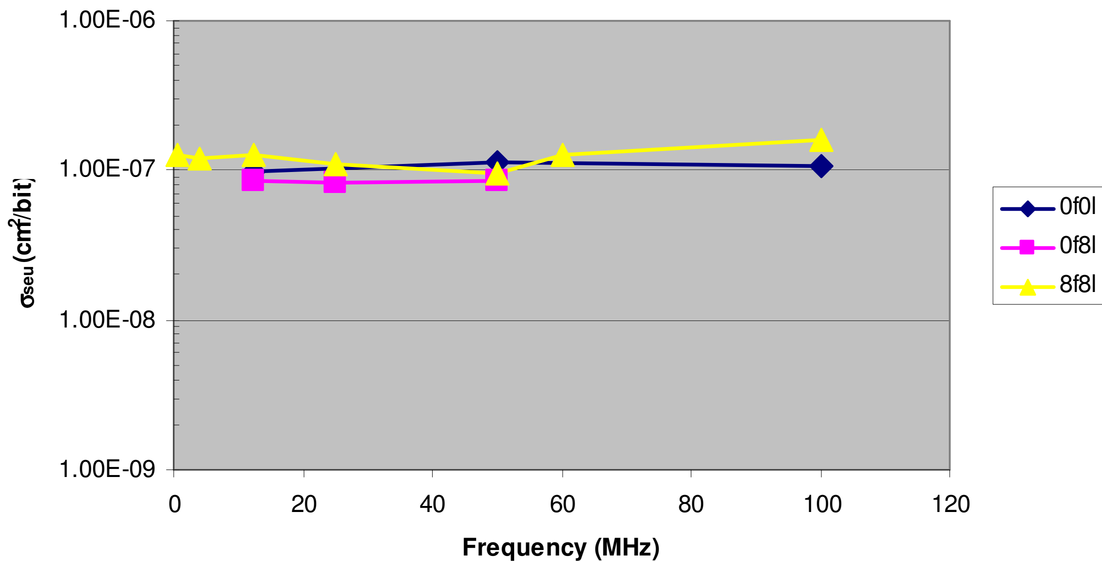

Figure 14: Frequency vs. Cross Section 2006 Test Suite

The shift register strings containing combinatorial logic (8F4L, 0F0L, 0F8L) had statistically similar error cross-sections. This follows with the absence of frequency effects – i.e. transients are not a significant factor. The research suggests that the softest portion of the Eclipse FPGA is the flip-flops.

6.4 Frequency Effects: -7/2007

Original DUT circuits contained shift register chains with 0, 4, and 8 inverters between each DFF. We tested another circuit containing 20 inverters between each DFF stage and observed that bit error cross-section decreased as frequency increased. This circuit was implemented in a device that contained 0 and 8 inverters between DFF's in order to obtain a statistically accurate cross-section. See Figure 15: Frequency and Data Pattern Effects at 30 MeV*cm^2/mg and Figure 16: Frequency and Data Effects at 54 MeV*cm^2/mg.

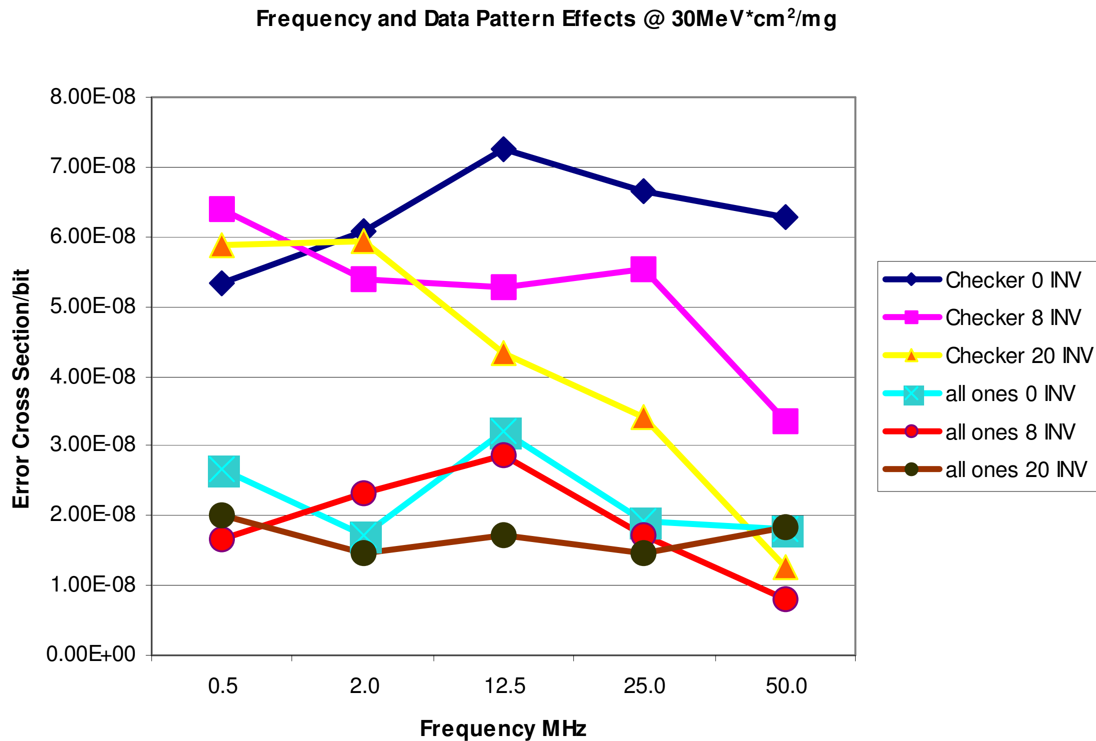

Figure 15: Frequency and Data Pattern Effects at 30 MeV*cm^2/mg

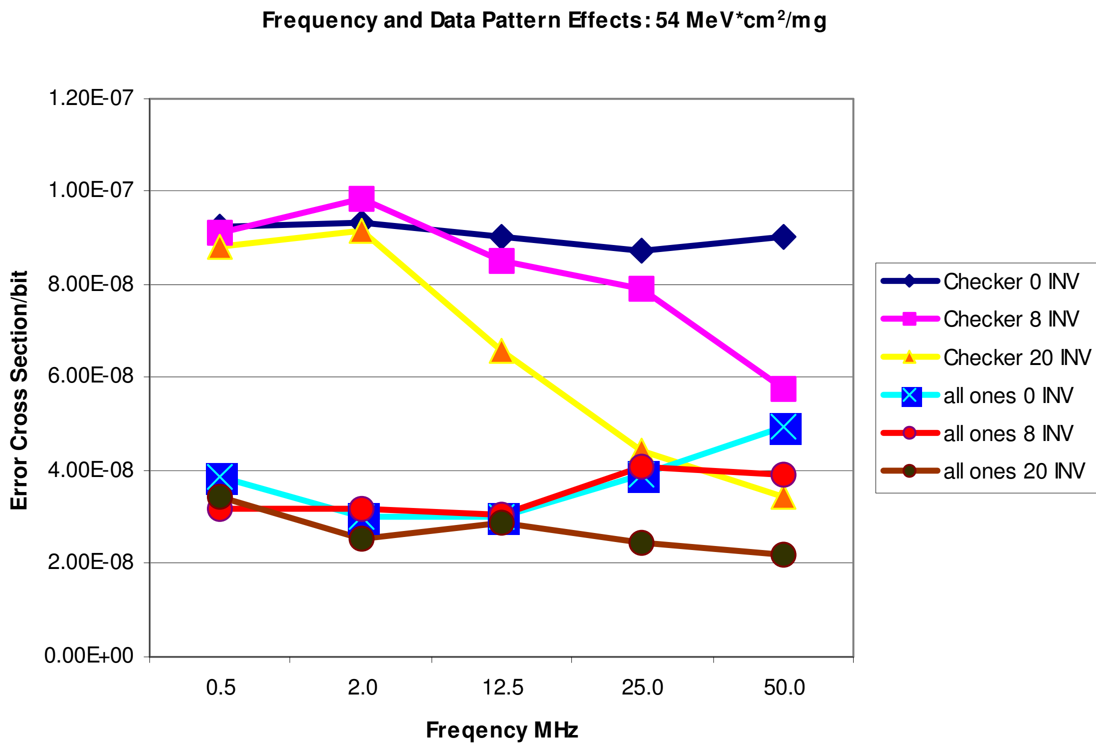

Figure 16: Frequency and Data Effects at 54 MeV*cm^2/mg

6.5 General Data Pattern Effects: Static vs. Dynamic Data

Static data input yielded lower error cross sections than the alternating data pattern for all shift register strings.

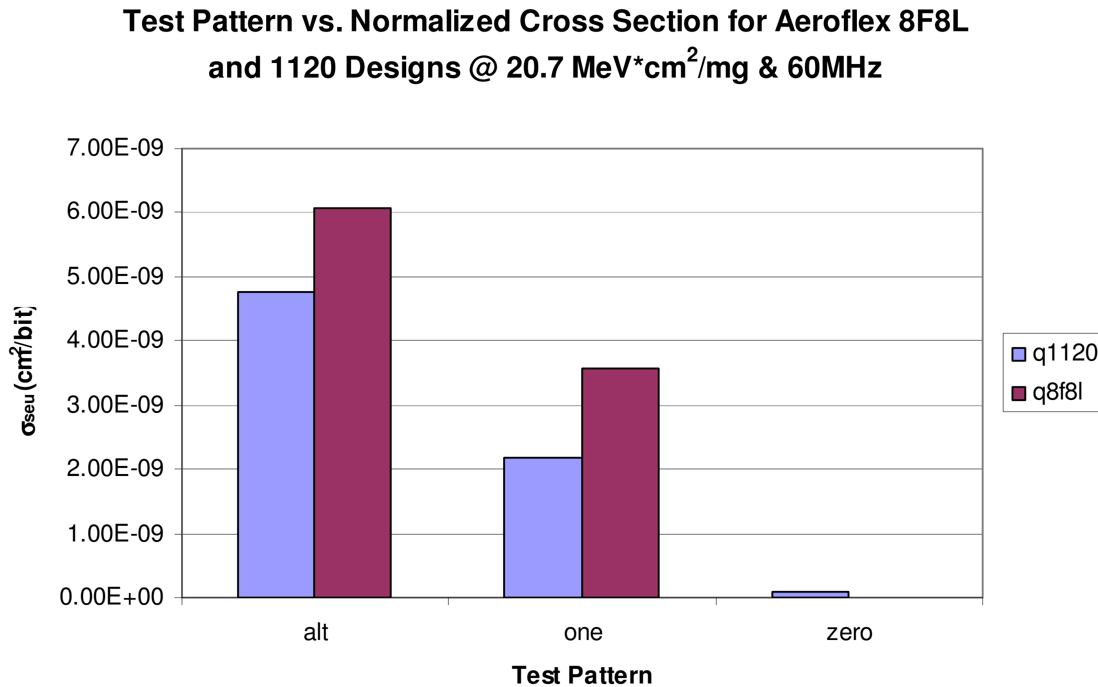

Figure 17: Test Patterns with respect to Normalized Cross Section

6.6 Device Timing after Testing: 3/2006 and 5/2006

All original circuits could be run at 100MHZ. After the initial Heavy Ion Testing, none of the circuits could be run at 80MHZ and above. Operating frequency was observed at 60MHZ (actual highest operational frequency may be somewhere between 60MHZ and 80MHZ). One circuit that has never been tested can still be run at 100MHZ. All circuits were full functional 4 moths after testing (see section 6.7). Cause is still unknown.

6.7 Device Timing : 11/2006 and 1/2006

We observed the old devices working at speed 10/2006. With Heavy ions, we retested the old devices and tested new devices between 4MHz to 100MHz (8MeV*cm^2/mg to 74MeV*cm^2/mg). We were unable to reproduce the old problem of a decrease in circuitry operational frequency… i.e. all circuits performed at 100MHz post irradiation. The anomaly in section 6.6 has never been observed again.

6.8 Bursts

Because of the synchronous nature of the tester in respect to the DUT, it is possible to capture, and analyze data every clock cycle (even at its highest speed – 100MHZ). Every fault is time stamped and a burst counter is incremented if there is a fault in the following clock cycle (as just previously analyzed – novel approach). This methodology of testing affords the analysis an increase in visibility to fault data interpretation.

Bursts were seen only at LET values greater than 21 Mev*cm^2/mg. When bursts were values of long strings of "0" with the existence of a SHFT_CLK no matter the data pattern – bursts were

assumed to be on the reset line. There were some occurrences when there was a loss of the (SHFT_CLK) with no recovery (only upon system reset)– the source has not been determined.

7. PROTON RESULTS : 3/2006

Limited tests performed due to the lack of samples and time. The following are the results from the separate test proton test trips (please refer to Section 3 Test Facility)

7.1 Proton dose levels (63 MeV protons) of 100 to 200 krads(Si) per device.

No SEUs observed at 15 MHz for any string. Few SEUs observed at worst case 150 MHz. SEU Cross-section of 6.65E-16 cm^2 per device for 4F4L. A SEU Cross-section of 3.5E-15 cm^2 per device for 4F8L has been calculated. There is roughly an order of magnitude confidence level on results (low statistics). There were no SEUs observed on other DUT strings at 150 MHz

7.2 Proton dose levels (195 MeV protons) of 300 krads(Si) per device

There were no SEUs observed at 18.75 MHz for any string. Just a few SEUs observed at worst case 120 MHz. A SEU Cross-section of 8.5E-16 cm^2 was calculated per device for 8F0L and a SEU Cross-section of 2.8E-16 cm^2 was calculated per device for 8F8L

8. FURTHER TEST REQUIREMENTS

Additional tests are required to further understand the Frequency Effect anomaly.

8.1 Appendix 1:

ECLIPSE URL:
http://ams.aeroflex.com/ProductFiles/DataSheets/FPGA/RadHardEclipseFPGA.pdf

For further information contact Melanie.D.Berg@nasa.gov