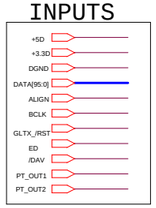
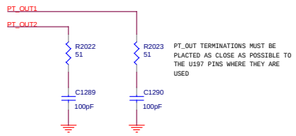
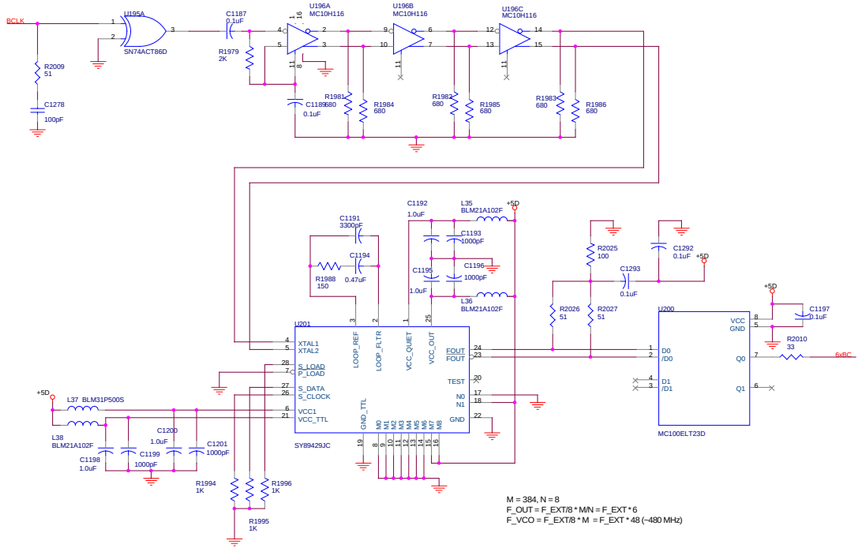
INPUTS



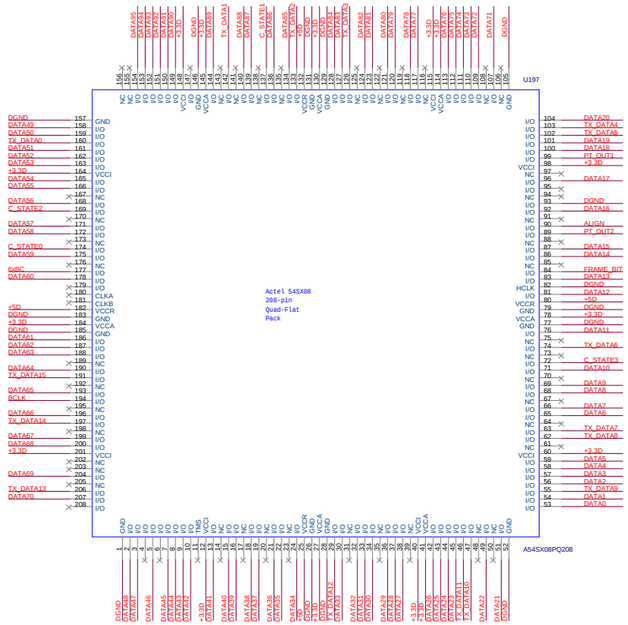


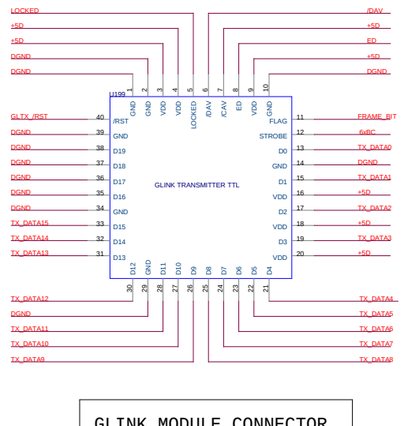
PT_OUT TERMINATIONS MUST BE PLACED AS CLOSE AS POSSIBLE TO THE U197 PINS WHERE THEY ARE USED

OUTPUTS



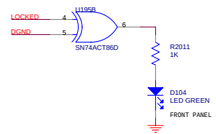
M = 384, N = 8
F_OUT = F_EXT/8 * M/N = F_EXT * 6
F_VCO = F_EXT/8 * M = F_EXT * 48 (~480 MHz)

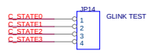




GLINK MODULE CONNECTOR

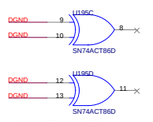
SEA ADVANCED INTERCONNECTIONS PART NUMBER KSS010-210TG SOCKETS ARE USED TO MOUNT THE GLINK MODULE





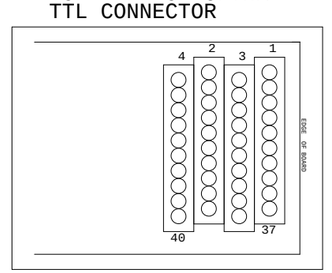
0.1 INCH SPACED SINGLE LINE HEADER

NO STUFF



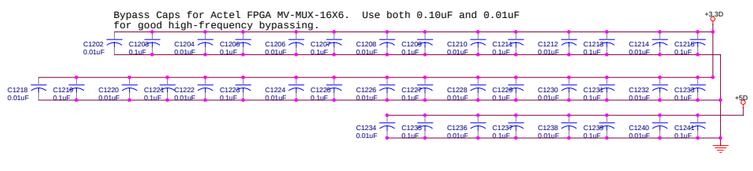
UNUSED GATES IN 74ACT86

TOP VIEW OF GLINK TTL CONNECTOR



POWER SUPPLY BYPASS CIRCUITS

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



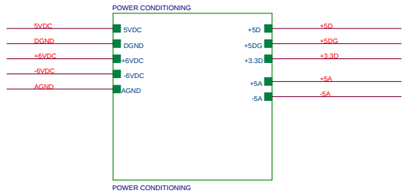
Notes:
1) Place parts as close as possible to keep traces short in general. High speed traces require special attention.
2) High speed traces must be kept short. Short means less than 1.7 inches. They must also be routed to avoid vias. Traces should stay on a single layer whenever possible.

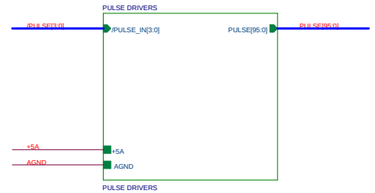
CHANGES FROM REV0

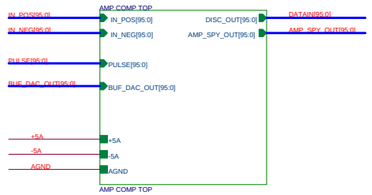
1. ADDED PT_OUT1 and PT_OUT2 SIGNALS TO GLINK CHIP
2. REPLACED 1013-50 CHIP WITH 1013-25
3. ADDED SOURCE TERMINATION RESISTOR TO 6xBC SIGNAL
4. MODIFIED BCLK TERMINATION
5. MODIFIED PLL OUTPUT TERMINATION AND POWER FILTERING ACCORDING TO MICREL AN06

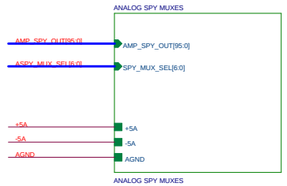
Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

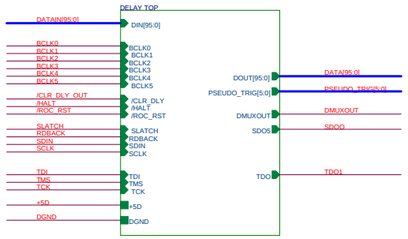
Title	GLINK	
Size D	Document Number 5.3.13.002-0313-170	Rev
Date: Tuesday, October 03, 2000	Sheet 1 of 34	

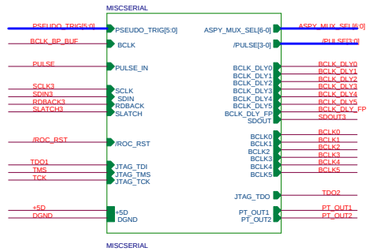


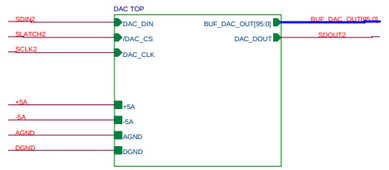


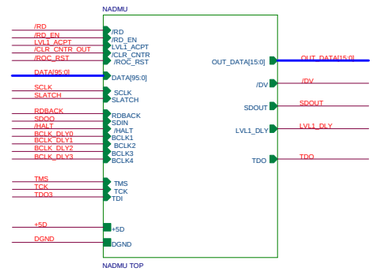


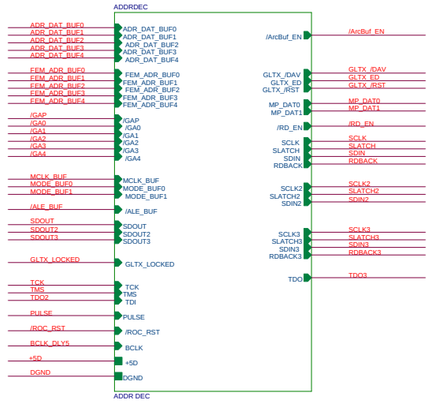












CHANGES FROM REV0

1. ADDED FIVE EVENT FIFO TO JTAG LOOP
2. ADDED PULSE, BCLK_DLY5, AND PULSE LINES TO ADDRESS DECODER
3. ADDED DGND TO DAC INPUT
4. CHANGED DGND TO AGND ON PULSE DRIVERS
5. ELIMINATED /SRESET SIGNALS

Phenix MuID ROC

Oak Ridge National Lab

Instrumentation and Controls Division

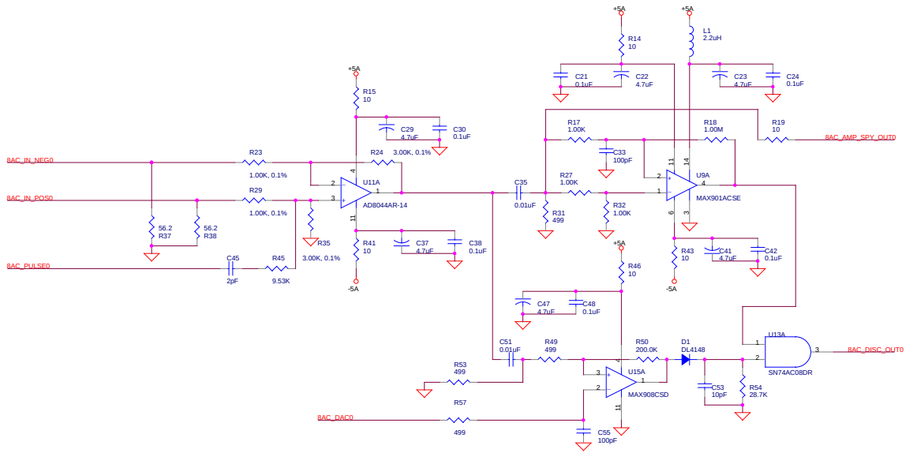
Title	TOP LEVEL	
Size D	Document Number 5.3.13.002-0313-100	Rev
Date: Tuesday, October 03, 2000	Sheet 2 of 34	

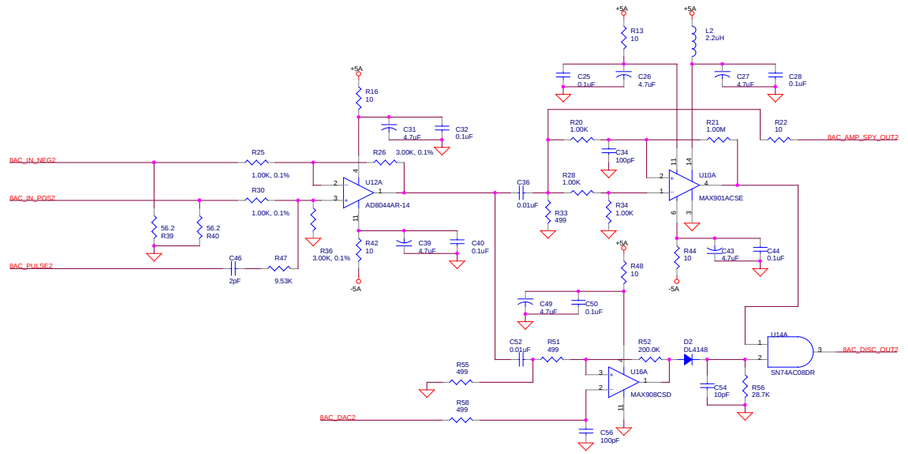
INPUTS

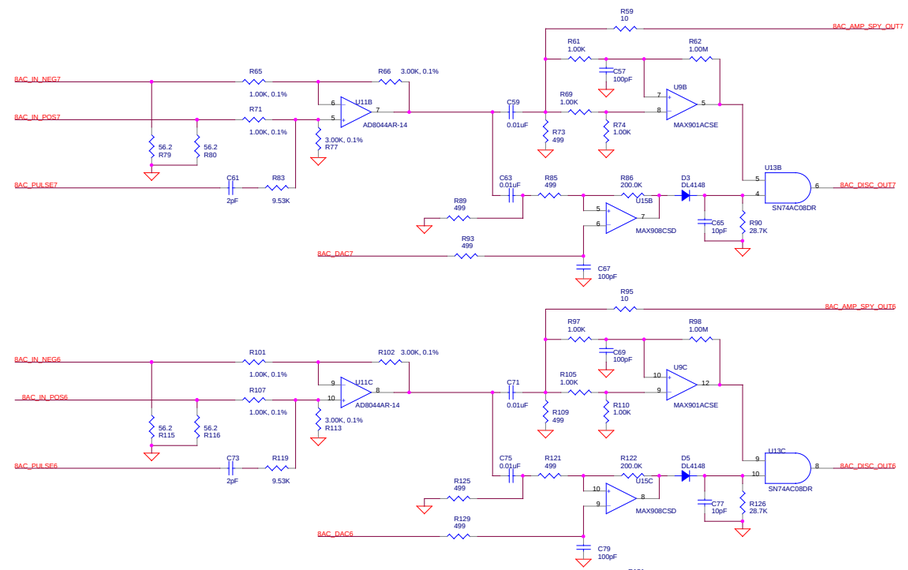
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

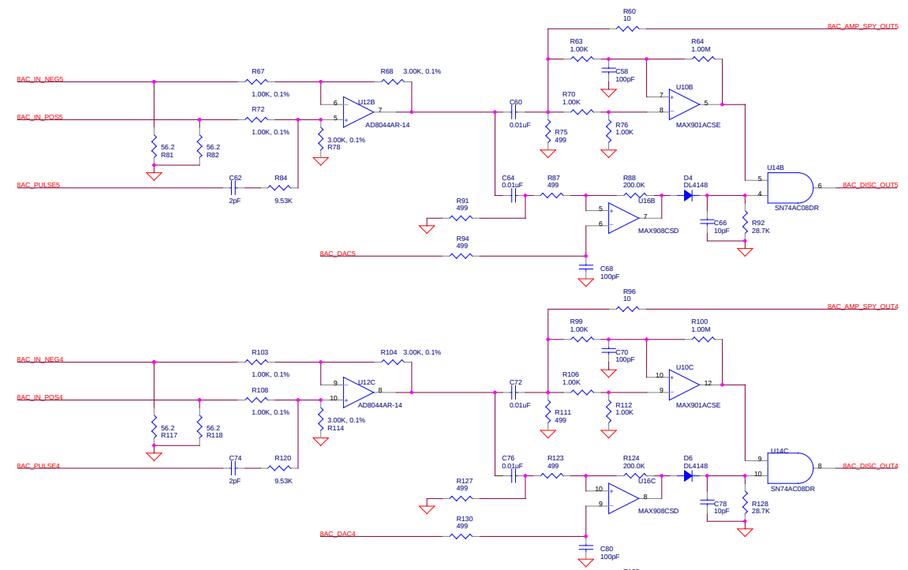
OUTPUTS

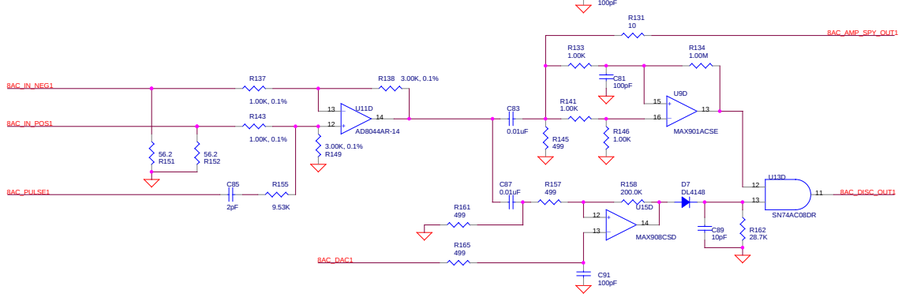
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

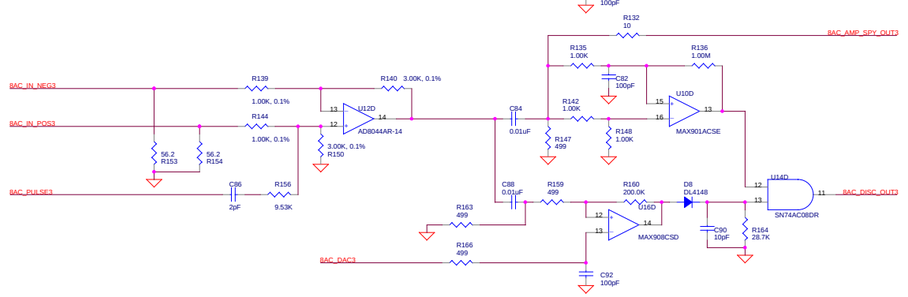


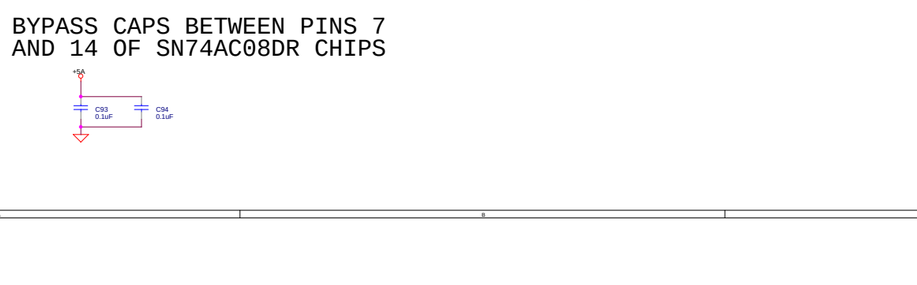












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-138	Rev
Date: Wednesday, November 01, 2000	Sheet 3 of 34	

INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
/ROC_RST
BCLK

U129
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

TDO
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG
/SLATCH
SDOUT

U130
3D7110D-4

U131
DS1021-25

+5D

R1891
51

C983
100pF

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C984 C985 C986 C987 C988 C989 C990 C991 C992 C993 C994 C995 C996 C997 C998 C999
0.1uF
DGND

CHANGES FROM REV0

1. **CHANGED BCLK TERMINATION**
2. **1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK**
3. **REMOVED CLR_SRL SIGNAL**
4. **REMOVED PULL-UP RESISTORS FROM DELAY CHIP**

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

Title: 16DLY

Size: D | Document Number: 5.3.13.002-0313-100 -299 | Rev:

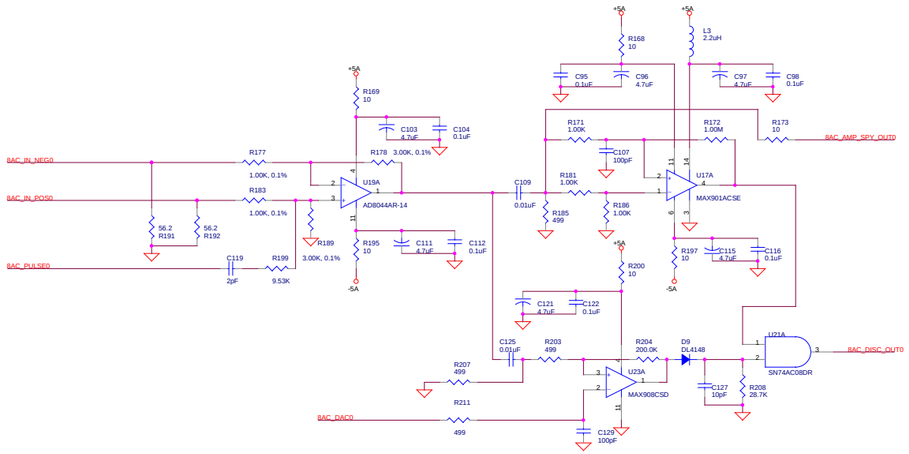
Date: Tuesday, October 03, 2000 | Sheet 4 of 34

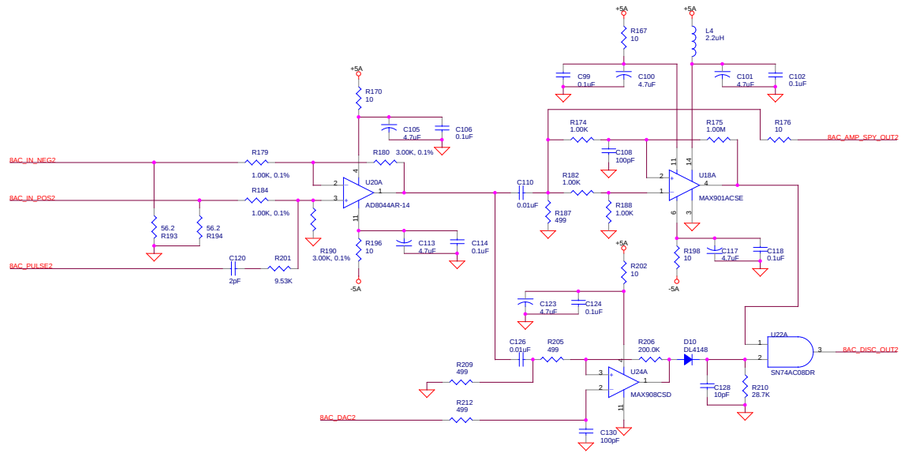
INPUTS

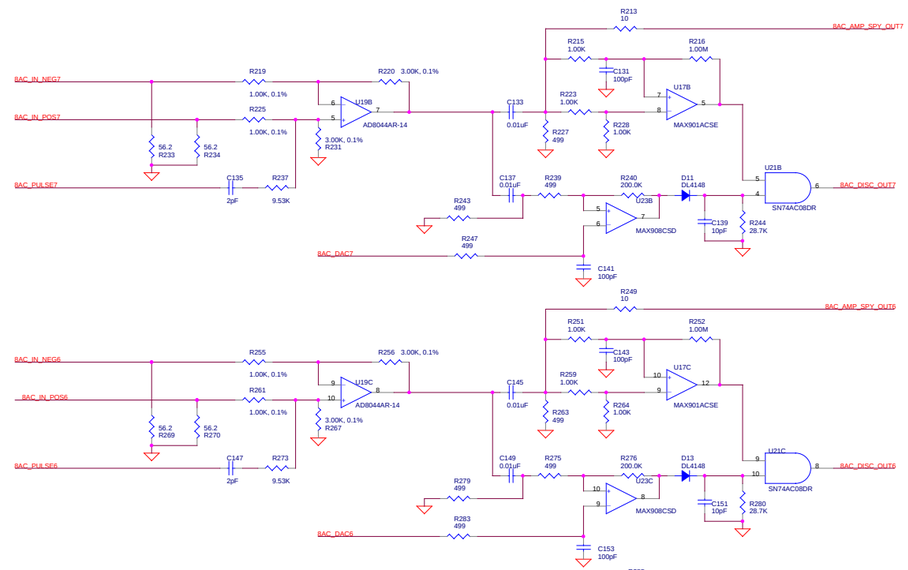
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

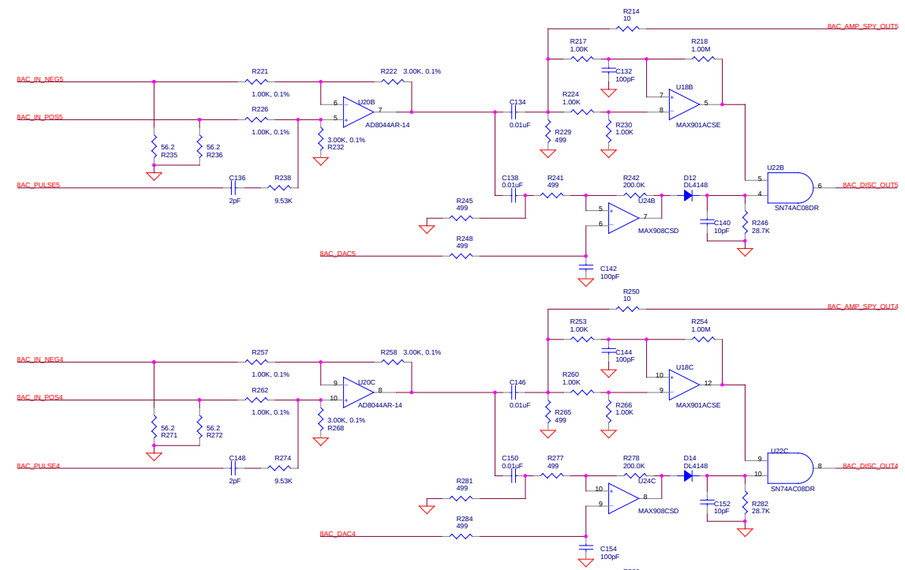
OUTPUTS

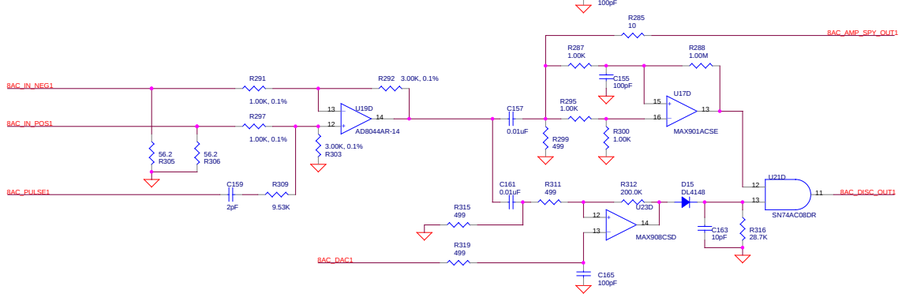
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

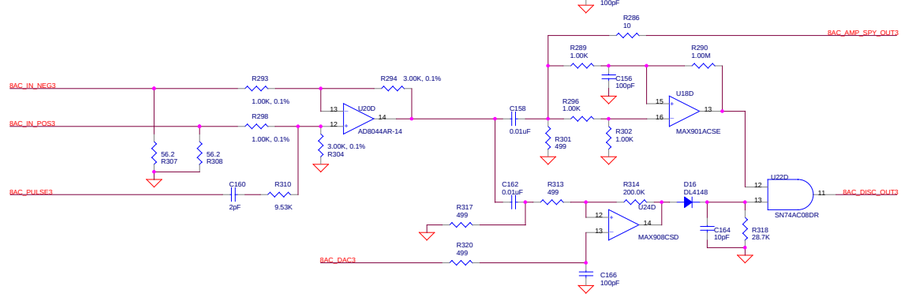


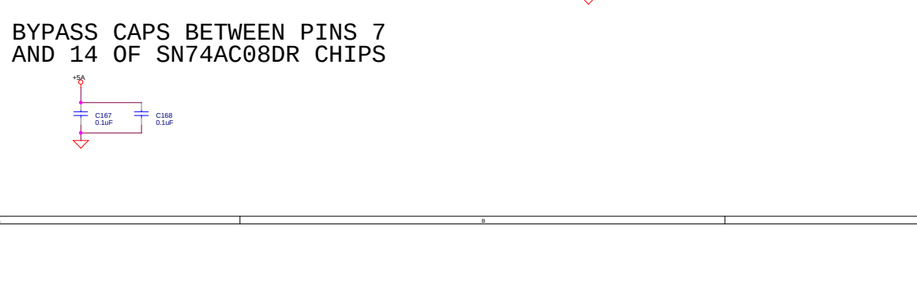












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

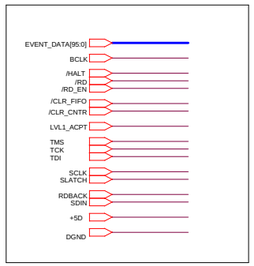
CHANGES FROM REV0

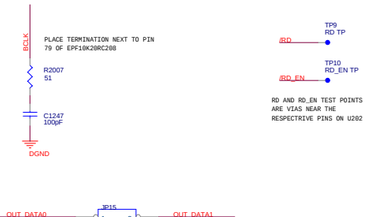
1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

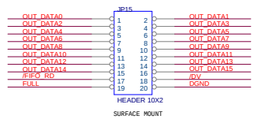
Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

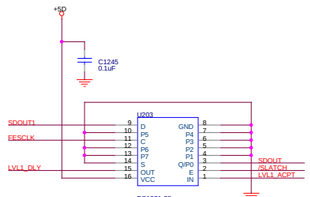
Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-133	Rev
Date: Wednesday, November 01, 2000	Sheet 5 of 34	

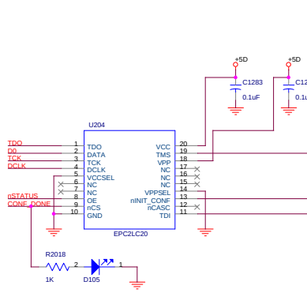
INPUTS

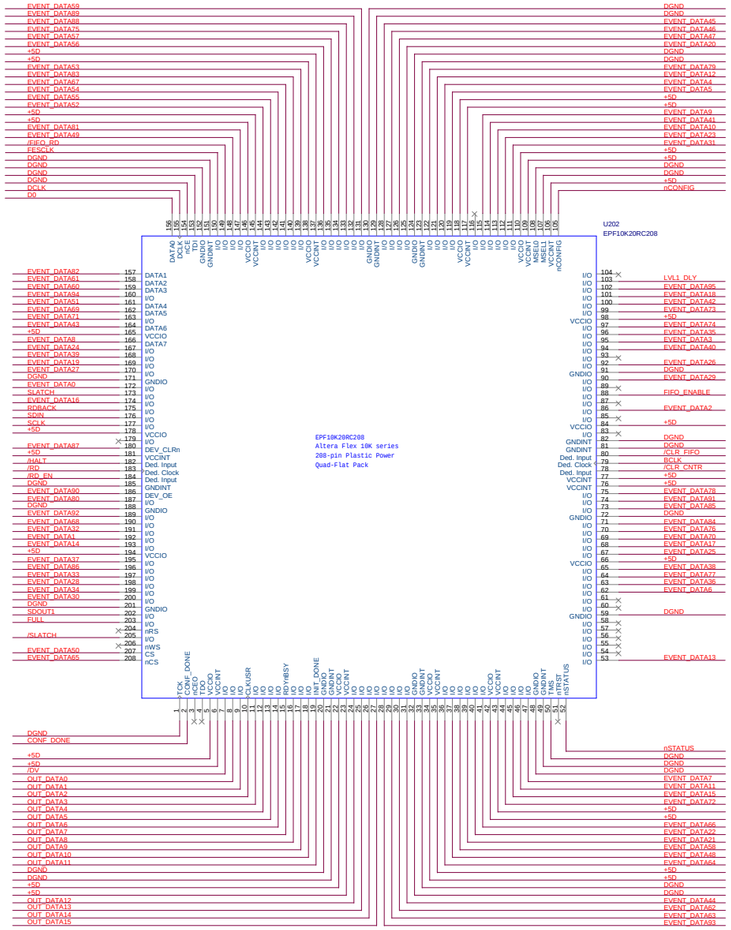




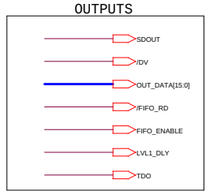






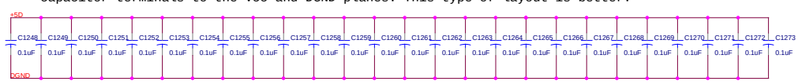


OUTPUTS



Place bypass caps next to pins 5, 6, 22, 23, 34, 35, 42, 43, 66, 76, 77, 84, 98, 106 ,109, 110, 117, 118, 137, 138, 145, 146, 165, 178, 181, and 194 of EPF10K20RC208

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



CHANGES FROM REV0

1. ADDED /HALT SIGNAL TO FIVE EVENT FIFO
2. ADDED JTAG I/O
3. CHANGED EEPROMTO GO ON COMMON JTAG LOOP
4. CHANGED TEST HEADER TO SURFACE MOUNT PART
5. CHANGED BCLK TERMINATION VALUES

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title: FIVE EVENT FIFO
Size: D | Document Number: 5.3.13.002-0313-212 | Rev:
Date: Tuesday, October 03, 2000 | Sheet 6 of 34

INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
/ROC_RST
BCLK
TDO
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG
/SLATCH
SDOUT

U120
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

U121
3D7110D-4

U122
DS1021-25

+5D
R1879
51
C932
100pF

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C933 C934 C935 C936 C937 C938 C939 C940 C941 C942 C943 C944 C945 C946 C947 C948
0.1uF
DGND

CHANGES FROM REV0

1. **CHANGED BCLK TERMINATION**
2. **1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK**
3. **REMOVED CLR_SRL SIGNAL**
4. **REMOVED PULL-UP RESISTORS FROM DELAY CHIP**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

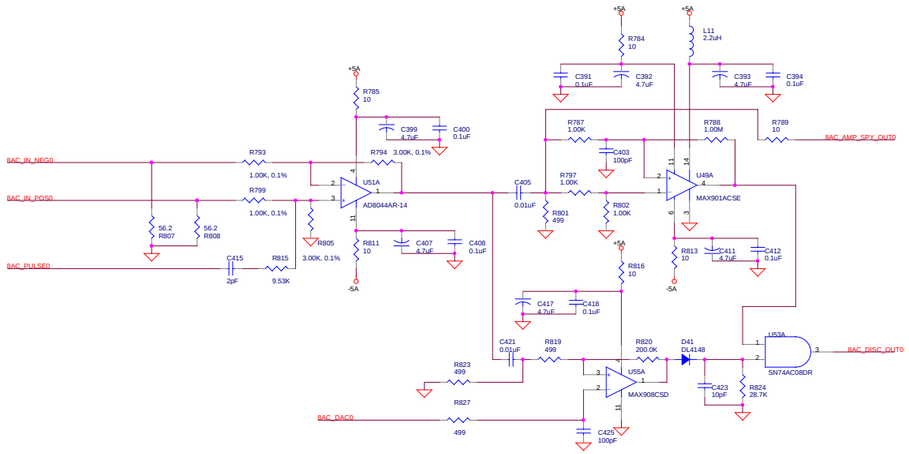
Title	16DLY	
Size D	Document Number 5.3.13.002-0313-100 -299	Rev
Date: Tuesday, October 03, 2000	Sheet 7 of 34	

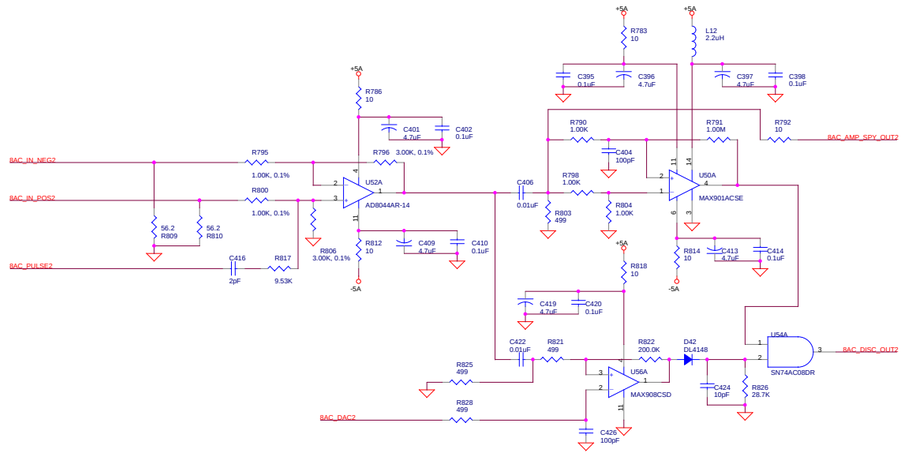
INPUTS

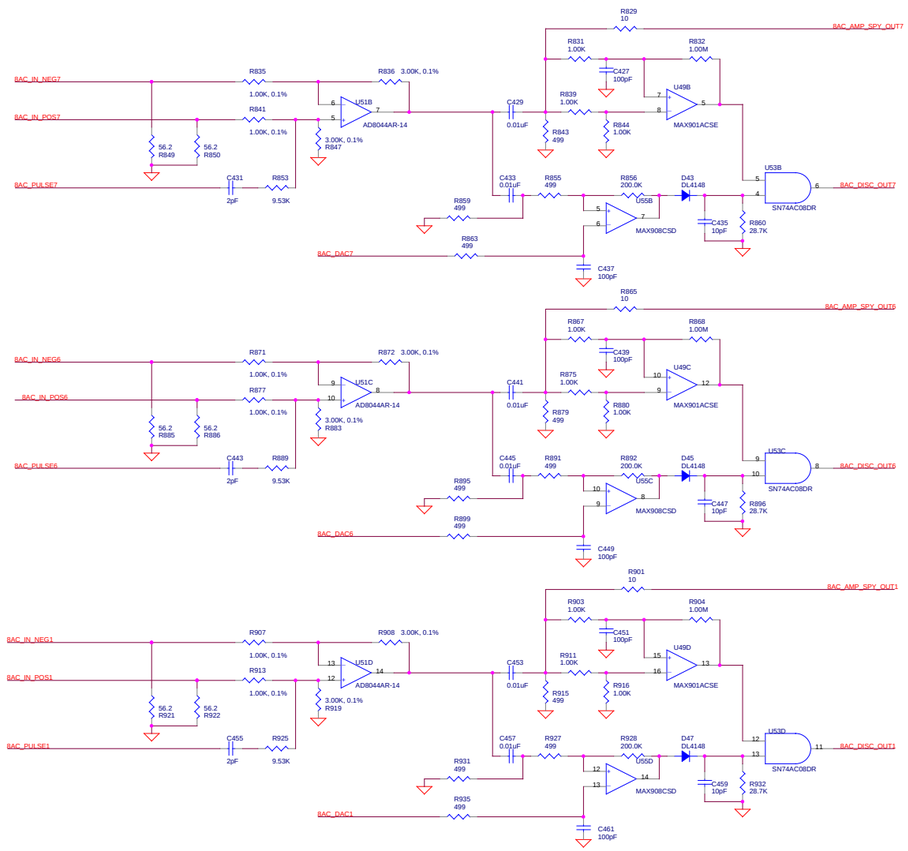
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

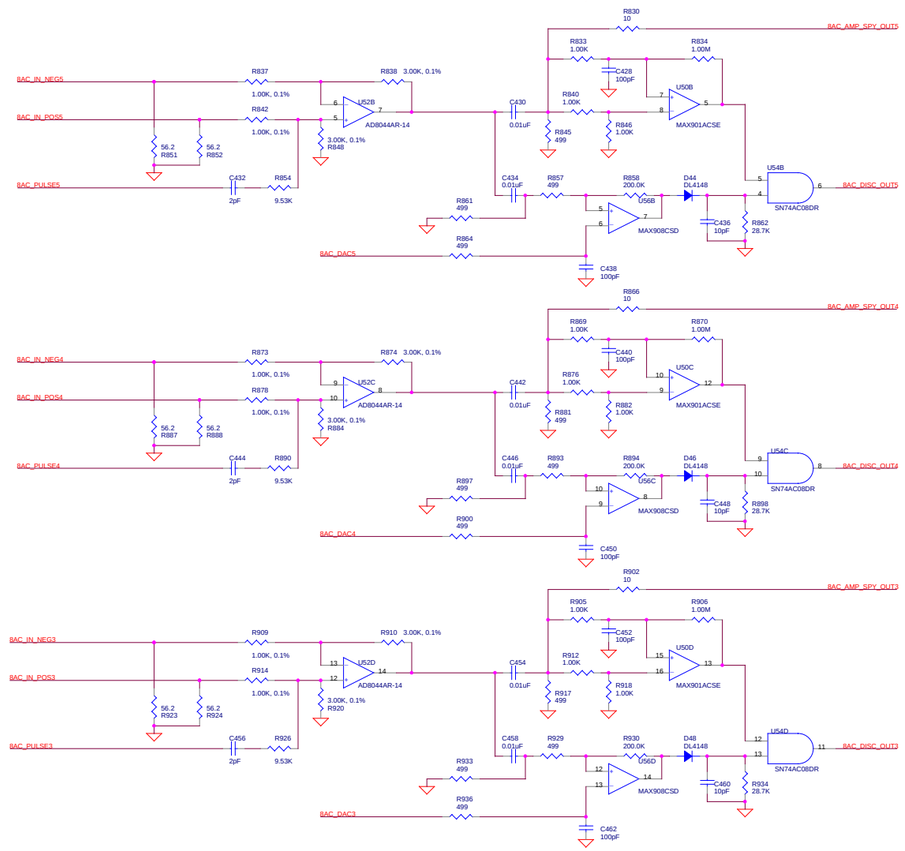
OUTPUTS

BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

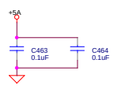








BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS



CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

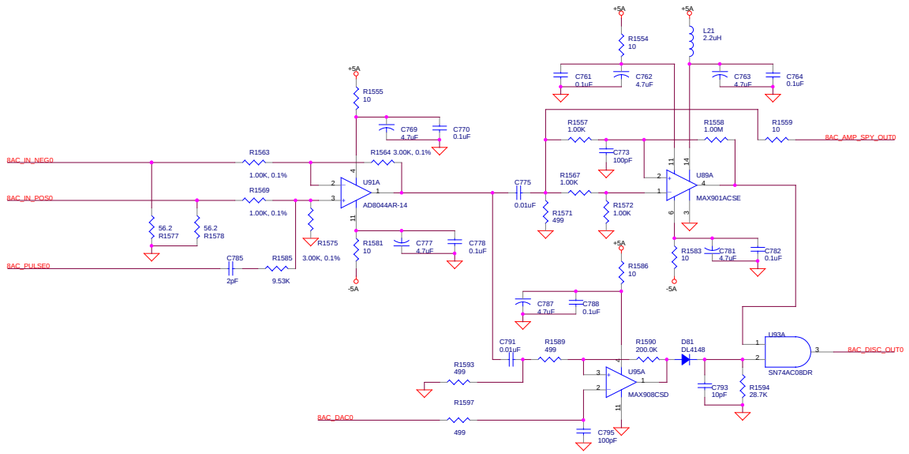
Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-131	Rev
Date: Wednesday, November 01, 2000	Sheet 8 of 34	

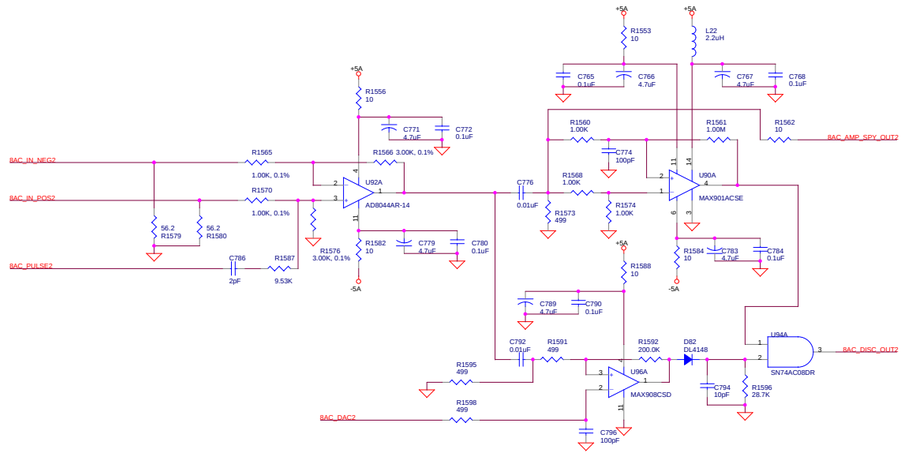
INPUTS

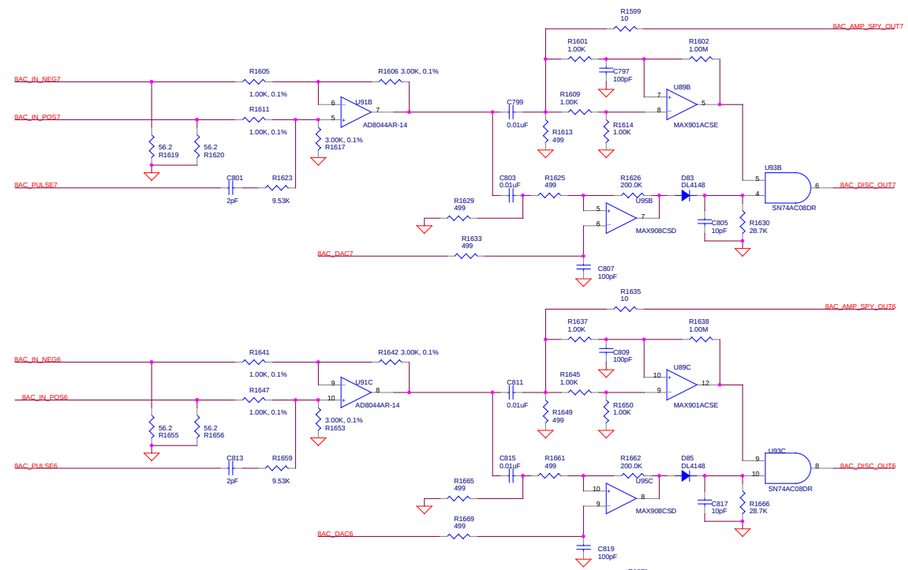
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

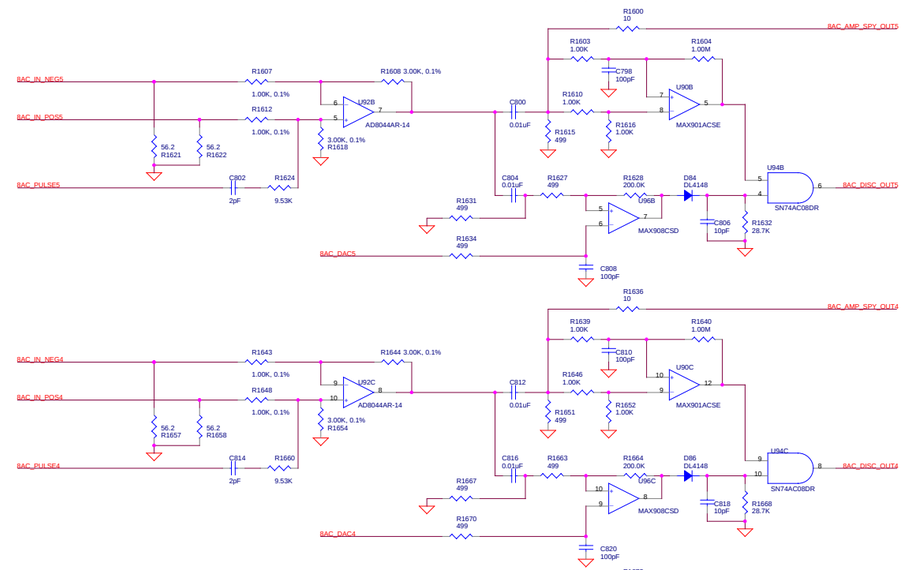
OUTPUTS

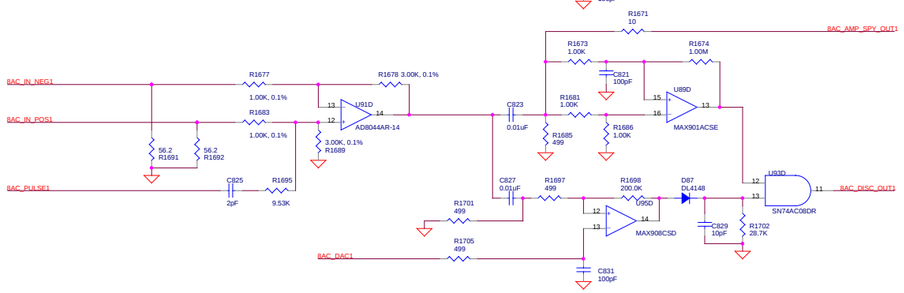
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

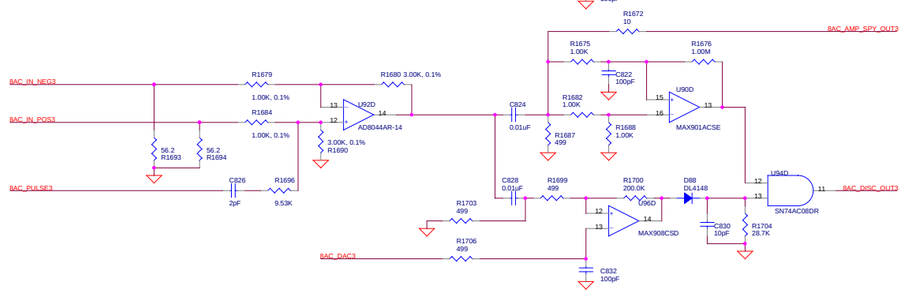




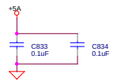








BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS



CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-142	Rev
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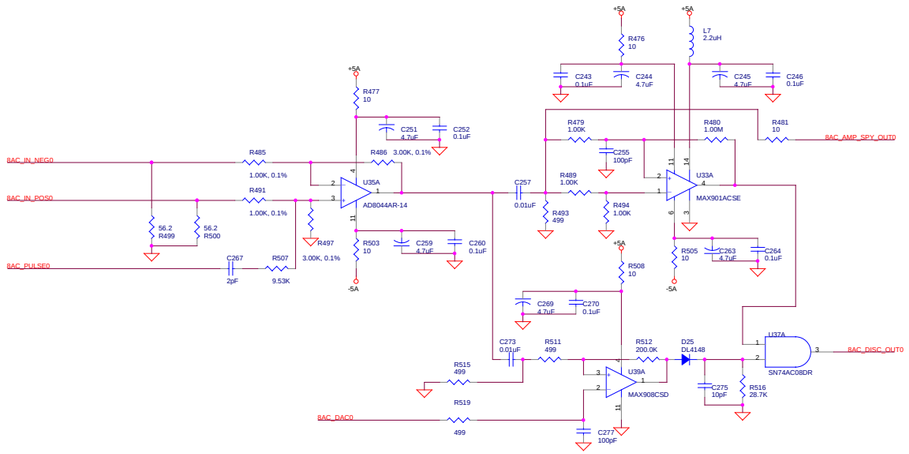
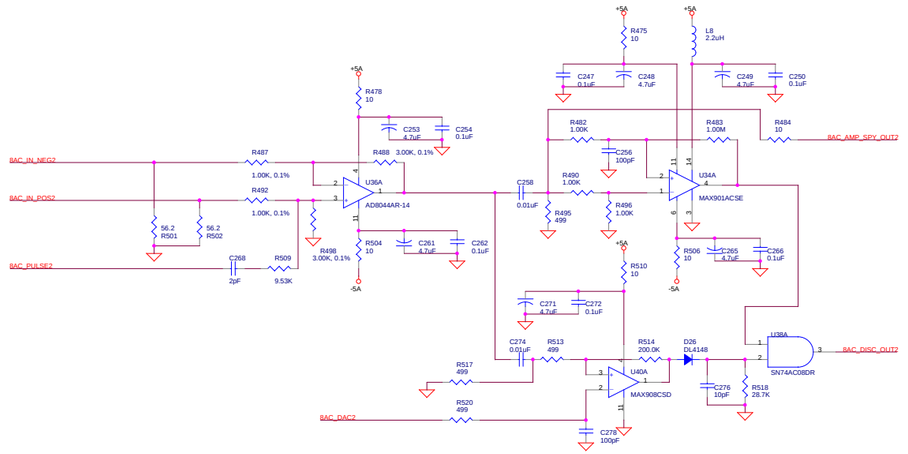
INPUTS

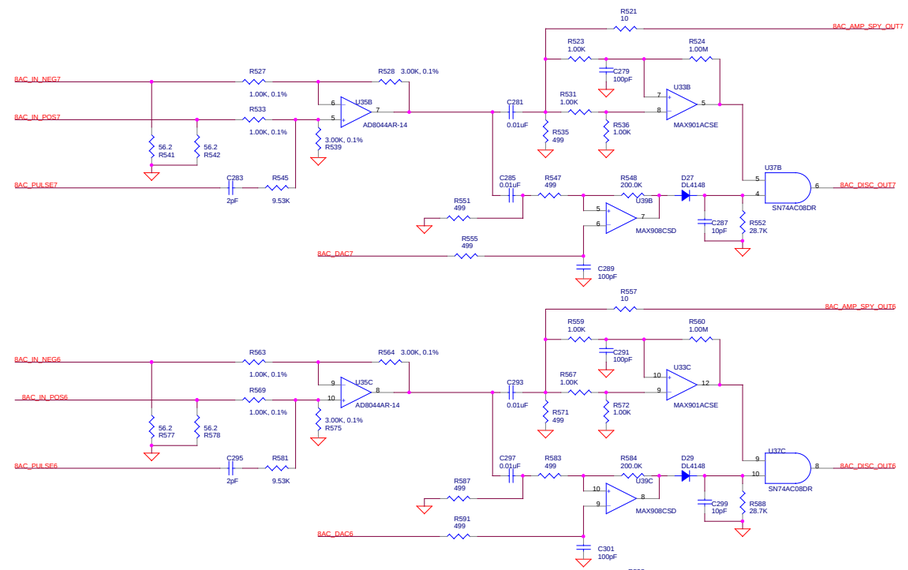
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

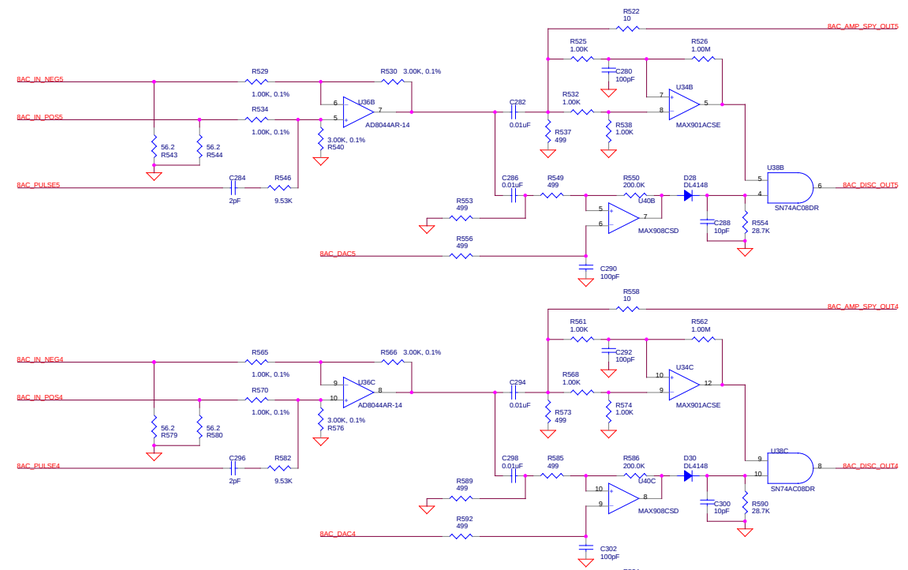
OUTPUTS

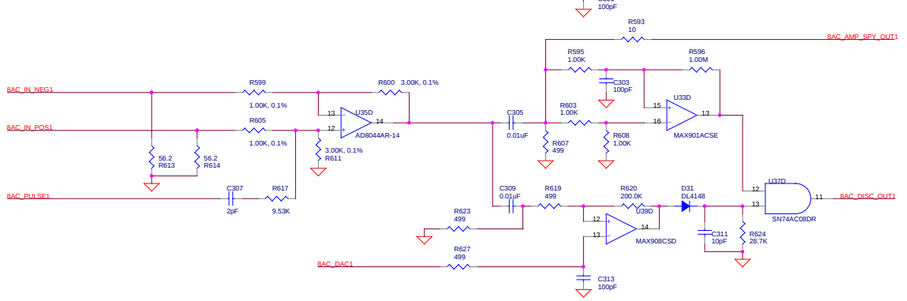
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

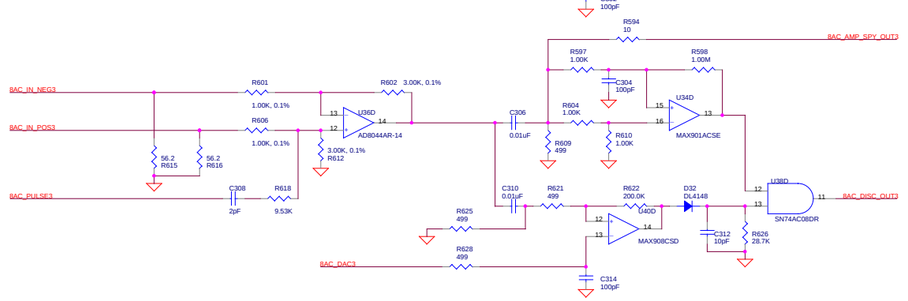


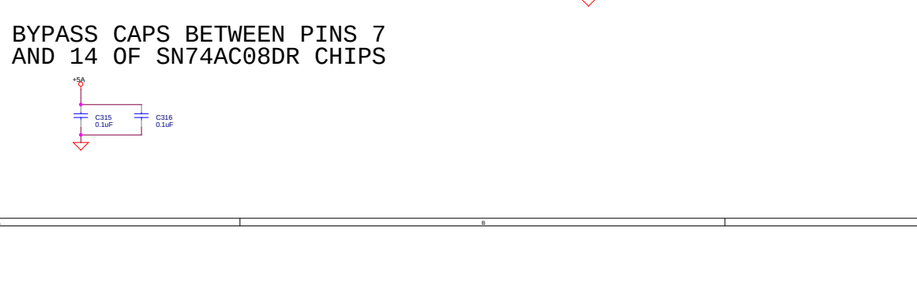


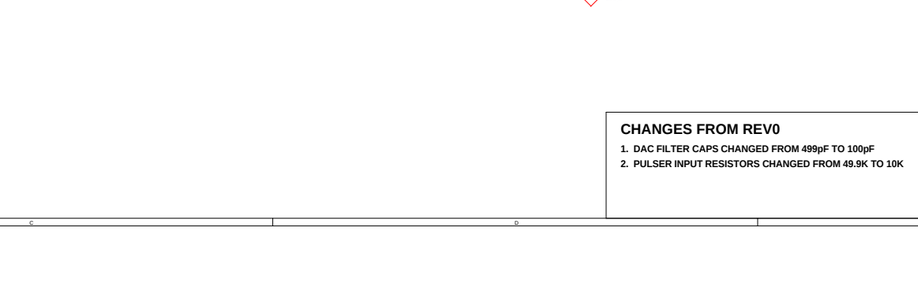












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-137	Rev
Date: Wednesday, November 01, 2000	Sheet 10 of 34	

INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3

U132
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15

OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG

/SLATCH

/ROC_RST
BCLK

U133
3D7110D-4

U134
DS1021-25

+5D

R1895
51

C1000
100pF

SDOUT

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016
0.1uF
DGND

CHANGES FROM REV0

1. CHANGED BCLK TERMINATION
2. 1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK
3. REMOVED CLR_SRL SIGNAL
4. REMOVED PULL-UP RESISTORS FROM DELAY CHIP

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

Title: 16DLY

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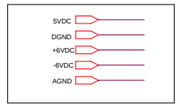
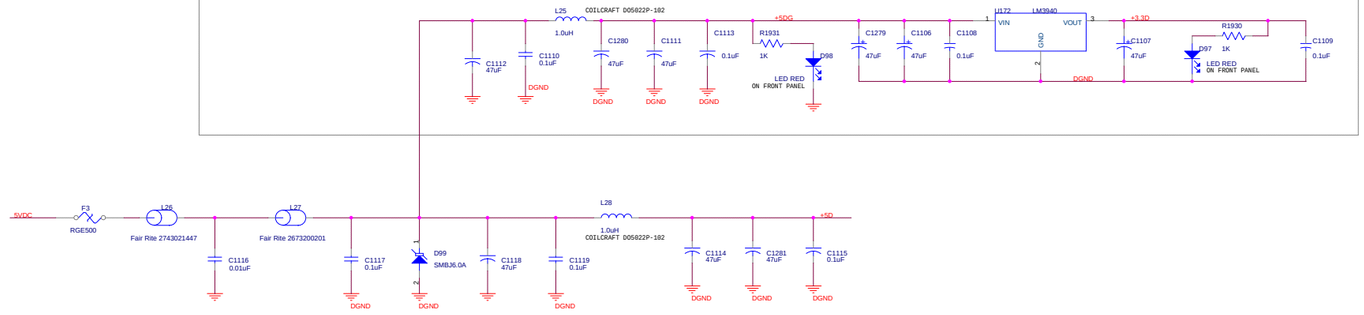
INPUTS



DIGITAL POWER CONDITIONING

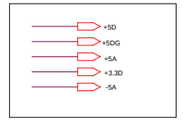
NEED TO HANDLE 5 AMPS.

COMPONENTS IN THIS BOX MUST BE LOCATED
NEAR THE GLINK POWER PLANE AND THE INPUT
TO THIS SECTION MUST BE A LARGE TRACE

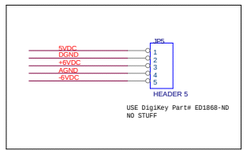


Each filter component must have its OWN via to DGND.

OUTPUTS



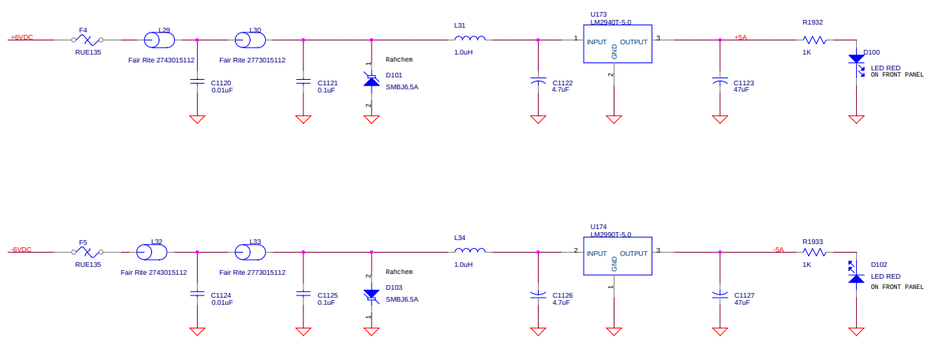
ALTERNATE POWER INPUT CONNECTOR



ALL LEDS ATE SIZE T! AND MOUNTED ON FRONTPANEL

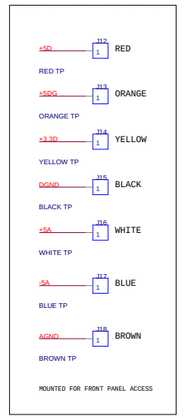
ANALOG POWER CONDITIONING

NEED TO HANDLE 1 AMPS.



Each filter component must have its OWN via to DGND.

TEST POINTS



CHANGES FROM REV0

1. ADDED FRONT PANEL TEST POINTS
2. CHANGED 100uF CAPACITORS TO SURFACE MOUNT
3. CHANGED FILTER COILS TO PART RATED FOR HIGHER CURRENT
4. CHANGED TAN. CAPS TO USE AVAIL. PARTS
5. CHANGED LED RESISTORS TO 1K FOR UNIFORMITY

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	POWER CONDITIONING	
Size D	Document Number 5.3.13.002-0013-110	Rev
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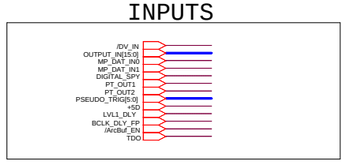
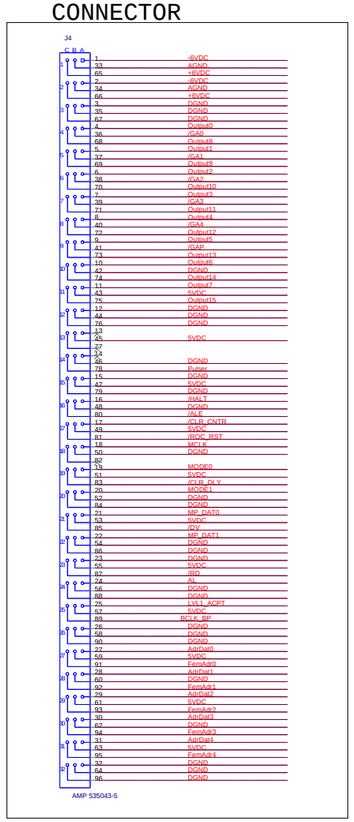
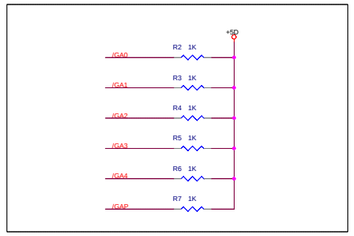
INPUTS



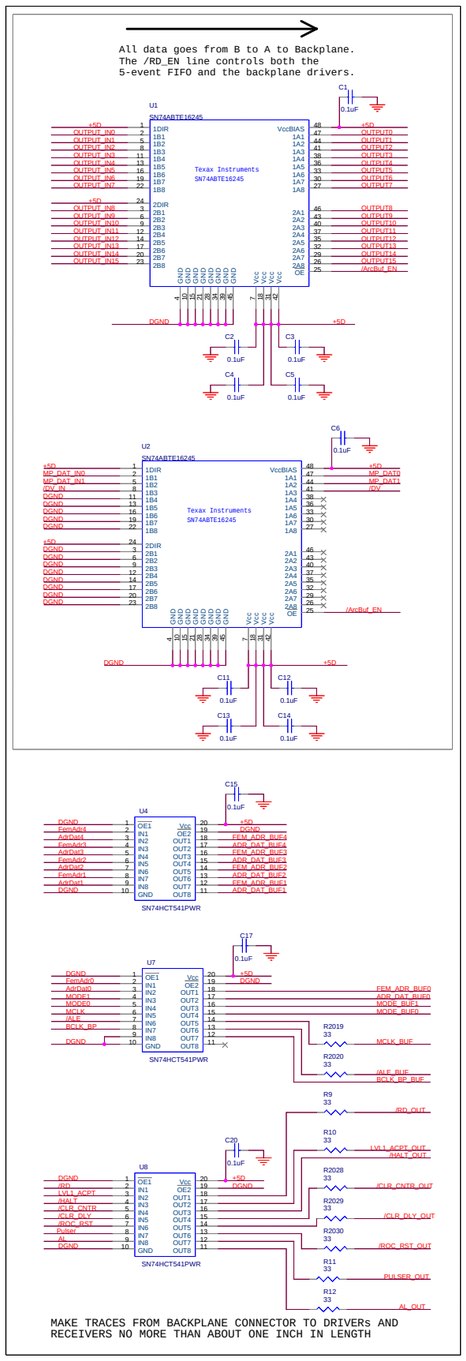
DIGITAL BACKPLANE CONNECTOR



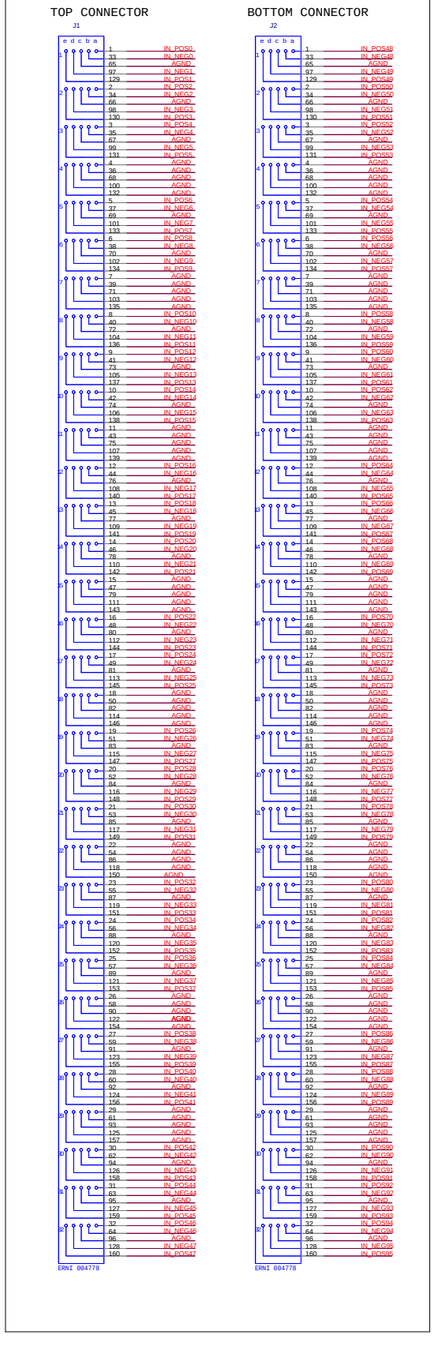
GLOBAL ADDRESS PULL-UPS



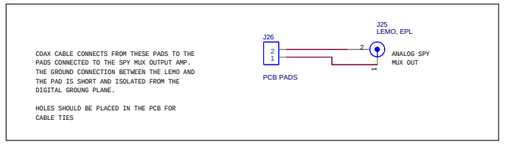
VME BUS DRIVERS AND RECEIVERS



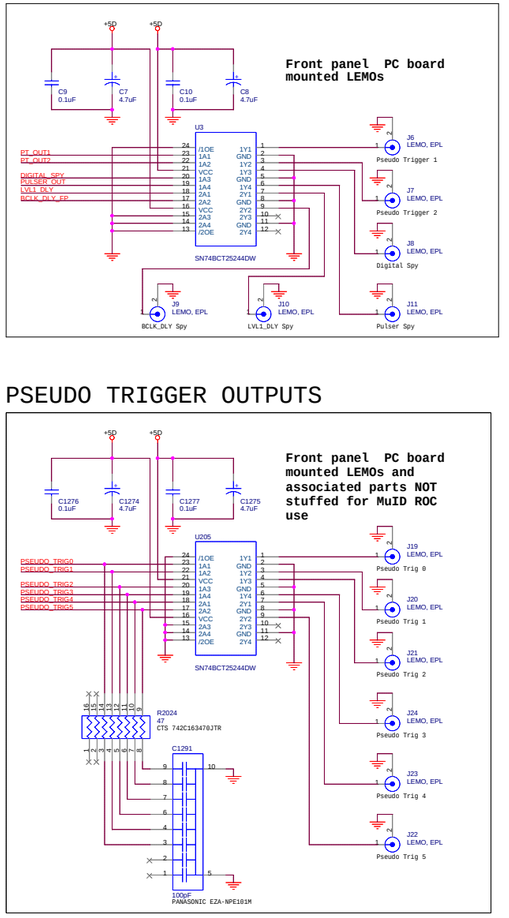
ANALOG INPUT CONNECTORS



FRONT PANEL ANALOG SPY OUTPUT

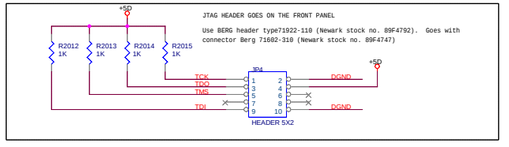


FRONT PANEL 50 OHM TTL OUTPUTS

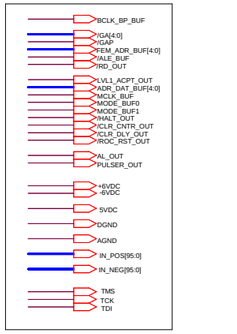


PSEUDO TRIGGER OUTPUTS

JTAG CONNECTOR



OUTPUTS



CHANGES FROM REV0

1. ADDED PSEUDO TRIGGER OUTPUTS
2. REMOVED BCLK_FP
3. PLACED JTAG HEADER ON THIS PAGE
4. ADDED 33 OHM SOURCE TERMINATION TO ALL CLOCK LINES
5. CORRECTED PART NUMBER FOR 74AHCT541
6. ADDED ADDITIONAL SERIES TERM ON INPUT DRIVER

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title: IO BLOCK		
Size: D	Document Number: 5.3.13.002-0313-200	Rev
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INPUTS

AMP_SPY_OUT[95:0]

SPY_MUX_SEL[6:0]

+5A

-5A

AGND

U140 ADG426BRS — C1037 0.1uF — R1908 10 — C1039 4.7uF — C1040 0.1uF — R1910 402.0 — R1911 1210.0 — U142A AD8044AR-14 — R1914 301.0 — R1916 10 — C1044 4.7uF — C1045 0.1uF — C1048 0.1uF

U141 ADG426BRS — C1038 0.1uF — R1909 10 — C1041 4.7uF — C1042 0.1uF — R1912 402.0 — R1913 1210.0 — U143A AD8044AR-14 — R1915 301.0 — R1917 10 — C1046 4.7uF — C1047 0.1uF — C1049 0.1uF

U144 ADG426BRS — C1050 0.1uF — R1918 402.0 — R1919 1210.0 — U142B AD8044AR-14 — R1922 301.0 — C1052 0.1uF

U145 ADG426BRS — C1051 0.1uF — R1920 402.0 — R1921 1210.0 — U143B AD8044AR-14 — R1923 301.0 — C1053 0.1uF

U146 ADG426BRS — C1054 0.1uF — R1924 402.0 — R1925 1210.0 — U142C AD8044AR-14 — R1928 301.0 — C1056 0.1uF

U147 ADG426BRS — C1055 0.1uF — R1926 402.0 — R1927 1210.0 — U143C AD8044AR-14 — R1929 301.0 — C1057 0.1uF

U138 ADG426BRS — C1034 0.1uF — R1906 402.0 — U139 LM6321M — R1904 10 — C1035 0.1uF — R1905 10.0 — C1036 0.1uF — R1907 10 — J27 PCB PADS

COAX CABLE CONNECTS FROM THESE PADS TO THE PADS CONNECTED TO THE FRONT PANEL LEMO

U142D AD8044AR-14

U143D AD8044AR-14

CHANGES FROM REV0

NO CHANGES

Phenix MuID ROC

Oak Ridge National Lab

Instrumentation and Controls Division

Title: ANALOG SPY MUXES

Size: D | Document Number: 5.3.13.002-0313-150 | Rev:

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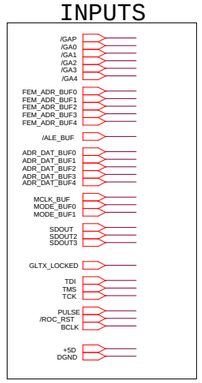
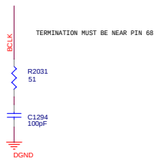
ADDRESS DECODER FPGA

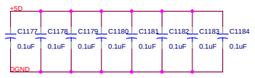
INPUTS

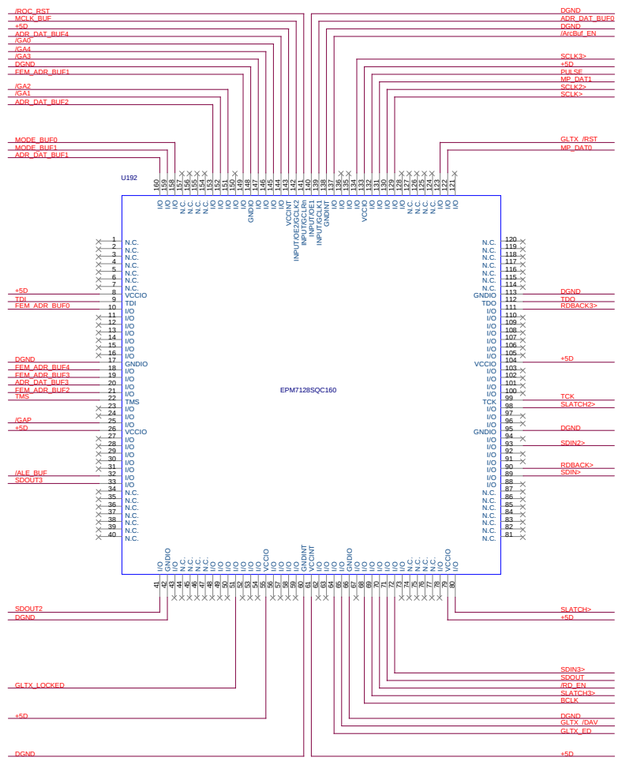




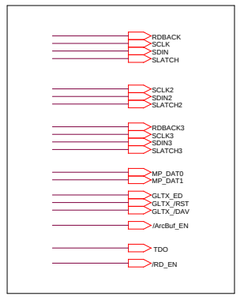
Place bypass caps next to each VCC pin for every IC

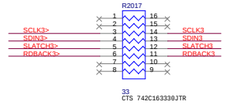
Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



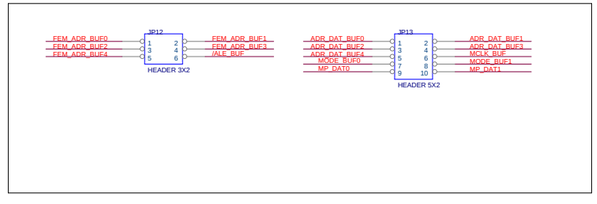


OUTPUTS





TEST HEADERS



CHANGES FROM REV0

1. **REMOVED TRI_STATE DRIVER AND ADDED SERIES TERMINATIONS**
2. **ADDED PULSE, ROC_RESET, AND BCLK TO EPM7128**
3. **REMOVED CONNECTIONS TO RDBACK2 AND /SRESET2**

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

Title: ADDR DEC		
Size: D	Document Number: 5.3.13.002-0313-220	Rev
Date: Tuesday, October 03, 2000	Sheet 15 of 34	

INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3

U123
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15

OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG

/SLATCH

/ROC_RST
BCLK

U124
3D7110D-4

U125
DS1021-25

+5D

SDOUT

R1883
51

C949
100pF

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C950 C951 C952 C953 C954 C955 C956 C957 C958 C959 C960 C961 C962 C963 C964 C965
0.1uF
DGND

CHANGES FROM REV0

1. **CHANGED BCLK TERMINATION**
2. **1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK**
3. **REMOVED CLR_SRL SIGNAL**
4. **REMOVED PULL-UP RESISTORS FROM DELAY CHIP**

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

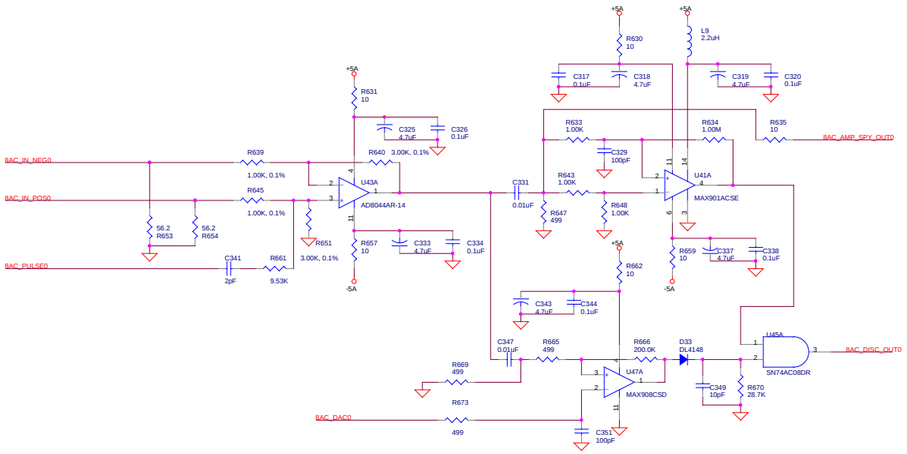
Title	16DLY	
Size D	Document Number 5.3.13.002-0313-100 -299	Rev
Date: Tuesday, October 03, 2000	Sheet 16 of 34	

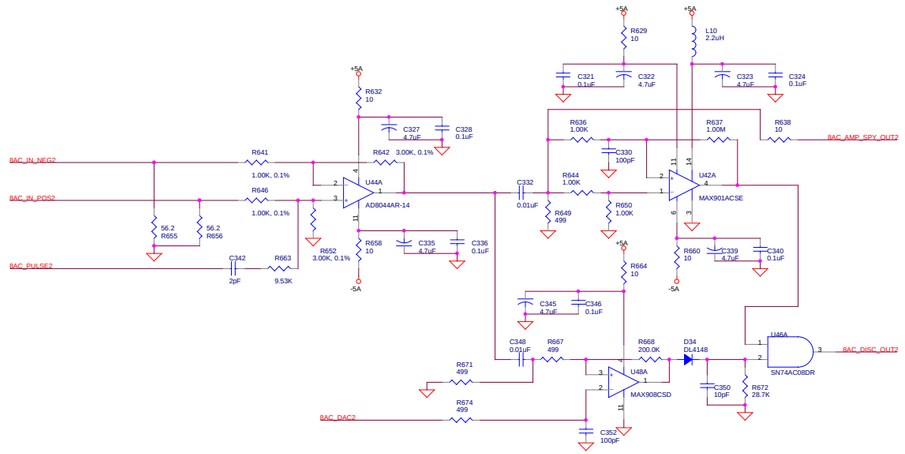
INPUTS

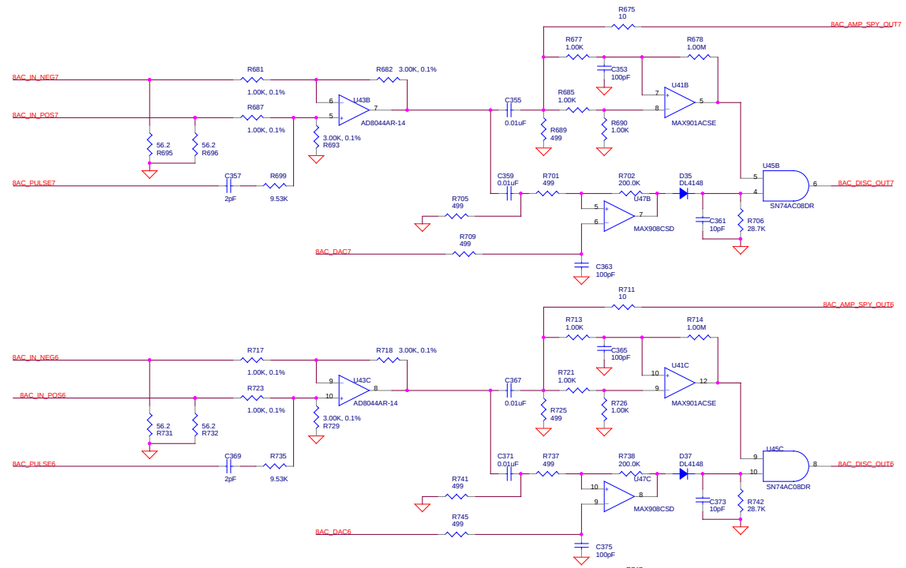
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

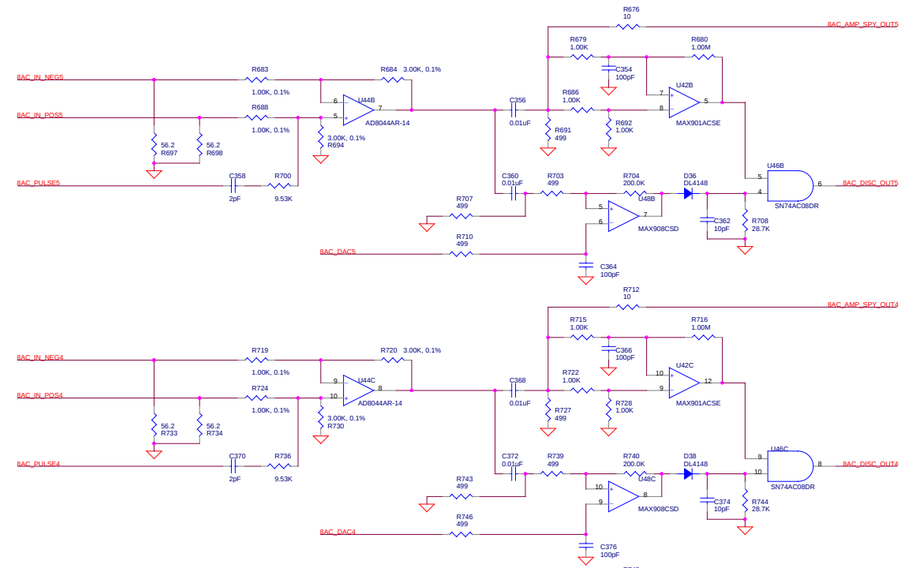
OUTPUTS

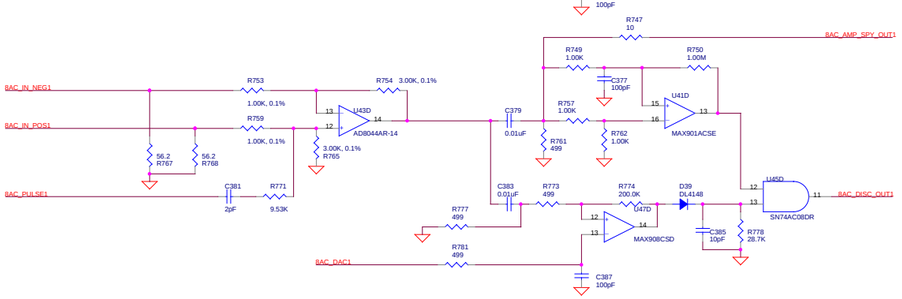
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

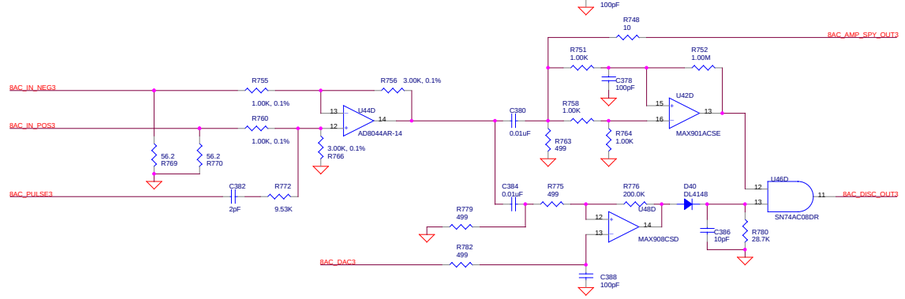


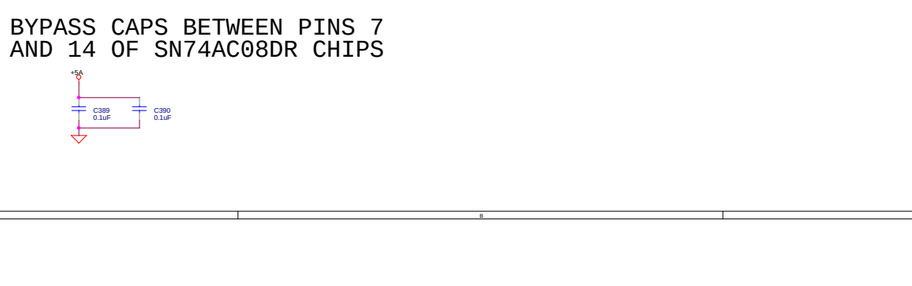












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

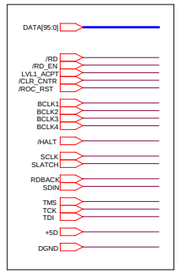
CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

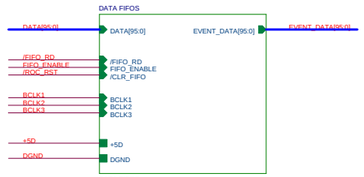
Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-132	Rev
Date: Wednesday, November 01, 2000	Sheet 17 of 34	

INPUTS

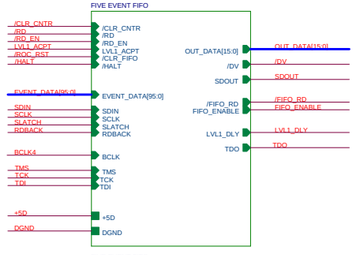


DATA FIFOS



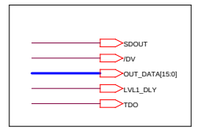
DATA FIFOS

FIVE EVENT FIFO



FIVE EVENT FIFO

OUTPUTS



CHANGES FROM REV0

1. **CHANGED TO USE JTAG HEADER ON I/O PAGE**

Phenix MuID ROC

Oak Ridge National Lab

Instrumentation and Controls Division

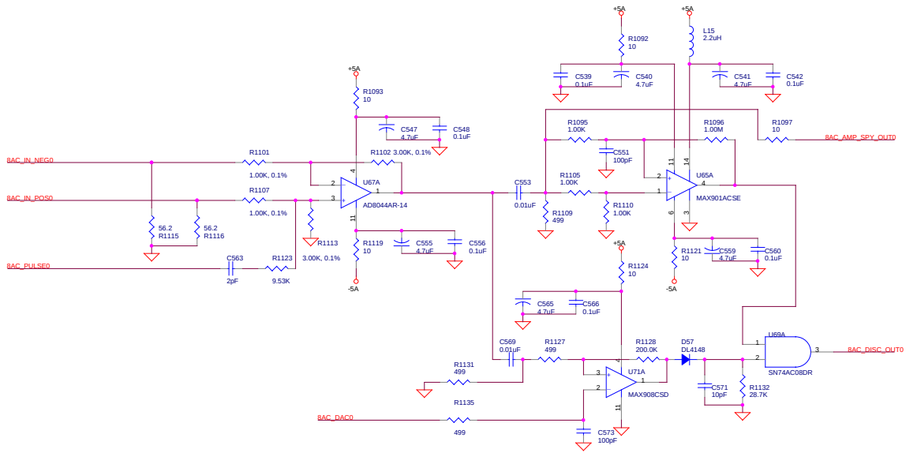
Title: NADMU TOP		
Size: D	Document Number: 5.3.13.002-0313-210	Rev:
Date: Tuesday, October 03, 2000	Sheet 18 of 34	

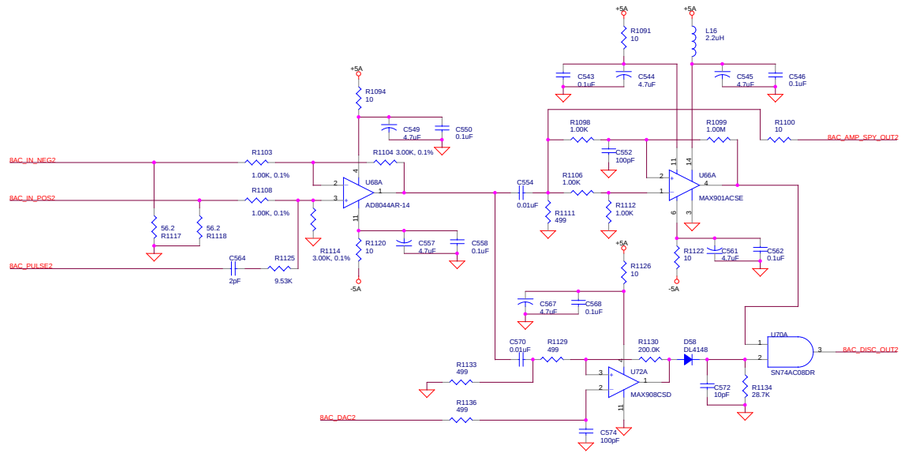
INPUTS

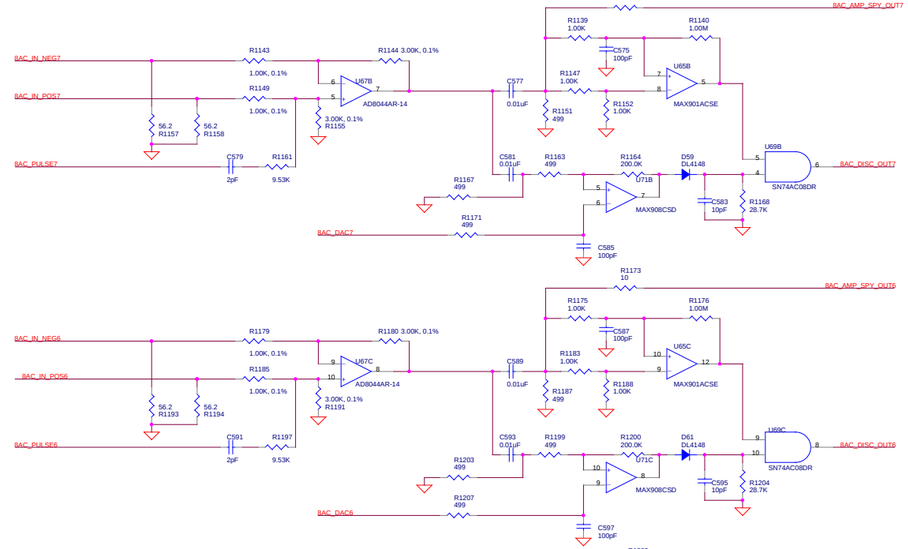
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

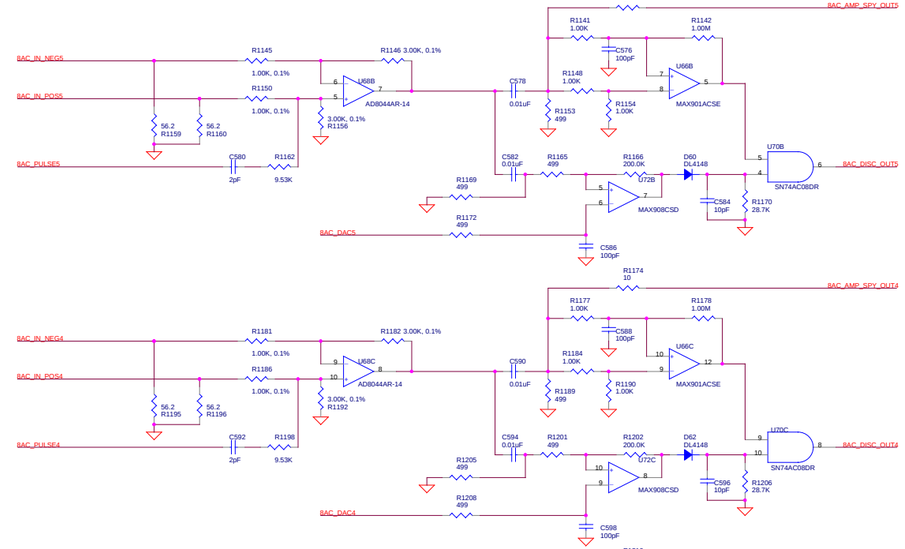
OUTPUTS

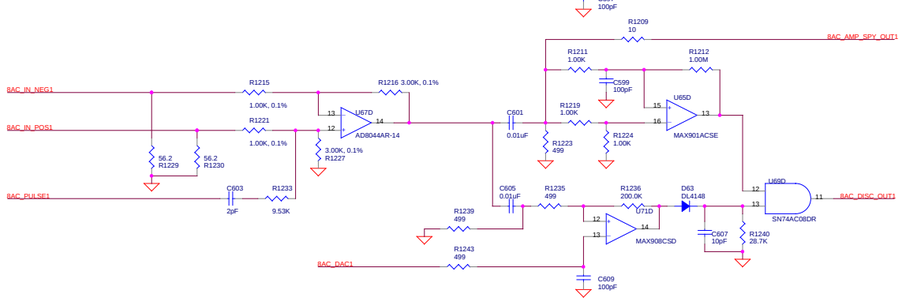
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

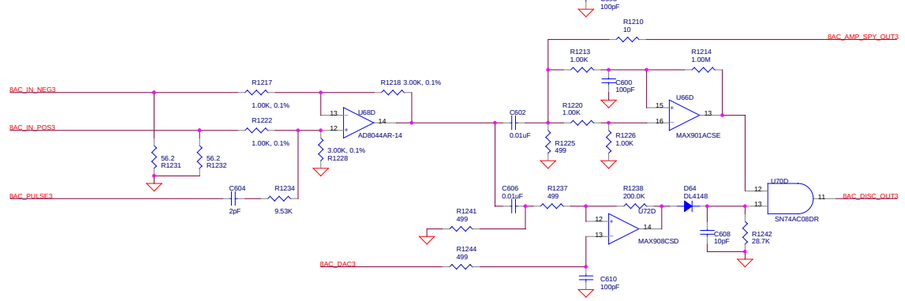


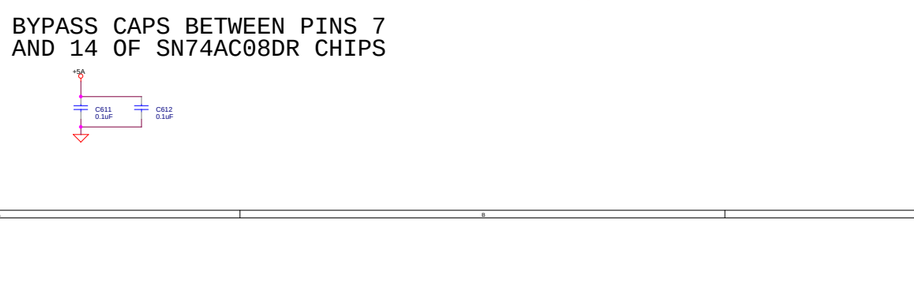


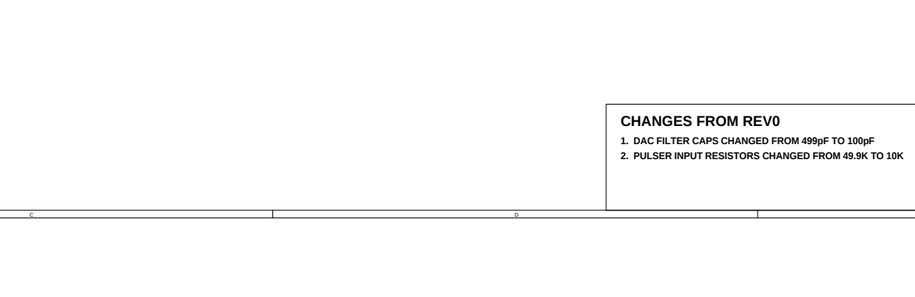












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. DAC FILTER CAPS CHANGED FROM 499pF TO 100pF
2. PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

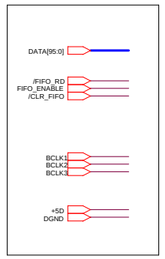
Title: BAMP COMP

Size: D | Document Number: 5.3.13.002-0313-139 | Rev:

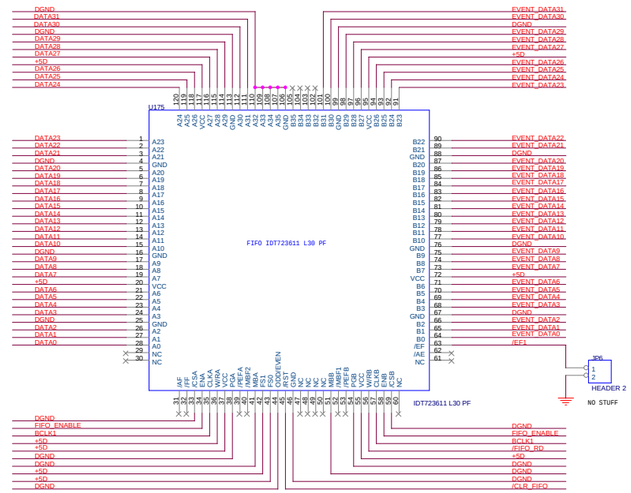
Date: Wednesday, November 01, 2000 | Sheet 19 of 34

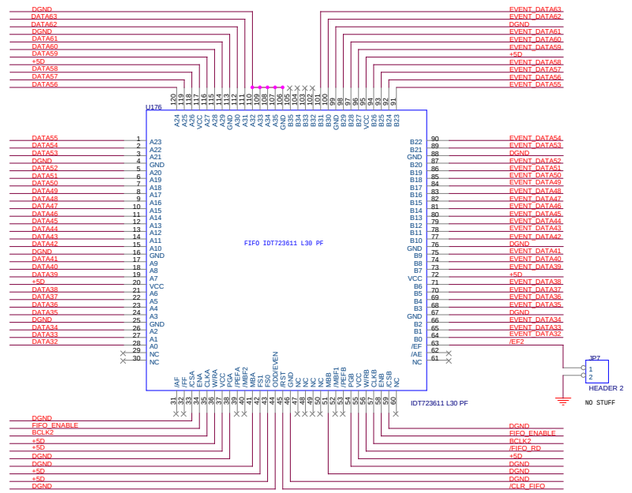
DATA FIFOS AND TEST HEADERS

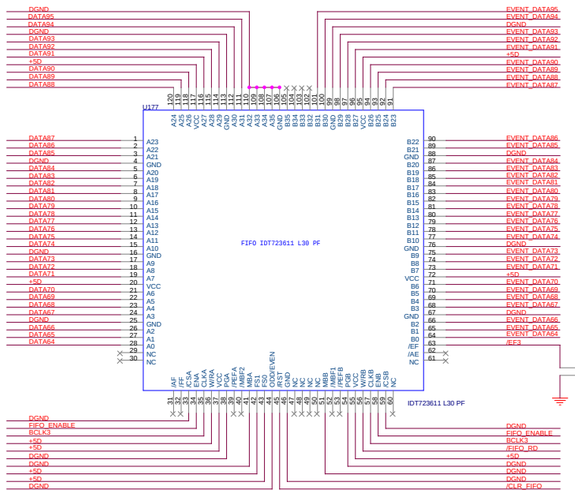
INPUTS

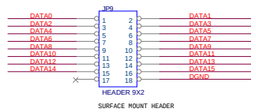


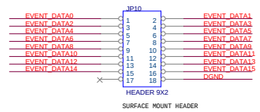
OUTPUTS







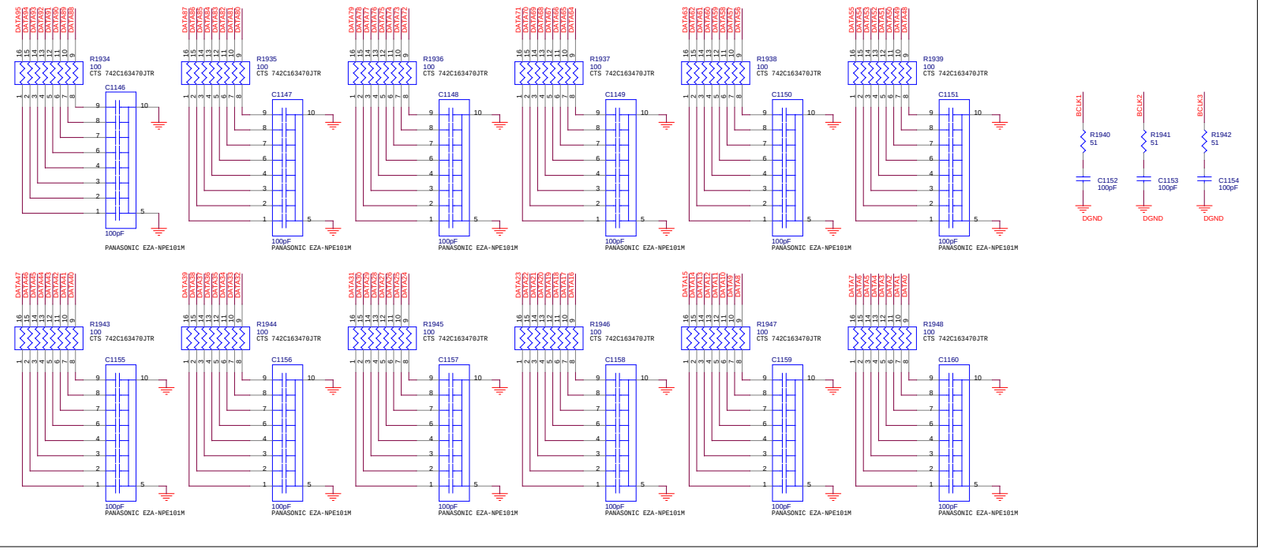




PARALLEL RC TERMINATION

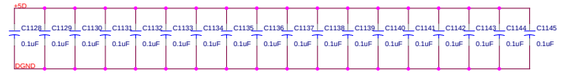
Use parallel RC termination in parallel with lines DATA0-DATA95 and BCLK. This is because the traces from Delay Mux FPGA will be long (>7.5 inches). Put a resistor and cap to DGND in parallel with each input pin. R = line impedance is assumed to be 100-ohms. Change if the actual line impedance differs. C > 100pf.

**Place Resistor/Cap as close to input pin as possible. **
** One BCLKn Termination PER CHIP! **



Place bypass caps next to pins 20, 37, 55, 72, 95, 117 for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



CHANGES FROM REV0

1. CHANGED BCLK TO BCLK1 ON TEST HEADER
2. CHANGED VALUE OF TERMINATION RESISTORS AND CAPS

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

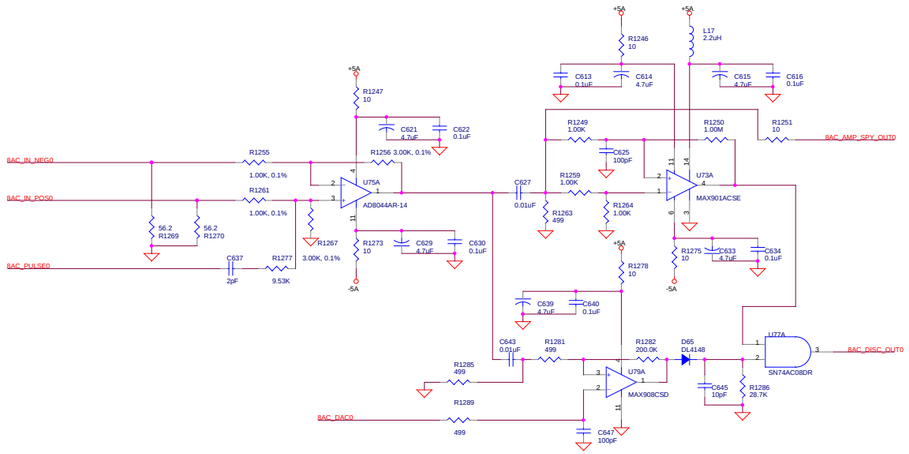
Title	DATA FIFOS	
Size D	Document Number 5.3.13.002-0313-211	Rev
Date: Tuesday, October 03, 2000	Sheet 20 of 34	

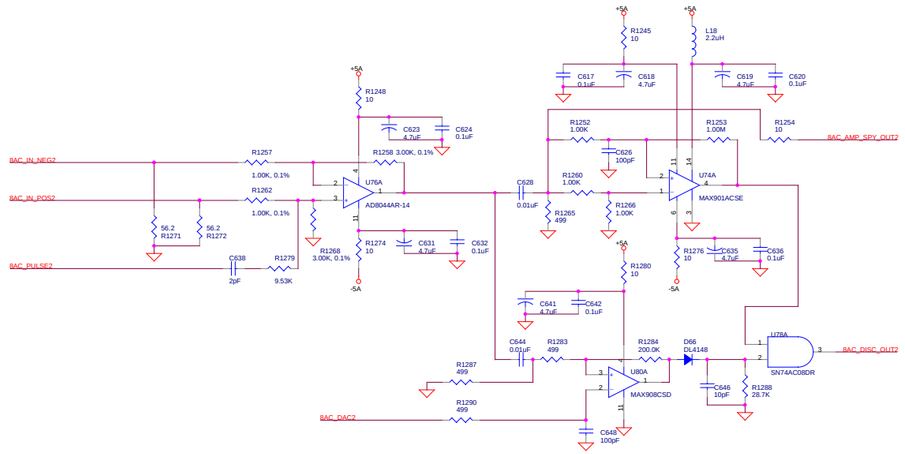
INPUTS

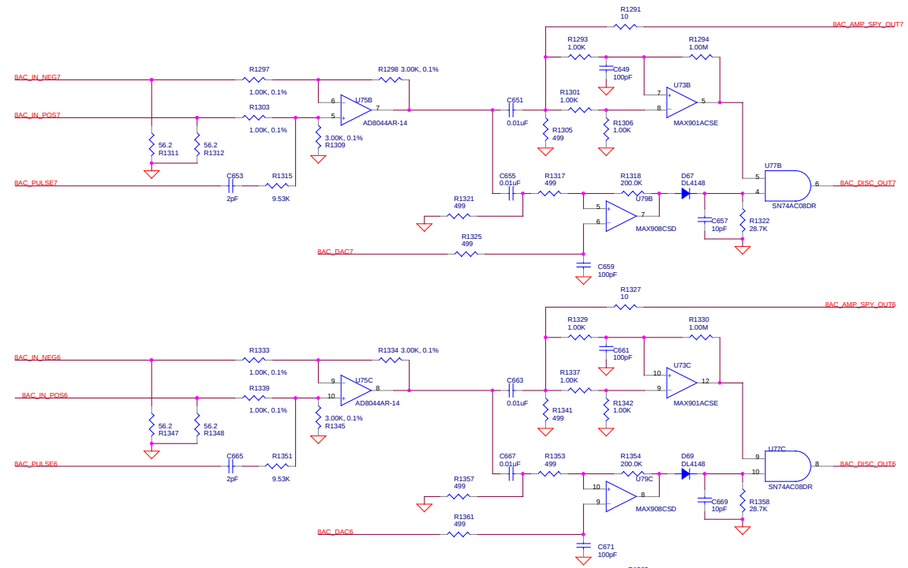
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

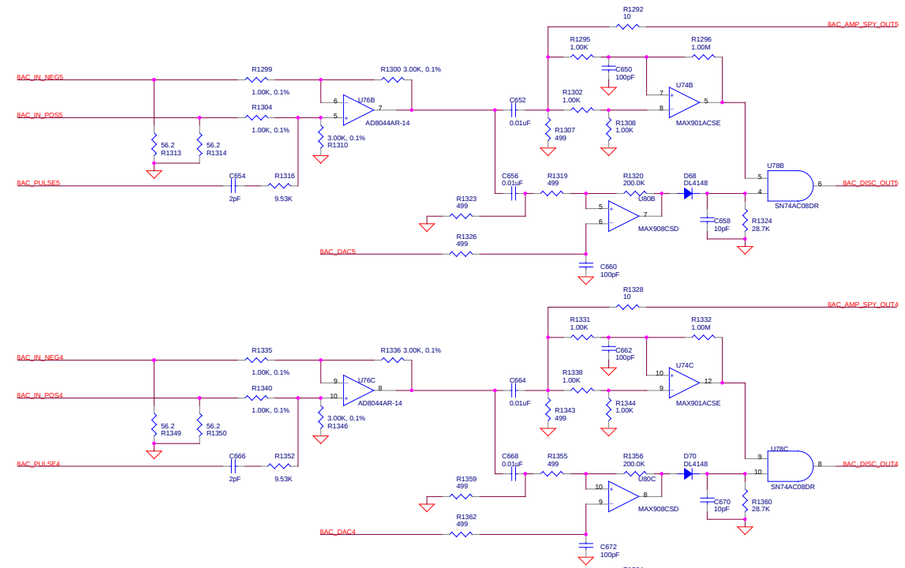
OUTPUTS

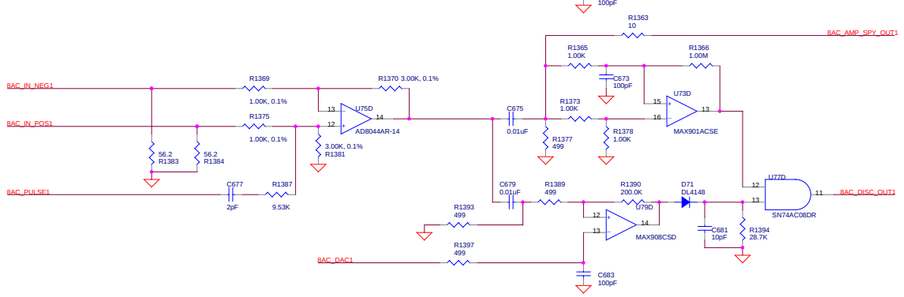
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

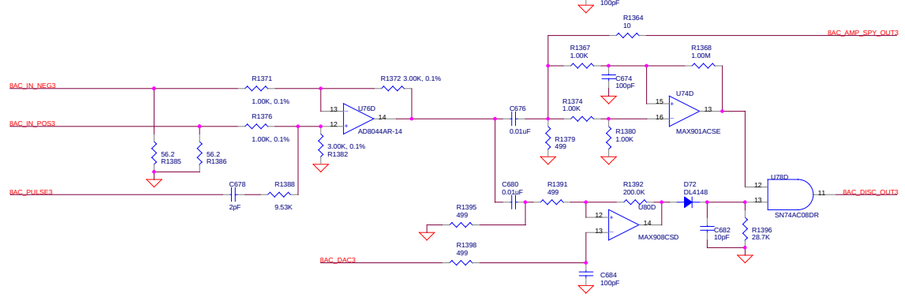


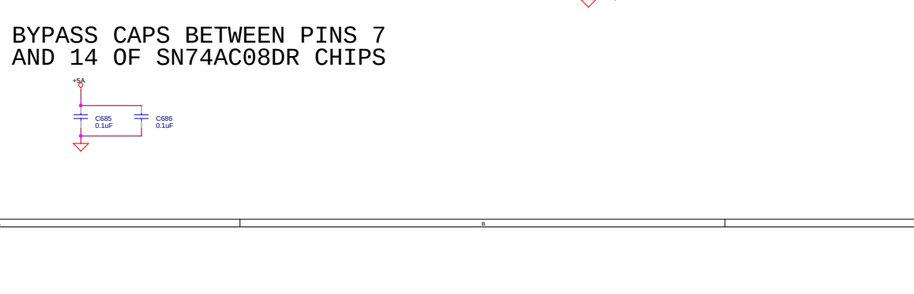


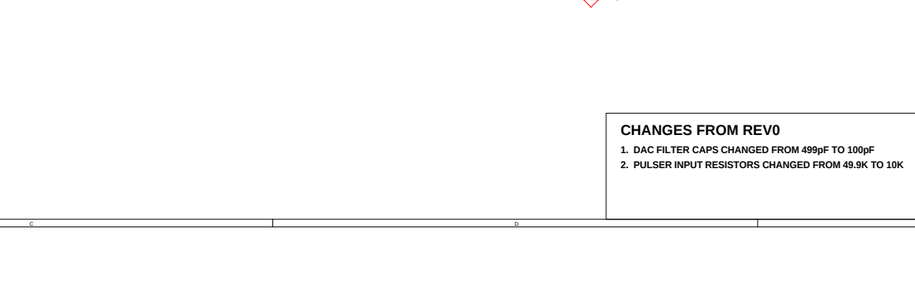












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

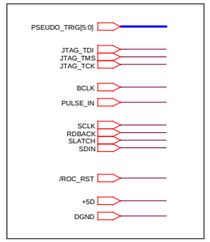
CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

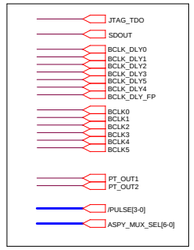
Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

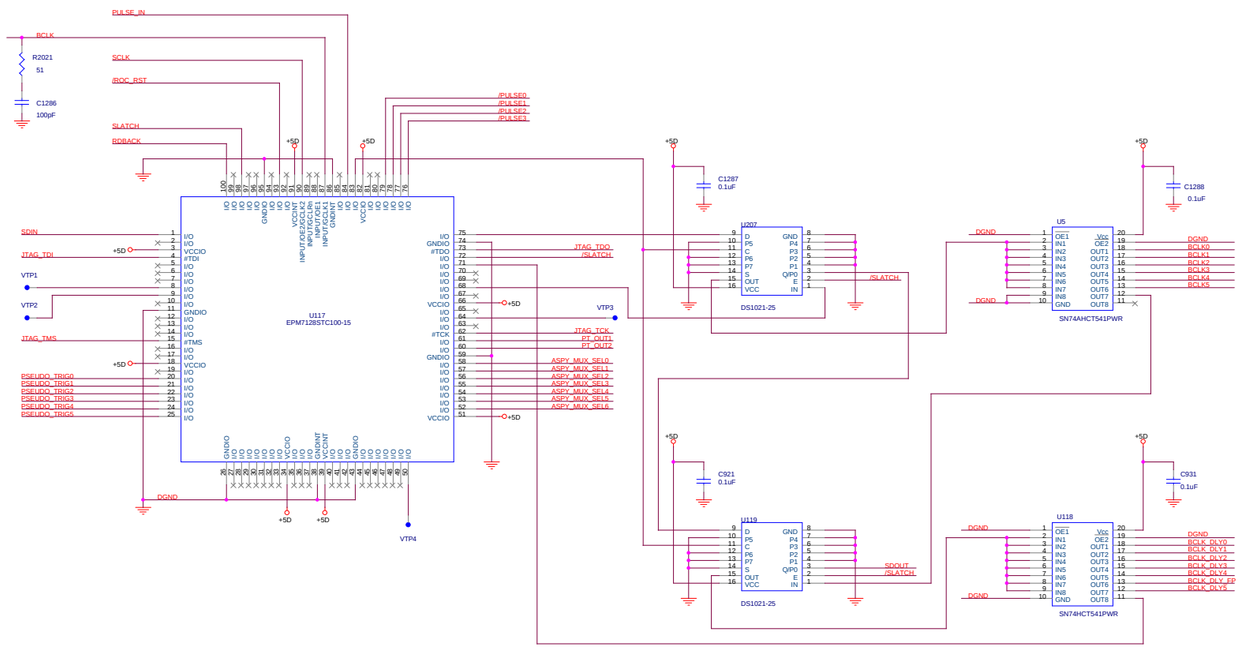
Title	BAMP COMP	
Size D	Document Number 5.3.13.002-0313-135	Rev
Date: Wednesday, November 01, 2000	Sheet 21 of 34	

INPUTS

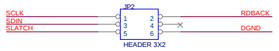


OUTPUTS





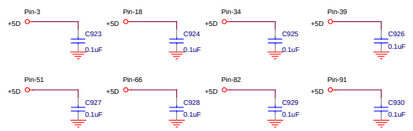
SERIAL DOWNLOAD



NO STUFF

BY-PASS CAPACITORS FOR Misc Serial FPGA

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



CHANGES FROM REV0

1. ADDED BCLK_DLY5
2. ADDED NO STUFF TO HEADER
3. SCLK TO DS1021 CONDITIONED TO ALLOW READBACK
4. REMOVED /SRESET
5. ADDED DELAY TO BCLKx SIGNALS
6. ADDED BCLK TERMINATION

Phenix MuID ROC

Oak Ridge National Lab

Instrumentation and Controls Division

Title	MISCSERIAL	
Size D	Document Number 5.3.13.002-0313-180	Rev
Date: Tuesday, October 03, 2000	Sheet 22 of 34	

INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
/ROC_RST
BCLK

U135
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

TDO
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG
/SLATCH

U136
3D7110D-4

U137
DS1021-25

SDOUT

+5D

R1899
51

C1017
100pF

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C1018 C1019 C1020 C1021 C1022 C1023 C1024 C1025 C1026 C1027 C1028 C1029 C1030 C1031 C1032 C1033
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF
DGND

CHANGES FROM REV0

1. CHANGED BCLK TERMINATION
2. 1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK
3. REMOVED CLR_SRL SIGNAL
4. REMOVED PULL-UP RESISTORS FROM DELAY CHIP

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

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INPUTS

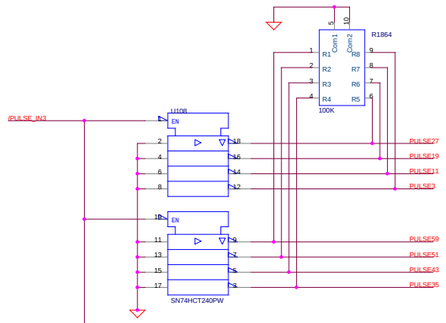
/PULSE_IN[3:0]

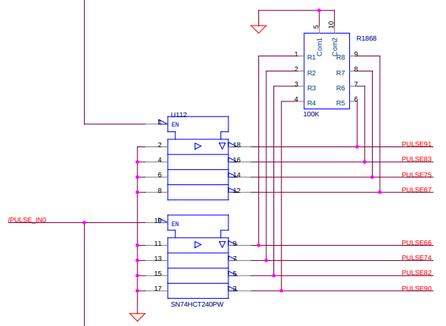
+5A

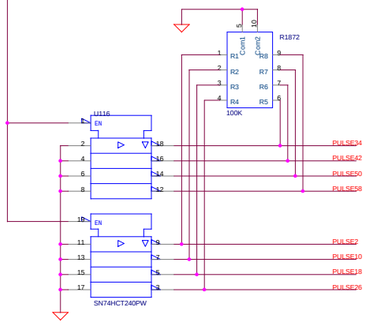
AGND

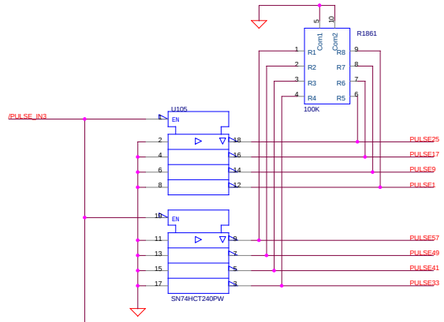
OUTPUTS

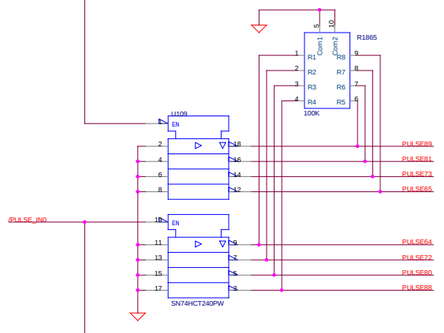
PULSE[95:0]

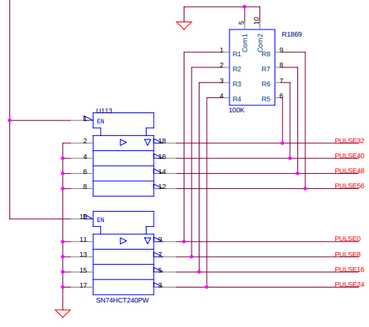


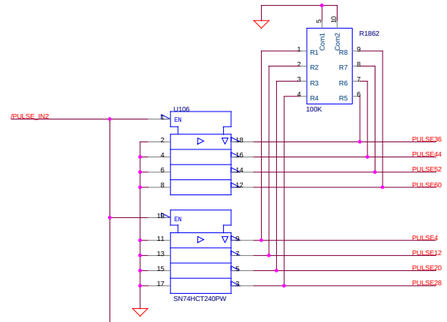


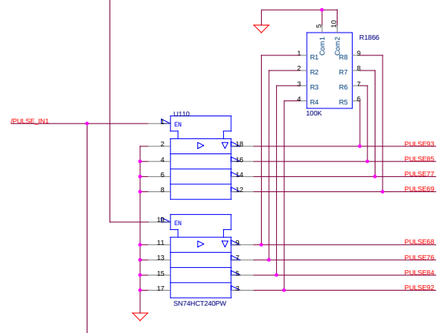


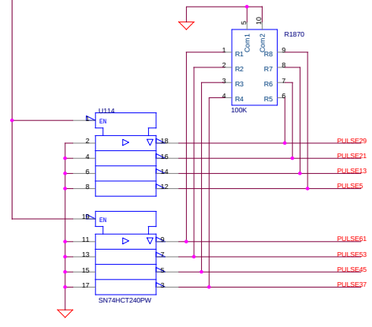


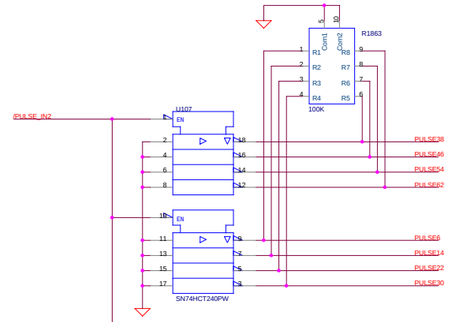


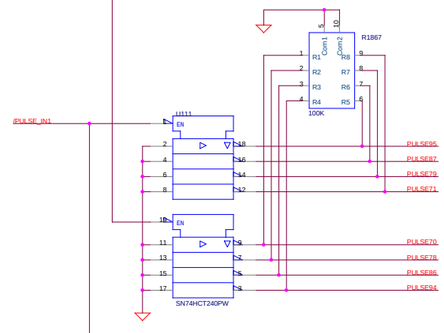


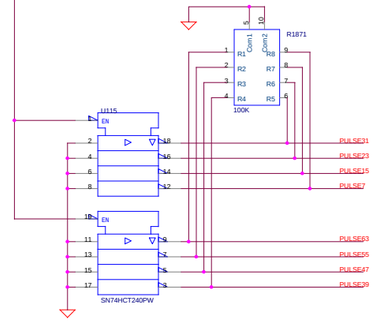




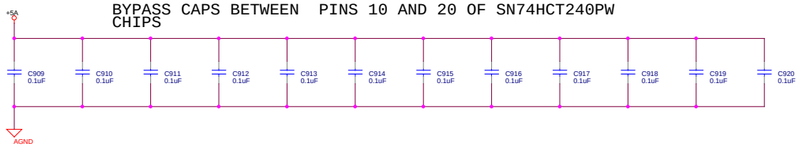








BYPASS CAPS BETWEEN PINS 10 AND 20 OF SN74HCT240PW CHIPS



CHANGES FROM REV0

1. PULSE DRIVER CHIPS CHANGED FROM 74ACT240 TO 74HCT240 TO REDUCE PULSE RISE TIME

2. MOVED ALL COMPONETS TO ANALOG POWER AND GROUND

Phenix MuID ROC

Oak Ridge National Lab

Instrumentation and Controls Division

Title	PULSE DRIVERS	
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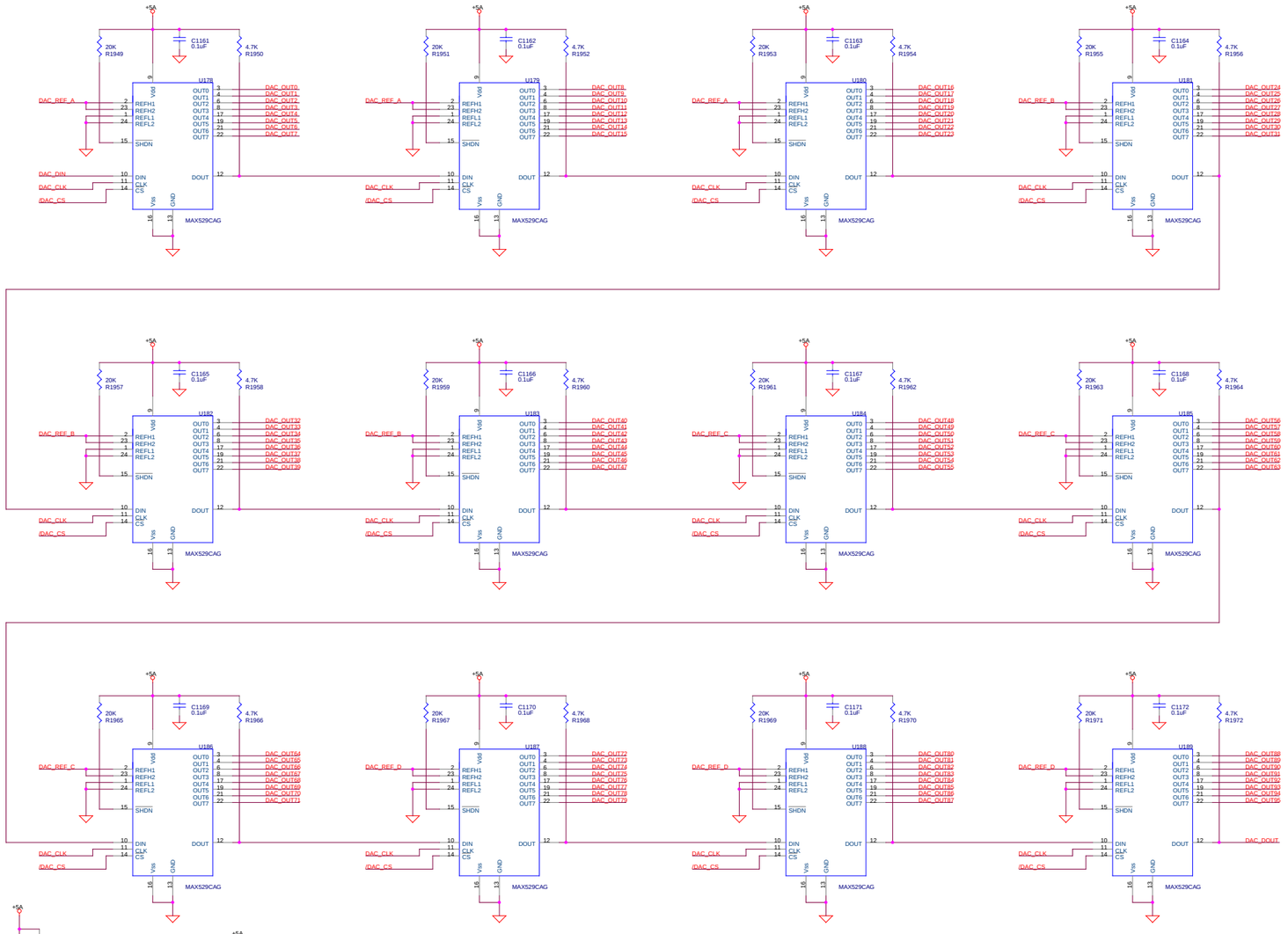
INPUTS

DAC_DIN
DAC_CLK
/DAC_CS
+5A
-5A
AGND

OUTPUTS

DAC_OUT[95:0]
DAC_DOUT



CHANGES FROM REV0

1. CHANGED MAX6125 TO SO PACKAGE FOR AVAILABILITY

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Instrumentation and Controls Division

Title	DACS	
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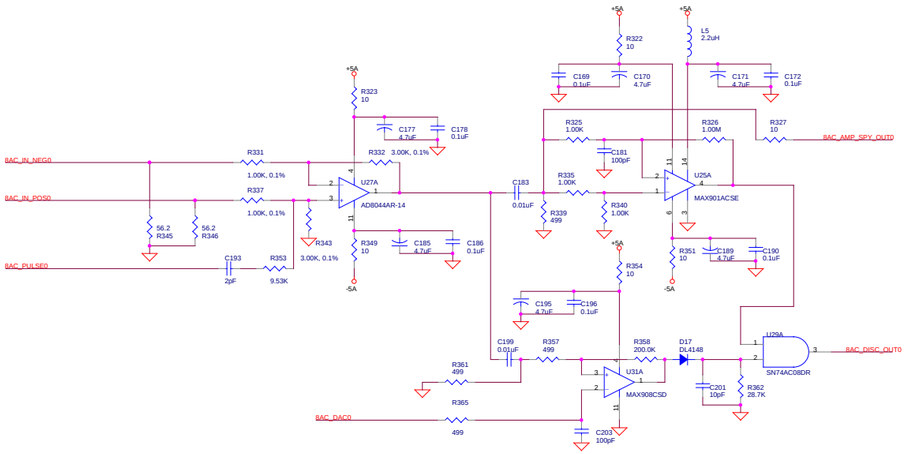
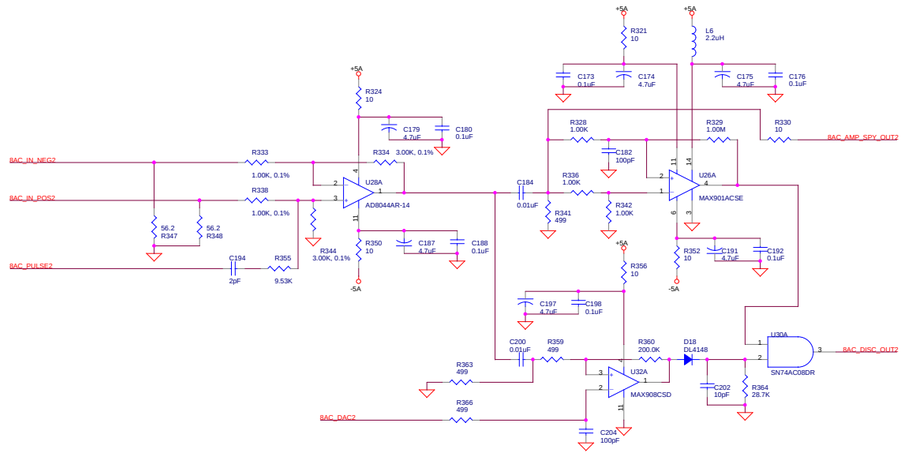
INPUTS

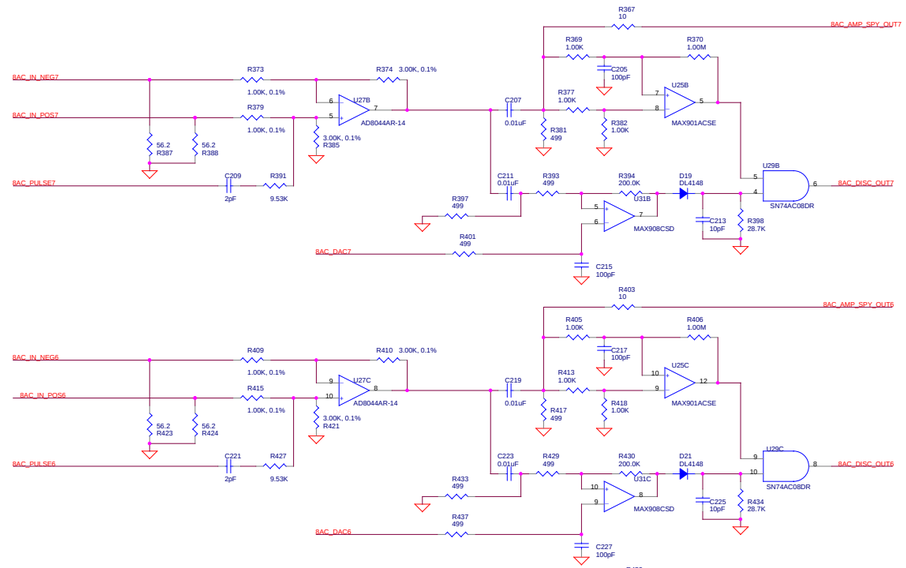
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

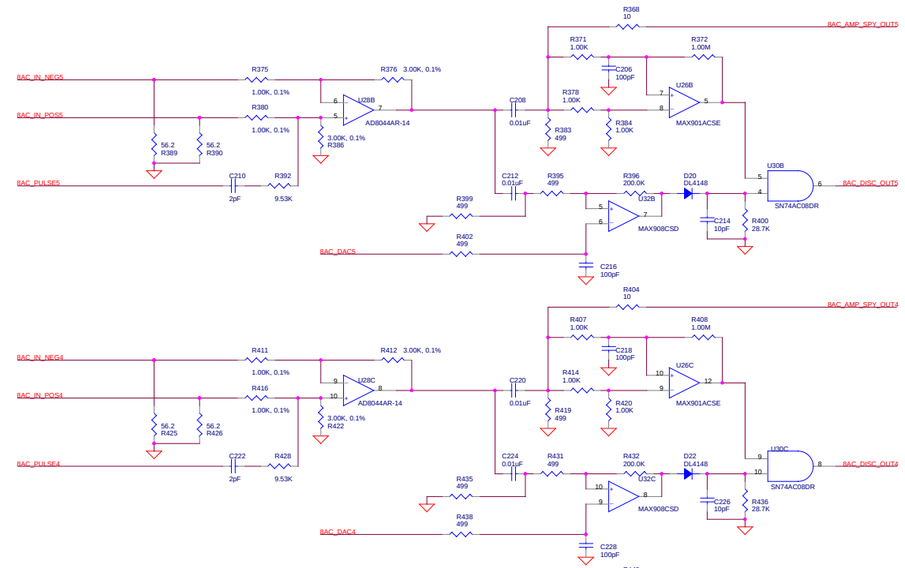
OUTPUTS

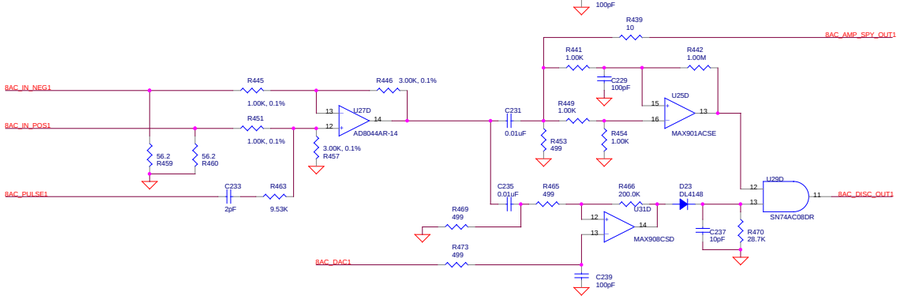
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

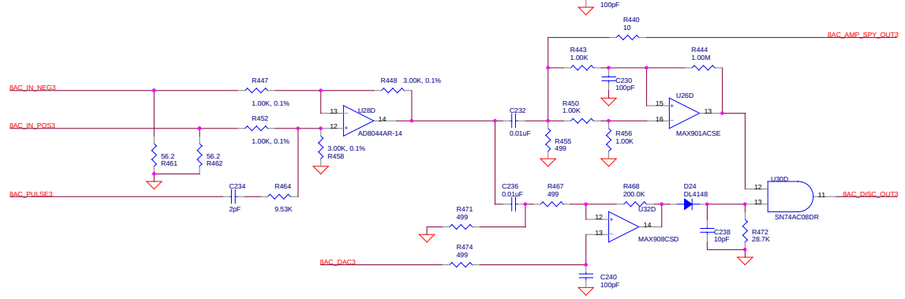




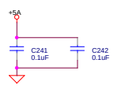








BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS



CHANGES FROM REV0

1. DAC FILTER CAPS CHANGED FROM 499pF TO 100pF
2. PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
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INPUTS

IN[15:0]

SCLK
SLATCH

RDBACK
SDIN

/HALT
/CLR_DLY
BCLK
/ROC_RST

TMS
TDI
TCK

+5D
DGND

OUTPUTS

OUT[15:0]

PSEUDO_TRIG

DMUXOUT
SDOUT
TDO

/HALT
SCLK
SLATCH
RDBACK
SDIN
/CLR_DLY
TCK
TMS
TDI
IN0
IN1
IN2
IN3

U126
EPM7256SQC208-15

EPM7256SQC208
Altera Max7000 series
208-pin Plastic
Quad-Flat Pack

IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15

OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
DMUXOUT
PSEUDO_TRIG

/SLATCH

/ROC_RST
BCLK

U127
3D7110D-4

U128
DS1021-25

+5D

SDOUT

R18B7
51

C966
100pF

Place bypass caps next to each VCC pin for every IC

Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.

+5D
C967 0.1uF
C968 0.1uF
C969 0.1uF
C970 0.1uF
C971 0.1uF
C972 0.1uF
C973 0.1uF
C974 0.1uF
C975 0.1uF
C976 0.1uF
C977 0.1uF
C978 0.1uF
C979 0.1uF
C980 0.1uF
C981 0.1uF
C982 0.1uF
DGND

CHANGES FROM REV0

1. CHANGED BCLK TERMINATION
2. 1021 CHIP SCLK CONNECTED TO CONDITIONED SIGNAL TO ALLOW SERIAL READBACK
3. REMOVED CLR_SRL SIGNAL
4. REMOVED PULL-UP RESISTORS FROM DELAY CHIP

Phenix MuID ROC

Oak Ridge National Lab
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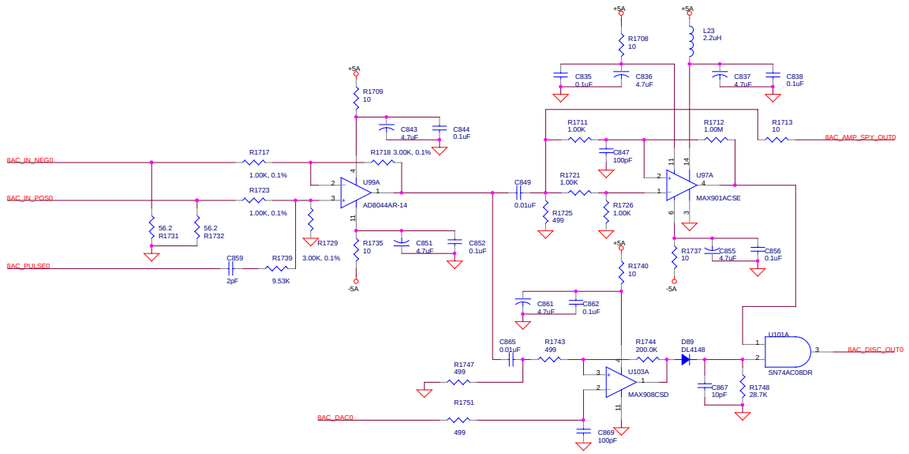
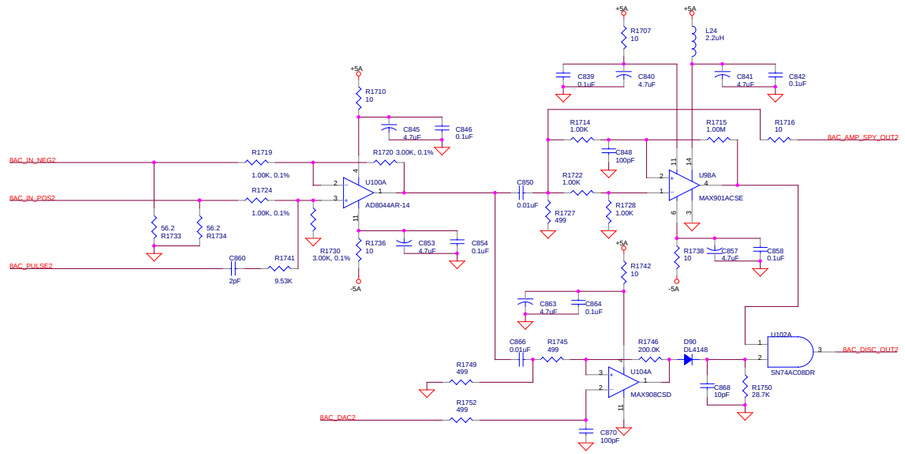
INPUTS

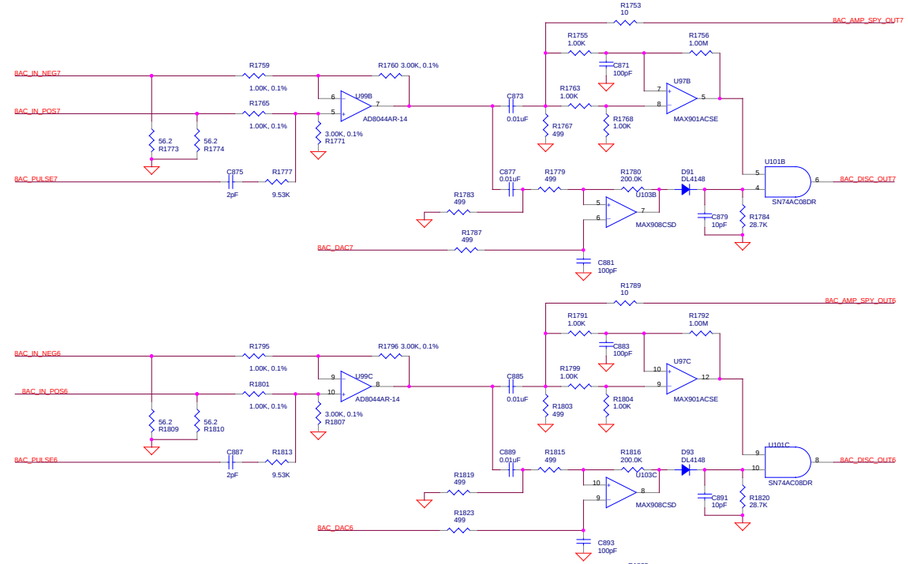
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

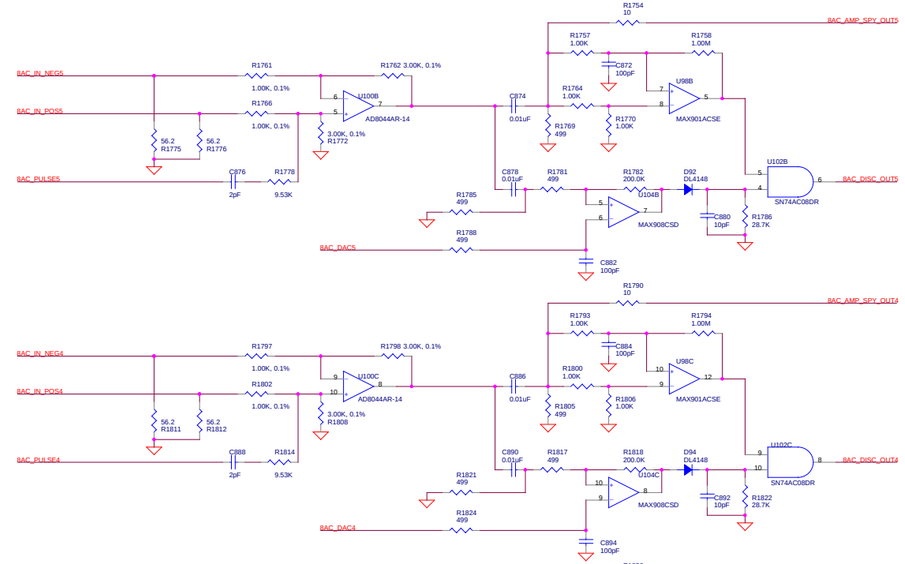
OUTPUTS

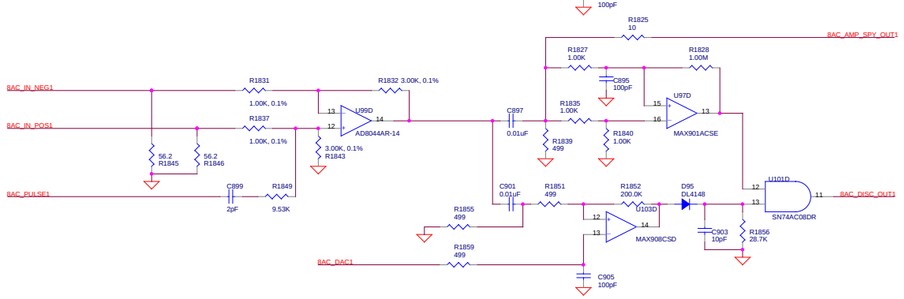
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

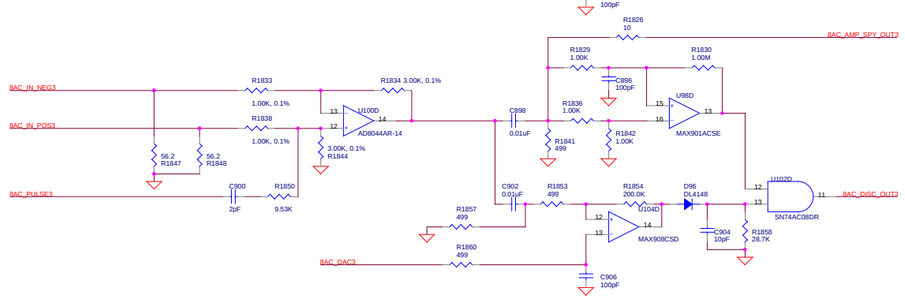


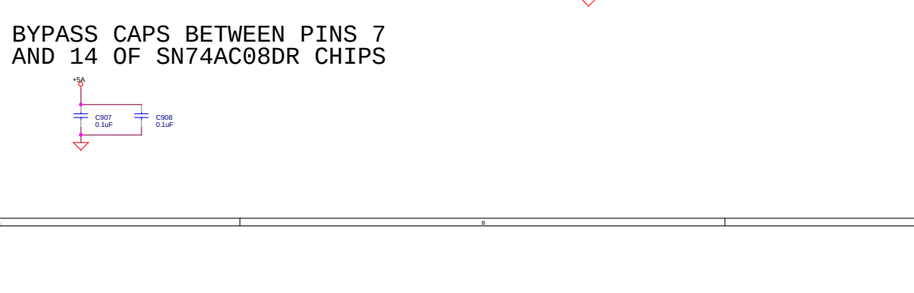












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

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Title	BAMP COMP	
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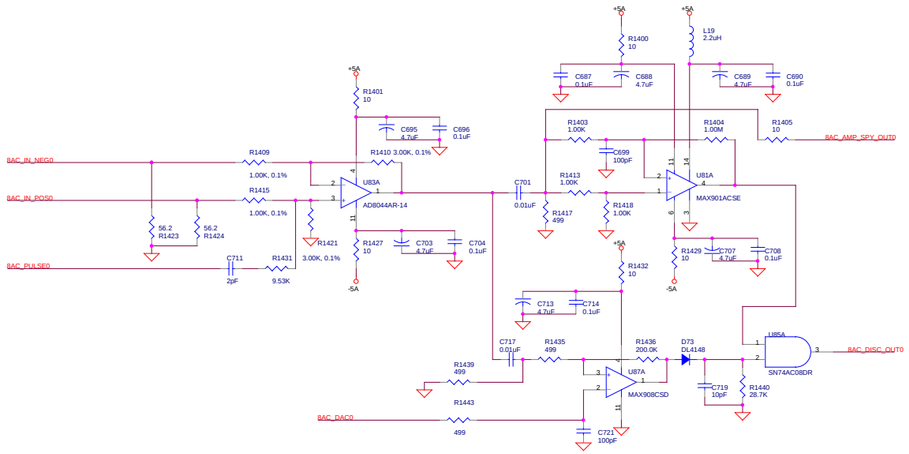
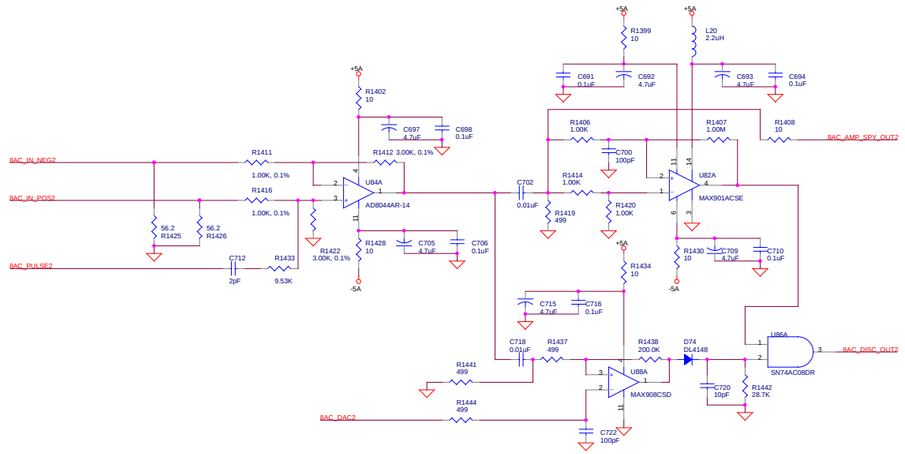
INPUTS

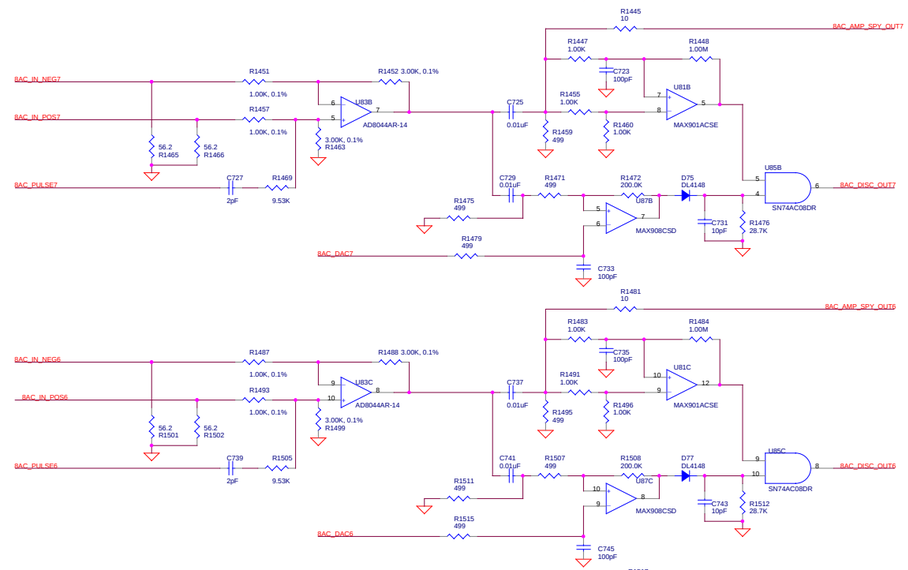
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

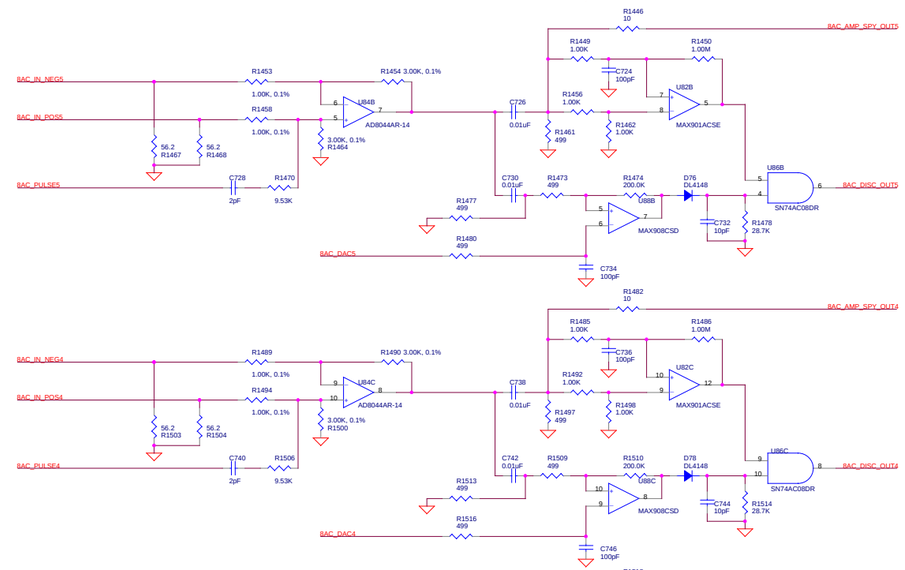
OUTPUTS

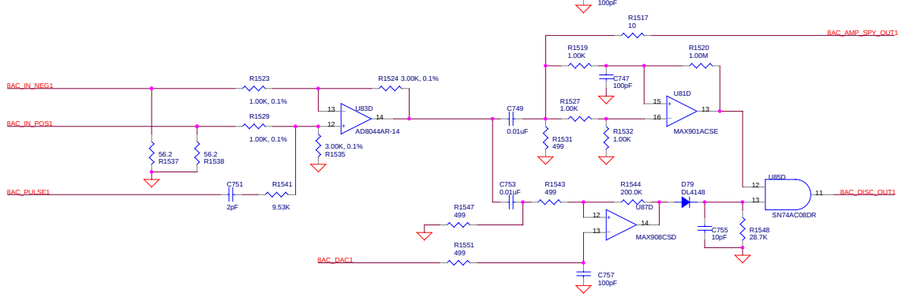
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

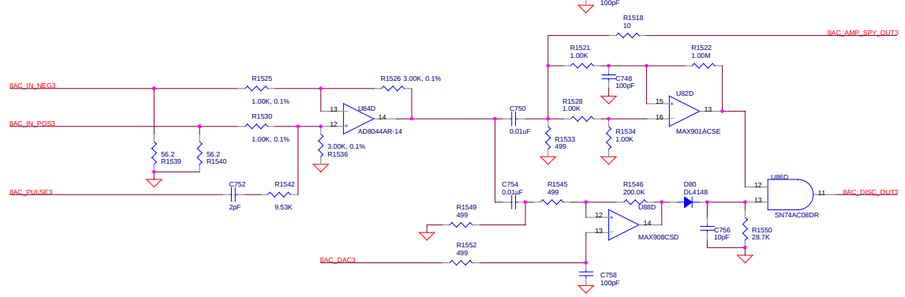


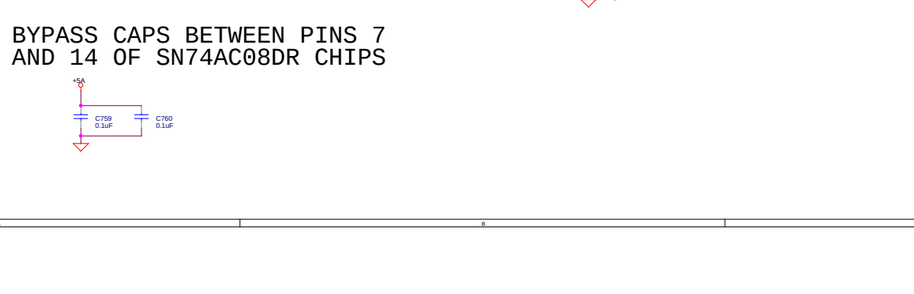


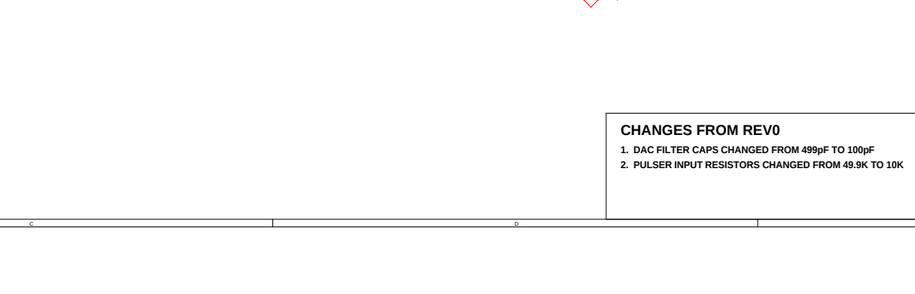












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

Phenix MuID ROC
Oak Ridge National Lab
Instrumentation and Controls Division

Title	BAMP COMP	
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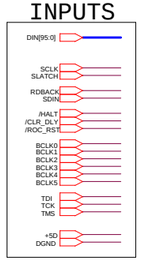
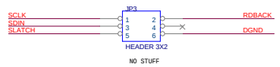
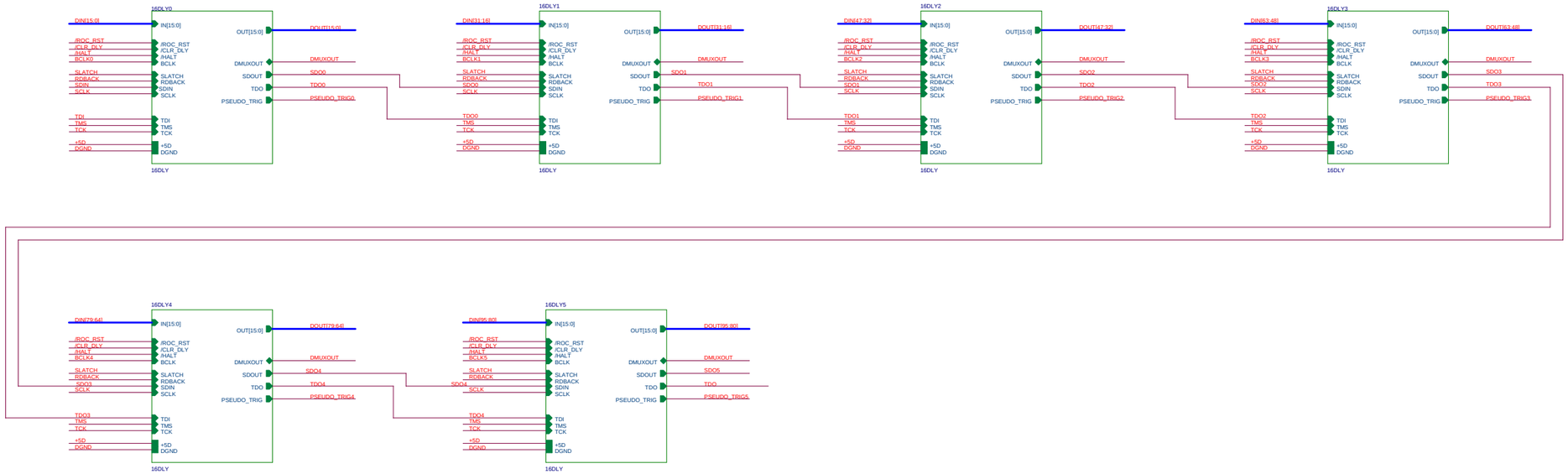
INPUTS



SERIAL DOWNLOAD



OUTPUTS



CHANGES FROM REV0

1. **REMOVED CLR_SRL**
2. **MOVED JTAG CONNECTOR TO I/O PAGE**

Phenix MuID ROC

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Instrumentation and Controls Division

Title: DELAY TOP

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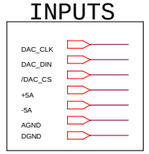
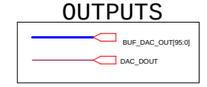
NO STUFF

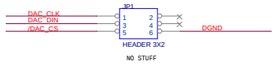
INPUTS

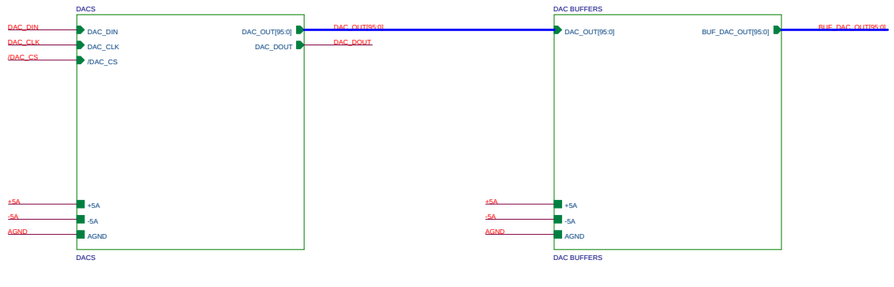


OUTPUTS



SERIAL DOWNLOAD





CHANGES FROM REV0

1. CHANGED DAC SERIAL BYPASS TO USE DGND
2. NO STUFF TEXT ADDED FOR CONNECTOR
3. ADDED DGND TO INPUT

Phenix MuID ROC

Oak Ridge National Lab
Instrumentation and Controls Division

Title: DAC TOP		
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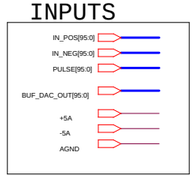
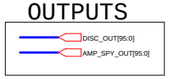
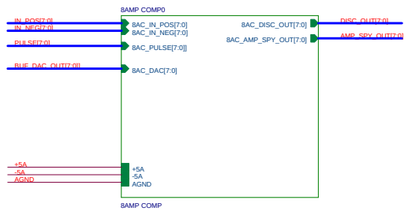
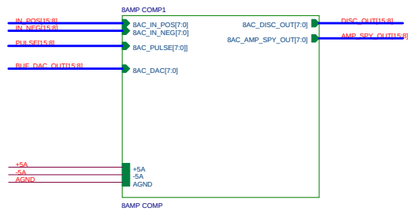
INPUTS

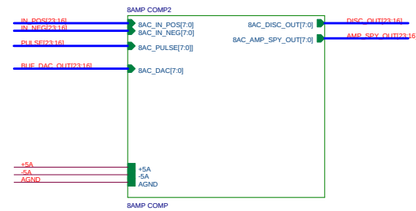


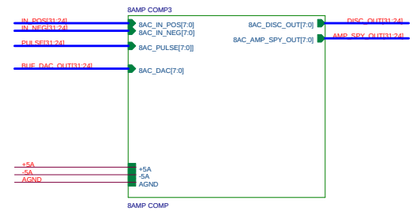
OUTPUTS

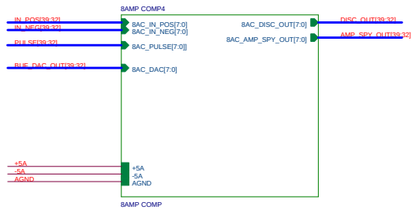


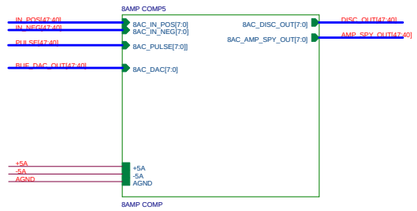


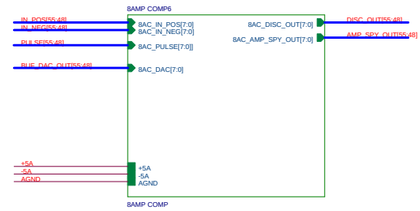


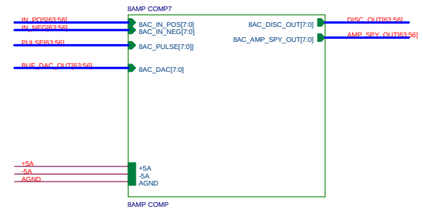


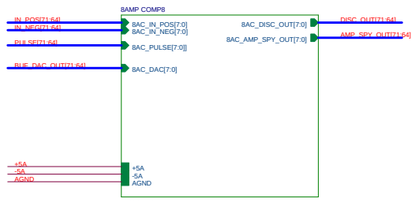


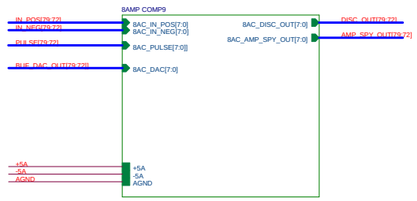


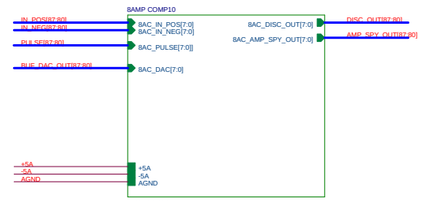


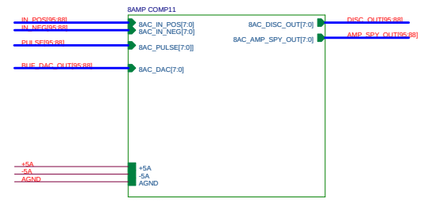












CHANGES FROM REV0

NO CHANGES

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Oak Ridge National Lab

Instrumentation and Controls Division

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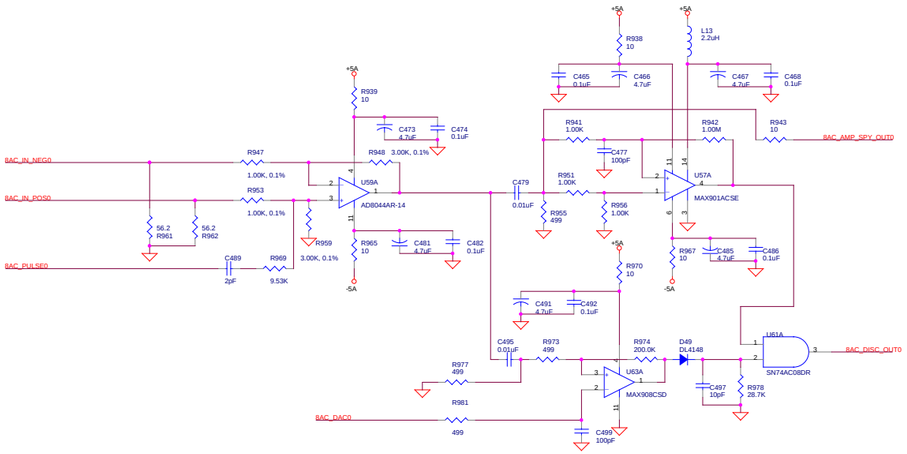
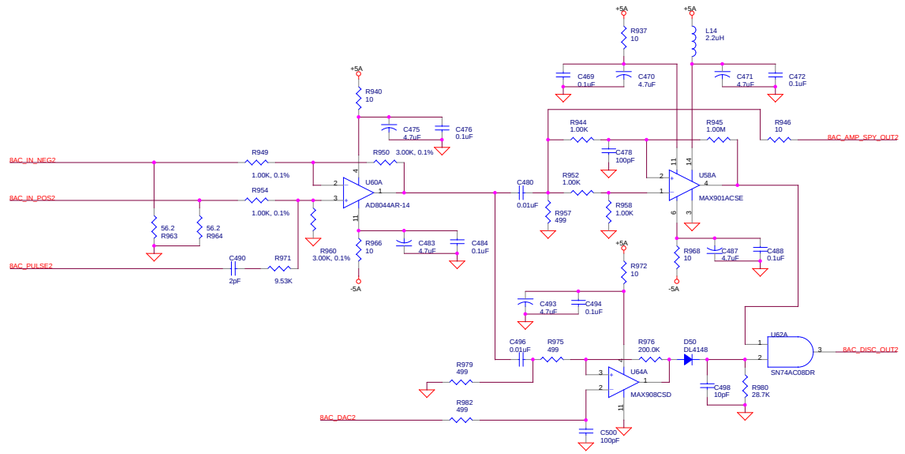
INPUTS

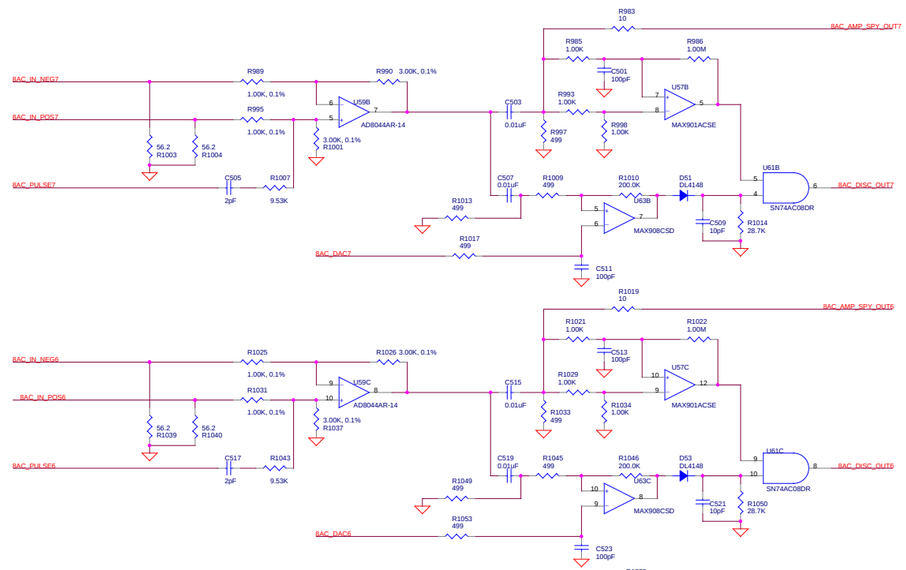
BAC_IN_POS[7:0]
BAC_IN_NEG[7:0]
BAC_PULSE[7:0]
BAC_DAC[7:0]
+5A
-5A
AGND

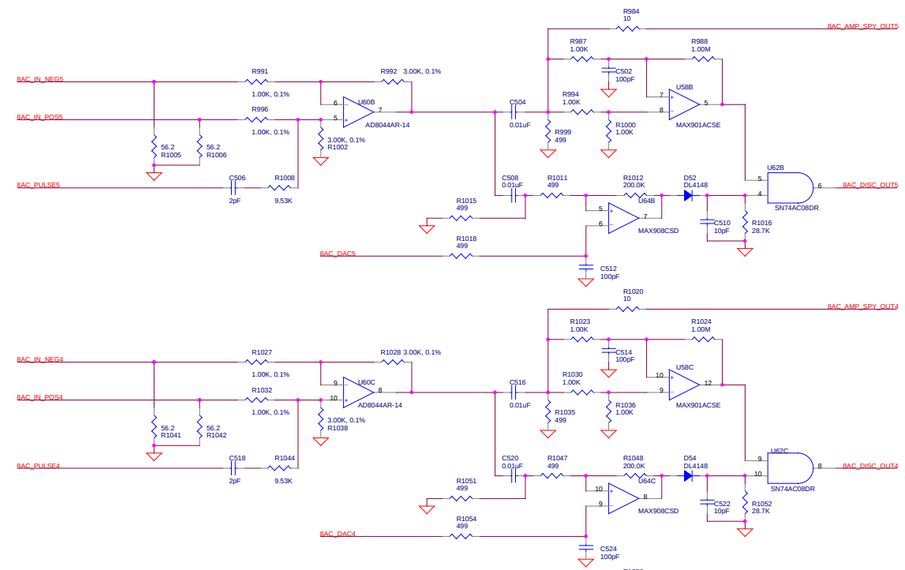
OUTPUTS

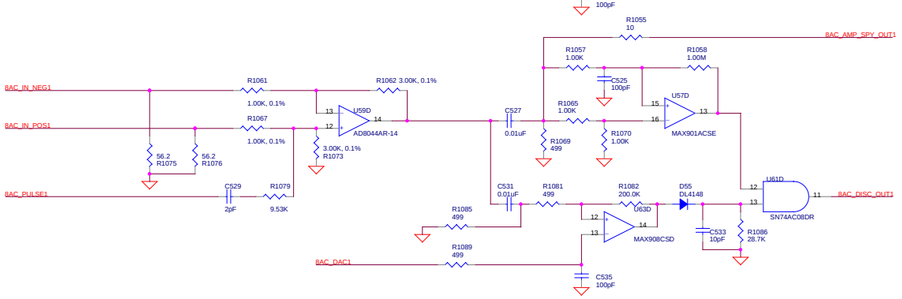
BAC_DISC_OUT[7:0]
BAC_AMP_SPY_OUT[7:0]

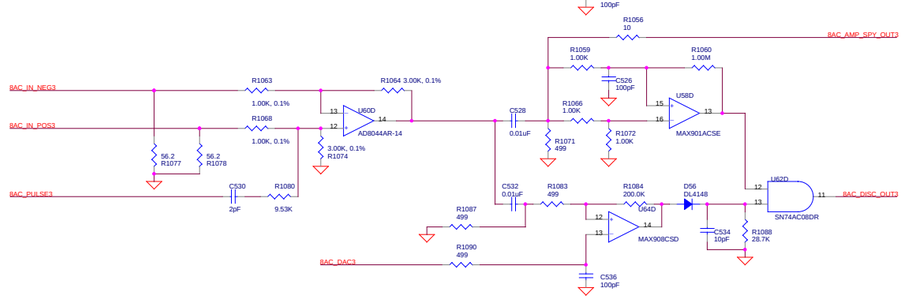


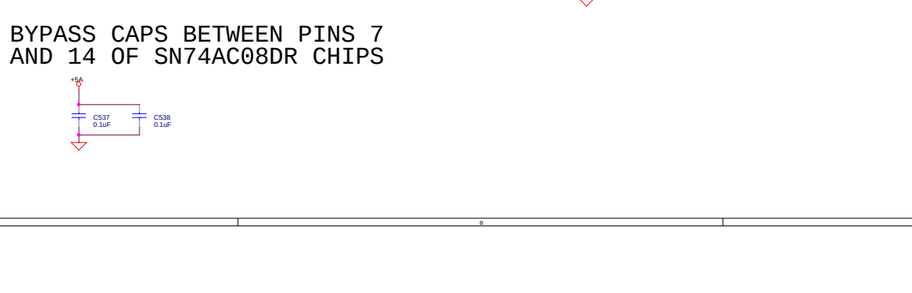












BYPASS CAPS BETWEEN PINS 7 AND 14 OF SN74AC08DR CHIPS

CHANGES FROM REV0

1. **DAC FILTER CAPS CHANGED FROM 499pF TO 100pF**
2. **PULSER INPUT RESISTORS CHANGED FROM 49.9K TO 10K**

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INPUTS

DAC_OUT[95:0]
+5A
-5A
AGND

OUTPUTS

BUF_DAC_OUT[95:0]

CHANGES FROM REV0

1. NO CHANGES

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