DØ Forward Proton Detector

Readout and Trigger Chains

Review

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6 December, 2001

Goals

Reasons for Meeting:

I. **Review FPD Readout/Trigger plan — anything forgotten or misunderstood**

II. **Establish a time frame for the most efficient installation, testing, and commissioning of all parts of the FPD Readout/Trigger chains.**

Goals:

A. Begin **NOW** testing components at an AFE test stand — complete by Christmas

B. Installation of a full Readout/Trigger chain for one spectrometer for Phase 0 — complete by mid January

C. Complete installation of Readout/Trigger chains for Phase I — 10 detectors/5 spectrometers — complete by late January

D. Complete installation of Readout/Trigger chains for Phase II — 18 detectors/9 spectrometers — complete by July

Outline

I. FPD Description

- Detectors
- Readout and Triggering Chains
- PW08 Configuration

II. Transition Patch Panel, *TPP*

- Features
- Production Time Scale
- Testing

III. AFE Issues

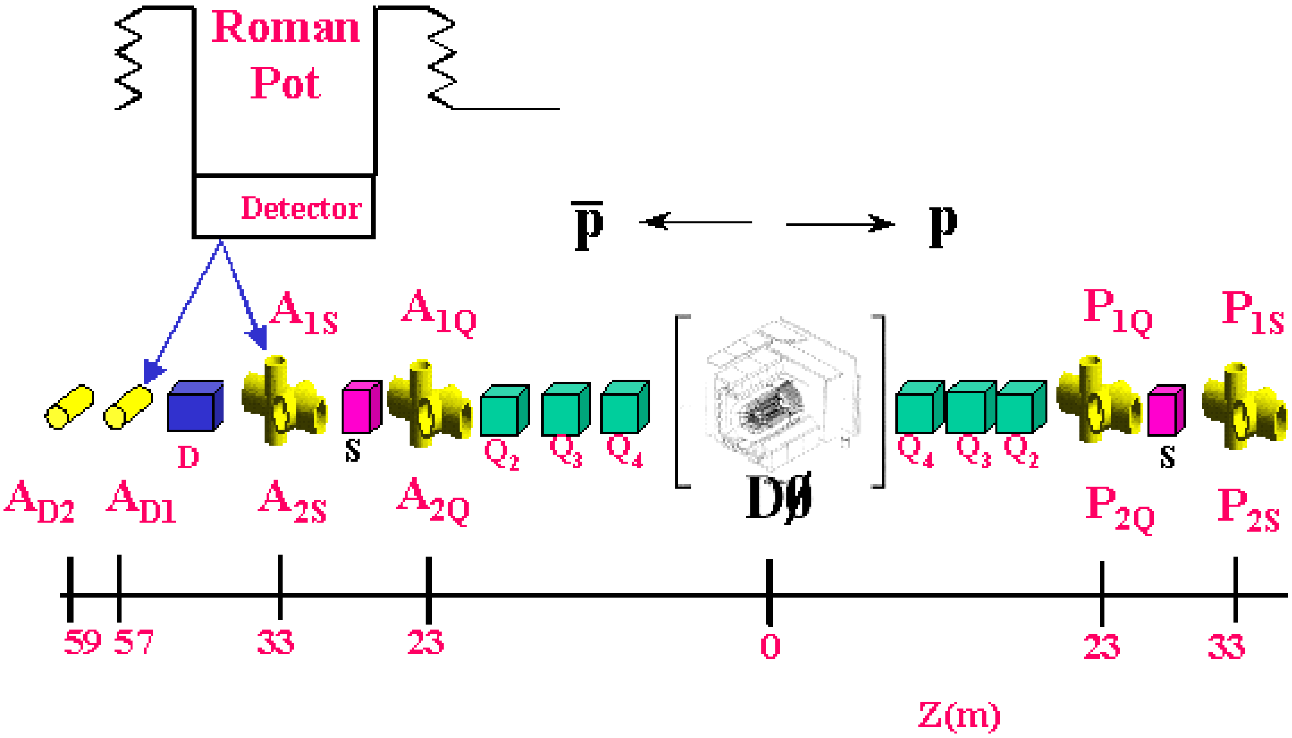
- Timings
- Mapping
  - DFE
  - Sequencers

IV. Outstanding Issues

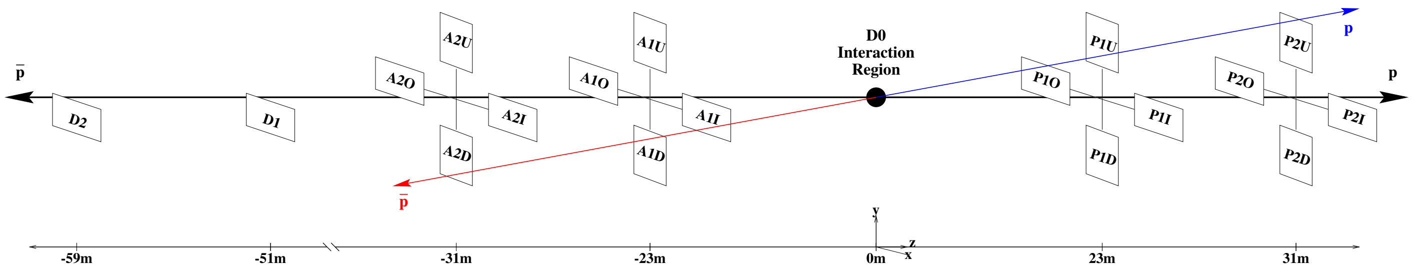
- Parts
- Software
- Testing

FPD Description

FPD Detectors

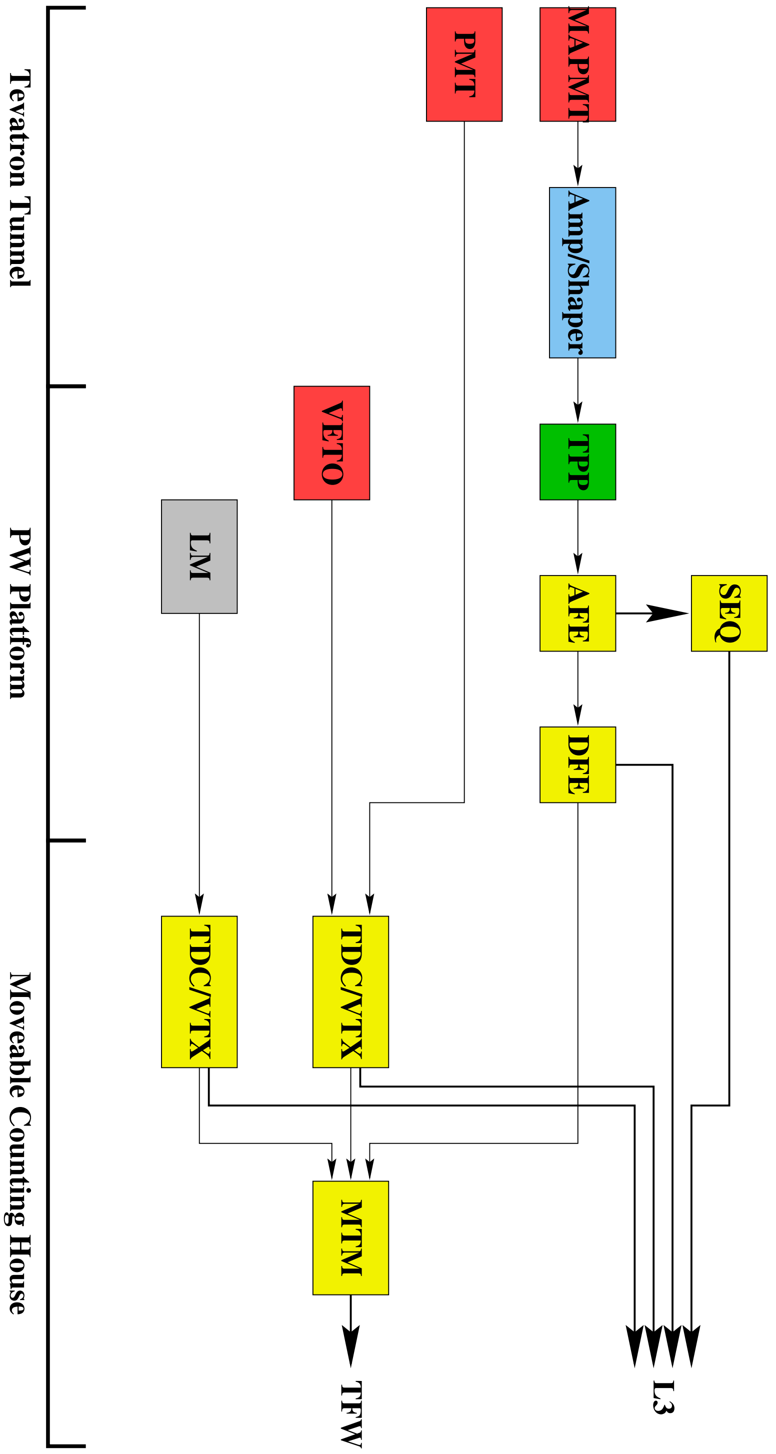


FPD Spectrometers



FPD Description

FPD Block Readout and Trigger Chains



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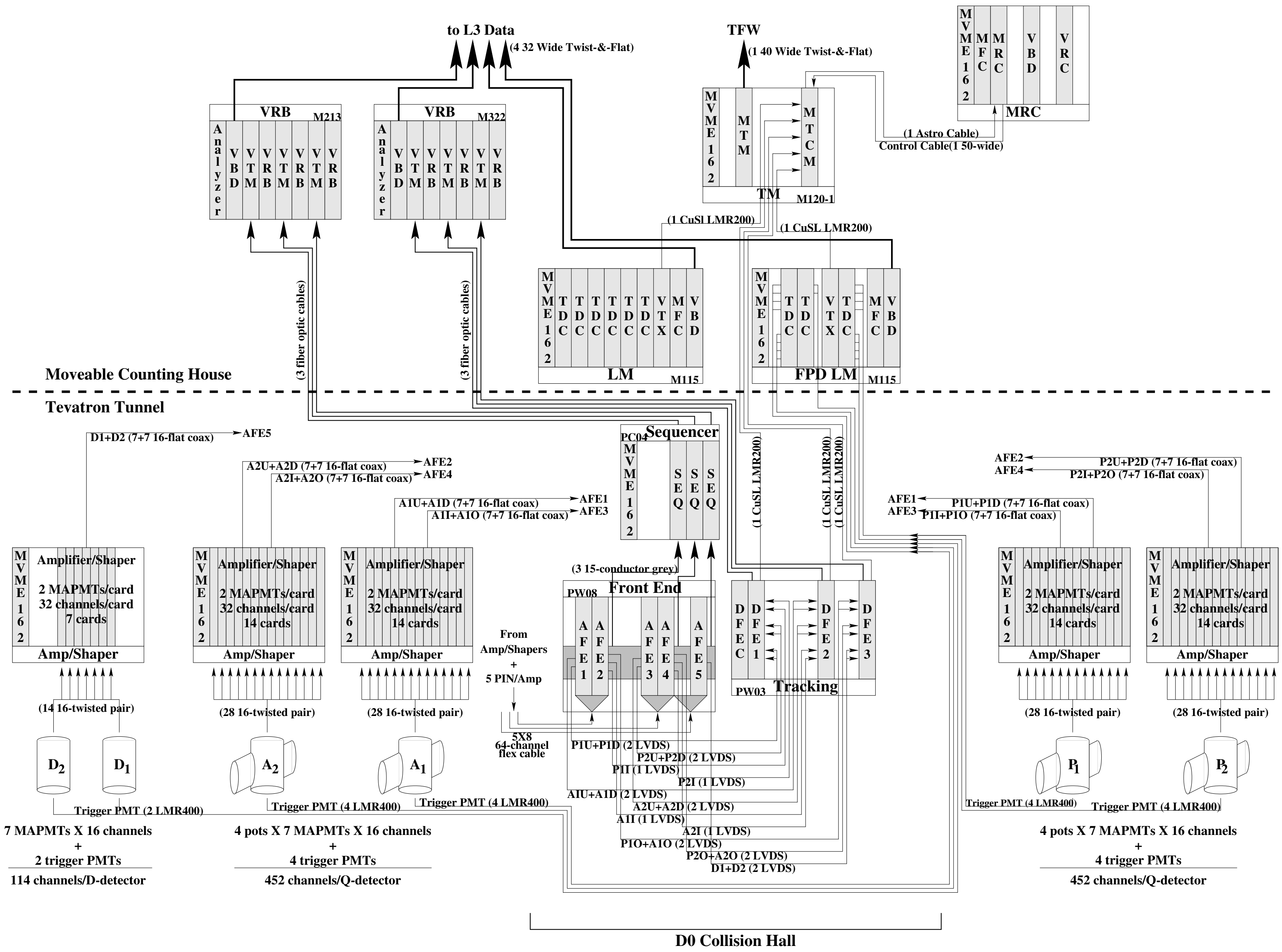

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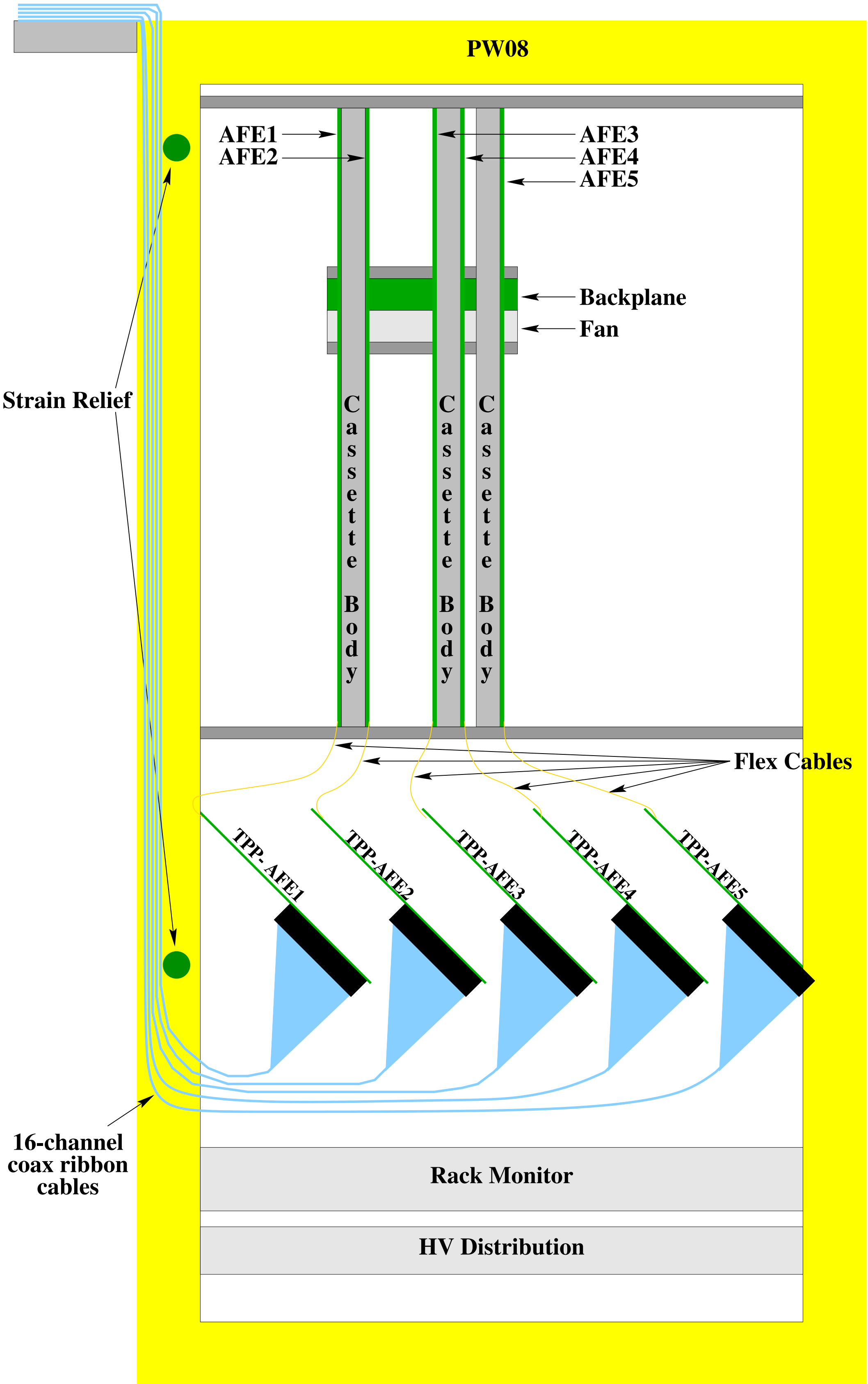


Transition Patch Panel

The TPP Serves to:

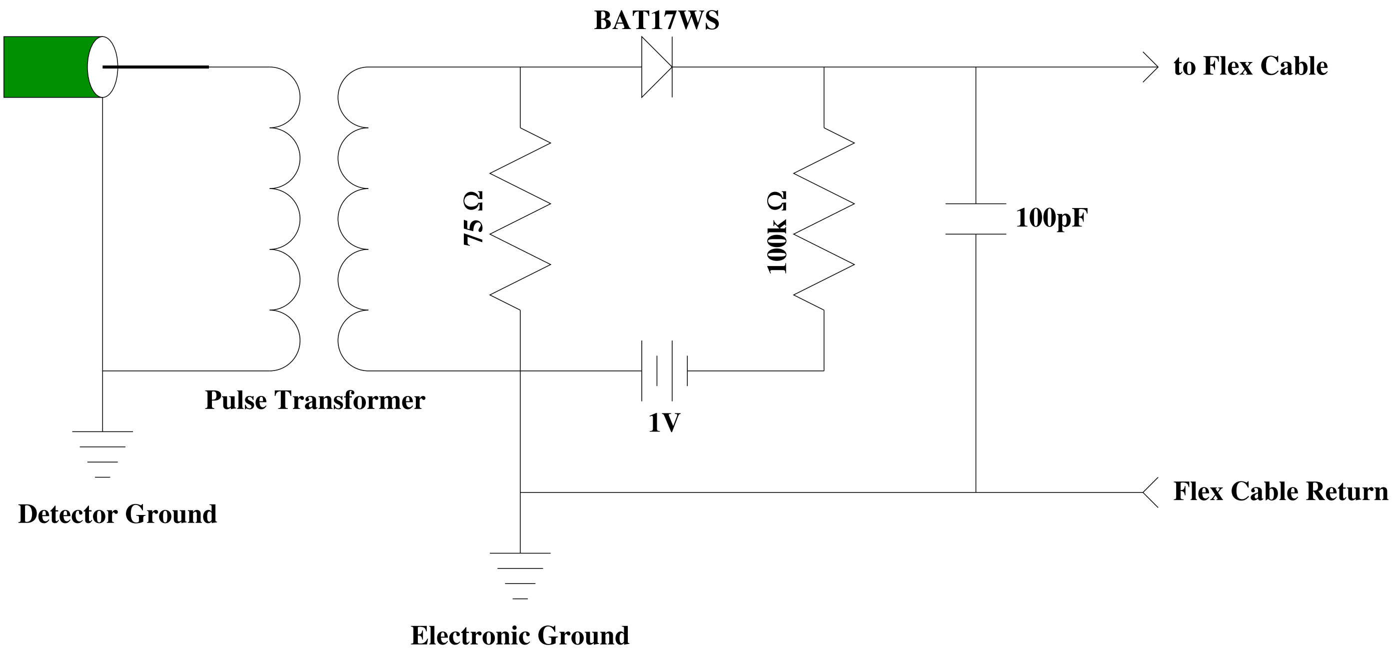
I. Make the transition from 16-channel bulkhead connectors to 64-channel flex cables

II. Isolate tunnel/detector ground from DØ platform ground

III. Transform signals to mimic output from VLPCs

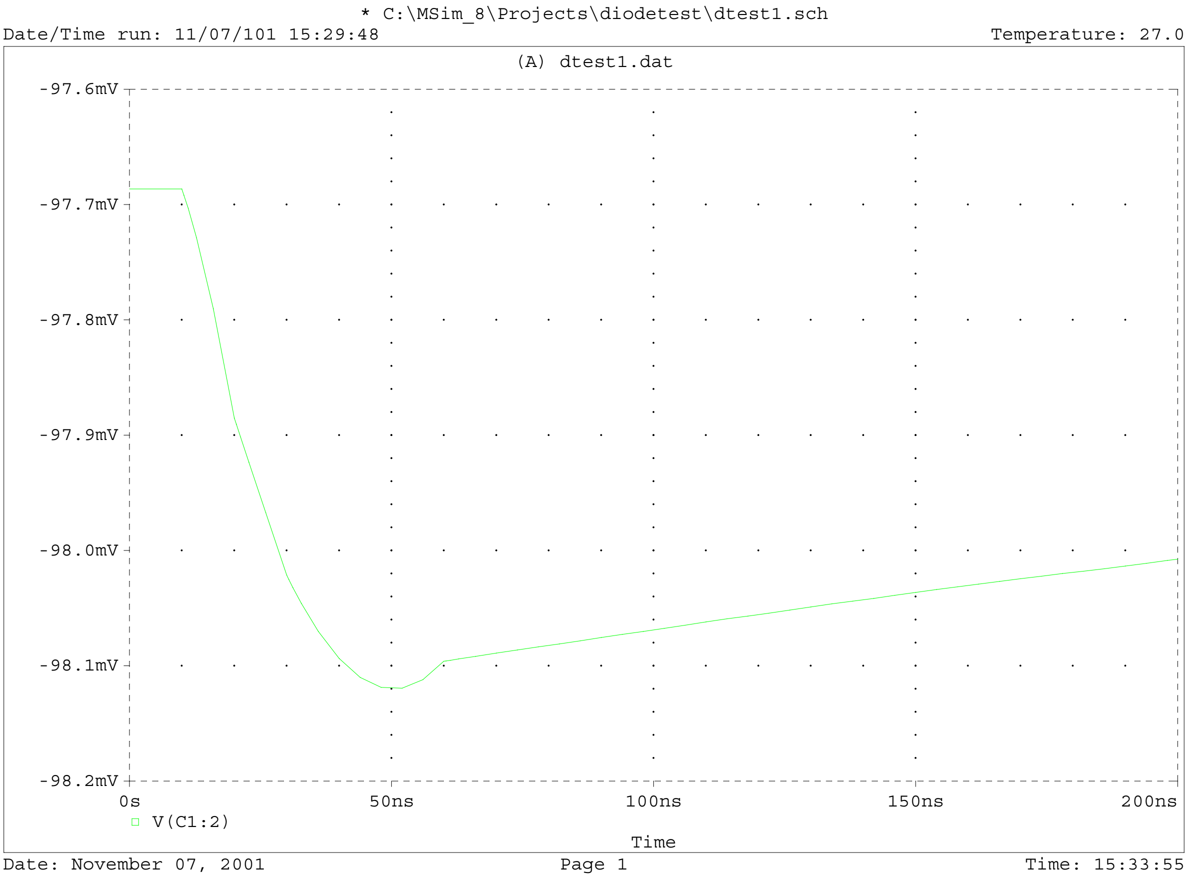
IV. Discard extra charge so as to use the dynamic range of the SIFT chips

TPP Circuit



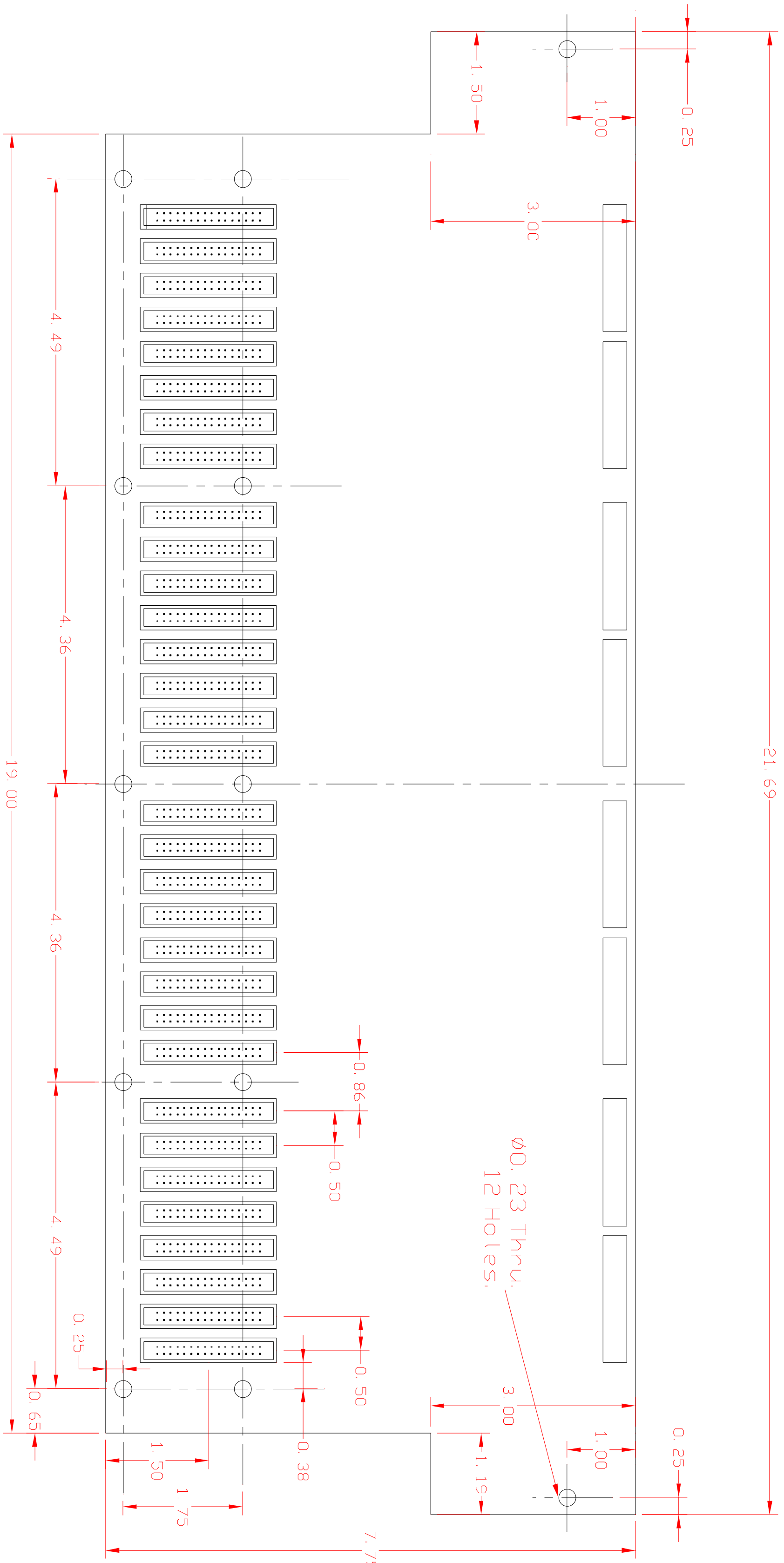
Transition Patch Panel

Spice Results



Transition Patch Panel

TPP Mechanical Design



Transition Patch Panel

Layout Specifications

Value	Description
FPD Patch Panel	Board Name
5	Quantity
8 Layers 5 signal 3 power	Board Type (# signal layers - # power layers)
.062 (in)	Board Thickness and Tolerance
21.69 X 7.75 (in)	Board Dimensions and shape
Smobc / Immersion Tin plating	Finish/Plating (smobc) / Immersion Tin plating
2oz	Cu Weight outer layers (ounces per square inch)
1oz	Cu Weight inner layers (ounces per square inch)
$576Top + 576Bot = 1152$	Number of gold contacts/side (50μm, HardGold over Electroless Nickel)
6 mils	Minimum Trace width & tolerance
6 mils	Minimum Trace clearance & tolerance
Top & Bottom	Solder Mask (top & bottom - top only)
LPI	Solder Mask Type (wet/dry/LPI)
Top & Bottom	Silk Screen (top & bottom - top only - white)
YES	Testing Required (yes/no/specify)
4160 Top + 4160 Bot = 8320	Number of Surface mount pads TOP/BOT (only needed for testing)
3977	Number of Through Holes
8	Number of Drill Sizes
.009(in)	Smallest Hole
.281(in)	Largest Hole
N/A	Number of Blind Vias
N/A	Number of Buried Vias
NO	Controlled Impedance (yes/no/specify)
———————————	Physical Board Stackup
EtchLayer1Top.gdo	Top layer name (Signals)
EtchLayer2.gdo	Inner layer (Signals)
EtchLayer3.gdo	Inner layer (Signals)
EtchLayer4.gdo	Inner layer (GNDA Plane)
EtchLayer5.gdo	Inner layer (VBB Plane)
EtchLayer6.gdo	Inner layer (GND Plane)
EtchLayer7.gdo	Inner layer (Signals)
EtchLayer8Bottom.gdo	Bottom layer name (Signals)
Gerber/Drill	Material Supplied (Film/gerber files/modem/ect)
10 Days	Required Delivery
N/A	Special NOTES
Gerald M. Dyche (630)840-5206	Technical Contact Personnel and phone number

Table 1: General Information for Manufacture of Printed Circuit Boards. **Note:** All dimensions are in inches unless specified

Transition Patch Panel

Testing the TPP:

- Check Channel Mapping from bulkhead connector to Cyn::Apse
- Study Signal Shape *Requires AFE test stand*
- Determine TPP components to optimize charge input into SIFT *Requires AFE test stand*
- ???

Note: These tests should only require on the order of hours at a test stand

AFE Issues

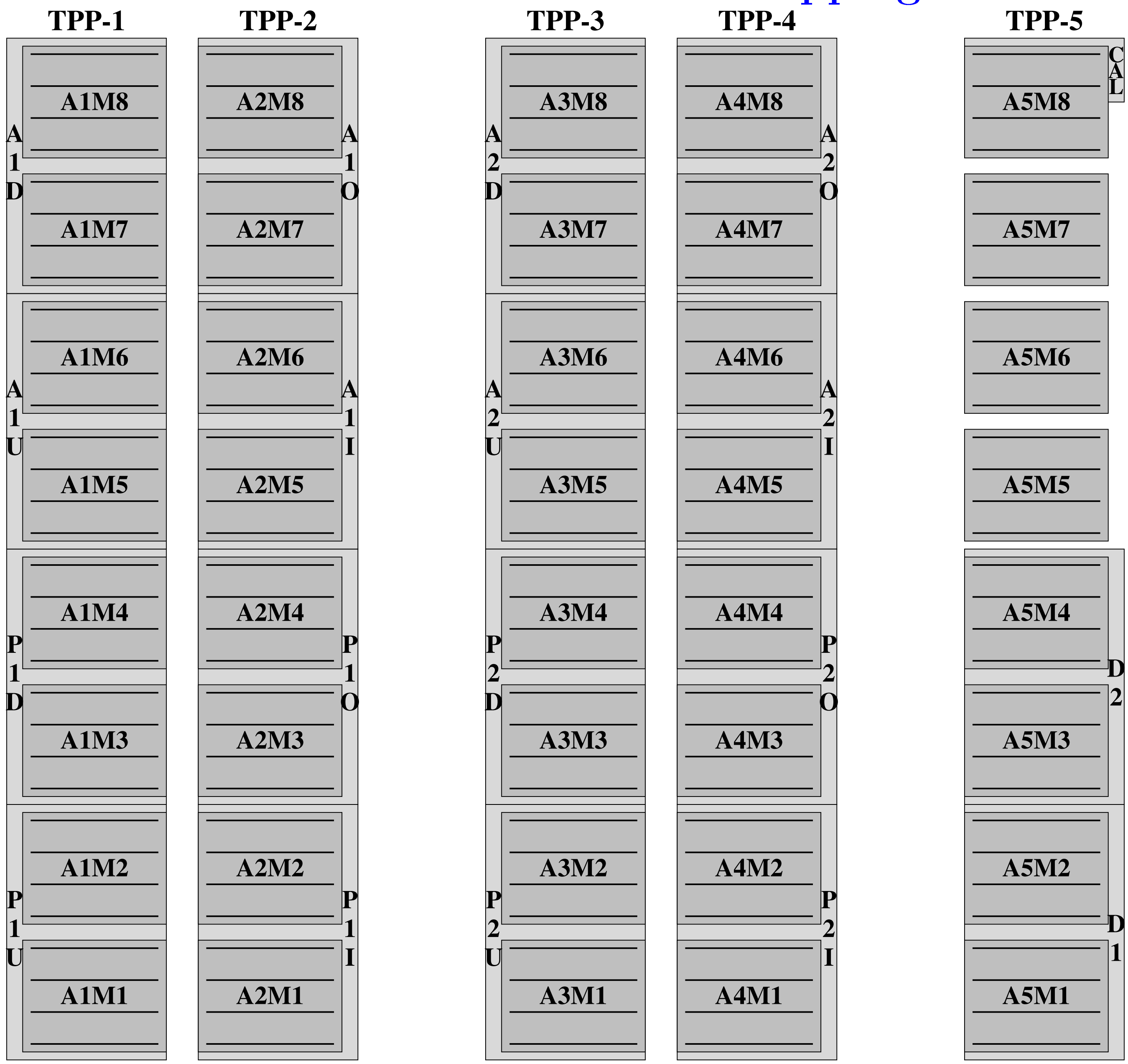
Timing

Detector	TOF (ns)	Readout Chain AFE (ns)	Readout Chain Sequencer (ns)	Readout Chain VBD (ns)	Trigger Chain AFE (ns)	Trigger Chain DFE (ns)	Trigger Chain TDC (ns)	Trigger Chain MTM (ns)	Trigger Chain TFW (ns)
A1 MAPMT	77	320			-	-	-	-	-
A2 MAPMT	103	555			-	-	-	-	-
P1 MAPMT	77	320			-	-	-	-	-
P2 MAPMT	103	555			-	-	-	-	-
D1 MAPMT	170	622			-	-	-	-	-
D2 MAPMT	197	649			-	-	-	-	-
A1 MAPMT	77	-	-	-	320	586	-	934	1304
A2 MAPMT	103	-	-	-	555	821	-	1169	1539
P1 MAPMT	77	-	-	-	320	586	-	934	1304
P2 MAPMT	103	-	-	-	555	821	-	1169	1539
D1 MAPMT	170	-	-	-	622	888	-	1236	1606
D2 MAPMT	197	-	-	-	649	915	-	1263	1633
A1 PMT	77	-	-	-	-	-	364	1694	2064
A2 PMT	103	-	-	-	-	-	390	1720	2090
P1 PMT	77	-	-	-	-	-	400	1730	2100
P2 PMT	103	-	-	-	-	-	426	1756	2126
D1 PMT	170	-	-	-	-	-	612	1942	2312
D2 PMT	197	-	-	-	-	-	639	1969	2339

Table 2: Estimated arrival times of signals at various elements of the Readout and Trigger Chains

AFE Issues

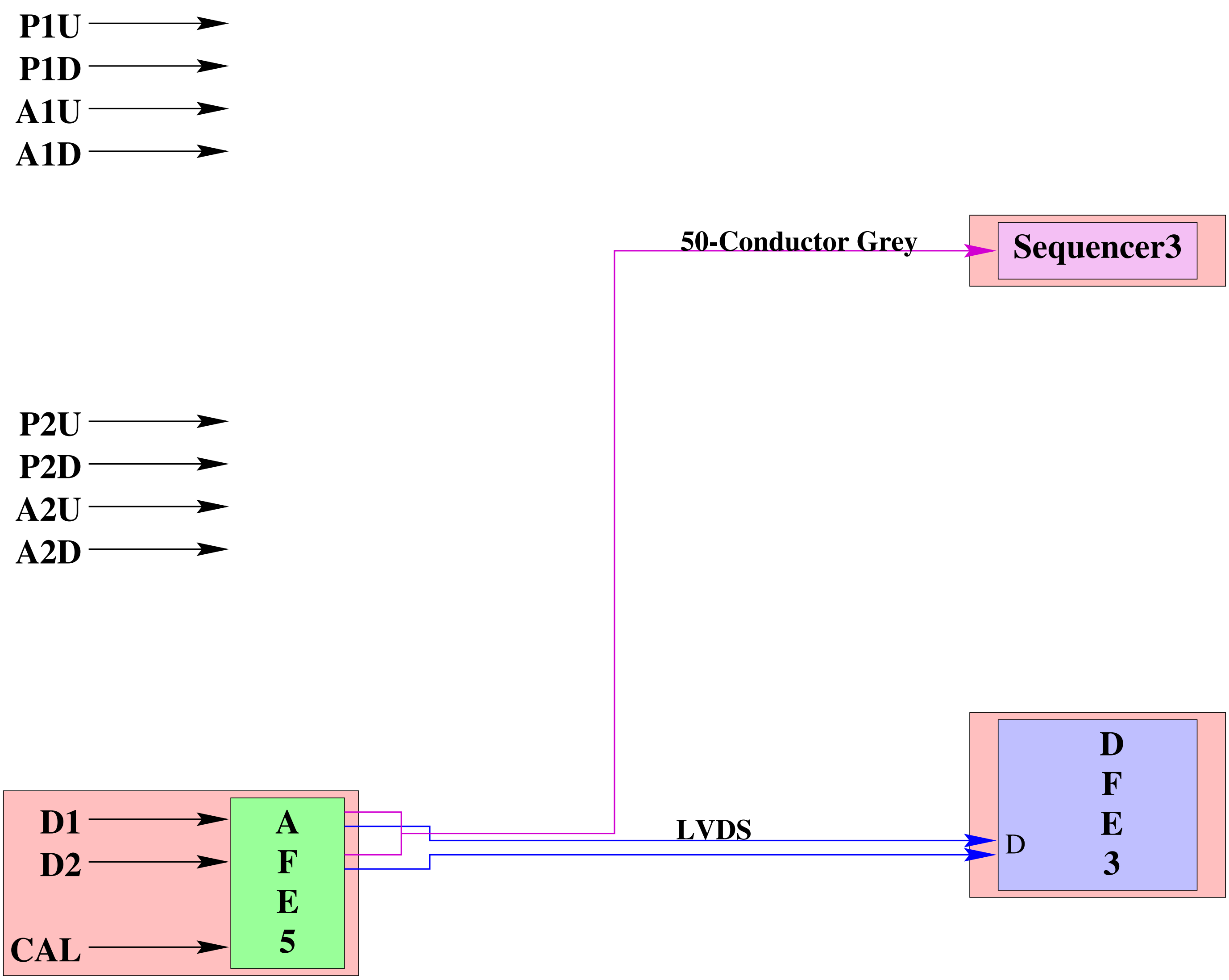
Detector to Electronics Mapping



to left side Cassette 1 AFE-1	to right side Cassette 1 AFE-2	to left side Cassette 2 AFE-3	to right side Cassette 2 AFE-4	to right side Cassette 3 AFE-5

AFE Issues

Detector to Electronics Mapping



In the figure:

- red outer boxes → Phase 0
- yellow outer boxes → Phase I
- cyan outer boxes → Phase II

The actual mapping is shown in the following two tables:

AFE Issues

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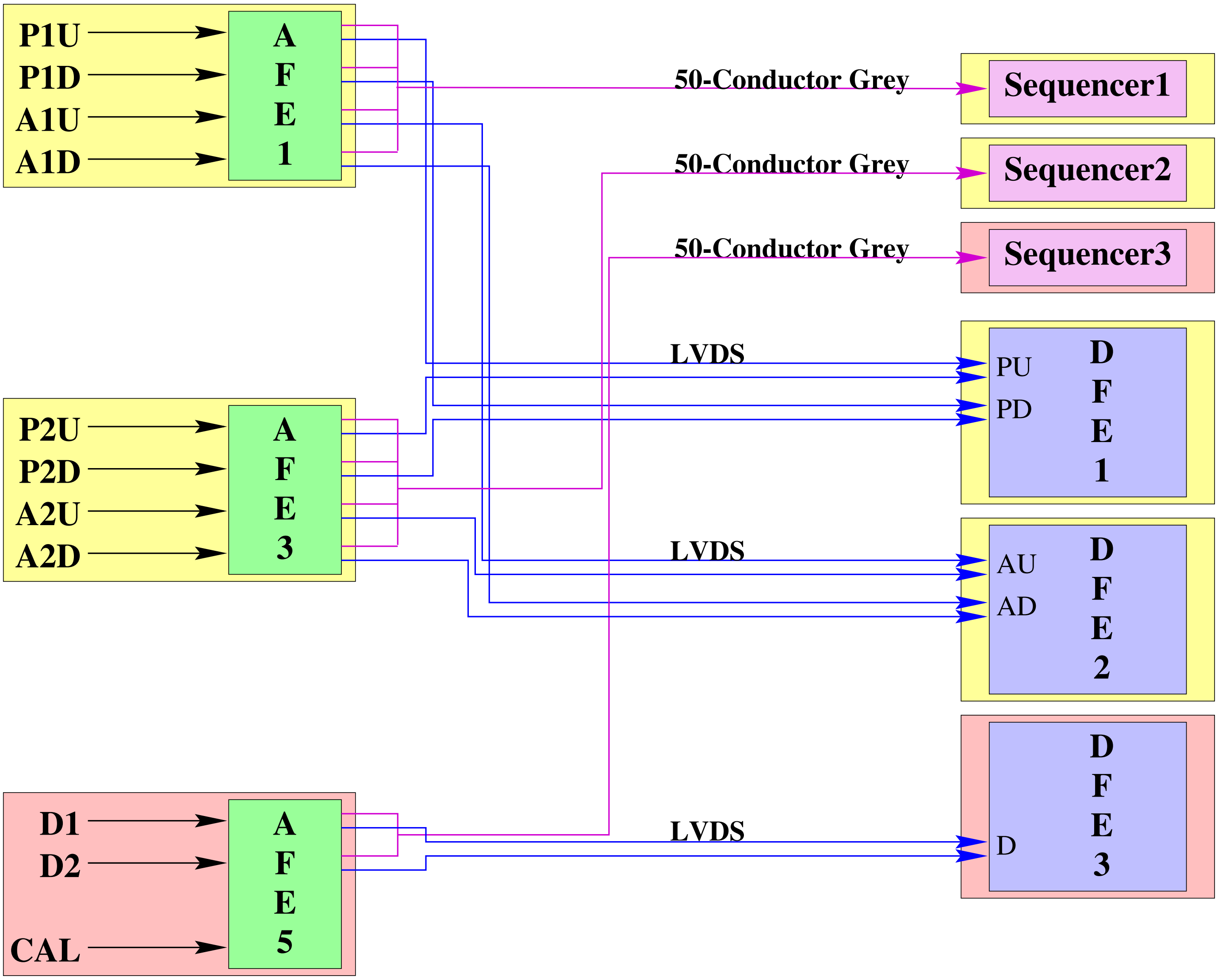

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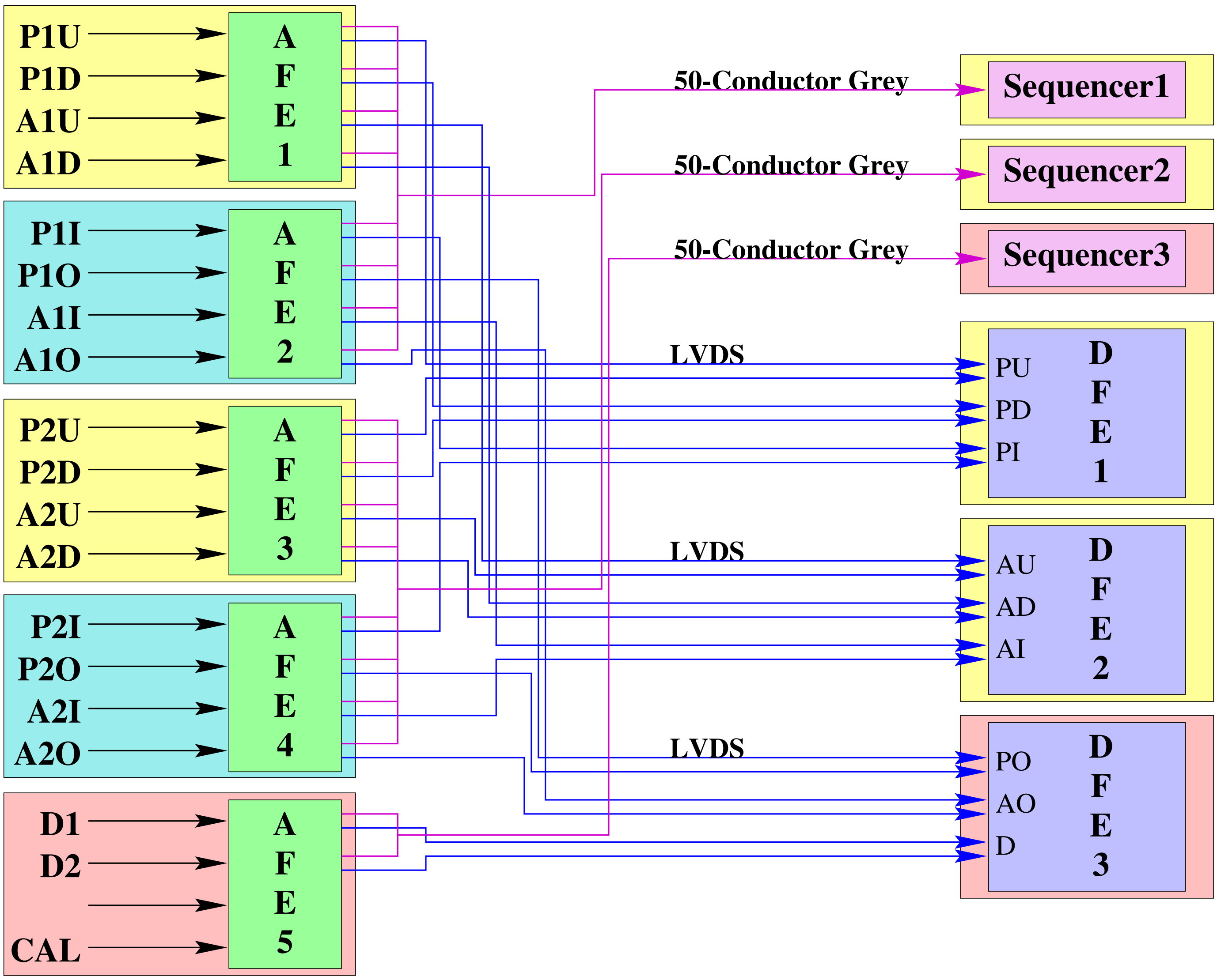

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- cyan outer boxes → Phase II

The actual mapping is shown in the following two tables:

AFE Issues

Mapping Detectors into AFE boards

MAPMT Detector	MAPMT Channel	TPP	Flat Coax Cables	Flex Cable	AFE Card	AFE MCM
P1U	1:64	1	1:4	A1M1	1	1[1:64]
P1U	65:112	1	5:7	A1M2	1	2[1:48]
P1D	1:64	1	1:4	A1M3	1	3[1:64]
P1D	65:112	1	5:7	A1M4	1	4[1:48]
A1U	1:64	1	1:4	A1M5	1	5[1:64]
A1U	65:112	1	5:7	A1M6	1	6[1:48]
A1D	1:64	1	1:4	A1M7	1	7[1:64]
A1D	65:112	1	5:7	A1M8	1	8[1:48]
P1I	1:64	2	1:4	A2M1	2	1[1:64]
P1I	65:112	2	5:7	A2M2	2	2[1:48]
P1O	1:64	2	1:4	A2M3	2	3[1:64]
P1O	65:112	2	5:7	A2M4	2	4[1:48]
A1I	1:64	2	1:4	A2M5	2	5[1:64]
A1I	65:112	2	5:7	A2M6	2	6[1:48]
A1O	1:64	2	1:4	A2M7	2	7[1:64]
A1O	65:112	2	5:7	A2M8	2	8[1:48]
P2U	1:64	3	1:4	A3M1	3	1[1:64]
P2U	65:112	3	5:7	A3M2	3	2[1:48]
P2D	1:64	3	1:4	A3M3	3	3[1:64]
P2D	65:112	3	5:7	A3M4	3	4[1:48]
A2U	1:64	3	1:4	A3M5	3	5[1:64]
A2U	65:112	3	5:7	A3M6	3	6[1:48]
A2D	1:64	3	1:4	A3M7	3	7[1:64]
A2D	65:112	3	5:7	A3M8	3	8[1:48]
P2I	1:64	4	1:4	A4M1	4	1[1:64]
P2I	65:112	4	5:7	A4M2	4	2[1:48]
P2O	1:64	4	1:4	A4M3	4	3[1:64]
P2O	65:112	4	5:7	A4M4	4	4[1:48]
A2I	1:64	4	1:4	A4M5	4	5[1:64]
A2I	65:112	4	5:7	A4M6	4	6[1:48]
A2O	1:64	4	1:4	A4M7	4	7[1:64]
A2O	65:112	4	5:7	A4M8	4	8[1:48]
D1	1:64	5	1:4	A5M1	5	1[1:64]
D1	65:112	5	5:7	A5M2	5	2[1:48]
D2	1:64	5	1:4	A5M3	5	3[1:32]
D2	65:112	5	5:7	A5M4	5	4[1:64]

AFE Issues

Mapping AFEs into DFEs

AFE Card	Detectors	LVDS Cables	DFE Card
AFE1	P1U, P1D	2	1
AFE1	A1U, A1D	2	2
AFE2	P1I	1	1
AFE2	A1I	1	2
AFE2	P1O, A1O	2	3
AFE3	P2U, P2D	2	1
AFE3	A2U, A2D	2	2
AFE4	P2I	1	1
AFE4	A2I	1	2
AFE4	P2O, A2O	2	3
AFE5	D1,D2	2	3

Outstanding Issues

Parts to be Acquired:

- Vicor Power Supply
- Backplane
- AFEs — 1 for Phase 0, 3 for Phase I, 5 for Phase II
- DFEs — 1 for Phase 0, 2 for Phase I, 3 for Phase II
- Sequencers — 1 for Phase 0, 3 for Phase I and Phase II
- Cables
  - 3 50–conductor grey cables
  - 18 LVDS cables
  - 1553 to PW08
- ???

Questions:

- When can we have the parts?
- Are any special orders required?

Outstanding Issues

Firmware:

- What do we need?
  - AFE firmware modifications — *need help*
  - Sequencer firmware modifications — *need help*
  - DFE trigger equations (Molina, Carvalho, Martens, Vaz) — is there more?
- What assistance can we get?

Testing Issues:

- We want to start setting up for testing immediately.
- Where?
- What can be made available to us?

Could we establish a laison person?