Electrical Production Testing of the DØ Silicon Microstrip Tracker Detector Modules

The DØ SMT Production Testing Group

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Abstract

The DØ Silicon Microstrip Tracker (SMT) is the innermost system of the DØ detector in Run 2. It consists of 912 detector units, corresponding to 5 different types of assemblies, which add up to a system with 792,576 readout channels. The task entrusted to the Production Testing group was to thoroughly debug, test and grade each detector module before its installation in the tracker. This note describes the production testing sequence and the procedures by which the detector modules were electrically tested and characterized at the various stages of their assembly.

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1 Introduction

The DØ Silicon Microstrip Tracker [1] is the innermost system in the Run 2 DØ detector. It consists of six four-layer barrel modules with microstrip silicon sensors parallel to the beamline, as well as twelve "F-disks" and four "H-disks" with silicon microstrip sensors normal to the beampipe. The main motivation for this interspersed Barrel-Disk design is the extended interaction region at the Tevatron and the desire to have all tracks intersect some of the detector planes at approximately normal incidence to provide optimal resolution. A total of 912 detector units, corresponding to 5 different types of assemblies, add up to a system with 800,000 readout channels. Hence the DØ silicon tracker is intermediate in size between the previous generation of silicon vertex detectors and those being designed for the LHC experiments. The silicon microstrip tracker was assembled in a modular fashion. The basic building blocks are the 12cm long ladders and the 30° wedges. Seventy-two ladders are arrayed in eight cylindrical concentric sub-layers to form a "barrel module". Beryllium bulkheads of a dodecagonal pattern at the ends of the barrels provide the major structural and aligning elements of the barrels; one of the two bulkheads incorporates the water cooling channel. Twelve wedges are mounted on a dodecagonal channel to form a planar "disk module". Six barrel sub-assemblies, each with an attached disk are mounted inside two 1.1 m long carbon-fiber half-cylinders which were the primary structural elements of the detector. Two special sub-assemblies, each consisting of three disk modules, complete the detector and are mounted at the ends of the silicon barrel structure. Four larger disks, at $z = \pm 94$cm and $z = \pm 126$cm provide improved momentum resolution up to $|\eta| < 3$.

Bringing this whole assembly together in a fashion that leads to a reliable, functioning, accurate, and surveyable detector is the major task of the silicon microstrip tracker project. The complications introduced by the large number of signal carrying cables, and the water manifold connections make this formidable task even harder. Thorough testing of each ladder and wedge is required to avoid costly or even impossible back-tracking during the detector assembly. This note details the production testing sequence and the procedures by which the modules were electrically tested at the various stages of their assembly. Each section includes results for the test performed and the description of the equipment used. We also describe the criteria used in assigning an electrical grade to the finished detector modules. Descriptions of the assembly procedure and the testing of the silicon sensors are described in separate notes.

2 Testing Sequence

The essential building blocks of a detector module are the silicon sensors, the SVX chips and the readout hybrids. The silicon microstrip sensors were acquired from three manufacturers. Detailed tests were performed on the sensors both by the manufacturers and at Fermilab, the University of Oklahoma and the University of California at Riverside. These tests are described in detail in reference [2]. Information about the depletion voltage and the number of bad strips was provided as input to the testing and assembly group and taken into account when choosing sensors for a particular detector module.

The SVX-IIe readout chip [3] is a radiation hard CMOS custom made 128 channel device which consists of preamplifiers, 32 cell deep analog pipelines, 8 bit ADC's and sparsification. A total of $\approx 23,000$ chips were probed and thoroughly tested at Lawrence Berkeley National Laboratory as described in section 3. The yield of die that passed all tests was 61%. The SVX chips and associated readout electronics were mounted on a flexible kapton circuit referred to as "High Density Interconnect", or HDI.

The HDI is a two layer, 0.005 inch thick flex circuit of Kapton-k with gold/nickel plated copper pads. The requirements of 5 mil wide pads and 2 mil wide via feedthroughs made the HDI a technical challenge for production. Four different vendors supplied the $\approx 1,500$ bare HDIs of 9 different types needed for the SMT. Bare HDIs were tested for continuity and shorts between each of the pads on the front end and the 28 lines of the tail at test stations at Fermilab, the University of California at Irvine and California State University at Fresno, as described in section 4. HDIs that passed the tests were laminated onto 300μm thick beryllium substrates at Fermilab. The substrate provides a thermal path from the readout heat sources to the coolant channels, maintains the flatness of the HDI and includes precisely machined notches for ladder positioning and stability. Laminated HDIs were sent to two commercial companies in California (Promex and Silitronics) where the passive components and the SVX chips were mounted and the wire-bonds made between the SVX chips and the HDI pads. At this time, the HDI was ready to undergo an initial functionality test that included a visual inspection (to ensure that the components were mounted correctly and wire bonds were made to the right pads), and examination of distributions for pedestal and noise as a function of channel number for each of the SVX chips on the HDI. The behavior of the HDI during a large number of successive downloads and when used in cal-inject mode was also tested. The initial functionality test was performed at the California State University at Fresno and at Kansas State University, as described in detail in section 6. The average fraction of HDIs that passed the initial functionality was 70%. Problems with HDIs that failed the initial functionality test were diagnosed at the test sites or at Fermilab, and sent back to the vendors or to Fermilab for repairs. The diagnostic of problems is described in detail is section 10.

HDIs that passed the initial functionality test were shipped to Fermilab. At this time, extensive electrical tests (burn-in) were carried out on the HDIs over a period of 72 hours over which they were kept powered at room temperature. Pedestal and noise was measured in data and cal-inject mode for each channel. Sparse readout and the monitoring of temperature was also tested. Less than 1% of the HDIs failed the burn-in test; the most common cause of failure would be bad response to cal-inject on the data of one chip. Details of the burn-in test can be found in section 8.

HDIs that passed the burn-in test were glued onto silicon sensors and assembled into detector modules at Fermilab. The 50μm strips on the silicon sensors were connected to the SVX chip preamplifiers by means of wire bonds. At each step of the assembly sequence, the HDIs were electrically tested repeating the short functionality test. Completed detector modules were handed over to the debugging team to investigate their performance under HV bias.

During debugging, detector modules underwent a visual inspection of the wire bonds, and the resistance between the Beryllium pieces and the HDI ground was measured to ensure proper grounding. Detectors were biased in 5V incremental steps to look for broken capacitors on the sensors; strips with a broken capacitor were disconnected from the SVX preamplifier by pulling the corresponding bond. V-I and V-noise curves were produced, and the value of $\mathrm{V}^{-}_{\mathrm{max}}$ was determined. The debugging process is detailed in section 7. The debugging of the double sided detectors was performed by expert physicists and was the bottleneck for the production testing effort. Once the detector module was operational under high voltage, it was sent for detector burn-in.

The detector burn-in test used the same setup and software utilized during the HDI burn-in test, with a few additions: first, the detectors were cooled so that they effectively ran at a temperature of about 5 to 15 degrees Celsius, depending on detector type. Second, the detectors were biased at 5 Volts above their depletion voltage as determined from sensor probing. Detectors that pass the burn-in test were sent to the laser test, where they were placed on an x-y movable table, biased and shined on with a pulsed IR laser. The laser could be pulsed at a very high rate (100 kHz) and with a very short pulse (10 ns), thus a lot of data could be accumulated over a very short time. In a few minutes all strips of a detector could be examined as the detector moved underneath the luminous spot. The laser test therefore provided a detailed and fast test of each and every strip of the detector modules in a functional setting. Details on the laser test can be found in section 9.

Based on the information provided by the burn-in test on noise and by the laser test on response for each individual strip, the detector modules were assigned an electrical grade. Only A or B grade detectors were installed in the SMT. Modules that failed the burn-in test or the laser test were sent for diagnosis and eventually repaired, as described in section 10.

At each step of the production testing process the information on the tests performed and the results obtained, as well as the physical location of the detector module in question, was recorded electronically into the DØ SMT Production database [1] and manually (or by means of a printout) in the corresponding "Traveler". As already mentioned, debugging and repair was done by expert physicists; the burn-in and laser tests were operated by non-expert physicists on shift with experts coordinating the activities and helping with the set up of the tests. Detailed instructions of the daily activities and the procedures to be followed proved to be crucial to the operation, as was the meticulous bookkeeping of all activities. In the following sections each step of the production testing sequence is described in detail. The overall yield of detector production was about 85%. The lost detectors failed to pass either electrical or mechanical tests.

[1] the database can be accessed at http://martureo.fnal.gov/d0smtproduction

3 Testing of the SVX chips

The SVX-IIe chip is the final version of the design that was developed for the DØ upgrade tracking detectors. The chips were produced on 5 inch wafers, with 148 usable die on each wafer. A total of 206 wafers were produced and 155 of those were tested using an automatic probe station at Lawrence Berkeley National Lab. 120 wafers were tested in the first half of 1997, and 35 wafers were tested in the spring of 2000. The testing and analysis procedures were identical for both groups of wafers, except that the noise picked up during the tests in 2000 was higher, forcing us to relax the cuts for the analog and miscellaneous tests slightly. The general idea behind the testing procedure is to drive all chip inputs with a computer-specified pattern, sample the output lines and check that the output states are correct. Since the SVX is a rather complicated chip, many different tests are needed to characterize its performance. The tests can be separated into three categories: digital, analog, and miscellaneous. The digital tests exercise the readout and pipeline sections of the chip, as well as requiring the chip current draw to be within bounds for all four supply voltages. The analog tests exercise the front-end preamplifiers and pipeline amplifiers, in both positive and negative modes. Pedestals and gains are measured for all 32 pipeline buckets for each of the 128 channels. Finally, the miscellaneous tests exercise all of the auxiliary registers, which control the calibration voltage, the ramp rate used for digitization, the input bandwidth, the pedestal level, and finally the chip bias current. The probe station was used to physically position the wafer so that the probe card makes contact with a specific die. One die is processed at a time; all the tests are run on that die, then the probe station moves the next die into contact with the probe card. Once the tests were completed, the wafer was diced and chips visually inspected for mechanical damage to the chips, such as scratched surfaces and missing corners. Two wafers were broken during the dicing process. A thorough description of the tests performed is beyond the scope of this note and can be found in [4]. 17593 chips (77%) passed the digital tests, 14701 chips (64%) passed the analog and miscellaneous tests, and 13988 chips (61%) passed the visual inspection after dicing and packaging and were distributed. The yields from the 55-wafer group were identical to those from the 120-wafer group.

4 Testing of bare HDIs

The HDI circuit had to meet the requirement of being of low mass, yet contain the high density of components necessary to support the SVX chips requirements. HDIs therefore are a two layer, 0.005 inch thick flex circuit of Kapton-k with gold/nickel plated copper pads. The requirements of 5 mil wide pads and 2 mil wide via feedthroughs made the HDI a technical challenge for production. The production process had an inherent low yield, particularly at the early stages of the SMT production effort. Nine different types of HDIs were installed in the SMT. They are summarized in Table 1. We usually refer to the HDI types by their number of chips and the length of its tail. Inner barrel HDIs have a longer tail than outer barrel HDIs, to carry the power and signals outwards to a radius beyond the active silicon. The nine different types of HDIs are:

Table 1: Summary of the nine different types of HDIs installed in the SMT tracker. DSDM stands for double-sided double-metal silicon sensors. Pairs of SS H-wedges were glued back-to-back.

HDI type	# of chips	HDI circuit number	detector ID	detector type
3-chip barrel long tail	3	3351	31xx & 32xx	SS axial
3-chip barrel short tail	3	3314	33xx & 34xx	SS axial
6-chip barrel long tail	6	3651	61xx & 62xx	DSDM 90deg
6-chip barrel short tail	6	3611	63xx & 64xx	DSDM 90deg
9-chip barrel long tail	9	3953 & 3954	91xx & 92xx	DS 2deg
9-chip barrel short tail	9	3911	93xx & 94xx	DS 2deg
6-chip F-wedge	6	4611	FW-xxx	DS ±15deg
8-chip F-wedge	8	4811	FW-xxx	DS ±15deg
6-chip H-wedge	6	7611 & 7612	HW-xxx	SS 7deg

The test stand initially at the University of California at Irvine, and later at the California State University at Fresno, checked for continuity and shorts between each of the pads on the front end and the 28 lines of the tail.

This was accomplished through the use of a Ruker & Kolls semi-automated wafer probe station, controlled through GPIB interface with a PC running LabView. Given a coordinate map of the HDI circuit, the probe station stage positions each pad under a probe tip, connection is made through a GPIB multiplexing box, and a GPIB controlled multimeter checks for continuity or shorts between the appropriate line on the tail and the probe. There are approximately 60 pads to check per mounted SVXIIe chip on the circuit.

Yield of good bare HDI varied significantly between vendors and production batches. Litchfield Precision had a very low yield of $\approx 30\%$ after "fixing" (zapping the shorts with a high current). Dyconex would only deliver HDIs after testing them themselves, so they had a 100% yield by definition, but the cost of the HDIs were significantly higher. A good compromise between cost and yield was finally reached with two additional vendors: Speedy and Compunetics. Obtaining working bare HDIs was one of the major struggles of the early stages of the SMT production.

5 PC based test stands

All the tests performed on readout hybrids and detector modules used essentially the same type of test stand, based on the Stand Alone Sequencer Board (SASeq) [5], developed at Fermilab. The SASeq based test stands were developed independently from the full DØ readout system, and were relatively cheap ($\approx$ \$15,000), which allowed us to replicate them in large quantities and distribute them at various locations at Fermilab and at Universities, long before the final version of the full readout system was available. Using an easily reprodusable, relatively cheap version of the readout system proved crucial to the success of the production testing effort. Esencially, two types of test stations were built: burn-in stations, that could operate 16 devices (HDIs or detector modules) at once, and one-SASeq test stands that could read out only two devices at once. The one-SASeq test stands were used for initial functionality tests of HDIs (section 4), debugging of detector modules (section 7), laser tests (section 9), repair(section 10), and for barrel/disk assembly. Nine stations existed at the Fermilab Silicon Detector Facility and three more stations existed at Universities. In addition, they were also used by the Fiber Tracker group in Lab3 and by the electronics group in the DØ assembly building.

The harware configuration for the burn-in stations is shown in Fig. 1. It consisted of a VME crate that contained a Bit-3 VME controller card, eight Stand-Alone Sequencers (SASeqs), scanning 12-bit 64 channel analog-to-digital converter board (VMIVME-3113A) for current and temperature measurement, and master vertical interconnect board for high voltage crate control. The two-channel SASeq board was a self-contained data acquisition card designed to interface to the SVX chips. Its basic function was to control the SVX chip for data acquisition, collect the SVX data when a data cycle was requested, and to relay the data to the processor in the crate. The crate also housed eight interface boards (IB) designed and produced by Kansas State University (KSU). Every card had two independent channels and was used as a bi-directional interconnect between the SASeq and the HDIs. The card provided the proper software to control the SVX power on and power off sequence and prepared the data for the monitoring of currents corresponding to the three SVX operating voltages (AVDD, AVDD2, DVDD), and for temperature measurement.

Each SASeq was connected to an IB by a 10 feet long 50 conductor cable with an impedance of 82 Ohms. Three low voltage power supplies were used to supply the three operating voltages needed by the SVX chips. A voltage SVX Power distribution panel was located between the power sources and the interface board crate and was used for the distribution of the SVX power and the interface board power for each of the eight IB.

Bias voltage was provided independently for each detector module via a bias voltage distribution panel. The panel was located between the high voltage sources and the interface board crate. A set of switches on the panel allowed for 3 different schemes for the biasing of double sided detectors: positive bias applied to the n-side, negative bias applied to the p-side, and "split bias", in which both positive and negative bias was applied at the same time to the n- and p-side respectively. The burn-in stations needed a separate VME crate to house the high voltage sources to bias the detectors. For the one-SASeq test stations the HV module was connected to the same VME crate than the SASeq.

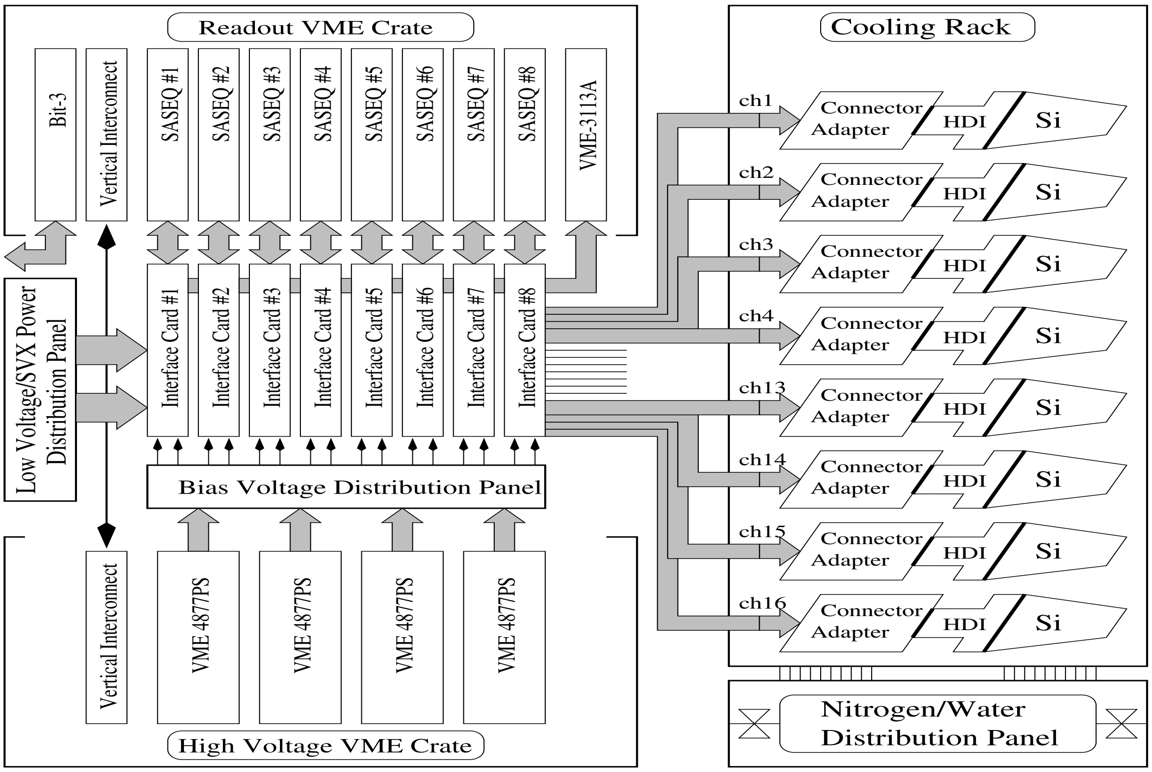

Figure 1: Burn-in test setup. For debugging/repair/laser stations only one SASeq/IB pair was used, and no cooling was provided.

The HV VME crate for the burn-in stations contained four VME 4877PS Motherboards and a slave vertical interconnect board for high voltage crate control. Every Motherboard carried eight HV pods. Thus the HV crate provided 16 positive and 16 negative independent voltages for silicon detector biasing and supported the current monitoring. The 4877PS Motherboard allowed the voltage to be set from 0 to 5000 V, with a maximum current of 2mA per channel. To ensure the safe operation of the burn-in stations, the over voltage hardware protection of the HV supply was set to 120 V.

The HDI tails were inserted into the Hirose connectors on the connector adapter boards. These boards contained the standard 3M 50 pin connectors and the Hirose connectors and were used as connector adapters between the signal cables coming from the interface boards and the HDI tails. The interface board was connected to the adapter board by a 10 feet long 50 conductor coaxial ribbon cable with an impedance of 75 Ohms.

The burn-in stations were outfitted with a cooling system to operate the detectors at low temperature. Up to 16 detectors were placed on shelves inside a regular rack that had been thermally isolated. The chiller temperature was set to 3C, and the detectors would run at temperatures between 5C and 15C, depending on the number of chips on the HDI. Each detector module was placed on a custom made, 7 x 9 inch aluminum plate, designed to accept any kind of HDI or Detector. Every aluminum plate was equipped with a pipe for cool water and special holes to provide nitrogen flow trough the box that enclosed the device under test. Two aluminum plates together with the connector adapter boards and signal cables were placed on a plywood board. This board was equipped with sliders to simplify loading and unloading of the devices under test. Plywood was chosen because it was a cheap, non thermo-conductive material that helped reduce the condensation on surfaces inside the rack. Every board had it's own water and nitrogen pipe. The control over the water and gas flow was provided by a control panel outside the rack. A software based interlock system monitored the temperature on each device and would shut down the power in the event that the temperature exceeded 50C, to avoid the melting of the epoxy used in detector assembly. The cooling system operated very reliably, except for the chiller, that broke down several times during the SMT production.

6 Initial functionality test of HDIs

Laminated HDIs were sent to two commercial companies for "stuffing". This included soldering of passive components, gluing of the SVX chips with conductive epoxy, and wire bonding of the SVX chips to the HDI pads. Stuffed HDIs were sent to the California State University at Fresno and to Kansas State University for the initial functionallity test. KSU was responsible for functional test of 628 HDIs, in all flavors. Personnel involved were a technologist, student, and a faculty member. Two test stands were initially available, although one was converted to full time use for interface board development. In addition a teststand at the University of Kansas was setup, and about 50 F and H disk HDIs were checked at that location. HDIs were received over a 12 month period from Sept '99 thru August '00. Test steps, all performed in a clean room, were:

1. **Visual Inspection:** This was done with 15-40X Zeiss microscope. The purpose was to obtain quick feedback for the vendors, such as wire bonder general problems (too-long tails for example) and to attempt to ameliorate any problems before electrical tests. Typical "repairs" at this point were to manually straighten out crushed bonds, identify missing or broken wire bonds for repair in-house, locate SVX chips with obvious defects, and also to blow off or pick off debris from previous handling. In some cases the inspectors were asked for additional information to be recorded such as glue coverage on the F-disk HDIs and other tasks. A K&S manual wire bonder was used to repair HDIs with modest numbers of bond problems. About ten such HDIs were successfully repaired at this stage.

2. **Electrical (static) tests:** A voltmeter was then used to check for power shorts, and to verify the electrical connection of platinum temperature measuring resistor. HDIs with shorts were set aside.

3. **Functional test:** This is the basic test of download and readout. 100 succesful downloads were required, and error free readout of 10K calibration and pedestal events. In addition one cycle (requiring about 15 minutes per HDI) of the standard burnin test was performed [2].

Download failures, were if possible, localized to a single chip using a manual probe station in conjunction with an oscilloscope and logic analyzer, and defective SVX chips marked for replacement. HDIs with problems were scanned at high magnification (50-250X) to search for chip and other defects. In about 50% of download and readout failures cases, a SVX flaw was visible. Chips which failed in readout were marked for replacement at Fermilab. Diagnostic success was anecdotally stated to be >70%, meaning that at least 70% of download and readout failures, when localizable to a single chip, could be recovered. About 30% of HDIs with shorts were recovered, in some cases by burning off debris at "high" current (less than 1A in order not to melt wire bonds), or by manipulation of HDI tails.

The average yield for working HDIs after stuffing was about 70%. As can be seen in table 2, the yield varied significantly between different HDI types and different batches of the same HDI. Similar results were obtained at the CSUF testing location.

7 Debugging of Detector Modules

The debugging of detector modules was the first attempt to read out and bias a completed ladder or wedge detector after assembly. The likelihood of damaging the detectors during asembly, and mainly during wire-bonding, was substantial. About 25% of the assembled detectors failed to download or to readout the SVX chips. Also, the leakage current was unacceptably high for about 95% of the double sided assembled detectors. We had to restore the functionality of the detectors before performing any electrical tests (burn-in or laser test).

The debugging process started with a thorough visual inspection of the finished module to ensure that no mistakes were made during wire bonding and no mechanical damage occurred. Resistance between the active Beryllium pieces and the HDI ground was measured. If the resistance was greater than 10Ω, the grounding had to be improved to avoid large coherent noise during operation. This was done by making a contact between one of the exposed ears of the active Beryllium piece and one of the HDI ground pads, either

[2] This short burn-in test was not performed at the CSUF testing location because of lack of appropriate equipment.

Table 2: Testing results for different HDI types. The HDI circuit numbers are detailed in Table 1.

HDI Type	Date Received	Devices Received	No. passed	% Pass	Original Condition
3611	11/99	16	16	100%	Untested
3651	12/99	50	43	86%	“
3351	2/00	19	19	100%	“
3911	7/00	26	16	62%	“
3953	2/00	6	1	17%	Bad
3954	2/00	12	9	75%	Untested
H Disk	12/99	27	22	81%	“
H Disk	Various	70	34	N.A.	Mixed
F Disk	various	192	108	56%	Untested

with a small wire or directly with a Silver epoxy trace. The next step was to perform a functionality test of the readout without applying bias to the detector. Download and readout failures were mainly caused by damaged SVX chips, misplaced or missing wirebonds and damaged HDI's. About 10% of the chips had to be replaced.

The next step was to bias the detector. The biasing scheme depended on the type of detector under considerations. For the single sided detectors (3-chip ladders and H-wedges), we applied positive bias to the ohmic side (the n-side, with no segmentation). Because single sided detectors did not have their bias applied on the coupling capacitor, they would not draw high currents and would remain operational even if a capacitor was broken during wire bonding. Debugging of the single sided detectors was a very fast and effortless process.

The situation was very different for the double sided detectors (6-chip ladders, 9-chip ladders and F-wedges). Double sided detectors were “split bias” by applying positive bias to the ohmic side (the n-side) and negative bias to the junction side (the p-side, corresponding to the axial strips for the ladders). As mentioned before, the leakage current was high even at low bias voltages for most of the assembled doubled sided detectors. Typically, the leakage current for a double sided detector was as high as 100μA at a bias voltage of about 10V applied on the ohmic side (positive bias voltage). When the bias voltage was applied to the junction side (negative bias voltage) the leakage current was somewhat lower but still much higher than desired. Such high values of the leakage current were due to broken AC coupling capacitors on either the ohmic or the junction side, that caused the leakage current to travel directly through the readout electronics connected to the broken AC capacitor. To substantially lower the leakage current we had to identify the broken AC coupling capacitors and disconnect them from the readout electronics by pulling the wirebond between the silicon sensor AC bonding pad and the SVX preamplifier.

To identify the broken AC coupling capacitors from one side of the detector it turned out to be more effective to apply the bias voltage on that side and to keep the other side grounded. In this way we maximized the voltage across the AC coupling capacitors located on the searched side. Typical diagrams of pedestal, noise (defined as pedestal fluctuations for each channel) and differential noise (defined as fluctuation of the noise difference between two consecutive channels) are shown in Fig. 2 for a chip containing one broken AC capacitor. The noise distribution proved to be the most useful one to identify broken channels, because the broken AC coupling capacitors would make the input of the preamplifier to be dominated by the DC component. The output of the preamplifier is almost constant and consequently the level of noise was low for broken channels and high for the neighbors (Fig. 2).

After pulling bonds we were able to raise the positive bias voltage applied to the ohmic side up to $V_{TS} + 30$ V. (The depletion voltage measured on the test structure V_{TS} was determined from sensor probing as explained in [2]). The leakage current at the test voltage V_{test} (defined as $V_{TS} + 20$ V, or 90 V, whichever is lower) was in the range from 5 to 25μA.

We had a few detectors with high values of the leakage current but no broken AC coupling capacitors. We concluded that the leakage current was due to defects in the bulk of the silicon sensors and could not be reduced by pulling bonds, or by any other means. The leakage current at depletion voltage was one of the

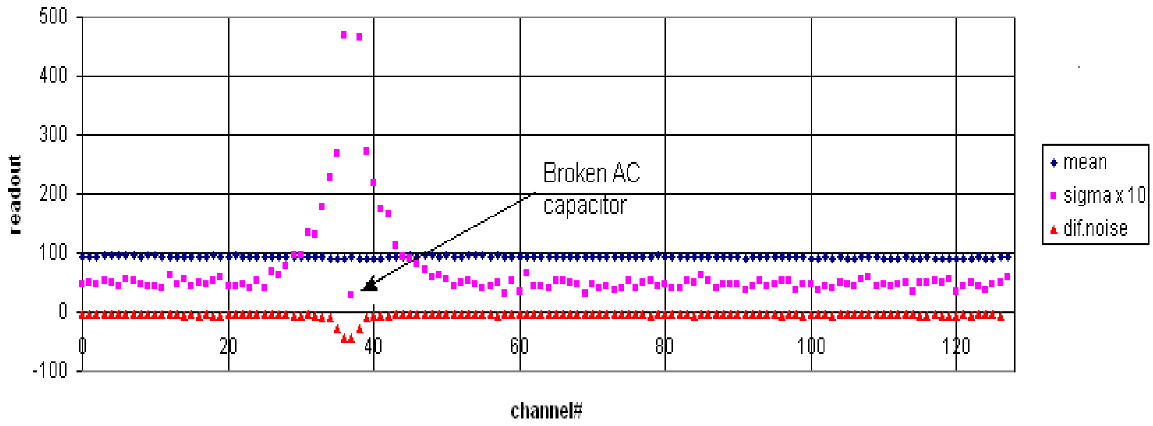

Figure 2: Distributions of pedestal, noise and differential noise for a chip containing a broken AC capacitor. The noise (sigma $\times$ 10) is low for broken channels and high for neighbor channels. The differential noise is plotted multiplied by -1 for better visual clarity.

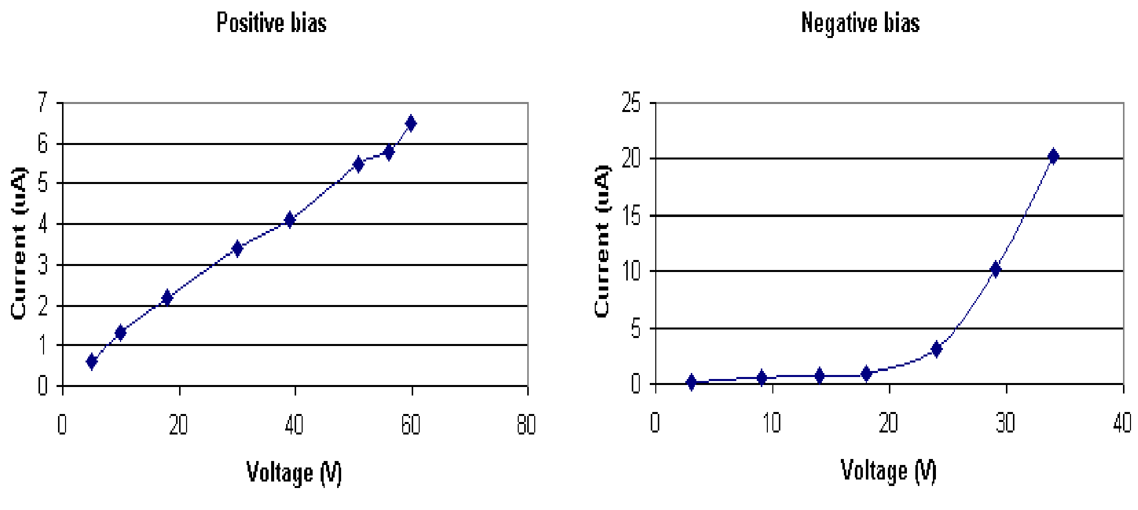

Figure 3: Typical I–V curves for positive (left) and negative (right) bias voltages. The onset of microdischarges can be observed in the negative bias plot at about 20V.

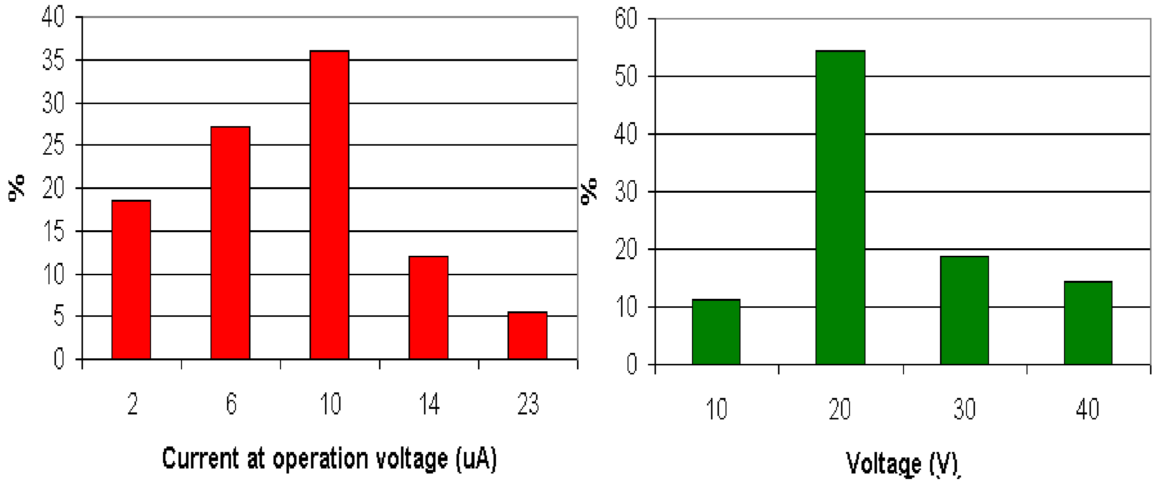

Figure 4: Distributions of leakage current at operating voltage (left) and V_{max}^{-} (right).

considerations in the final electrical grade of the detector. Detectors with very high leakage current were not installed in the SMT.

One additional consideration for our Micron detectors was that the negative bias voltage applied to the p-side was severely limited by micro discharges [6]. In the absence of broken AC coupling capacitors, V_{max}^{-} was defined as the highest voltage that could be applied on the p-side before the current started to grow exponentially. Above this value the leakage current, and also the noise, increased rapidly. In the absence of microdischarges, V_{max}^{-} was set to $\frac{1}{2}V_{test}$. Typical I–V curves for both positive and negative bias are shown in Fig. 3. In this example, V_{max}^{-} was set to 20 V. The distributions of leakage current at testing voltage and the values for V_{max}^{-} for our double sided detectors are shown in Fig. 4

Our studies indicate that the micro discharges will move from the p-side to the n-side after type inversion, expected to occur at an irradiation dose of about 0.4 MRad. Once the sensors type-invert, micro discharges will severely limit the bias voltage that can be applied to the n-side (Fig. 5). No evidence of breakdown for negative voltage applied to the p-side is observed in irradiated detectors after type inversion. To preserve the functionality of the detector modules, we will have to gradually increase the p-side bias component. It is therefore crucial that we stress the AC coupling capacitors as much as possible during debugging and testing while we still have the ability to disconnect a broken capacitor from the preamplifier on the SVX. If a capacitor were to break after the detector module was installed in the SMT, the whole module would become inoperable. Additional problems introduced by radiation damage are a significantly increased leakage current (about 1 mA compared with 10μA) and a 30-40% noise increase.

For double sided detectors, 0.8% of the channels were disconnected from the readout electronics during the debugging process. Because the bare silicon sensors were tested before assembly, and the broken channels skipped from bonding, we conclude that the capacitors broke during wirebonding. Only about 10% of the coupling capacitors broke when the bias voltage was raised above 20V.

The debugging of double sided detectors was performed by expert physicists working three 6-hour shifts on 2 dedicated test stands. A technician was readily available to pull bonds. It was the most time consuming step of the production testing effort, and therefore its bottleneck. It can be completely avoided by using single sided detectors.

8 Burn-in

The burn-in test was a part of the standard testing procedures during the SMT production testing. With small variations, it has been performed twice for each SMT detector module. First, the burn-in test was done on the HDI after its initial functionality test. At this point the goal of the test was to select good HDIs

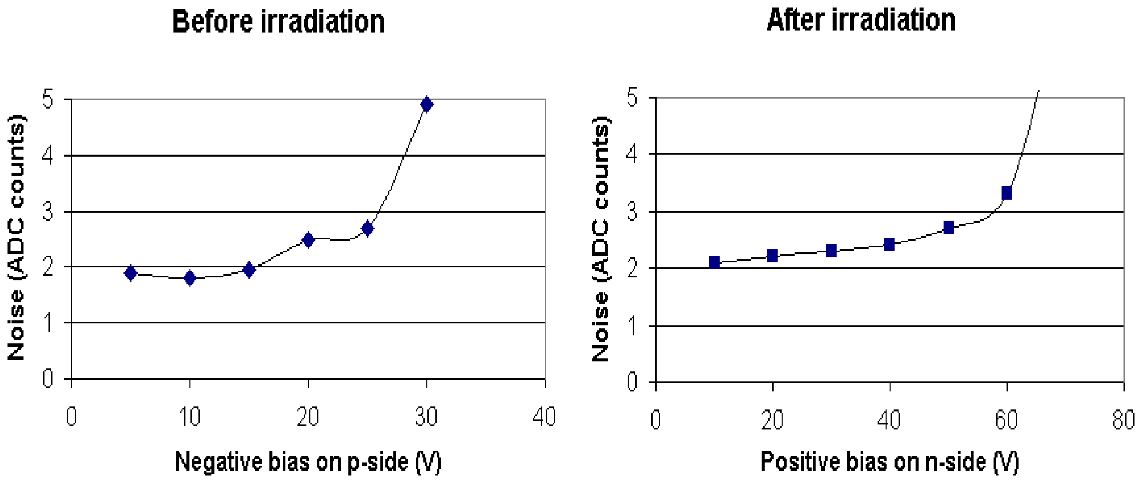

Figure 5: Typical diagrams of the total noise as a function of one side bias voltage for non-irradiated detectors (left) and irradiated detectors (right).

for future detector assembly. The second burn-in test was carried out after ladder or wedge assembly. The idea of the burn-in test is to run every SMT component for a long period of time (up to 72 hours) under conditions similar to those expected in the experiment and monitor its performance, in particular, measure pedestals, total noise, random noise and gain and examine occupancy in the sparsification mode. Monitoring information also included temperature measurement using the temperature sensor located on the HDI, chip current measurements corresponding to the three voltages applied to the chip (AVDD, AVDD2, DVDD) and, for ladders/wedges, detector bias voltage and dark current measurement. Typical problems revealed by the burn-in test were SVX chip failures, broken and shorted bonds, grounding problems, noisy strips and coupling capacitor failures, etc. At the early stages of the SMT R&D and construction the burn-in test was set up using the prototype DØ DAQ and electronics [7]. The setup was controlled by a graphic user interface on a Silicon Graphics host through the 68K Motorola computer running the VxWorks operating system booted from an SGI host [8]. Later the decision was made to use a PC based system for all the SMT production testing, which allowed us to avoid the complete data acquisition system assembly and provided a simpler, easier to manage and more reliable testing setup. To meet this requirement the Stand Alone Sequencer board (SASeq) [5] was designed and produced. It interfaced directly to the HDIs through the interface board (IB) and read out the data directly to a BIT-3 VME controller card. During the SMT construction phase, two PC based stations carrying eight SASeqs and correspondingly eight IBs each (16 readout chains) were put together to perform the burn-in test: one for HDI and another one for ladder/wedge burn-in test. After most of the HDIs had been tested, the HDI burn-in station was upgraded to run the ladder/wedge burn-in test. So the total capacity of the burn-in setups was 32 devices. This allowed us to keep up with the peak production rate of ≈ 20 detector modules per week.

The large volume of information coming from the burn-in test and the necessity to run the test for many devices imposed the requirement on the burn-in test software to be user friendly so that the burn-in stations could be operated by non-expert physisists on testing shift. A natural implementation of this requirement was a Graphic User Interface, written in the TCL/TK scripting language with the graphical toolkit in the Windows NT environment. The GUI allowed to solve two problems: first, it created a flexible and easily extendable system for performing a variety of tests and, second, it allowed us to put together executables written in different programming languages (Fortran, C, C++) for data taking from SVX chips, monitoring devices, and data analysis (see Table 3).

Several different tests were incorporated into the burn-in GUI: temperature sensor test, check of SVX chip download errors, check of readout errors, full burn-in test and short pedestal test. Fig. 6 shows the main burn-in panel (upper window); functionalities include temperature and burn-in test panel creation (upper row of buttons) and performing quick tests of the readout prior to burn-in test or for debugging purposes. Quick

Table 3: Burn-in test program constituents

Program name	Purpose	Language & authors
saseq.tcl	GUI and script to run burn-in test	Tcl/Tk E.Shabalina
teststand	Reads/writes data into the chip creates raw data file	C++ P.Padley, E.Shabalina
newdaq	Converts raw data into ntuples	C M.Roco
anal_ped	Reads ntuples, fills pedestal histograms and calculates total and random noise	Fortran E.Shabalina
anal_gain	Reads ntuples, fills histograms and performs linear fit to extract gain	Fortran E.Shabalina
adcmon	Reads monitoring data from ADC	C++ S.Grinstein, E.Shabalina
hvpn	Operates HV supply	C++ E.Shabalina
burn.kumac	A collection of macros to plot the burn-in test results	PAW kumac E.Shabalina

test implies the initialization of eight sequencers (second row of buttons), downloading of the chips attached to two chains of each sequencer (third row) and data taking (lower row). Chip downloading is performed using the dedicated panel (lower left window in Fig. 6) which allows to set the download parameters, create download file and display the result of the downloading comparing the download parameters in the file with the ones read back from the chips. Data is taken with the lower right window in Fig. 6 where the user can specify the type of run required (data or calibration run), the calibration voltage, the number of events and the file name to store the data.

The different tests performed during burn-in were the following:

Temperature sensor test:
All HDIs (except 6-chip F-disk HDIs) have temperature sensors mounted close to the SVX chips dissipating significant power (4 mW per channel) during operation. The temperature sensor is a resistor with a known linear dependence of the resistance with temperature: $1000\Omega@0C + 3.85\Omega/C$. So the voltage measured on it is proportional to the temperature. Since at high temperature the glue used for ladder and wedge construction melts, causing damage to the assemblies, the termosensor will be used in the experiment to keep track of the operating temperature of the ladders and wedges, and set off the alarms, if necessary. The purpose of the temperature sensor test is to make sure that the sensor measures correct temperature. The test is performed with all readout electronics off. In this case the sensor is expected to measure the room temperature. The voltage on the temperature sensor measured by the 64 channel ADC is converted into temperature based on the ADC and interface board calibration. Fig. 7 shows the temperature test panel. The user is expected to enter the device names into the appropriate windows and start the test by clicking on the "START" button. The program measures the temperature five times with an interval of 20 seconds between measurements. The average temperature is displayed in the lower row of windows for each device. The most common failure of the temperature test was due to the bad contact of the termoresistor to the HDI. These HDIs were repaired.

Data integrity check:
The goal of the data integrity test is to check the stability of the SVX chip downloading and the correctness of the individual chip identification number (ID) and channel numbers in the SVX data. Chip ID is specified in the chip download file. "Run Check" button on the long term test main panel (Fig. 8) provides the window to run this test. To test downloading the user has to create an arbitrary download file and define the number of download cycles. For each download cycle the program compares the initial download file with the one read back from the chip and counts the errors. Only those HDIs that had no download errors were

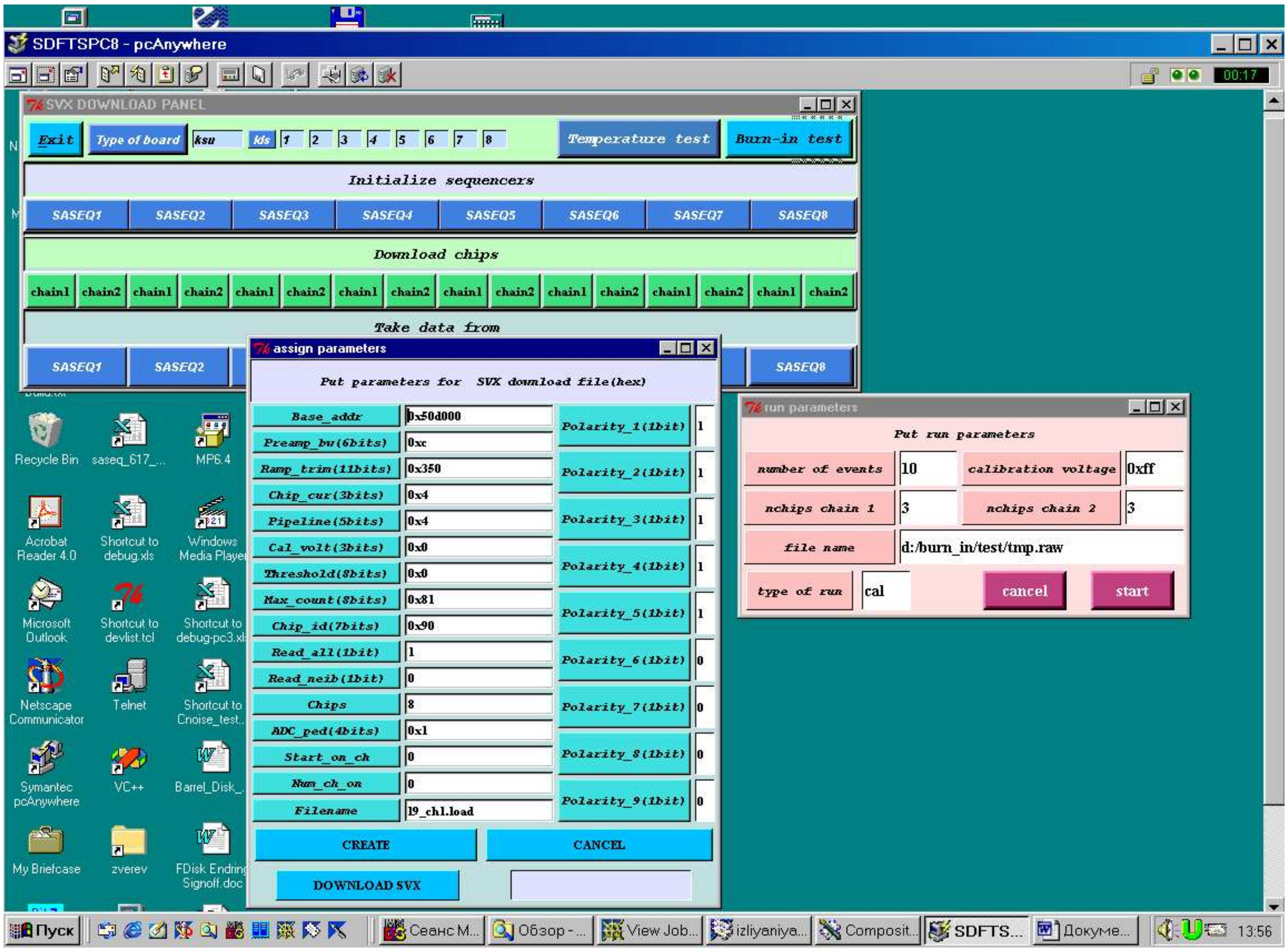

Figure 6: The main panel of the burn-in test GUI (upper window) with the windows for chip downloading (lower left) and data taking (lower right).

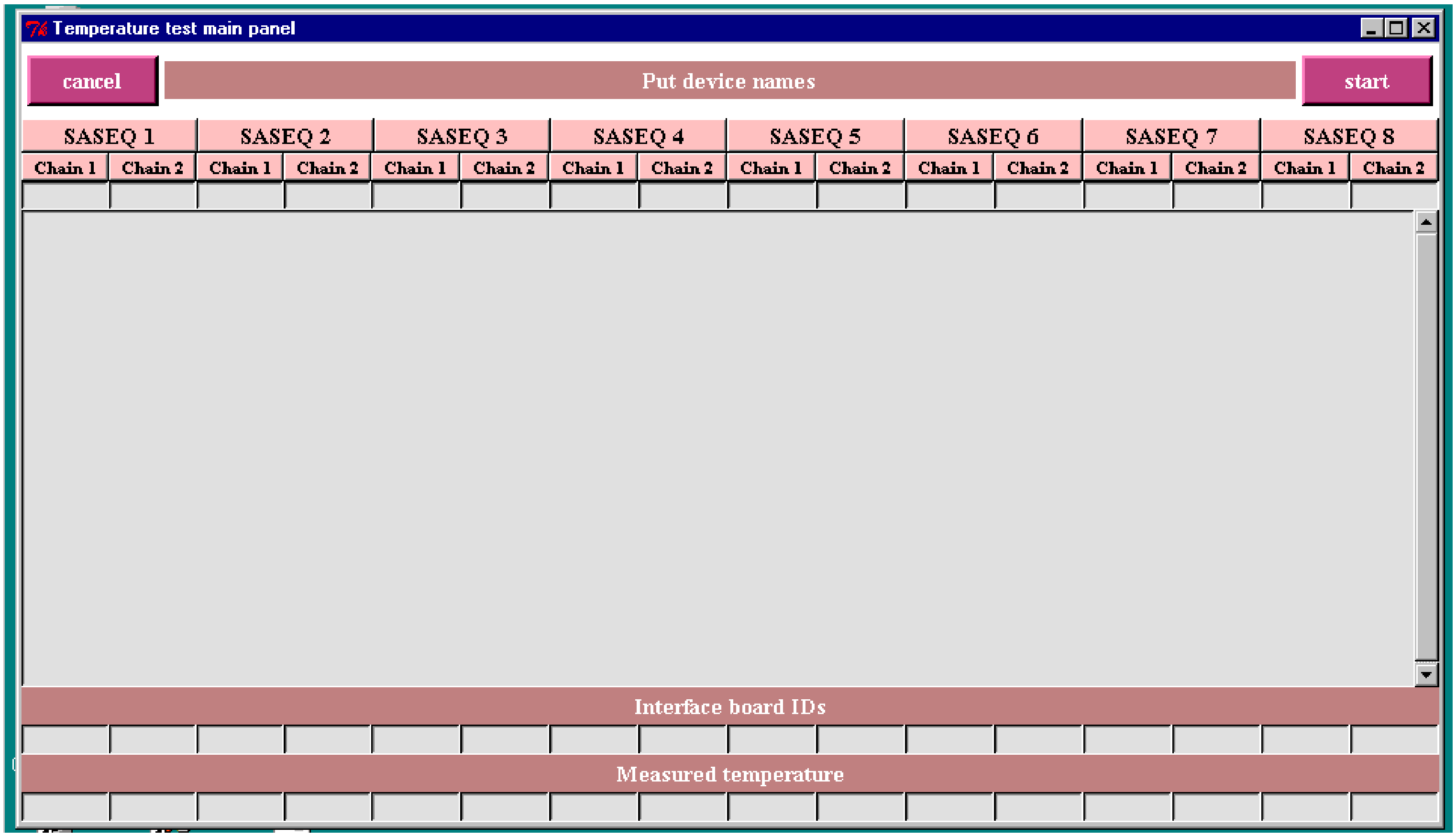

Figure 7: Temperature test panel. User specifies the names of devices under test in the upper entry windows. The measured temperature for each device is displayed in the lower row. The window in the middle informs about the current status of the test.

accepted for future tests. For chip IDs and channel numbers check, the known chip IDs are downloaded into the SVX chips. For every read out cycle the program compares the chip IDs in the data with the expected ones and also checks the sequence of the channel numbers (from 0 to 127) and pedestal values. The pedestal values are required to be nonzero and less than 254 ADC counts. The errors are counted and written out into the file. HDIs with no errors were accepted for production.

High voltage source operation:
To operate the high voltage supply a separate GUI has been created (Fig. 9). It allows to specify the address of the supply and its channel (pod) number, set the current limit and the bias voltage and read back the measured values of bias voltage, bias current and voltage and current limits. To provide smooth change of the bias voltage, the voltage is set in steps with a delay between them. The step size is calculated as a difference between the measured initial and the requested voltage value divided by 20. Minimum step size was 1V. Typical step values were from 2V to 4V. A typical time to bias the detector from 0V to 40V was 20 seconds. To avoid the detector breakdown the current at every step was required to be less than 15μA.

Long burn-in test:
Long burn-in test consists of a number of runs with a user defined interval between them. In each run, the SVX chips are tested in “read all” and “read neighbor” modes. In “read all” mode, chip pedestals are read out to evaluate the noise in each SVX channel and then chip calibration is performed. In sparsification (“read neighbor”) mode, where only the channels whose response exceeds the preset threshold and their immediate neighbors have to be read out, the frequency of false readouts is studied. To start a burn-in test the user is required to fill in the upper row of the long term test main panel (Fig. 8) with the names of the devices hooked up to the particular sequencer chains, select one of the six SMT device types (L3, L6, L9, FW6, FW8 or HW6, see Table 4) and specify the bias type (direct, inverse, split or no bias for HDIs). One also has to select the number of runs and delay between the runs. Since the chip parameters such as pedestal, random noise and gain depend on the values downloaded into the chip during chip initialization, a standard set of download files was created for all types of ladders and wedges. The download file parameters are listed in Table 5.

Table 4: Device types and bias voltage application scheme

Device type	Description	Bias type/polarity
L3	3-chip single-sided barrel ladder	Direct positive
L6	6-chip double-sided 90 deg barrel ladder	Direct negative or inverse positive or split
L9	9-chip double-sided 2 deg barrel ladder	Direct negative or inverse positive or split
FW8	8-chip p-side of double-sided F-disk wedge	No bias
FW6	6-chip n-side of double-sided F-disk wedge	Direct negative or inverse positive or split
HW6	6-chip single-sided H-disk wedge p-side	Direct positive

The run starts by taking one hundred pedestal events in data mode to obtain the total and random noise of the device under test. The raw data is written into a file, then converted into ntuples and analyzed with the analysis program using HBOOK. The analysis program fills the pedestal histogram for each readout channel. The average and the width of these distributions define the average pedestal and total noise in every channel respectively. For every event the program also calculates the common line shift (average pedestal over 128 SVX chip channels) and subtracts it from the pedestal in every channel. Then the “corrected pedestal” histograms are filled for every channel and the channel random noise is defined as the “corrected pedestal” distribution width. The output is stored as ascii and hbook-files. The ascii-file contains the list of all channels with average pedestal, total noise and random noise in each channel and the same parameters averaged over all channels of a chip along with the list of the noisy channels. A channel is added to the noisy channel list if its random noise exceeds the average one of the chip by $2\sigma_N$, where σ_N is the width of the chip random noise distribution. Note that for final grading a different definition of the noisy strip has been used. Pedestal analysis in the data mode is followed by a similar one for the pedestal read in the calibration mode of the chip.

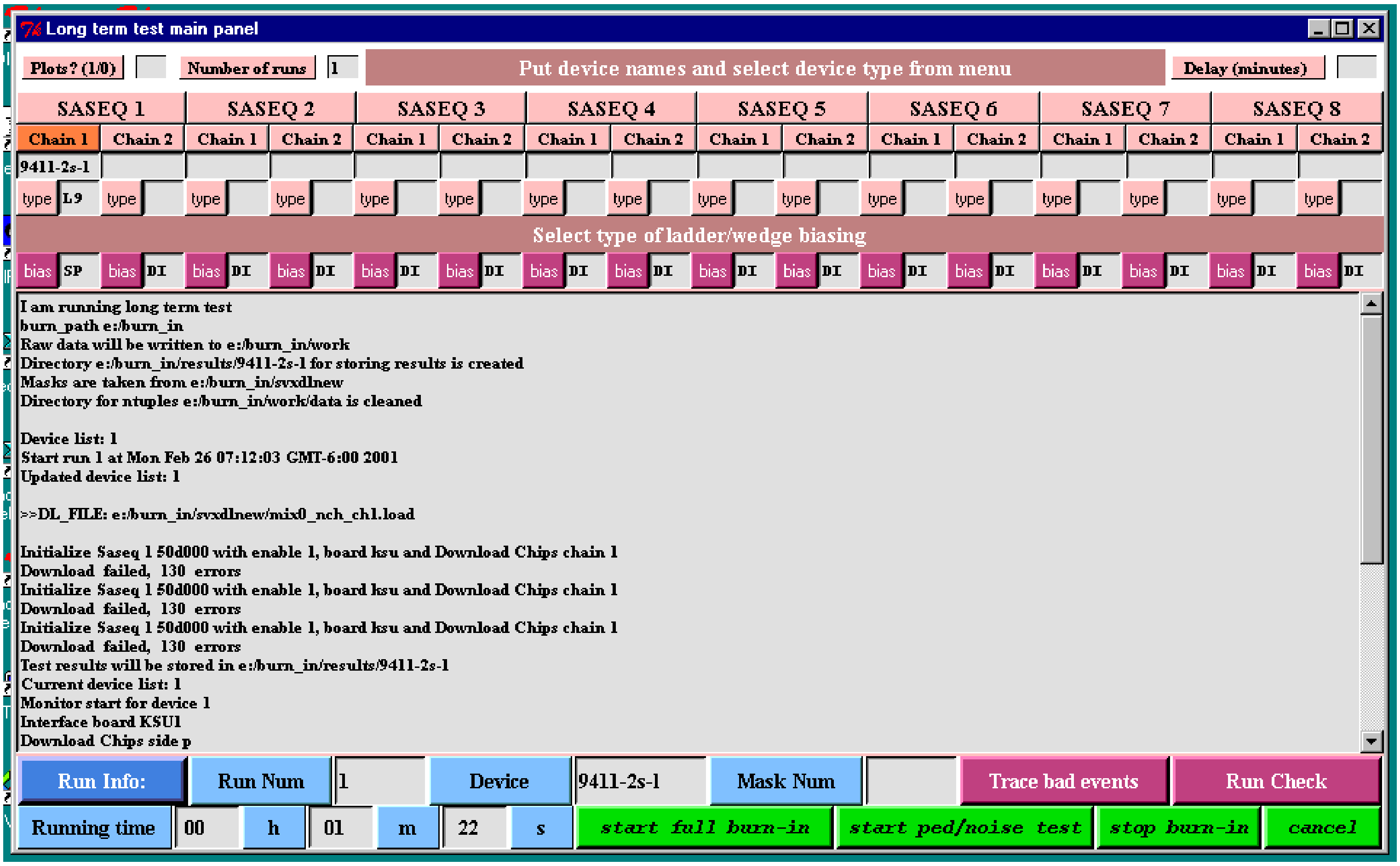

Figure 8: Long term test panel. Green buttons allow to start full burn-in pedestal test and interrupt the test. Maroon buttons start the data integrity checks. The middle and bottom windows show the current status of the test and running time.

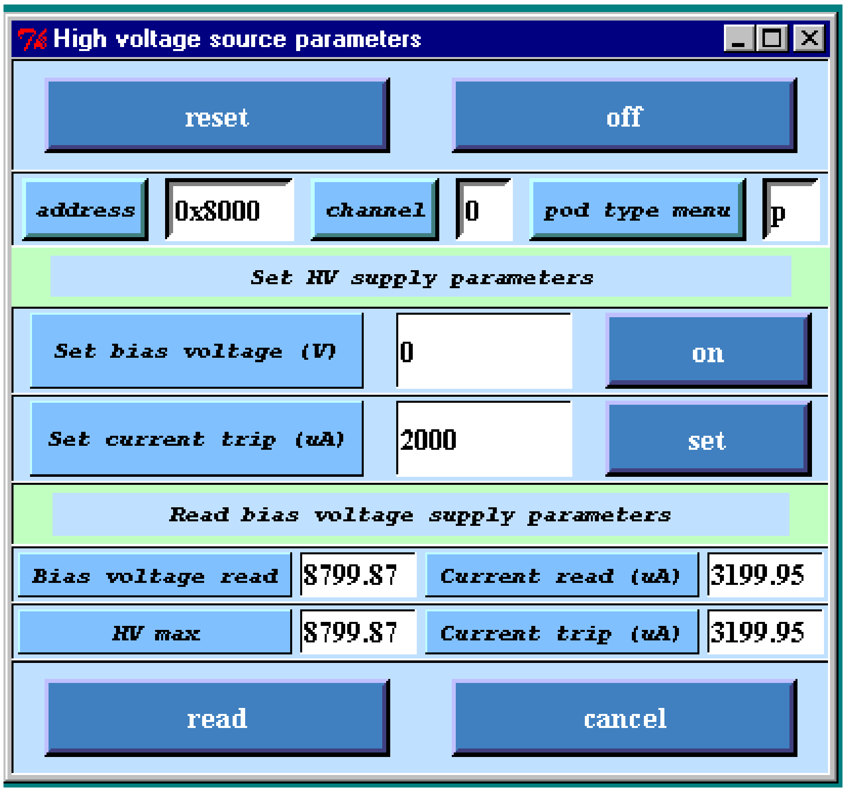

Figure 9: User interface for high voltage source operation. The panel allows to set and read back voltages and currents.

Table 5: Basic download file parameters used in burn-in test (hex)

Parameter	Value	Comment
Preamplifier bandwidth (6 bit)	0c	Adjusts preamplifier bandwidth for different detector capacitances and Interaction time; the value is chosen for operation at 132 ns
Ramp trim (11 bits)	0700	Adjusts the ramp capacitor value over a 20% range by adding binary Weighted capacitors; the value is chosen to set full scale (255 ADC) equal to 40 fc
Chip current (3 bits)	04	Sets scale of chip autobias currents
Calibration voltage (8 bits)	00	Sets internal calibration voltage; since in burn-in external calibration was used, the parameter is set to zero
Pipeline depth (5 bits)	02	Sets analog storage delay from 0 to 31 samples
Threshold (8 bits)	010	Sets threshold in digital comparator, this parameter is used in sparse mode and calculated for each chip
Pedestal (4 bits)	02	Fine adjustment of the ADC pedestal value; the value corresponds to about 100 ADC pedestal
Maximum counter (8 bits)	081	Sets the stop value of the A/D Gray Code counter, the value corresponds to 255 ADC

The next step is the chip calibration. Each channel of the SVX chip is connected to a build-in test input capacitor. This capacitor allows each channel to be pulsed independently or simultaneously. For gain studies, a known increasing charge has to be injected into each channel. However, to minimize the effect of the cross talk between the adjacent channels on one hand and to obtain the reasonable run time of the test on the other hand, not all channels of the chip but every 8th one is pulsed simultaneously. This is achieved by downloading the appropriate mask into the chip. For this mask four calibration pulses provided by the sequencer (Hcal = 0xf4, 0xee, 0xe8, 0xe2 for p-side and Hcal = 0x4, 0xa, 0x10, 0x16 for n-side) are applied one after another to the chip. For each value of the calibration voltage 100 events are taken, written into the file and converted into ntuples. The injected charge corresponding to the applied calibration pulse is calculated according to the formula:

$$Q = C_{test} \times (V_{AVDD} - V_0 \frac{H_{cal}}{255})$$

where $V_{AVDD} = 5.17$V, $V_0 = 5$V, and $C_{test} = 17fF$ is the capacitance of the SVX chip test capacitor. The analysis program reads in ntuples for four calibration pulses, subtracts the average pedestal for each of the 128 channels in a chip (obtained from the preceding pedestal run in calibration mode) and extracts the gain as a slope of the linear fit over four responses in the injected channels. The same analysis cycle is repeated for 8 masks so that the charge is injected in every channel of the SVX chip. The gain and the gain error obtained from the fit are stored as hbook and ascii files. Gain error characterizes the quality of the linear fit as well as the errors of the channel response for each value of the injected charge. The list of the channels with the gain three sigma away from the average chip gain is also written out to an ascii file.

The calibration is followed by the sparse readout test. To perform it the appropriate thresholds have to be set for each chip. The threshold is defined as the average pedestal of a chip plus three times its average total noise measured in calibration mode and the corresponding download file is created. To test the sparse readout the program loops over eight masks as during chip calibration and the calibration charge is injected into every 8th channel of a chip. In sparse mode of operation, a chip is expected to read out only those (injected) channels that are above the threshold and their two neighbors. The value of the injected charge should not be too low to provide the chip response above the threshold. On the other hand the charge should not be too large to minimize the cross talk between the channels which could cause false readouts. To evaluate chip performance in sparse mode the program calculates the frequency of false readouts of every channel. The readout is called false if the channel appears in the data more often than expected (this behavior is typical for noisy channels) or less often than expected (it happens for dead or low gain channels). For double sided devices calibration and sparse readout test were performed separately for p- and n-side because of the different polarity of the calibration pulse required for p- and n-side.

In the course of data taking, as well as during the intervals between the runs, the monitoring information was collected once per minute. The conversion of the ADC monitor counts into the corresponding chip current or temperature is performed according to the following formula:

$$I_j = k_j \times (\frac{V_{ADC} - V_{offset}}{C_{ADCtoV}} - k_{j0}).$$

Here I_j corresponds to the measured parameter ($I_{AVDD}, I_{DVDD}, I_{AVDD2}$ or T), V_{ADC} is the voltage in ADC counts, V_{offset} is the offset of the ADC monitor scale ($V_{offset} = -0.44$) and C_{ADCtoV} is the conversion coefficient of ADC counts into volts obtained from ADC monitor calibration ($C_{ADCtoV} = 204$ ADC/V), k_{j0} and k_j are calibration coefficients from interface board calibration. The interface board identification numbers are specified at the start of the burn-in test and the appropriate sets of calibration coefficients are used. Bias voltage and bias current (for ladder and wedge tests) are measured through the high voltage supply. Measurement date and time along with the values of parameters are stored in an ascii file. Since a temperature in excess of 50C would cause the melting of the glue used in the assembly of the silicon detectors, the temperature limit in the burn-in program was set to 50C. If the measured value happened to be higher, the burn-in test was stopped immediately. During the testing period this kind of emergency break off took place several times due to failures of the chiller in the cooling system. To keep track of the current status of the long burn-in test, the information about the steps being executed by the program and the duration of running is represented in the window of the main burn-in panel.

In the end of the burn-in test all raw data files for the last run and ascii files containing pedestal, gain and monitoring information are automatically copied to the storage disk and later linked to the data base. Burn-in script also creates the kumac-files used by the shifters to make plots after the end of the burn-in test or during it. The plots for all runs are analyzed and the data quality evaluation is performed by a shifter. The plots for the last run are printed out and inserted into the travelers.

In addition to the full burn-in test, there is a possibility to skip the chip calibration and sparse mode test and read pedestals only. This mode has been used to study noise mainly at the early stages of the SMT production. To add or withdraw a particular device from the long burn-in test without disrupting the other devices under test, the device burn-in panel was developed (upper window in Fig. 10). The panel would allow us to obtain a list of components under test and plot the monitoring information for them. Fig. 10 displays the plots showing the temperature and bias current dependence on the elapsed time. The drop in the bias current from 9μA to 6μA is clearly seen as the temperature goes down from 35C to 20C.

The typical results of the detector performance monitoring during the burn-in test are shown in Figs. 11 to 13. All chip currents are stable featuring the reliable functioning of the SVX chips and the read out chain. Minor fluctuations of DVDD current correspond to chip downloading. The temperature plot in Fig. 12 demonstrates the effect of the detector cooling. The bias current dependence on the elapsed time follows that of temperature.

Figs. 14 and 15 represent a typical output of the burn-in test for pedestal and noise of 3-chip ladder. The pedestal (upper plot in Fig. 14) and the corrected pedestal (pedestal with the common line shift subtracted, upper plot in Fig. 15) dependences on the channel number reveal some features common to most ladders and wedges. First, pedestal in channel 0 of each chip is significantly lower (10-15 ADC) than the average. This is true for all chips, even for HDIs that are not connected to sensors. Rather pronounced odd-even structure is seen in the corrected pedestal plot. It was observed for about 10% of all devices. The pedestal shape typical for the channel(s) with broken AC capacitors disconnected from the readout is seen around channels 43-45 of chip #1 and channel 48 of chip #2 in Figs. 14 and 15. The pedestal dip and lower total and random noise are the indications of the disconnected ("dead") channel with lower load capacitance. The neighbor

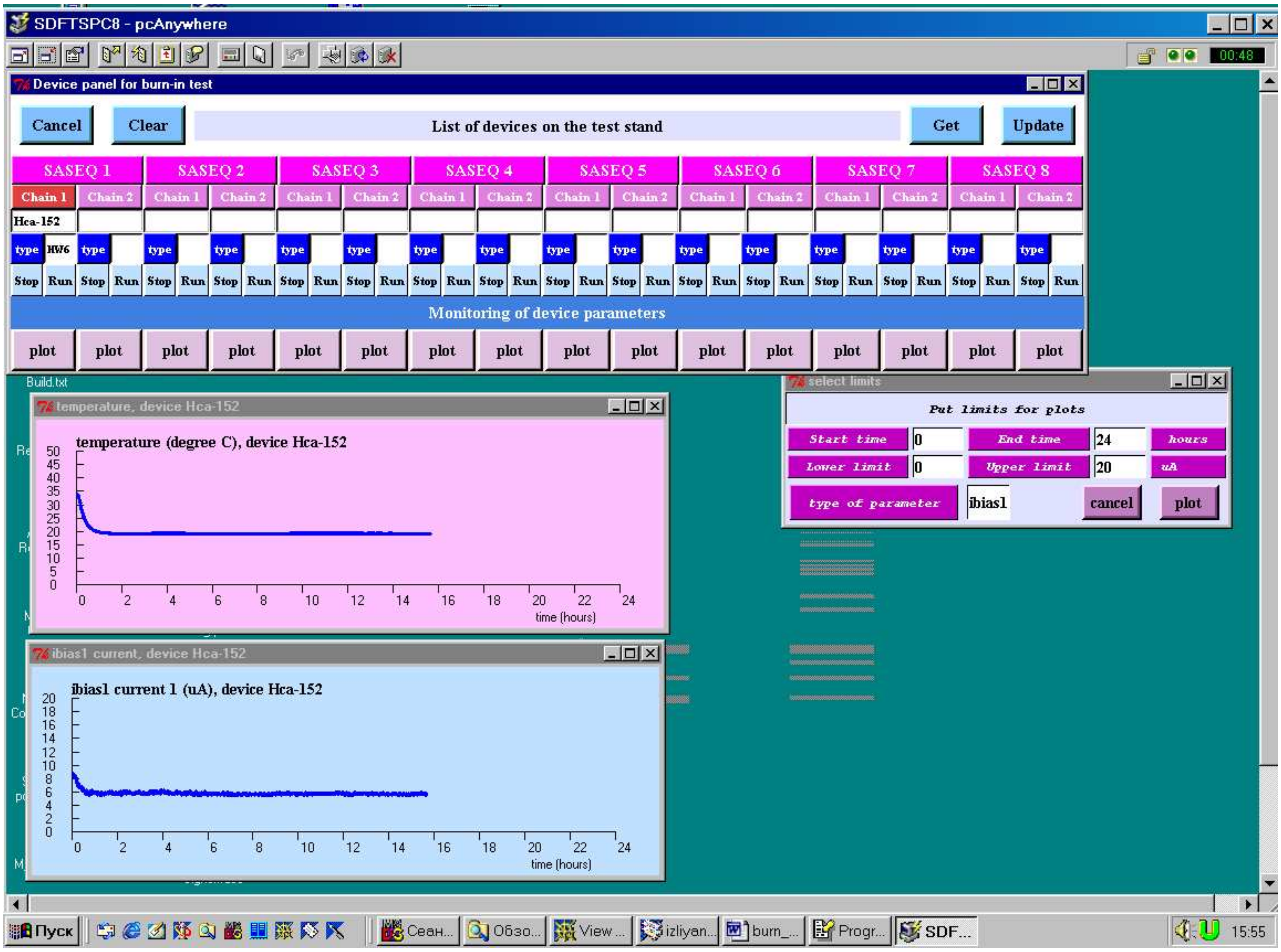

Figure 10: Device control panel. The plots display the temperature and bias current.

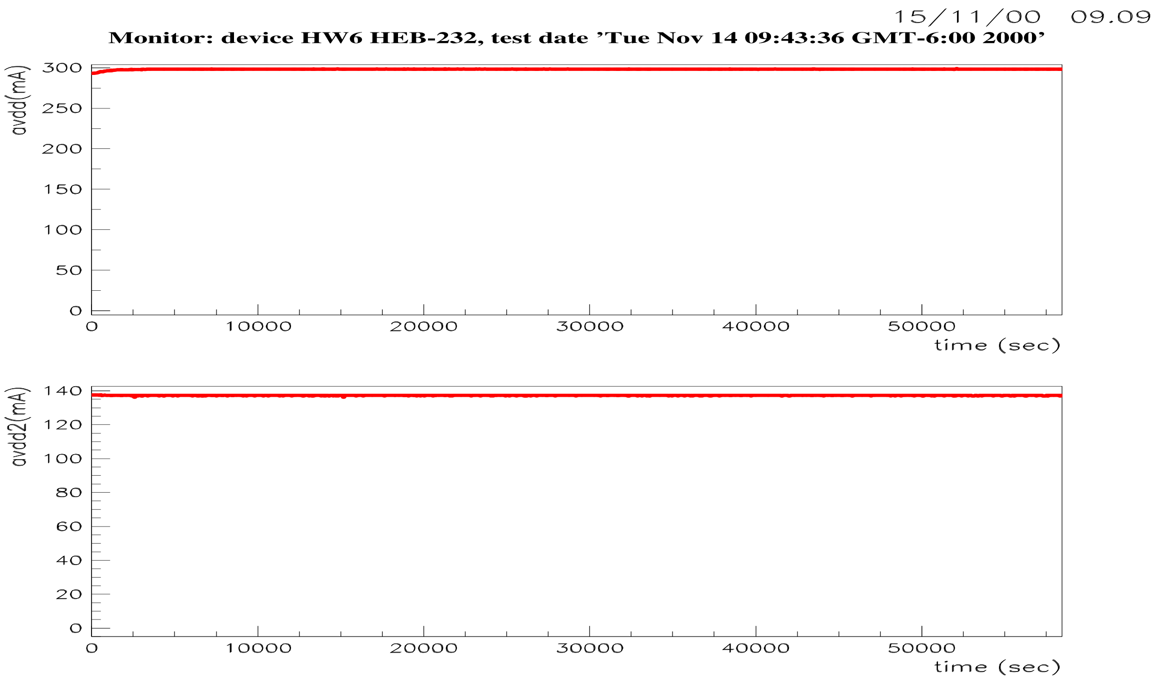

Figure 11: AVDD and AVDD2 chip current dependence on time for an H-wedge as measured during the burn-in test.

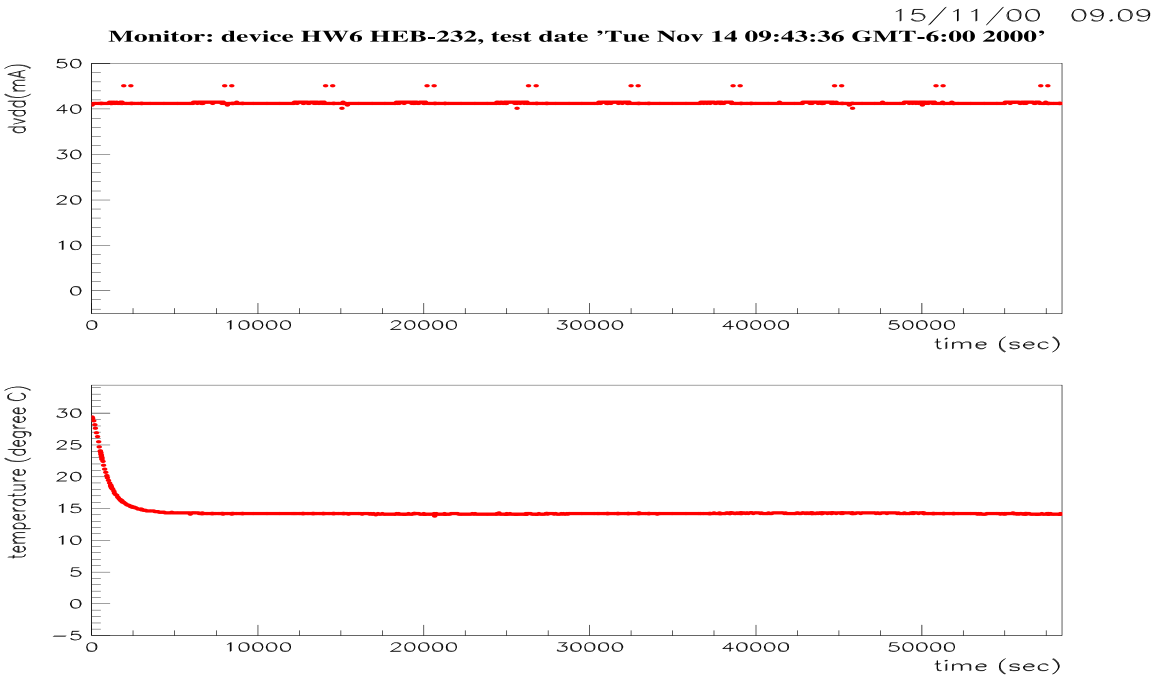

Figure 12: DVDD chip current and temperature dependence on time for an H-wedge ladder as measured in the burn-in test.

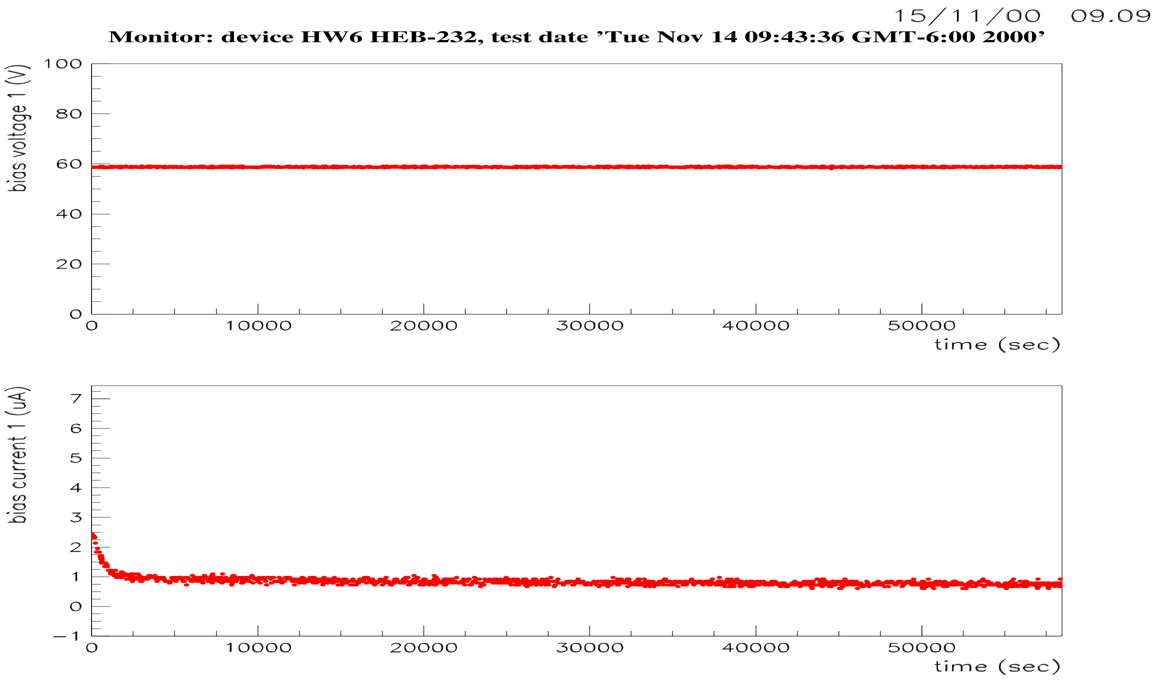

Figure 13: Bias voltage and bias current dependence on time for an H-wedge as measured in the burn-in test.

channels usually have somewhat higher pedestal and noise. Based on these burn-in test data channels 41, 42 of chip #1 and channel 47 of chip #2 are qualified as noisy because their random noise exceeds 6 ADC counts. [3]

Fig. 16 shows the same data as in Fig. 15 presented as the corrected pedestal and random noise distributions for each chip. Mean random noise for all chips is about 1.5 ADC counts. Fig. 17 displays the distributions of the total noise (left plot) and random noise (right plot) averaged over 128 channels for 34 3-chip ladders (102 chips) that passed the burn-in test. High values of the mean total noise were observed due to the improper pipeline depth in the SVX download file. At high pipeline depth the effect of the interference between the SVX preamplifier reset and the acquire mode has been observed leading to the large pedestal fluctuations in all channels of the chip in some events when data is taken with the software-generated triggers. The occurrence of even one such event per one hundred read out for total noise calculation leads to the dramatic increase of the total noise. The effect can be eliminated by setting the pipeline depth below 0×10. It was not seen in the burn-in data taken once pipeline depth equal to 0×2 had been selected in the SVX download files. This effect will not be a problem for the real run where read out is controlled by the accelerator clock and the preamplifier reset will take place during the large gap between beam bunches.

Another chip pedestal feature clearly seen in Fig. 15 is its noticeable slope. For most of the ladder and wedges, the corrected pedestal is not flat but its variation does not exceed 3 to 4 ADC counts. Pedestal slope affects the sparse readout leading to the loss of efficiency on the low pedestal side of the chip and increased occupancy on the high one. The output of the sparse mode test shown in Fig. 18 demonstrates in part these effects. The ideal result of the sparse readout test would be zero false readings for all channels (straight line at $y = 0$ in Fig. 18). If the point on the graph in Fig. 18 is above zero, it means that the particular channel is above the threshold with a probability y, even though the charge has not been injected in it or in its neighbor. This is a measure of occupancy. The groups of channels with increasing probability of false readout are seen beyond channel 100 of chip #0 and #1 in Fig. 18. This is a consequence of the nonzero pedestal slope of those chips, and the fact that the sparsification threshold can only be set to one value across each chip. On the contrary, if the point on the graph is below zero, the channel being injected is nevertheless below the threshold with a probability $|y|$, and has therefore not been read out. This is a

[3]This is the standard definition of noisy channel used for ladder/wedge grading, as explained in section 11.

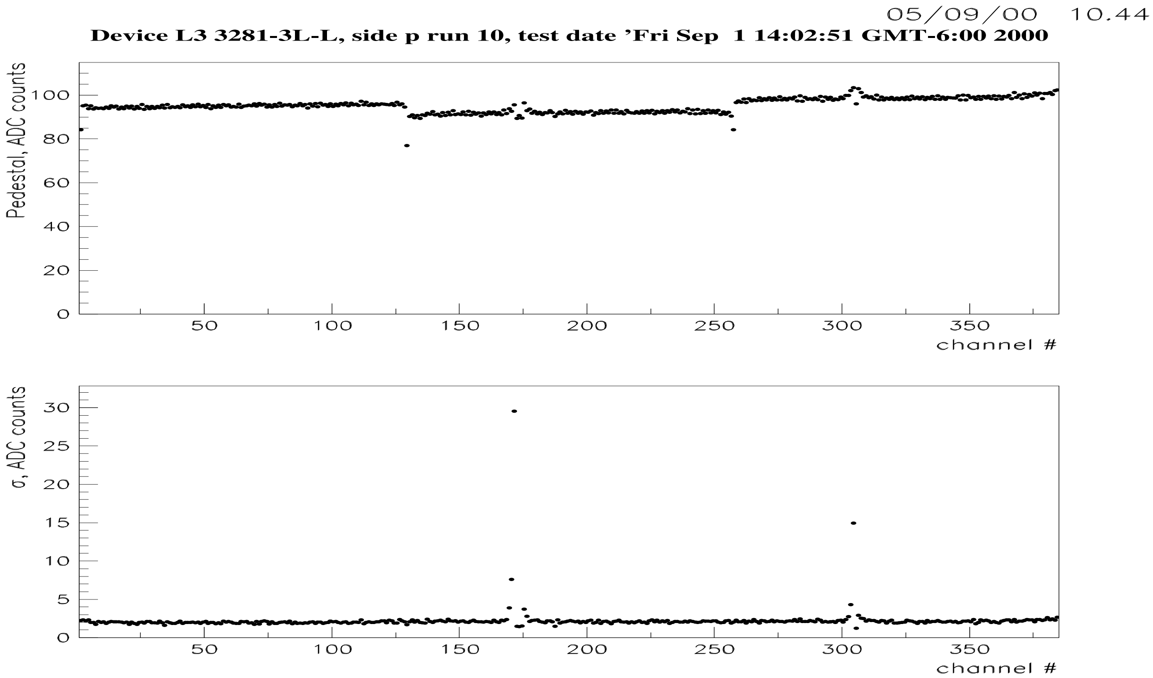

Figure 14: Pedestal and total noise versus readout channel number for a 3-chip ladder. Channels 43-45 of chip #1 and channel 48 of chip #2 are disconnected from the sensor.

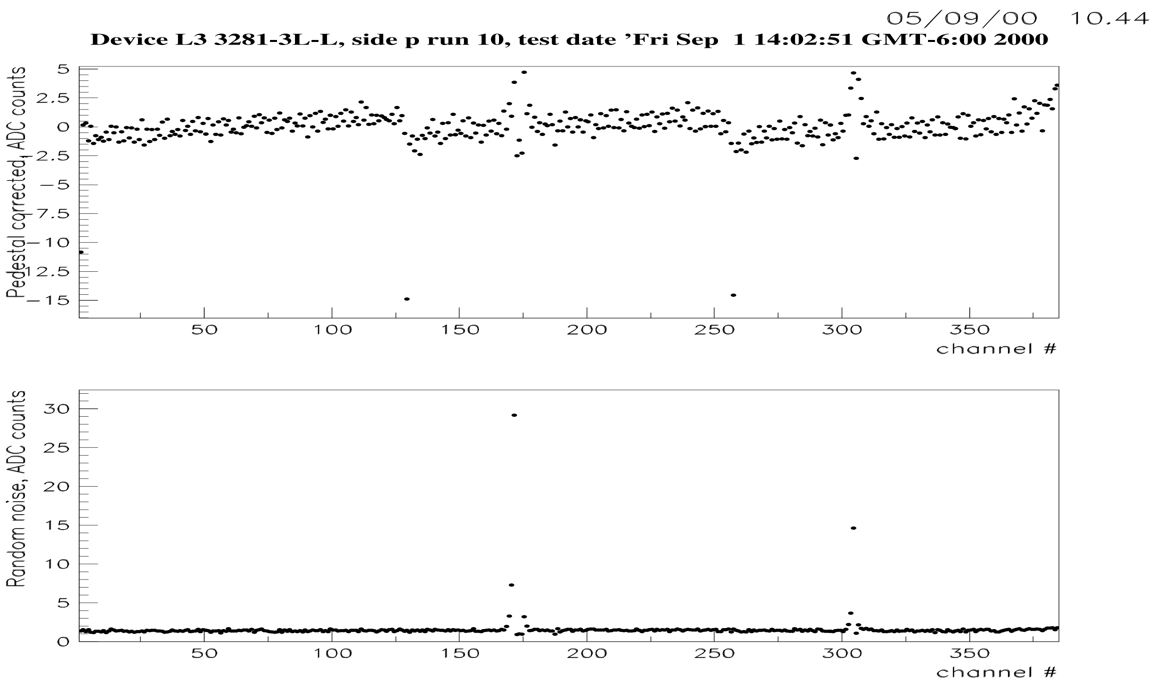

Figure 15: Corrected pedestal and random noise versus readout channel number for a 3-chip ladder. Channels 43-45 of chip #1 and channel 48 of chip #2 are disconnected from the sensor.

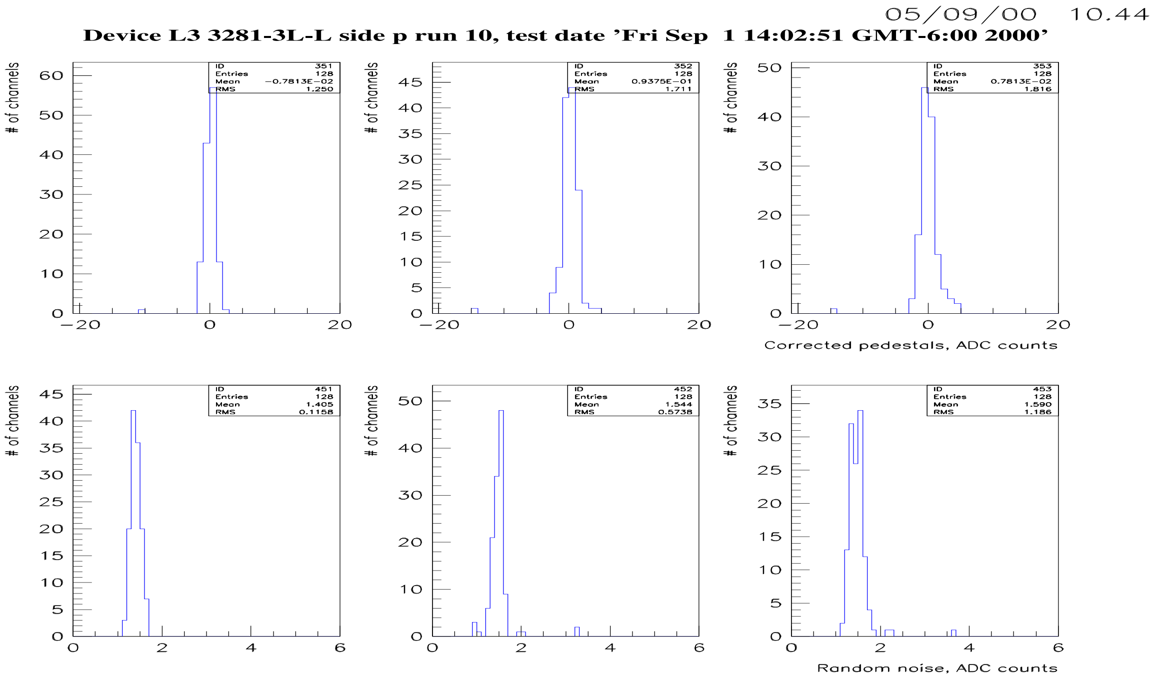

Figure 16: Corrected pedestal and random noise distributions for a 3-chip ladder.

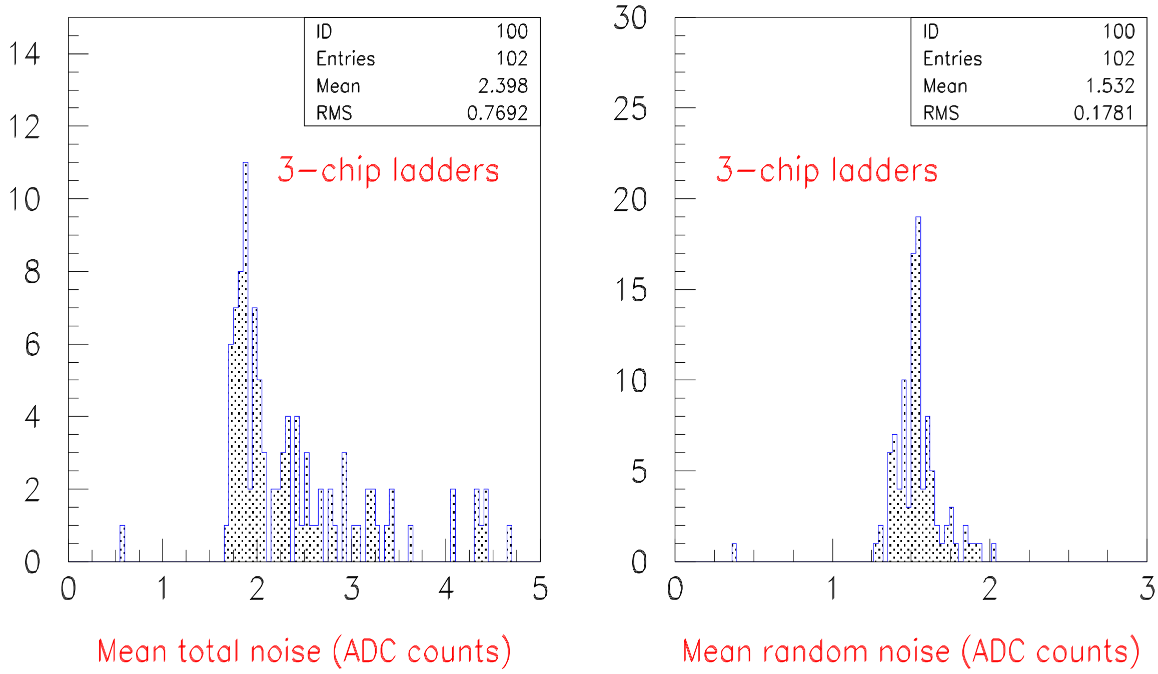

Figure 17: Distributions of the mean total and random noise per chip for 3-chip ladders.

Figure 18: The frequence of the false readouts versus channel number for a 3-chip ladder.

measure of the channel inefficiency.

In Fig. 18, channels 19-23 and 125-126 of chip #2 are below the threshold with the probability of one and can be qualified as dead. [4] Dead channels usually originate from failures of the coupling capacitor, and have very low gain. They are accompanied by the noisy channels (the ones with $y.gt.0.5$ in Fig. 18). To avoid the saturation of the corresponding preamplifier and the effect on the neighboring channels, the wire bonds of these channels are disconnected. Gain of the disconnected channels becomes equal to that of an HDI (see channel 42 of chip #0 in Fig. 19) while it is close to zero prior to the bond pulling (see channels 19-23 and 125-126 of chip #2 in Fig. 19).

The distributions of the average chip gain measured in the burn-in test for all types of barrel ladders are presented in Fig. 20. Mean value in the histogram relates to the p-side chip gain. The entries (if any) in 12-14 ADC/fc gain range relate to the corresponding HDIs, and correspond to readout channels that are not bonded to the sensor. Similar distributions for the disk wedges are shown in Figs. 21 to 23 for each chip separately. The dependence of the average chip gain on the strip length read out by a chip is clearly seen.

The most important characteristic that can be extracted from the burn-in data analysis is the noise performance of the SMT detectors. Mean noise in the system together with the number of noisy channels governs the SMT efficiency and occupancy. Figs. 24 and 25 show the distributions of the mean total and random noise for 6- and 9-chip barrel ladders. The fitted average of the mean total and random noise (as well as the fitted widths of the distributions) are similar for both types of ladders and lie within 1.70 ± 0.15 ADC counts. The long tails seen in the total noise distributions for 9-chip ladders are due to the interference between SVX chip preamplifier reset and readout cycle described above for 3-chip ladders. The shoulders in the total and random noise distributions for both types of ladders originate from the ladders with many noisy strips that were not installed in the SMT.

The performance of the 9-chip ladders in terms of the fraction of dead and noisy channels is presented in Fig. 26. In these plots noisy channels are identified following the standard noisy channel criteria of random noise larger than 6 ADC counts. The channel is called dead if its gain is below 2 ADC/fc or exceeds 10 ADC/fc. The lower limit selects the channels with low response, while the upper one selects the ones disconnected from the read out. The arrows show the 2.5% limit on the fraction of noisy and dead channels used for ladder and wedge grading, as explained in section 11. Both distributions peak at about 1% and

[4] Note that final identification of the dead channels is based on the laser test results.

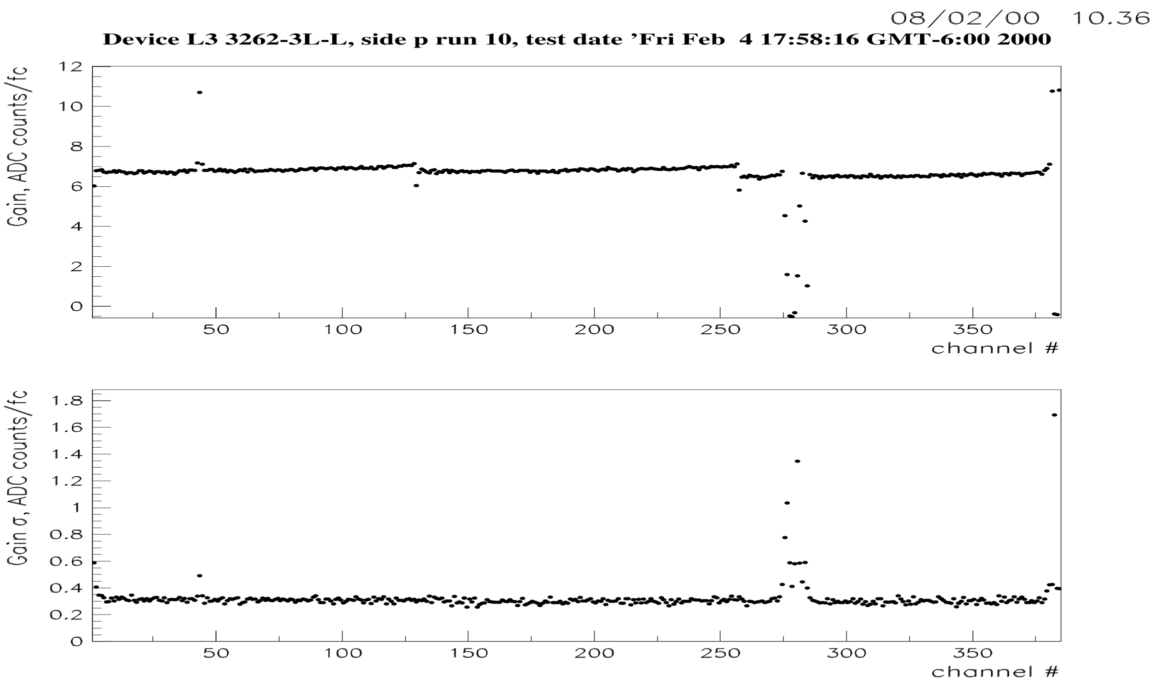

Figure 19: Gain and gain error versus readout channel number for a 3-chip ladder. Channels 19-25 and channel 125,126 of chip #2 have broken coupling capacitors not yet disconnected. Channel 42 of chip #0 has been disconnected.

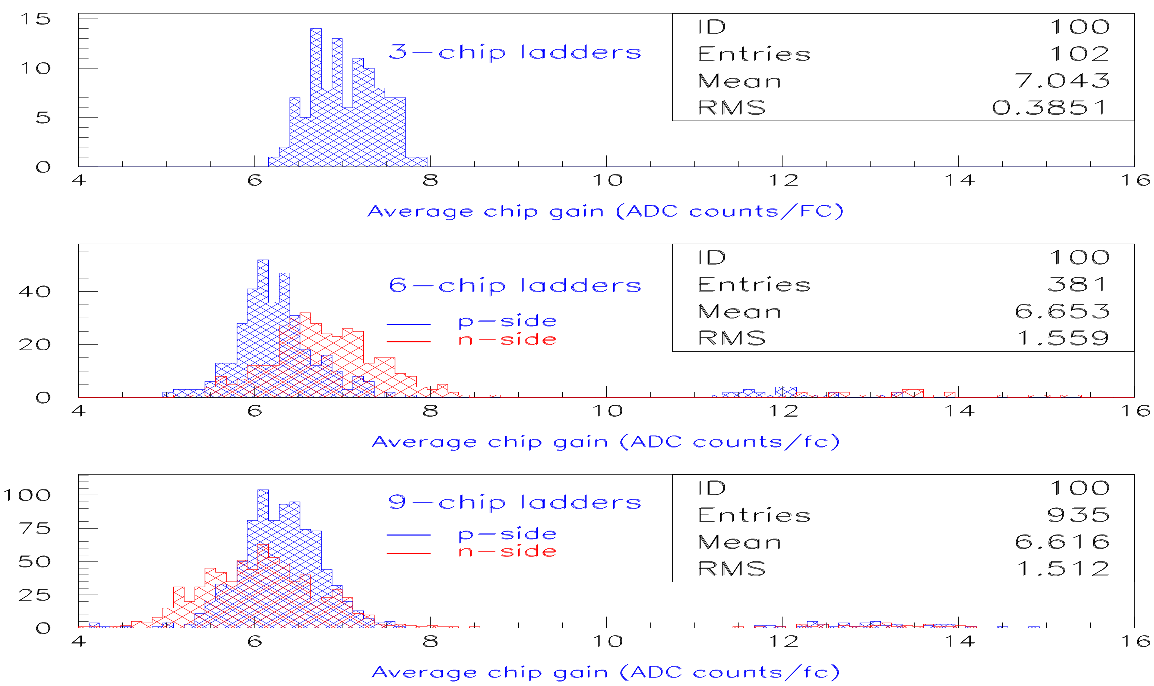

Figure 20: Average chip gain of barrel ladders. Entries in 12-14 ADC per fC gain range relate to the corresponding HDIs, and correspond to readout channels not bonded to the sensor.

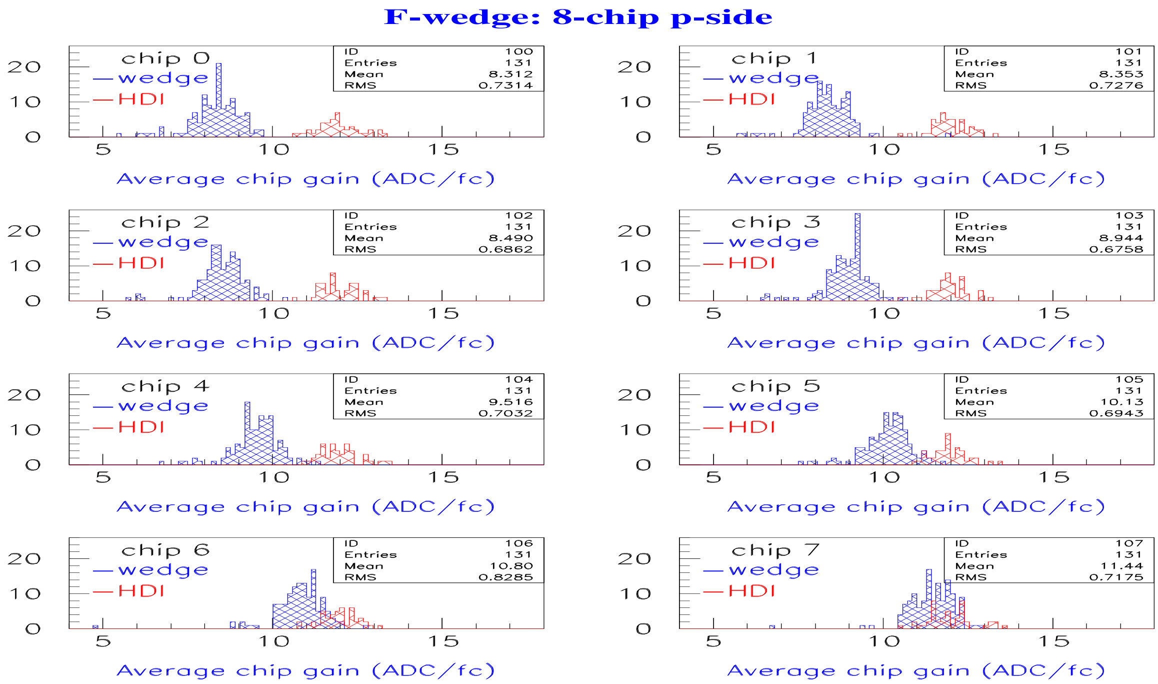

Figure 21: Average chip gain of F-wedge p-side. Red histograms represent HDIs.

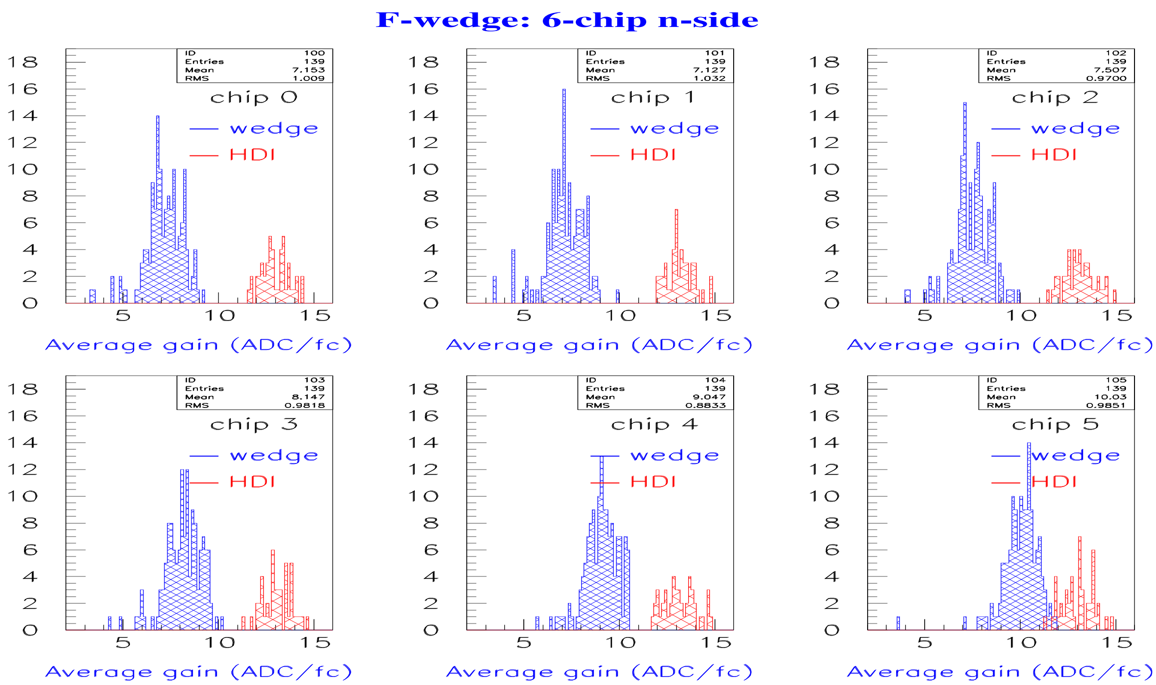

Figure 22: Average chip gain of F-wedge n-side. Red histograms represent HDIs.

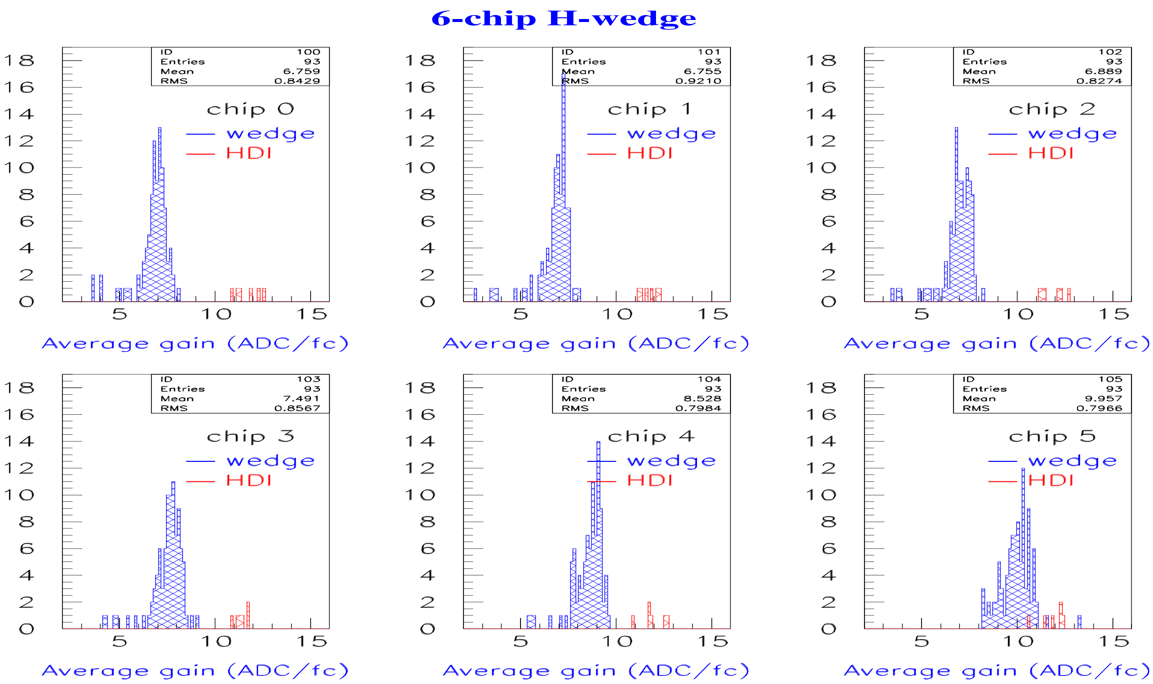

Figure 23: Average chip gain of H-wedge. Red histograms represent HDIs.

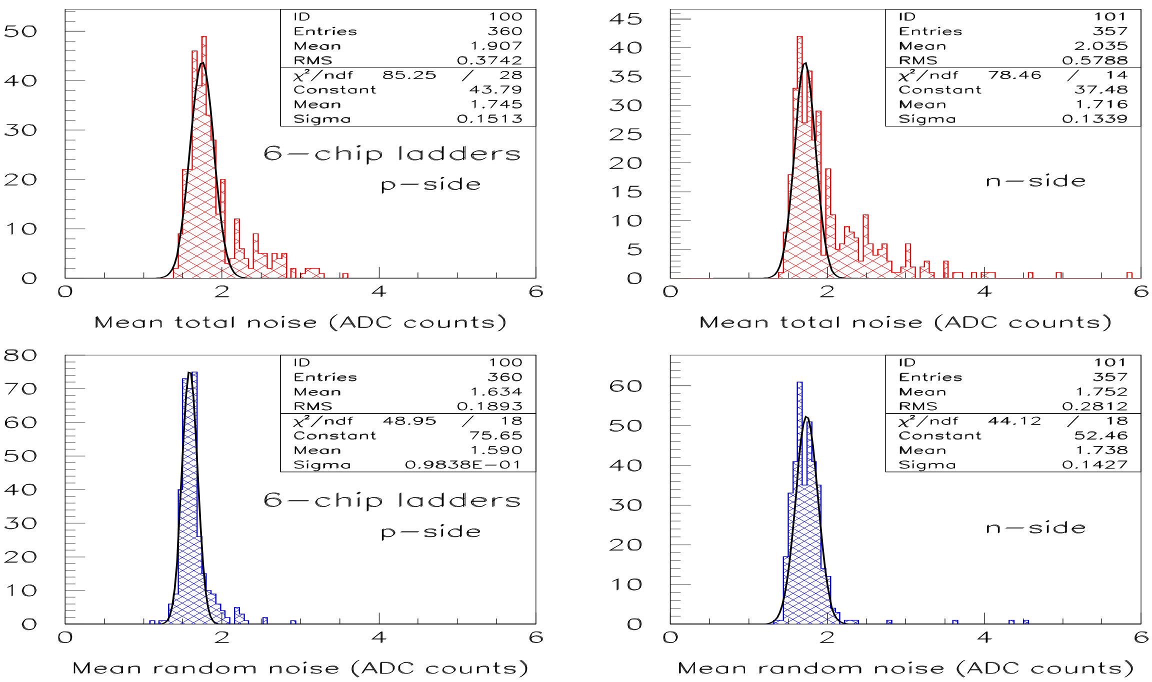

Figure 24: Distributions of mean total and random noise per chip for 6-chip ladders.

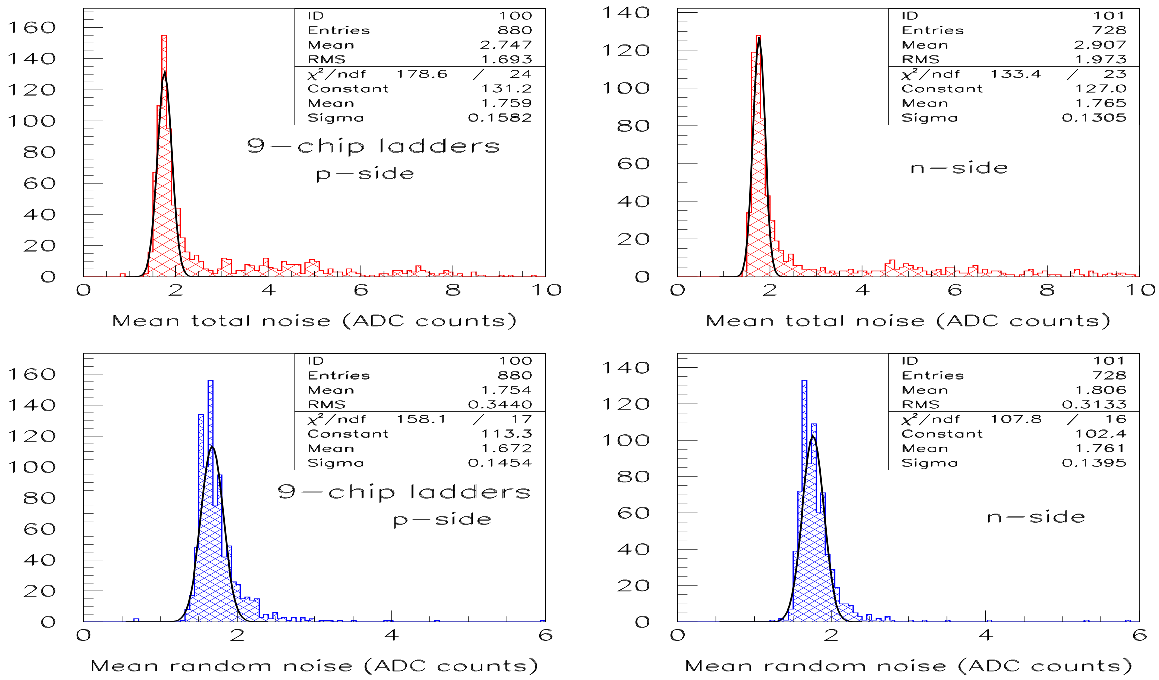

Figure 25: Distributions of mean total and random noise per chip for 9-chip ladders.

most of the ladders are well below the limit.

The distributions of the mean random noise for F- and H-wedges are plotted in Figs. 27 to 29. Mean random noise of the chip (blue histograms) goes down from 1.7-1.8 to 1.3-1.4 ADC counts as the wedge strips it reads out become shorter, approaching the values for HDIs (red histograms). Since all distributions presented in this section are based on the data from about 80% of all burned-in ladders and wedges without any pre-selection, the burn-in test results demonstrate the excellent noise performance of all types of SMT detectors and low expected inefficiencies due to dead channels. The performance of the detectors selected for the barrel and disk construction are even better, as can be seen in section 11.

In summary, the burn-in test proved to be an efficient and reliable tool to test the long term reliability of the detector modules before installation into the SMT. HDIs were selected for detector construction based entirely on the results of the burn-in test. Together with the laser test, the burn-in test allowed us to characterize the detector modules and select those devices that could be installed in the tracker. Over a thousand HDIs and detector modules were tested during the SMT production testing project. Taking into account the average load of 75%, this corresponds to approximately 6,000 hours of stable running by each of the two burn-in stations. The excellent performance of the burn-in stations, including the robustness of the system and low coherent noise, has been achieved owing to the thorough debugging and tuning of all elements of the test stand read out chain. The burn-in test is also being used in studies of irradiated detectors to gather important information about the detector degradation due to radiation damage. The existing burn-in test stands will undoubtedly be re-fitted to be used as production testing tools for the construction of the new silicon tracker.

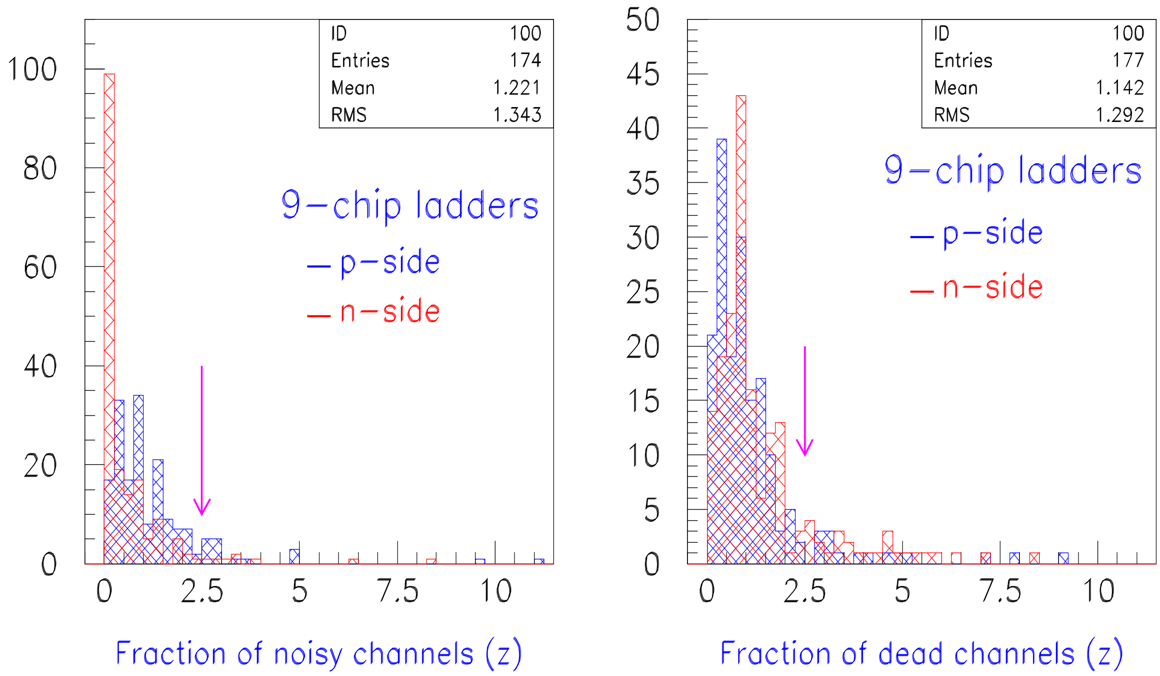

Figure 26: Distributions of the fraction of dead and noisy channels for 9-chip ladders.

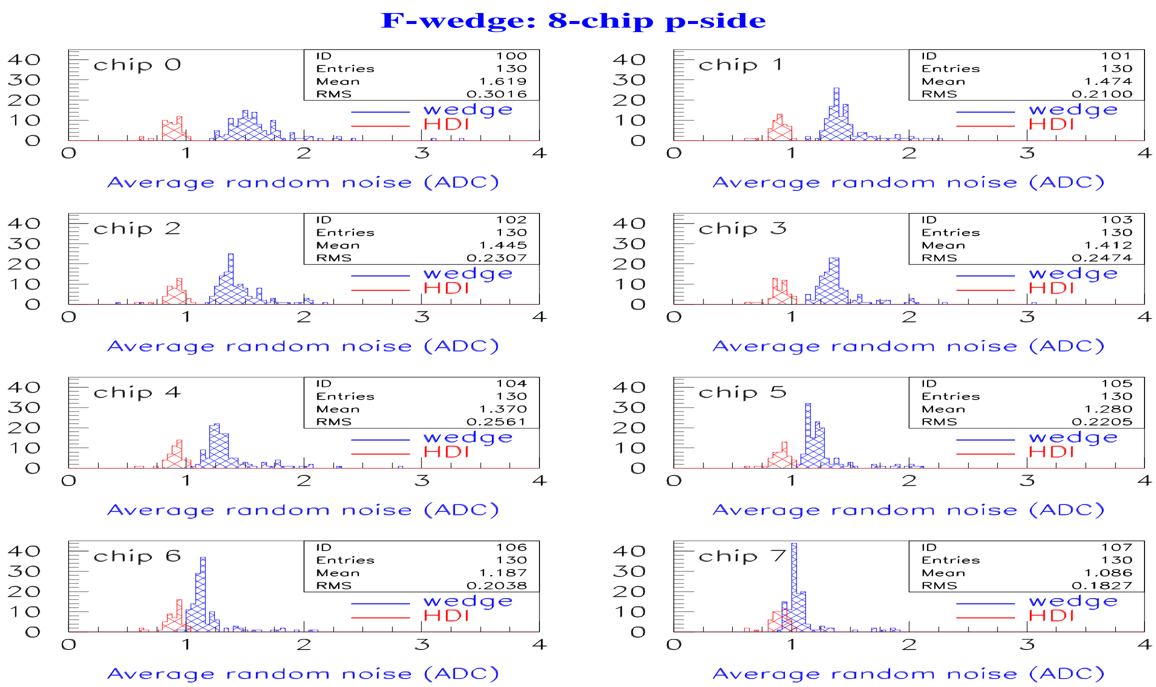

Figure 27: Mean random noise distributions for the p-side chips of F-wedges.

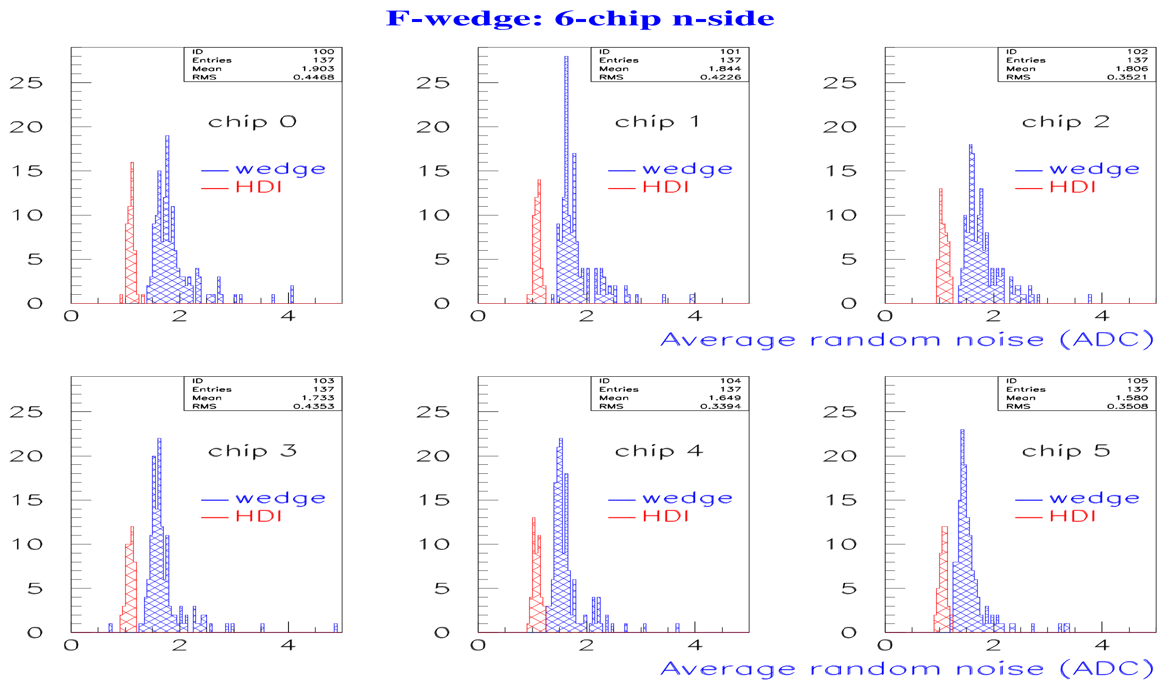

Figure 28: Mean random noise distributions for the n-side chips of F-wedges.

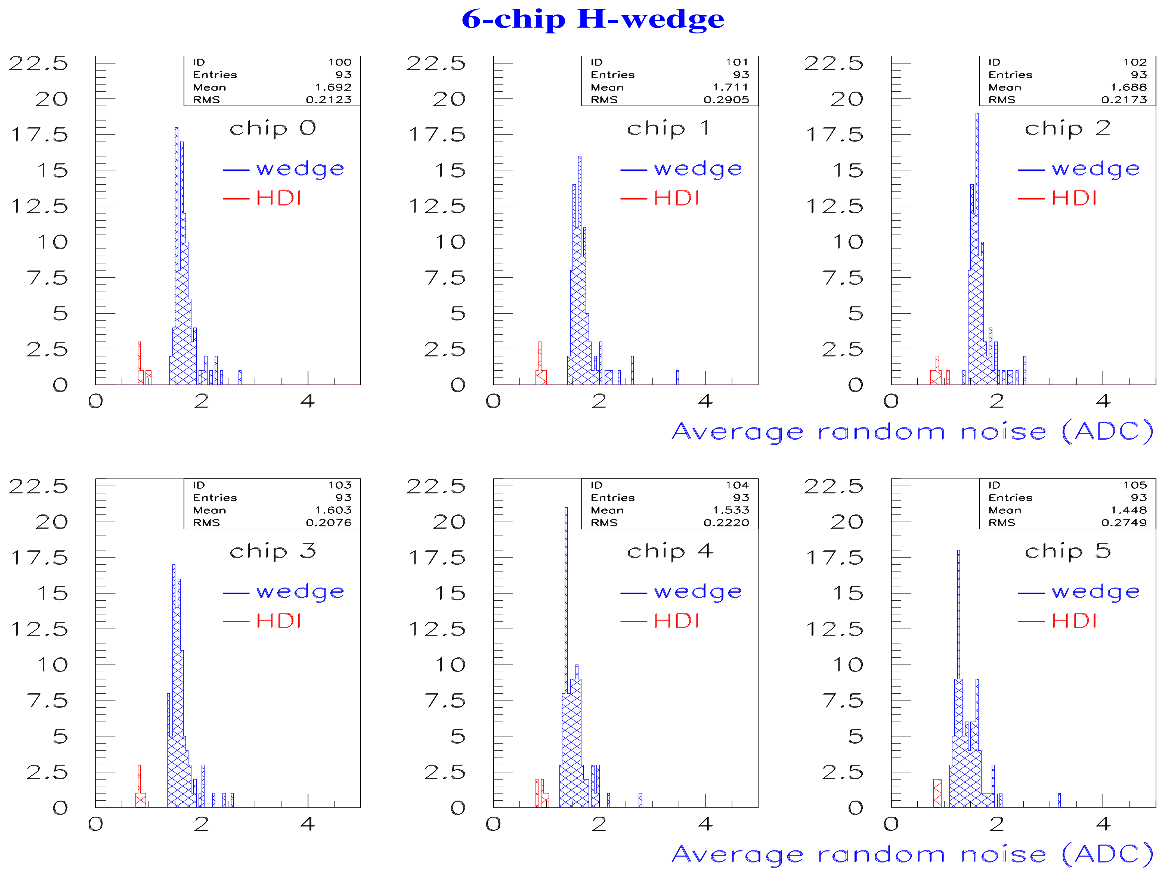

Figure 29: Mean random noise distributions for H-wedges.

9 Laser Test

One of the goals of the production testing effort was to characterize the individual ladders and wedges before installation in the SMT. Laser stations were found to be suitable tools in such investigations, allowing for an accurate, detailed and fast check of each and every strip and determining the operating voltage for each detector module. The laser test of the detector modules was the only test performed during production that allowed to check each strip's response to charge.

The idea behind the use of a laser to test the silicon detectors can be shortly described as follows: The solid state laser used operates at a wavelength of 1064 nm, a wavelength chosen because the high resistivity silicon used in the detectors is partially transparent to it. The attenuation as a function of silicon thickness had been measured, resulting in an attenuation length of 206 μm, and so this laser will test the whole depth of the 300 μm thick detector and not just a surface layer. When the light from the laser penetrates the silicon sensors, electrons and holes are produced. If the microstrip detector is biased, the electric field forces the charge carriers to move. The charge collected on each strip is read out and converted to ADC counts by the SVX chips.

Two test stands were used for the laser test. They required a relatively fast readout system, and an x-y moving table to shuttle the completed detector modules underneath the laser head. Completed modules were mounted onto a test structure on the x-y moving table, and the whole setup was kept in a dark and dry environment. The laser test performed two functions:

- The depletion voltage and operating bias voltage of the module were determined, measuring the amplitude of the signal as a function of increasing bias voltage. Simultaneously, the leakage current was measured as a function of bias voltage.
- Scanning the strips while monitoring the readout response allowed to check the operability of each channel. The result of this scan gave the information about the number of dead and noisy channels.

Further details of the laser test setup can be found in [9] and [10]. The simplified scheme of the laser test stand is shown in Fig. 30

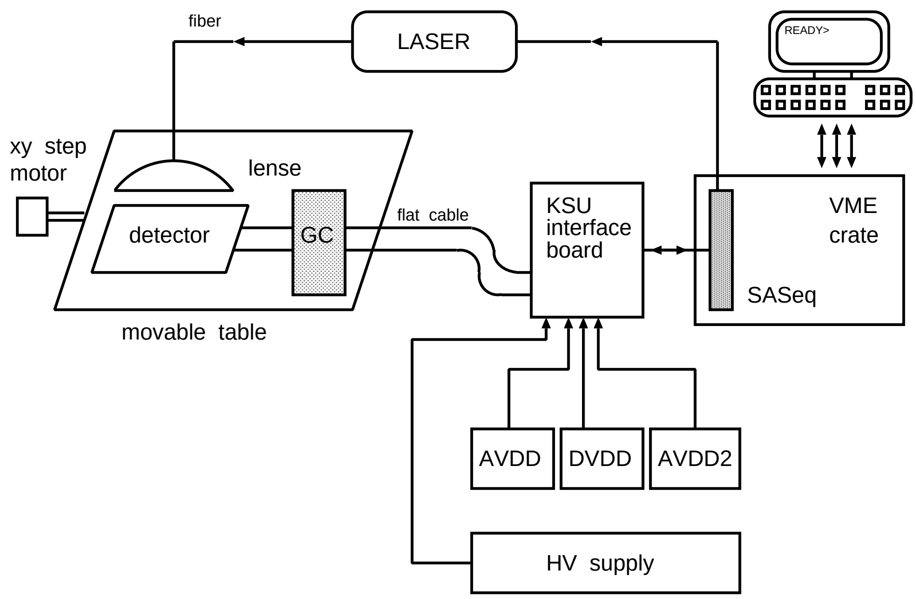

Figure 30: Simplified scheme of the laser test stand setup.

As already mentioned, the laser test stand set up was based on a stable infrared laser system. The laser pulse generator had a wavelength of 1064nm and was connected to an optical fiber. At the end of the fiber, the focusing lens was placed allowing to collimate the laser spot. The lens system was fixed, so the detector had to be moved under the light. The detector was placed on an aluminum plate attached to the movable table and its HDI tail was inserted into the Hirose connector on the adapter card, labeled "green card" (GC) in Fig. 30. The GC was connected to the KSU interface board through a flat cable. The KSU interface board provided the power to the chips and the high voltage to the detector. One source of high voltage HV and three low voltage power supplies AVDD, AVDD2 and DVDD needed for the SVX chip operation, were connected to the KSU interface board. The data passed from the KSU interface board through the StandAlone Sequencer (SASeq) to the computer. The SASeq was placed in the VME crate, and there was a connection between the VME crate and the computer by means of a BIT-3 VME controller card. After the chips had been successfully downloaded and the detector biased, the ladder was moved under the laser spot by the robot (xy step motor on the scheme) and further measurements were performed.

The dedicated software for the laser test was written by J.Rha, from the University of California at Riverside . It included two different packages running on PC under Windows NT. The first package named *Laser-Test* was written in Visual Basic. This package was the online program which allowed to manage all steps of the laser test in the dialog regime. It included a robot control for the speed and directions of movement of the movable table, a data acquisition system and a user interface to select the parameter settings and the display of the data. When initialized, the Laser-Test program opened a GUI with a set of menus. The first step was the initialization of the readout system and the downloading of the SVX chips. If all chips downloaded successfully, the system began to read them out immediately, at an average readout frequency of 15 Hz. The next step was the proper biasing of the detector. The same biasing scheme and voltages used during detector burn-in were used during this part of the laser test. The program was now ready to calibrate the position of the detector. At this step, the fine correspondence between strip number and global coordinates of the detector in the plane of the table was established by detecting the position of the laser spot. This was the final preparation step for the depletion voltage measurements and the laser scan of the channels. The Laser-Test package was extremely flexible. Non-expert shifters could use the program following the instructions, while advanced users had the possibility to make non-standard measurements of the silicon detector. In fact, the laser test was used for the characterization of irradiated detectors, to study noisy strips and to investigate irregular charge collection on some silicon ladders. The second package named *Laser-Anal* was used for the analysis of the data and for storing the results into the database. This interactive package consisted of a the set of scripts written in MicroSoft Excel. It was used to analyze the data collected with the first package.

Two important properties of the detector modules were obtained with the laser test: the operating voltage and the number of dead strips.

Determination of the depletion and operating voltage:

The depletion voltage is one of the most important electrical characteristics of the silicon microstrip detectors. If the detector is not fully depleted, the bulk material is divided into two zones: a depleted region and a non-depleted region. The non-depleted region has high concentrations of both n and p free carriers and has therefore a very high conductivity. When a charged particle passes through the non-depleted region, it produces electrons and holes in much smaller amounts compared to the concentration of the free carriers. The electrons and holes encounter a region with no electric field, they recombine or are transported by diffusion, resulting in a signal too small to be detected. The depleted region, on the contrary, has no free carriers, and the electron-hole pairs generated by the charged particles are well separated by the electric field. The holes in the depleted area drift towards the p-side and the electrons drift towards the n-side. The maximum signal can be obtained if the depth of the depletion zone is equal to the total thickness of the silicon detector. In the case of the double-sided detectors, there is an additional problem introduced by a non-depleted region: due to its high conductivity, all the strips on the non-depleted side are effectively connected to each other, spreading any charge that may be collected over all strips and loosing the signal. It is therefore of uttermost importance to determine the depletion voltage of each device correctly.

The depletion voltage was measured by monitoring the charge collected on the readout strips that detected the laser as function of the bias voltage. The procedure for the single-sided detectors was the following: First, the range of the voltage variation was set from 0 V to V_{test}. [5] Then, the high voltage was increased automatically in steps of 5V, and after each step the amplitude of the laser signal in ADC counts was measured. The leakage current of the detector at each voltage setting was also recorded. The typical

[5] V_{test} was defined as $V_{TS} + 20$V or 90V, whichever is lower.

dependence of the number of ADC counts and the leakage current with the bias voltage is shown in Fig. 31 for a single-sided H-wedge. One can see that the amplitude A of the signal increases almost linearly with the high voltage V up to a value V_{min}, after which the $A(V)$ curve reaches plateau. As a first approximation, the $A(V)$ curve can be described by a slope and a plateau that fit the data linearly in the ranges $0 \div V_{depl}$ and $V_{op} \div V_{test}$, respectively. The depletion voltage was defined as the voltage corresponding to the point where the two linear fits intersect. This method for determining the depletion voltage V_{depl} was in good agreement with the results obtained with the C–V method of the depletion voltage measurements used on silicon sensors. The minimal operating voltage was defined as the voltage at the beginning of the plateau. The operating voltage V_{oper} of the detector was obtained by adding 5V to the minimal operating voltage.

The procedure was very similar for double-sided detectors. The p-side of the double-sided detector was biased with negative voltage at the predetermined value of V^{-}_{max} while the positive bias applied to the n-side was increased in 5V steps between 0 and $V_{test} - V^{-}_{max}$. Typical results of the measurement of the depletion voltage and leakage current measured on the double-sided detectors are shown in Fig. 32

Three of the SMT detector types, the 3-chip ladders, the 9-chip ladders and the H-wedges, consist of two silicon sensors that have their strips wire-bonded by pairs to each other. Let us define the sensor on which the HDI is mounted as the active sensor, and the other as the passive sensor. Two different pieces of silicon could have different electrical characteristics, so it was necessary to measure the depletion voltage on both silicon sensors independently. To do so, the depletion voltage was measured with the laser shining on the active sensor at a position labeled Point 1 in Fig. 33, and then the measurement was repeated after the robot moved the detector until the laser shined on the same readout strip on the passive sensor, position labeled Point 2 in Fig. 33. Because sensors were paired into detectors based on their depletion voltage, these two measurements were always very close. The higher of the two operating voltages was taken as the detector operating voltage. All measurements were copied to the Laser-Anal program data buffer and saved to the database.

Determination of dead channels:

The second task of the laser scan was to find all dead and noisy channels in a detector module. The information about the number of dead and noisy channels of a detector module was the most important detector characteristic considered during module grading. The number of channels that did not respond to charge was an important consideration for the ultimate performance of the SMT.

The laser scan was performed with the detectors biased at V_{oper}, as determined from the laser test. For DS detectors, the negative bias voltage was set to V^{-}_{max} and the positive bias voltage was set to $V_{oper} - V^{-}_{max}$. Before performing the laser scan, the amplitude of the readout signal was adjusted to be between 90 and 120 ADC counts for most of the channels. Every channel i was read out 10 times [6], resulting in the set of raw amplitudes A^j_i, where $j = 1, ..., 10$. The average amplitude $\langle A_i \rangle$ and the standard deviation σ were calculated over 10 measurements. One channel was counted as *dead* if its average amplitude $\langle A_i \rangle$ was less than 40 ADC counts. The standard deviation of the amplitude for good channels did not depend on the channel number and was about 2 ADC counts. All channels with $\sigma > 8$ ADC counts were counted as *noisy*. Note that the threshold of 8 ADC counts corresponds to four times the average noise in the laser test, and that the final determination of dead channels is based on the burn-in test results, as explained in section 11. For detector modules built of two silicon sensors, the laser scan was repeated on each sensor independently. The reason for this practice was that some silicon-to-silicon wire bonds might be missing causing the corresponding strips on the passive silicon sensor contribute to the dead channel count. In Fig. 33(right), the scheme of the laser scan of the two silicon sensors is shown. The first scan is performed between the edge of the detector and chips across the strips on the active silicon sensor. In order to check the strips wire-bonded to the active sensor strips, the detectors was moved to position B, and the scan repeated. As expected, the total number of dead channels on the passive sensor was never less than the one on the active sensor.

In Fig. 34 the average amplitude (blue circles) and standard deviation (red squares) are shown as functions of the channel number. The data correspond to a laser scan of a 3-chip single-sided detector. In the ideal case, the amplitude is flat over all channels. Channel 0 on each chip appears low, which is a feature of the

[6] This number was one of the parameters in the Laser-Anal package. Studies indicated that a larger number of events was not needed and would prolong the test unnecessarily.

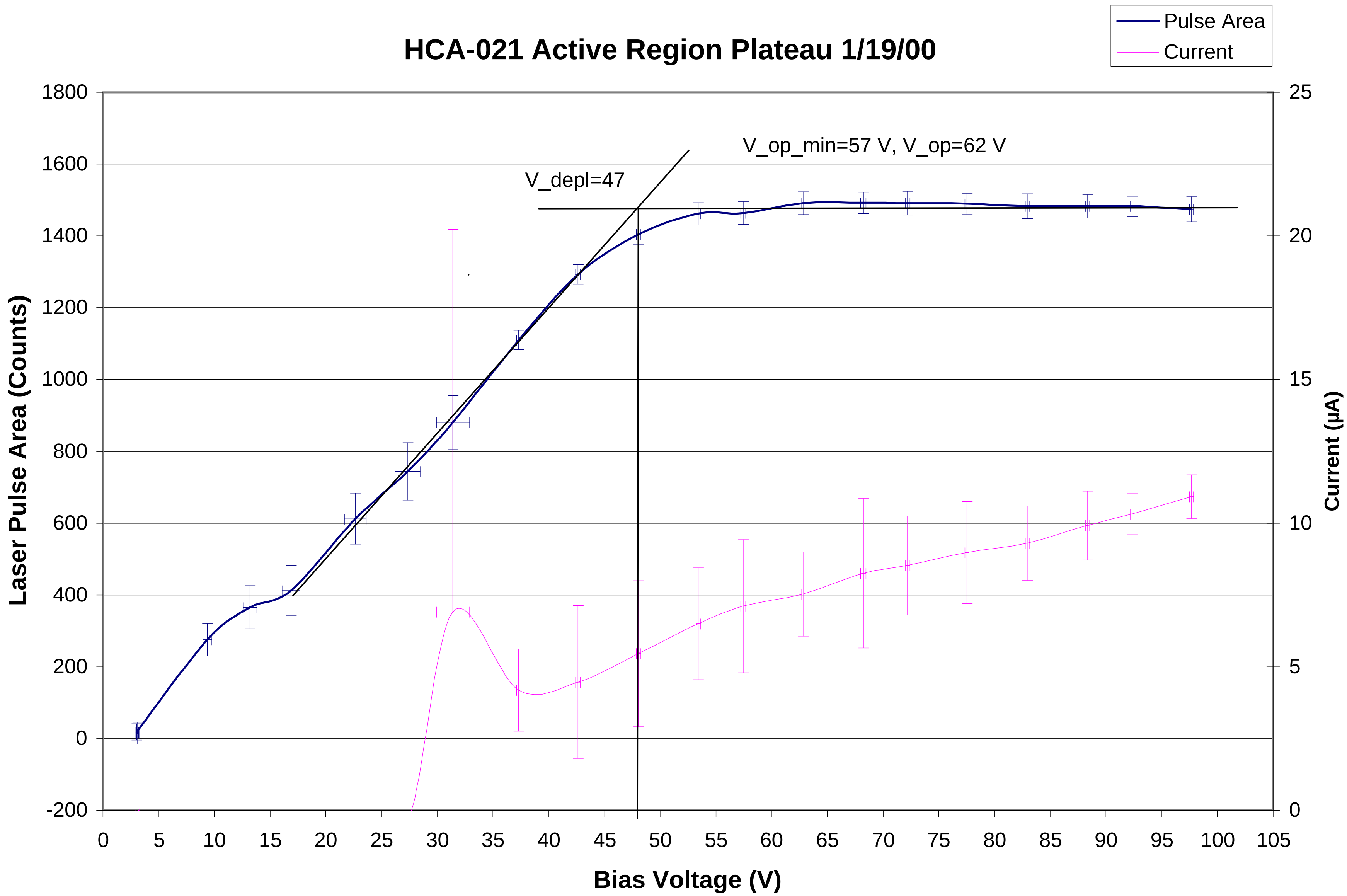

Figure 31: Amplitude and leakage current as functions of bias voltage measured on an H-wedge.

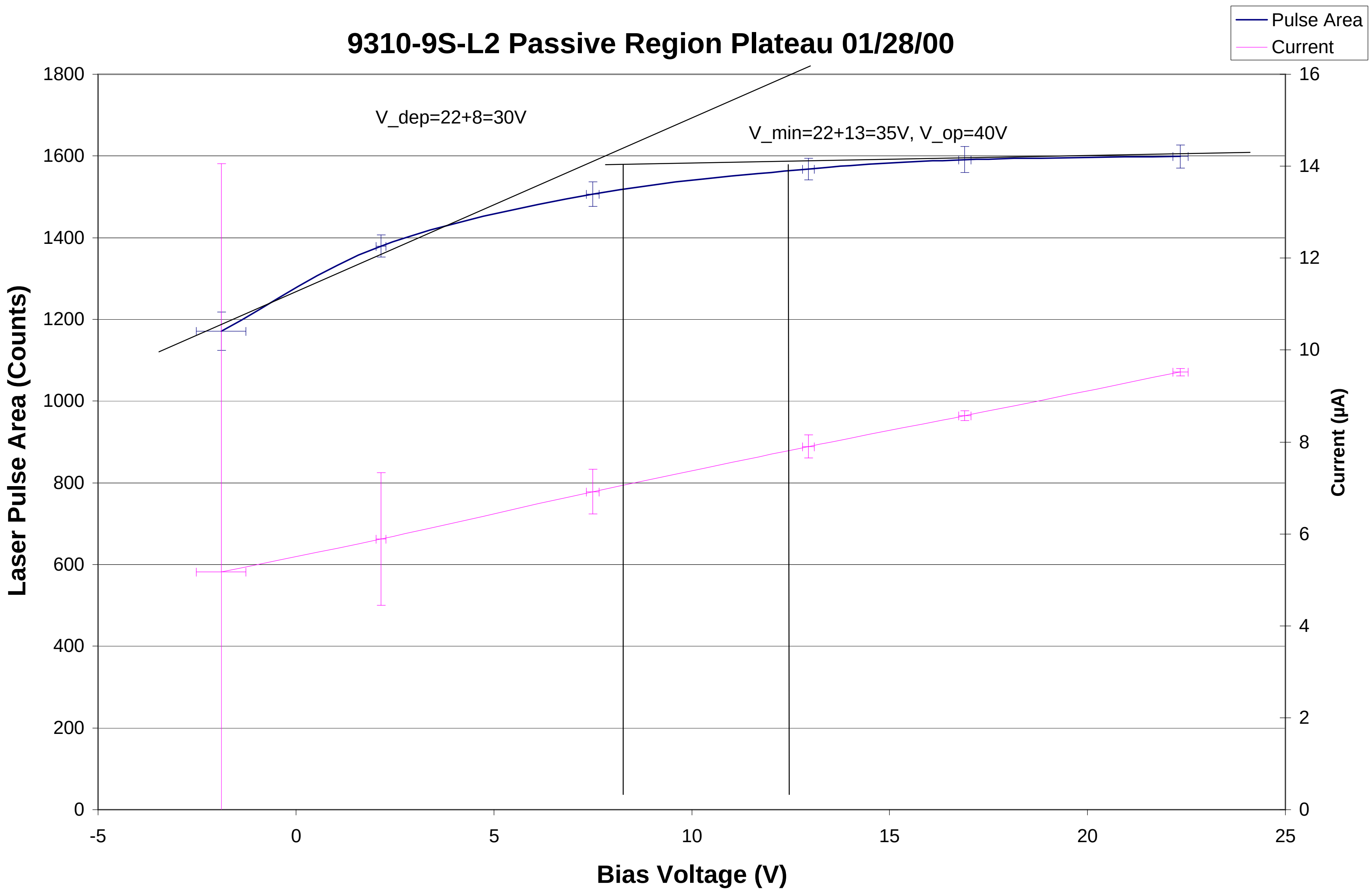

Figure 32: Amplitude and leakage current as functions of bias voltage measured on a 9-chip double-sided detector.

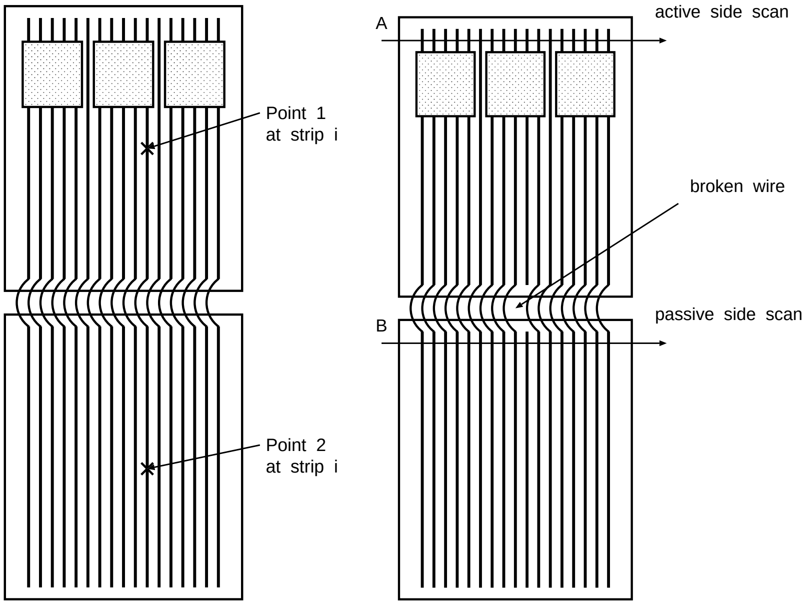

Figure 33: Schematic of a 3-Chip ladder undergoing laser test.

SVX chip, and was observed even on HDIs that were not connected to a silicon sensor. The Laser-Anal package read the data and produced a list of dead and noisy channels which was stored in the database. All of the DØ SMT silicon detectors modules were laser tested during 1999-2000. The laser test stations played a crucial role in the determination of the detector characteristics during production testing. In addition, the laser test became a useful tool in the diagnostics of some detector problems, and in studies of irradiated detectors. We plan to continue using the laser setup for additional detector performance studies after irradiation of Run 2a DØ detectors, as well as in Run 2b R&D.

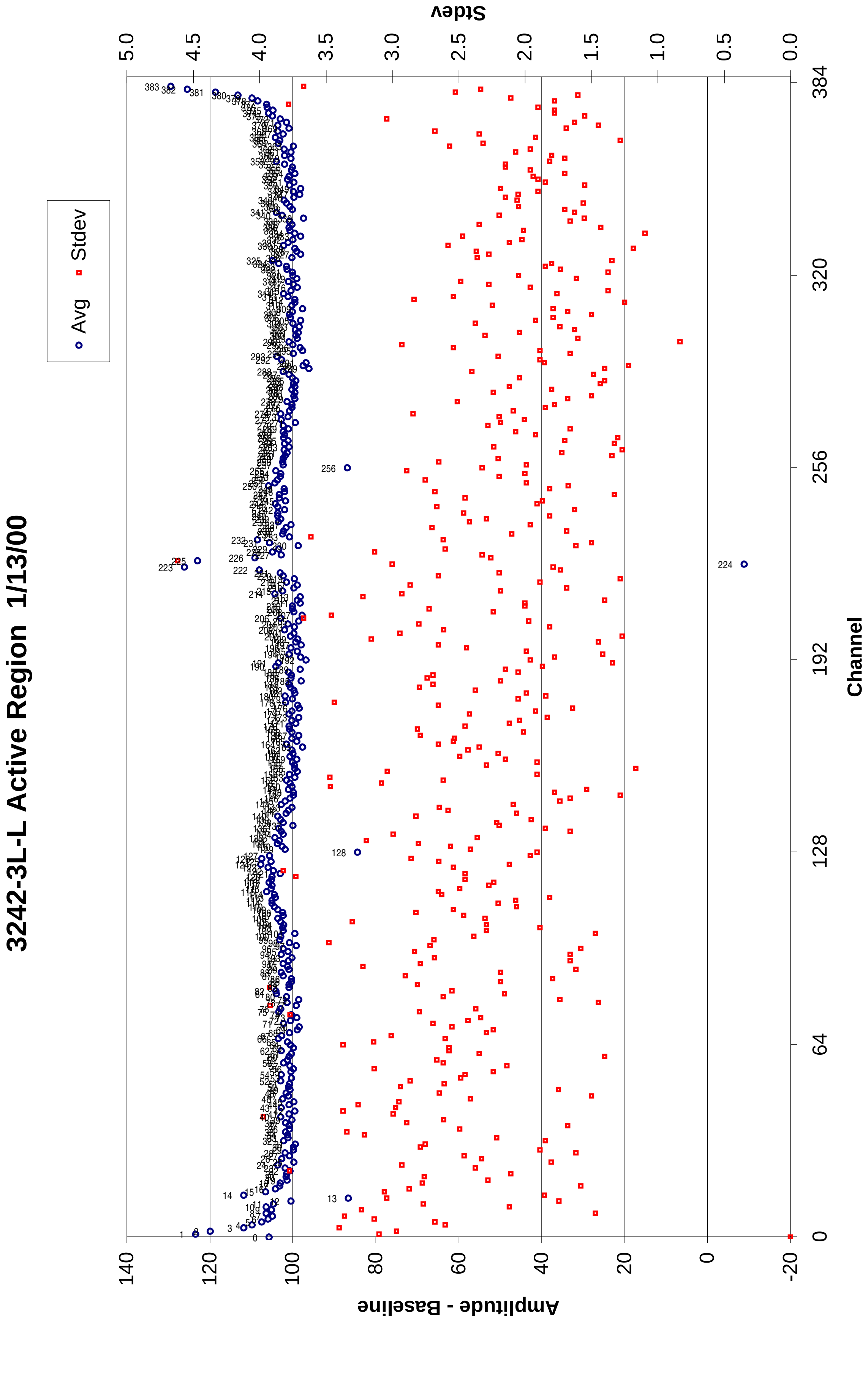

Figure 34: Average amplitude (blue circles) and standard deviation (red squares) are shown as functions of the channel number.

10 Diagnosis and repair of defective modules

HDI and detector modules with download problems or some kind of readout problems had to be diagnosed and repaired. Two test stations had special equipment to be able to do the diagnose. More than 300 HDI's and detectors were diagnosed and most of them were also repaired. Some of the repairs were done at the test stations, however, most of them were done by trained technicians. The HDI's with problems had these already when they arrived to Fermilab from the commercial companies after stuffing. For the detectors the error could occur at any time in the production and testing process: during debugging, burn-in or laser test, or they could be damaged when during installation on the rings or in the barrels.

The stations used for this effort were the basic PC based test stations with the addition of microscopes and probes which made it possible to probe the pads on the SVX chips. There was also an oscilloscope at each station and a logical analyzer. On the interface "green" card the lines Priority-Out and Priority-In were disconnected and the signal was sent either through an extra wire on the "green" card to the SVX chips or via the probe. This made it possible to download the chips one by one. This turned out to be a very effective tool to find bad chips on a device that was showing download errors.

The procedure to diagnose modules with problems was the following: all the HDI's and detectors with some kind of problems were first visually inspected and broken or shorted bonds were looked for and if any faults were found they were repaired. On HDI's that had never worked properly, it was also checked that all capacitors and resistors were mounted properly. When the HDI tail had been plugged into the Hirose connector it was checked that there were no shorts between the three voltage power supplies and ground. Many of these shorts where found in the tail of the HDI and these shorts normally disappeared after sanding the tail with sandpaper. Shorts between ground and other channels also often occurred at the end of the tail. Shorts on SVX chips were found by pulling the relevant bonds on the chip. When the chip was isolated one could measure the resistance by probing the ground and the shorted channel on the isolated chip. If a short was found on a chip, the chip was replaced.

If the power supplies were not shorted one tried to download the chips. However, a very common error was that there were download errors on one or several chips. To find the error one checked with the logic analyzer if the time lines were correct. Non correct time lines could, for example, show that a line was broken. Broken traces on the HDI could in most cases be repaired by adding an extra wire. This kind of problem was very common on the H-wedges for which the traces often got broken close to the Hirose connector that was mounted on the HDI tail. To further investigate which chip had download errors the chips were downloaded one by one. In this case the chips were isolated by pulling the priority-in and the priority-out bonds. When the chip with the download errors was found it was checked once more for bad bonds and if none was found the chip was replaced.

If the chips were downloading but one or several chips had any kind of readout problems the chip was checked with the logical analyzer to see if all the time lines were correct. If one line was bad the bonds were checked again and often replaced. If the problem persisted after that, the chip was in most cases replaced. When a chip had no gain it could be because a resistor was missing. If the correct resistors were in place, the chip was replaced.

Other kinds of errors were for example shorts on the tail because there was some solder on it. After cleaning, the short was gone. Shorts could also occur because the solder under a resistor got in contact with another pad or a broken trace. Several H-wedge HDIs developed shorts between D0 and ground. These shorts occurred on several chips, sometimes more than three on the same HDI. It turned out that it was caused by sparks from a capacitor between the bias voltage line and ground to the D0 trace. A number of HDI's had no AVDD2 current. This was caused by shorts between AVDD and AVDD2 which in all cases were found on one of the chips.

When detectors stopped working after the bonds had been encapsulated the error could be caused by damaged bonds and the detector often worked again after removing the encapsulant and rebonding the chips. It could also be caused by a scratch on a chip and after removing the encapsulant the chip had to be replaced. It also happened that chips were damaged when the encapsulant was removed.

Several times when a chip was, replaced another chip was damaged in the process. This could lead to several chips having to be replaced even if just one had problems initially. This was especially common for the F-wedges. To give an idea of what could happen to one detector one example is described here:

FW-218 had been working and the bonds were encapsulated. However, after encapsulation there were readout problems on the 6 chip side. The encapsulant was removed and after that there was a short between DVDD and ground. The short was found on one chip which was replaced. After replacement the short was gone but the replaced chip only read out half the chip and it was replaced again. After that the readout worked for that chip. However, the chip next to the replaced chip had been damaged, would not readout, and had to be replaced. Before the 6-chip side worked, another chip had to be exchanged. The 8-chip side of the wedge had stopped downloading and the encapsulant had to be removed. In this case some bond must have been damaged since after the removal and rebonding the detector finally worked. Errors that were impossible to repair were shorts between AVDD and ground which were caused by holes in the HDI between AVDD and ground. These holes could have been made when removing the chips from the HDI. In some cases the sensor was scratched and the detector could not be repaired. For some HDI's the bonds did not stick and the HDI had to be scrapped.

In total 339 devices (181 HDI's and 158 detectors) were documented by the repair group. Many detectors came back several times as can be understood from the previous example. Out of this 74 only had minor problems, like bad grounding or missing or damaged bonds that were solved by rebonding. The number of devices which were fully recovered were 264, including the ones with simple errors. There were 38 detectors which could not be repaired and another 37 which were not fully repaired since there was a lack of SVX chips and the HDI and detectors were not needed. A total of 288 SVX chips were replaced, out of them 145 were replaced because they had readout problems, 83 did not download and 60 had a short on the chip. A total of 14 missing components were found on the HDI's. Problems with the tail or the traces on the HDI's occurred for 51 devices and other kind of problems for 31 of the devices.

The type of devices with most problems were F-wedges and 9-chip ladders:113 and 114 respectively. 73 H-wedges, 32 6-chip ladders, and 7 3-chip ladders were sent to the repair group. F-wedges often took a long time to repair since they many times were damaged during repairing. H-wedges were also difficult to diagnose since they often had many broken traces close to the connector on the tail.

The effort of the repair group was essential to complete the SMT. We did not have enough spares to replace broken detector modules or non-functioning HDIs, so we would have run out of parts if defective HDIs and detectors would not have been successfully fixed.

11 Electrical Grading and characteristics of Detector Modules

During real data taking in a collider run, the detectors will be read out in sparse mode, meaning that only strips with charge above a certain threshold, and its two neighbors, will be read out. The reason for this practice is the prohibitive amount of time it would take to read out all the (mostly empty) channels. The maximum amount of SMT channels that can be read out in the allotted time is about 3 to 5%. Charge produced by minimum ionizing particles is distributed over a few strips that form a cluster. The number of strips in the cluster determines the precision of finding the coordinates of the particle traversing the silicon detector. This precision translates into impact parameter and transverse momentum resolution. One additional consideration is that for tracks intersecting a detector module at a small angle, the total charge will be shared by many strips, possibly resulting in a loss of hits. One would therefore like to set the threshold as low as possible to see all the signal. Unfortunately, at a very low sparsification threshold, the occupancy due to noisy channels increases. An optimal value of the sparsification threshold needs to be chosen, to effectively suppress the noise, keeping as much signal as possible.

Fig. 35 shows the probability to read out a strip as a function of the sparsification threshold for various fractions of a 1 MIP charge. The sparsification threshold will be set to 4 ADC counts at the start of Run2. This would lead to an inefficiency of about 2% for a hit on a strip that collects a charge of 1/3 of one MIP. Fig. 35 also shows the probability to have a fake hit due to noise as a function of the signal amplitude. The green line corresponds to strips with a typical Gaussian noise of $\sigma = 2$ ADC counts. The probability to have a signal above 4 ADC counts for those strips is negligibly small. The red line shows the probability to have a signal from noisy strips with Gaussian noise of $\sigma = 6$ ADC counts. The probability to have a fake hit from a noisy strip increases to about 18%.

After the detectors suffer from radiation damage, the leakage current will increase significantly. This will lead to large charge collection fluctuations and effectively increases the width of the amplitude distribution. Once this happens, all channels in the detector will look like noisy channels, and the sparsification

threshold will need to be increased. Eventually, the signal-to-noise ratio will deteriorate beyond the point of having a usable detector.
The results collected for each detector module during detector burn-in and laser test were used to assign an electrical grade to each detector module. We defined two types of "exceptional" channels:

- A channel was called **DEAD** if its response to the laser in the laser test was less than 40 counts (the average response was 100 counts). For detectors with two sensors the sensor with the larger count of dead channels was considered in the electrical grading.
- A channel was called **NOISY** if its random noise in data mode during burn-in was larger than 6 counts (average noise was 1.5 counts)

A detector was assigned an "A" grade, if the sum of the number of dead and noisy channels was less than 2.6% of the total number of channels. This corresponds to 10 channels for a 3-chip ladder, 20 channels for a 6-chip ladder, etc. No distinction between n-side and p-side bad channels was made in the grading. A detector was assigned a "B" grade, if the sum of the number of dead and noisy channels was more than 2.6% but less than 5.2%. Detectors with more than 5.2% of bad channels were graded as "C". In addition, we required that the leakage current be less than 10μA at operating voltage and that the burn-in results were stable over time. Mostly "A" grade detectors were installed in the SMT. No "C" grade detectors were installed in the tracker.
In Fig. 36, the distributions of dead and noisy channels, as well as of operating voltage and leakage current are shown for all 3-chip ladders installed in the SMT. These kind of ladders are installed on layers 1 and 3 in the two outer barrels, 1 and 6. One can see that the expected inefficiency of the 3-chip ladders due to dead strips is small, about 1.1% on average. The fraction of noisy channels is approximately four times less that of dead channels ($\sim 0.24\%$), resulting in a very low rate of fake hits in these detectors. The distribution of the operating voltage is centered at 47V with a sigma of 6V. Because every 4 detectors share the same power supply for bias voltage, the uniformity in the operating voltage ensures that the detectors with lower operating voltage will not be strongly over biased in the experiment. This is important from the point of view of the detector life after irradiation. Leakage current is well below the requirement of 10μA.
Fig. 37 shows the characteristics of 9-chip 2^o detectors. This type of ladders are installed in layers 2 and 4 of all six barrels. The distributions of dead and noisy channels are wider compared to single-sided detectors, but on average, the inefficiency due to dead channels is still small, about 1.7%. The fraction of noisy channels is about 0.37% on average. The distributions for 6-chip ladders are similar to the ones presented for the 9-chip ladders. 6-chip ladders are installed in layers 1 and 3 in the four central barrels, 2–5.
Another interesting question is how dead channels are distributed throughout the SMT. Groups of dead channels could form dead areas in the tracker, leading to loss of information about particles in certain trajectories. For those 6-chip detectors installed in the SMT, the distribution of number of dead strips in the different high voltage groups is shown in Fig 38. The high voltage groups roughly correspond to 2-ladder wide/2-sublayer deep ϕ segments in each barrel. Care was also taken during grouping to keep the overall quality of detector modules uniform throughout the tracker.
Analogous analysis performed for all other types of detectors shows that the distribution of the number of dead strips in the HV groups does not depend on detector type, and that the average number of dead strips in each group is 1.2–1.3.
The performance of F-wedges is shown in Fig. 39. The distribution for the operating voltage for F-wedges has a two-peak structure. The reason for this is that the sensors were produced by two different vendors, and had significantly different depletion voltages. Detectors with similar electrical characteristics were selected for every disk, so different F-disks will be operated at different bias voltages.
The performance of detector modules installed in barrels and F-disks is summarized in Table 6 and Table 7, respectively. It can be seen that the characteristics of the devices are very similar throughout the different barrels and disks, resulting in a uniform acceptance of hits produced by charged particles.

Barrel	Layer 1		Layer 2		Layer 3		Layer 4	
	dead,%	noisy,%	dead,%	noisy,%	dead,%	noisy,%	dead,%	noisy,%
1	0.85	0.4	1.99	0.8	0.93	0.4	1.77	0.6
2	0.95	0.56	2.13	0.43	1.34	0.22	2.01	0.44
3	0.70	0.30	1.4	0.4	0.77	0.12	1.27	0.3
4	0.56	0.18	2.1	0.5	0.84	0.06	1.50	0.2
5	0.77	0.51	1.65	0.27	1.22	0.32	1.54	0.2
6	1.1	0.07	2.7	0.4	1.48	0.12	1.85	0.16

Table 6: Fractions of dead and noisy channels in barrel detectors.

Disk	dead,%	noisy,%
1	0.92	0.23
2	1.0	0.21
3	1.75	0.05
4	1.0	0.32
5	1.65	0.05
6	1.02	0.25
7	1.25	0.33
8	1.4	0.13
9	1.22	0.45
10	1.32	0.15
11	1.15	0.45
12	1.25	0.35

Table 7: Fractions of dead and noisy channels in F-disks.

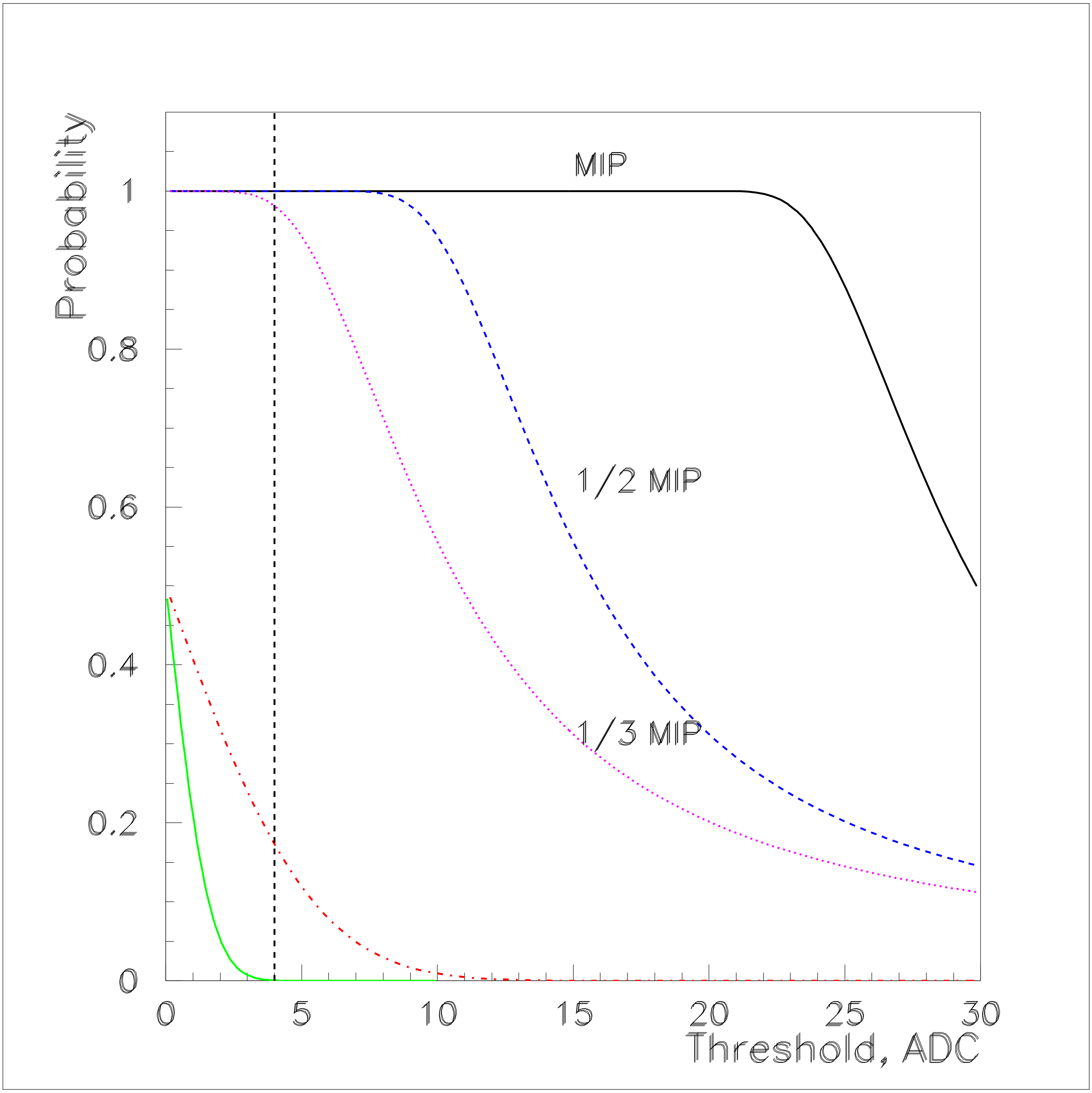

Figure 35: Probability to read out a strip as a function of the sparsification threshold for various fractions of a 1 MIP charge and due to noise.

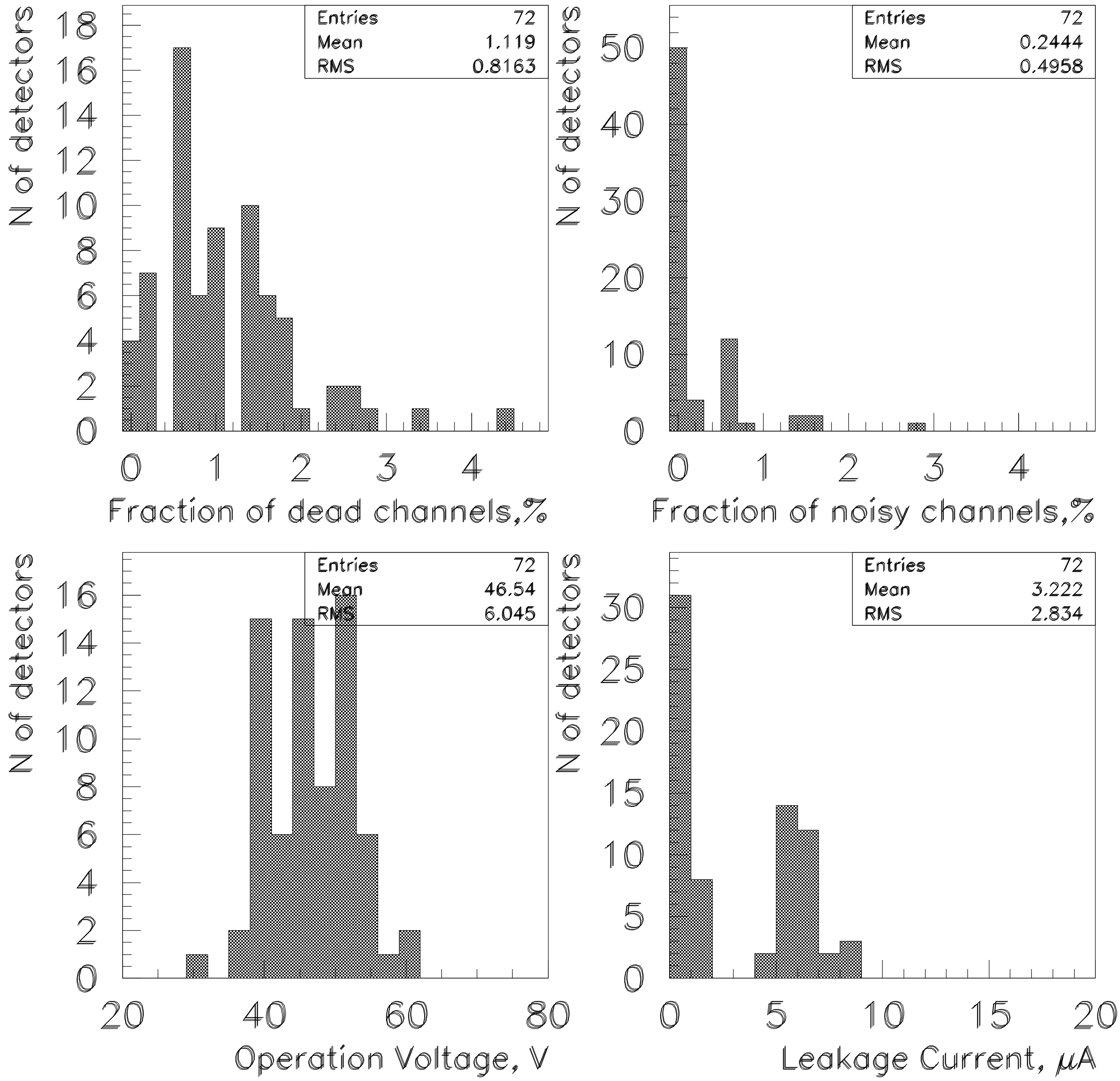

Figure 36: Characteristics of the 3-chip ladders installed in the SMT.

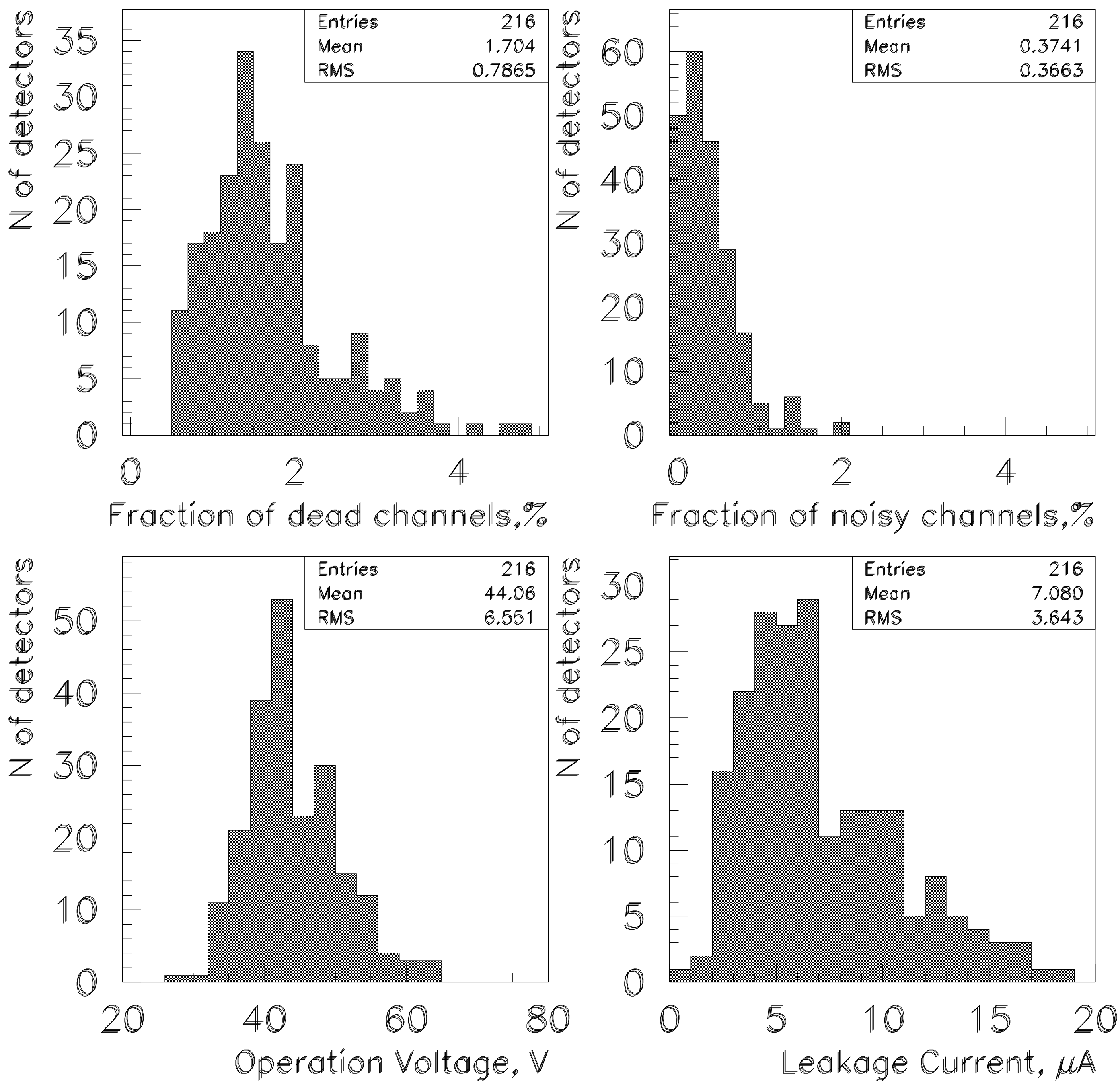

Figure 37: Characteristics of the 9-chip ladders installed in the SMT.

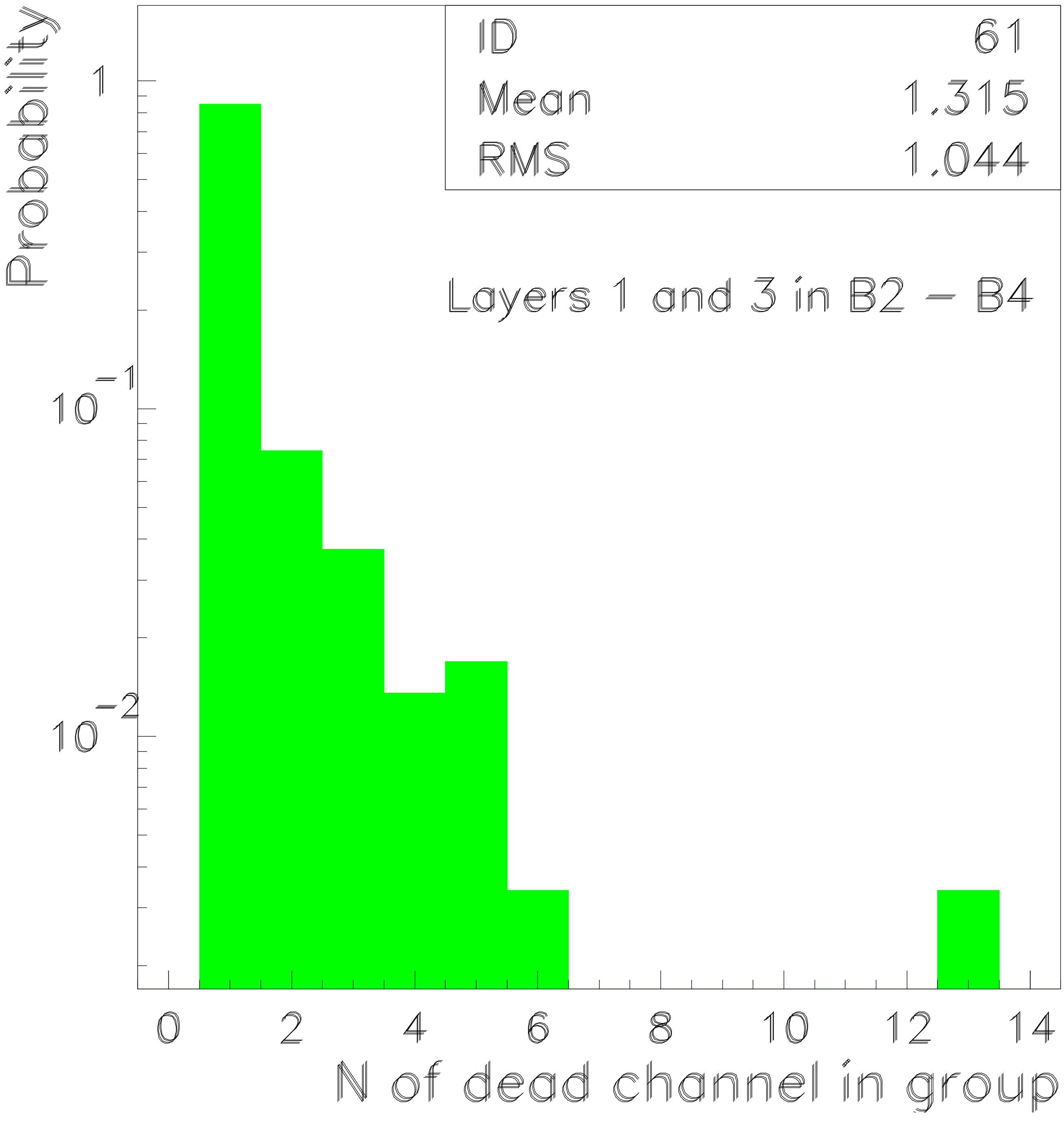

Figure 38: Dead areas on 6-chip ladders installed in the SMT. Each HV group consists of 4 ladders.

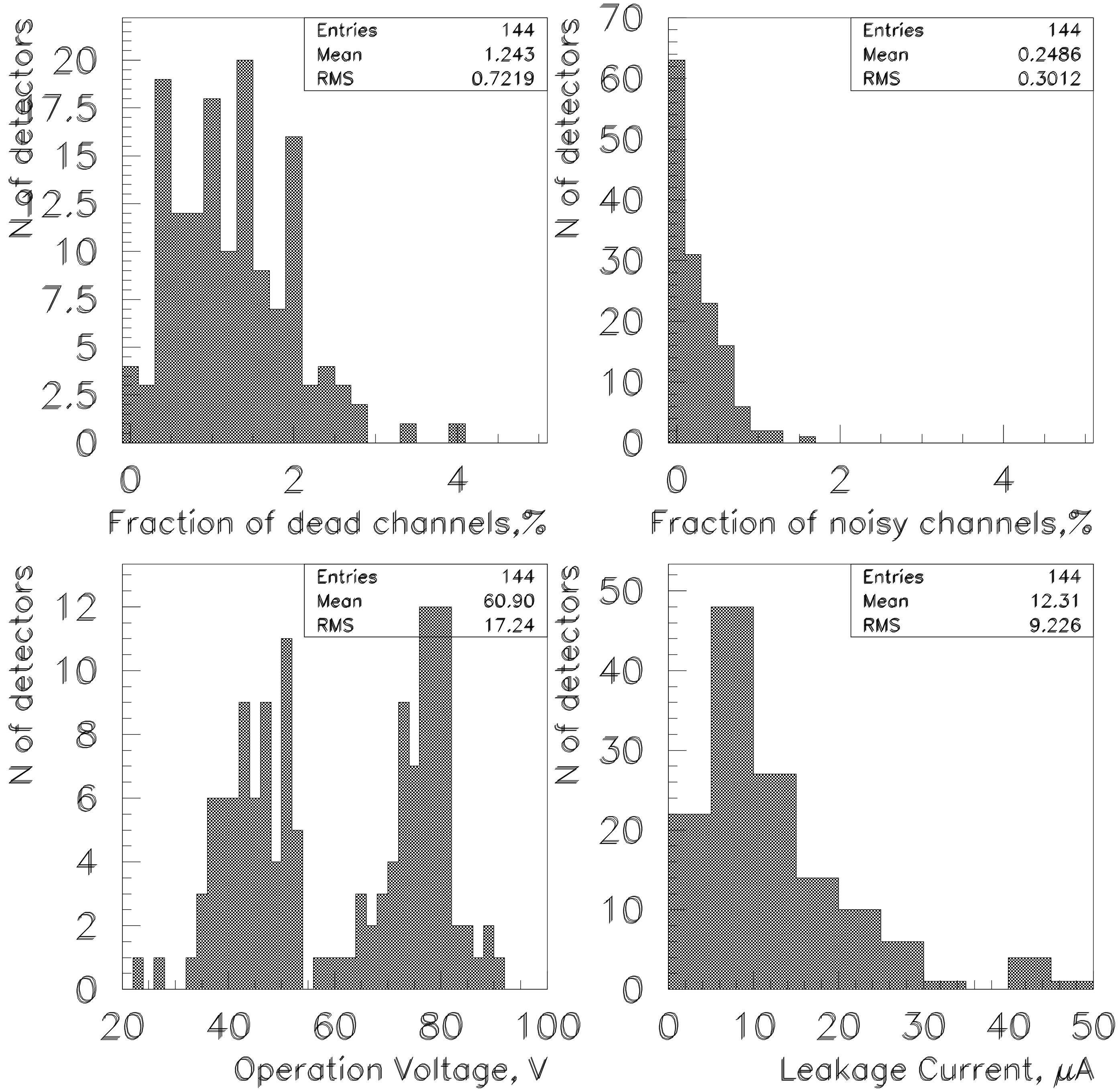

Figure 39: Characteristics of the F-wedges installed in the SMT.

12 Conclusions

The SMT production testing group was trusted with the very complex and multi-faced task of developing testing, debugging and repair procedures for 5 different type of silicon detector modules, each with its own characteristic problems and features. During approximately 18 months of production, close to 1000 silicon detector modules were fully debugged, tested and graded, as has been explained in this writeup. This corresponds to over one million readout channels that have been fully characterized. Considering that the readout hybrids were also fully characterized before gluing them onto silicon sensors, the number of channels that have been tested at least doubles. The magnitude of the testing effort required that a large number of dedicated physicists, engineers and technicians [7] collaborate in a well orchestrated way to keep up with the production. The addition of testing shifters was invaluable to the project. The DØ SMT is a crucial component of the upgraded DØ detector; it was completed in a timely manner and will allow DØ to achieve its physics goals during Run2a.

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[9] P.Rapidis et al, "Pulsed laser for testing silicon strip detectors", DØ Note 1681 (1993)

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[7] For the organization chart of the production testing effort see file://D0server4/projects/Silicon/www/Organization/organization.htm