A 200 $\times$ 200 CCD Image Sensor Fabricated On High-Resistivity Silicon

S.E. Holland, G. Goldhaber, D.E. Groom, W.W. Moses, C.R. Pennypacker, S. Perlmutter, N.W. Wang
Lawrence Berkeley National Laboratory
University of California, Berkeley, CA 94720

R.J. Stover, M. Wei
University of California Observatories/Lick Observatory
University of California, Santa Cruz, CA 95064

Abstract

A charge coupled device (CCD) image sensor fabricated on high-resistivity silicon is described. The resistivity, about 10,000 Ω-cm, allows for operation of the CCD with the entire 300 μm substrate depleted. This results in better red to near infrared response when compared to conventional and thinned CCDs. In addition the CCD has good blue response when back illuminated. Since the substrate is fully depleted, thinning, with its inherent difficulties, is not necessary in order to enhance blue response.

1. Introduction

Scientific imaging applications using charge-coupled devices often require photon detection with good quantum efficiency over a broad spectral range. CCDs that are illuminated at the front side of the device have poor quantum efficiency in the blue region of the visible light spectrum due to the strong absorption of short wavelength photons in the polycrystalline silicon gates. The blue response can be improved significantly by thinning the CCD substrate to a thickness of 15–25 μm and illuminating the back side [1].

While excellent results are achieved with thinned, back-illuminated CCDs, these devices have several drawbacks:

1. In many scientific applications, the incident light has strong components which are nearly monochromatic. For long-wavelength photons (in the red) the absorption depth becomes comparable to the thickness of the CCD and interference fringes are produced by multiply-reflected waves.
2. At even longer wavelengths the CCD becomes transparent. Typically the quantum efficiency for a thinned CCD falls off rapidly for $\lambda \geq 750$ nm.
3. The thinning process is difficult, expensive, and time consuming.

We have investigated an alternative approach to scientific CCD fabrication that does not require thinning. Based on work to develop fully-depleted p-i-n detectors for high-energy physics applications [2], we have fabricated p-channel CCDs on high-resistivity ($\geq$ 10 kΩ-cm) n-type substrates. The test devices consist of three-phase, 200×200 (15 μm)^2 pixel CCD arrays processed in a conventional triple-polysilicon MOS process except with high-resistivity starting material.

In contrast to previous deep-depletion CCDs with typically 50 μm deep potential wells [3–6] these devices can be operated with the entire 300 μm-thick substrate depleted [7]. As a result, the red fringing problem is eliminated and the response is extended about 200 nm into the near infrared region, which is of interest in astronomy and other fields. In addition, the CCD described here is expected to have good quantum efficiency for the direct detection of low-energy x-rays [3–7].

A fully-depleted CCD can potentially be back illuminated in order to enhance the response at short wavelengths. For this to be viable a suitable back-side contact must be developed and charge spreading due to diffusion must be minimized [8, 9]. The CCD described in this work is fully depleted, can be back illuminated, and is fabricated in a standard CCD process.

2. CCD Design

Although CCDs are almost universally fabricated on p-type silicon, we chose n-type material on the basis of our work with detectors for high-energy physics. One of the first steps in the fabrication process is the deposition of an in-situ doped (phosphorus) polysilicon layer on the back surface of the wafer for gettering purposes [2]. This technique reliably yields leakage currents on the order of 1 nA/cm^2 for p-i-n diodes with 300 μm-thick depletion regions, even for fully processed MOS devices [10]. In addition, the use of n-type material simplifies the problem of back-side illumination in that the potential well formed on p-type silicon due to the fixed oxide charge is eliminated. Unless accounted for by charging of the back surface [1], this potential well will result in a loss of quantum efficiency at short wavelengths due to recombination of charge carriers near the surface.

Regardless of the type of substrate chosen, in order to minimize noise it is necessary to include the source follower and reset transistors directly on chip. For buried channel CCD output transistors the source/drain regions can be offset from the gate in order to minimize overlap capacitance (and as a result maximize the CCD charge to voltage conversion gain) [3]. To minimize process complexity it is desirable that the reset and source follower transistors be fabricated directly in the high-resistivity silicon. This eliminates the extra steps and long, high-temperature drive-in associated with the fabrication of a p-type well. However, punchthrough is a concern due to the extremely small dopant level in the high-resistivity substrate.

Two-dimensional simulations were carried out in order to predict device behavior and guide the design. CCD cross sections were generated from a process simulator and input to a two-dimensional device simulator (TSUPREM4 and MEDICI, respectively [11]).

Buried-channel PMOSFETs with offset source and drain were simulated for various combinations of channel lengths and gate to source/drain spacings. Based on the simulation results a channel length of 6 μm was chosen for both source follower and reset transistors. Punchthrough characteristics were acceptable, with higher substrate voltages resulting in less punchthrough.

Figure 1 shows the simulated potential distribution for a three-phase 15 μm pixel. A channel implant of 1.5×10^{12} cm^{-2} was used. The substrate doping assumed was 6×10^{11} cm^{-3} (corresponding to a resistivity of ≈ 7000 Ω-cm). The 5 μm wide collecting electrode was held at -5 V and the barrier phases were at 5 V. The substrate bias voltage generates a drift field that extends to the back-side contact (the y dimension in Fig. 1).

Based on the simulation results a three phase, 200×200 full-frame CCD with 15 μm pixels was designed. The overall architecture was adapted from standard CCD designs provided by Lick Observatory. The overlap between polysilicon gates was 1.5 μm and the CCD was surrounded by a p^+ guard ring used to collect leakage currents generated outside the active volume of the CCD. Various test structures were included on the prototype chip, including transistor arrays with varying gate lengths and widths, and gate to source/drain offsets.

3. Fabrication Technology

The starting material was float-zone refined, high-resistivity n-type silicon. The crystalline orientation was $\langle 100 \rangle$. After processing to form the n^+ polysilicon gettering layer on the back side of the wafer, a 48 nm oxide was grown in dry O_2 at 900°C. A 50 nm layer of Si_3N_4 was deposited and the oxide/nitride stack formed both the CCD gate insulator and the masking layer for the LOCOS field oxidation. After etching of the nitride the channel-stop region was implanted with phosphorus, followed by field oxidation at 900°C in steam.

The CCD channel was then implanted with boron followed by deposition of undoped polysilicon. A high-dose boron implant was used for polysilicon doping followed by plasma etching of the polysilicon gates. In order to minimize gate nitride removal during polysilicon etching, particular attention was given to the overetch step. The polysilicon was etched in a Cl_2/He plasma. After optical endpoint detection a more selective etch with $Cl_2/HBr/O_2$ was used. This process yielded very good results, with typically only 25–50 Å of nitride removed at each etch step.

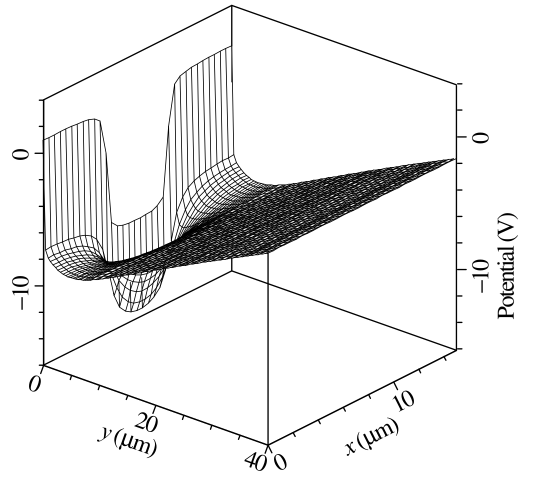

Figure 1: Simulated potential distribution for a 15 μm pixel. The substrate doping was 6×10^{11} cm^{-3} and the buried-channel implant dose was 1.5×10^{12} cm^{-2}.

The first polysilicon layer was then oxidized at 950°C in steam. Second and third polysilicon layers were processed similarly. After third layer polysilicon oxidation, a high-dose boron implant formed the sense node and source/drain regions of the transistors. A low-temperature (425°C) SiO_2 layer was deposited and the wafers were then annealed for 1 hour at 950°C in forming gas (4% H_2 in N_2). Contacts were etched, followed by deposition of aluminum containing 1% silicon. After metal masking and etching, the wafers were sintered in forming gas for 20 minutes at 400°C.

With the exception of ion implantation and plasma etching, all processing was performed in a class 10 clean room (Microsystems Laboratory of the Lawrence Berkeley National Laboratory). Ion implants were carried out at a commercial implant facility, and plasma etching was done at the University of California-Berkeley Microfabrication Laboratory.

4. Experimental Results

After fabrication, process monitor test structures were evaluated in order to determine the effectiveness of the polysilicon gettering. The leakage currents measured on fully depleted, 2 mm^2 p-i-n diodes were approximately 0.8 nA/cm^2, which is comparable to results achieved with the simple three mask detector process [2]. Hence the gettering process is compatible with the extended high temperature steps of a full CCD process. The depletion voltages extracted from C-V measurements were 15–20 V.

Figure 2 shows the measured subthreshold characteristics for the 47/6 buried channel output transistor at source to substrate biases of 12 and 20V. The gate to source/drain spacing was 1.5 μm . The effect of substrate bias on punch-

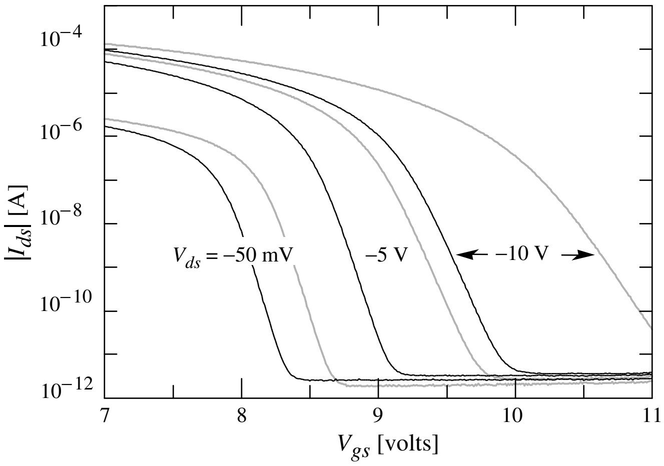

Figure 2: Subthreshold characteristics of a 47/6 buried channel PMOSFET with 1.5 μm gate to source/drain spacing. Data are shown for source to substrate biases of 12 and 20V (grey and black lines, respectively).

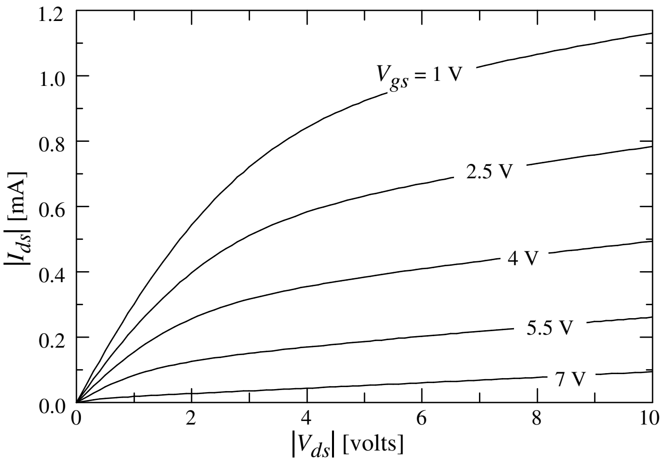

Figure 3: Output characteristics for a 47/6 buried channel PMOSFET with 1.5 μm gate to source/drain spacing. The substrate bias was 20V.

through is evident. At a 20V substrate bias the subthreshold slopes were 95 mV/dec and 144 mV/dec for drain to source voltages of -50 mV and -10 V, respectively. Although the device shows substantial variation of threshold voltage with drain bias, the output characteristics shown in Fig. 3 are acceptable. The measured source follower gain with a 20 kΩ load resistor was 0.7 at room temperature.

The initial application is for low-light imaging where the CCDs are operated cold. The CCDs were tested on a wafer probe station at Lick Observatory and good devices were then packaged for detailed characterization at low temperatures. The data acquisition system is described in [12] and contains a low-noise preamplifier and double-correlated sampling circuitry.

Packaged devices were cooled to approximately $-120°$C in a liquid nitrogen dewar [12]. CCDs were irradiated with a ^{55}Fe source, which emits characteristic x-rays that deposit a known amount of energy in silicon. From measurements of the output signal corresponding to absorption of an x-ray photon in a single pixel, the gain of the system (electrons to digital counts) was calibrated.

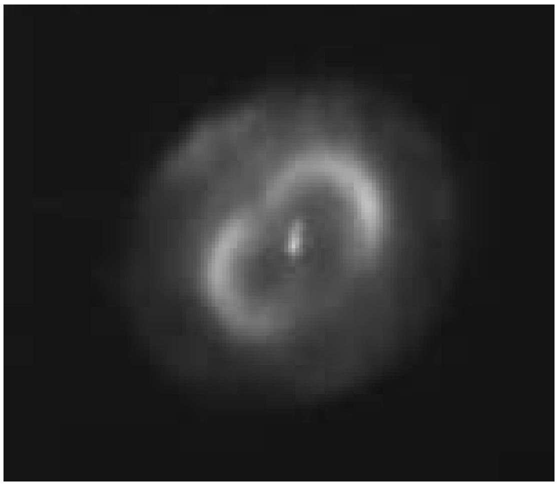

Figure 4: Planetary nebula NGC7662. The CCD was cooled to $\approx -120°$C and the exposure time was 100 seconds. The image was taken at the Lick Observatory 1-meter telescope.

The dark current was measured by integrating the current for 1000 seconds, and the result was 0.09 electrons per pixel per second. The rms noise, measured at an output data rate of 20 kHz, was approximately 6 electrons and the full-well capacity was 240,000 electrons (all at $-120°$C). Astronomical images were obtained at the Lick Observatory 1-m telescope with a front-illuminated CCD (Fig. 4).

The preceding results were for front-illuminated devices with the standard 1 μm polysilicon layer on the back of the device. However, 1 μm is prohibitively thick for back-side illumination at short wavelengths. For CCDs that are to be back illuminated, this thick layer is removed after the 950°C forming gas anneal and replaced with a thin layer of in-situ doped polysilicon. We have verified on simple p-i-n photodiode structures that this layer can be made as thin as 10 nm while still maintaining low leakage currents [13]. Figure 5 shows the measured quantum efficiency versus wavelength for back-illuminated photodiodes with varying polysilicon layer thicknesses. As expected the short wavelength response improves with decreasing polysilicon thickness. In addition, because of the relatively thick depletion region (300 μm) the response in the near infrared extends to a wavelength of approximately 1 μm .

CCDs were fabricated with a 20 nm back-side polysilicon layer. In addition, an antireflection coating of approximately 50 nm of indium tin oxide was sputter deposited over the polysilicon [13]. This layer is conducting and reduces the resistance of the back-side contact in addition to acting as an antireflection coating.

CCDs were mounted on specially designed aluminum nitride substrates that allowed for back-side illumination. Aluminum nitride was chosen for its excellent coefficient of thermal expansion match to silicon, in addition to its

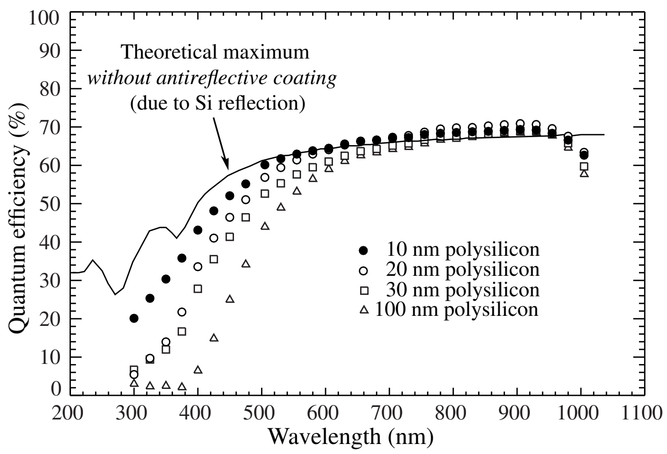

Figure 5: Quantum efficiency versus wavelength for varying poly thicknesses. The results are for 300 μm-thick p-i-n photodiodes.

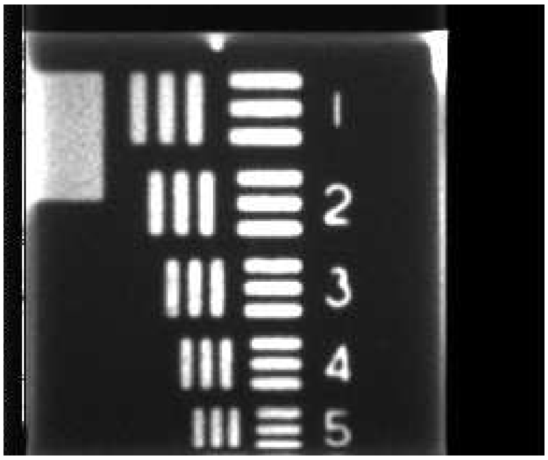

Figure 6: Back-illuminated image of a test pattern using 400 nm light.

high thermal conductivity. A standard package used at Lick Observatory was modified to accommodate the aluminum nitride substrates. Figure 6 shows a test pattern image taken with a back-illuminated CCD at $-120°$C. The substrate bias of 25 V resulted in overdepletion of the substrate. The wavelength of the incident light was 400 nm. The absorption depth in silicon at this wavelength is approximately 0.2 μm [1]. The photo-generated holes must therefore drift to the CCD potential wells located 300 μm away. Figure 6 demonstrates back-side imaging at short wavelengths for this fully-depleted technology. Preliminary measurements indicate that the quantum efficiency at 400 nm is approximately 67%. In addition, first measurements indicate that lateral charge diffusion at 25 V substrate bias is about one pixel width.

Conclusion

A CCD image sensor fabricated on high-resistivity silicon has been described. In contrast to conventional and thinned CCDs, the long wavelength response is improved and back-illumination imaging with short-wavelength light has been demonstrated.

Acknowledgments

This work was supported by the U.S. Department of Energy under contract No. DE-AC03-76SF00098.

References

[1] J. Janesick and T. Elliot, "History and advancement of large area array scientific CCD imagers," *in Astronomical CCD Observing and Reduction*, Astron. Soc. of Pacific Conf. **23**, BookCrafters, Inc. (1992).

[2] S. Holland, "Fabrication of detectors and transistors on high-resistivity silicon," Nuclear Instrum. Methods, **A275**, 537 (1989).

[3] B.E. Burke, R.W. Mountain, P.J. Daniels, M.J. Cooper, and V.S. Dolat, "CCD soft x-ray imaging spectrometer for the ASCA satellite," IEEE Trans. Nucl. Sci., **41**, 375 (1994).

[4] B.E. Burke, R.W. Mountain, D.C. Harrison, M.W. Bautz, J.P. Doty, G.R. Ricker, and P.J. Daniels, "An abuttable CCD imager for visible and x-ray focal plane arrays," IEEE Trans. on Electron Devices, **38**, 1069 (1991).

[5] S.R. Kamasz, M.G. Farrier, and C.R. Smith, "Characterization and modeling of CCD devices on high-resistivity silicon substrates," SPIE Proc., **2172**, 76 (1994).

[6] H.Y. Tsoi, J.P. Ellul, M.I. King, J.J. White, and W.C. Bradley, "A deep-depletion CCD imager for soft x-ray, visible, and near-infrared sensing," IEEE Trans. Electron Devices, **32**, 1525 (1985).

[7] L. Strüder et al, "The MPI-AIT x-ray imager (MAXI)-High speed pn CCDs for x-ray detection," Nuclear Instrum. Methods, **A288**, 227 (1990).

[8] M.W. Bautz, G.E. Berman, J.P. Doty, and G.R. Ricker, "Charge-coupled-device x-ray detector performance model," Optical Engineering, **26**, 757, 1987.

[9] G.R. Hopkinson, "Analytic modeling of charge diffusion in charge-coupled-device images," Optical Engineering, **26**, 766, 1987.

[10] S. Holland and H. Spieler, "A monolithically integrated detector-preamplifier on high-resistivity silicon," IEEE Trans. Nucl. Sci., **37**, 463 (1990).

[11] Technology Modeling Associates, Inc.

[12] L.B. Robinson, R.J. Stover, J. Osborne, J.S. Miller, S.S. Vogt, and S.L. Allen, "Lick Observatory charge-coupled-device data acquisition system," Optical Engineering, **26**, 795, 1987.

[13] S.E. Holland, N.W. Wang, and W.W. Moses, "Development of low noise, back-side illuminated silicon photodiode arrays," to be published.