The SVX II Silicon Vertex Detector at CDF

STEVEN WORM†
New Mexico Center for Particle Physics,
Department of Physics and Astronomy, University of New Mexico,
Albuquerque, New Mexico 87131, USA

The CDF silicon vertex detector is being upgraded for use in Run II of the Fermilab collider. The increased luminosity in Run II, coupled with the desire for increased acceptance and secondary vertex triggering, necessitates a complete redesign of the previous generation tracker. Details of the design are described.

1 Introduction

A silicon vertex detector (SVX II) is currently being constructed for the upgraded Collider Detector at Fermilab (CDF) [1]. Upgrades to Fermilab's Main Injector will increase the luminosity to $\sim 10^{32}$ cm^{-2}s^{-1}, with a higher number of bunches and a shorter bunch spacing (396 ns and ultimately 132 ns). These factors necessitate a complete redesign of the silicon sensors and data acquisition system. Features of the SVX II include:

- Five layers of double-sided silicon strip sensors with both 90° and small-angle stereo.
- Three dimensional vertex reconstruction with $\sigma_{r\phi} < 30$ μm and $\sigma_z < 60$ μm for central tracks.
- Radiation hardness to a luminosity to 3 fb^{-1}. The dose for the inner layer is expected to be 0.5 Mrad/fb^{-1}.
- Extensive coverage of the interaction region and tracking to $|\eta| < 2$.
- A "deadtimeless" data acquisition system designed to allow SVX II data to be processed for a vertex-based trigger.

The SVX II has been designed to operate in a high luminosity environment and maintain high acceptance for b and top events. It incorporates three-dimensional tracking and the ability to trigger on secondary vertices. The combination of 90° and small-angle stereo sensors has been selected on the basis of z resolution and pattern matching to outer tracking systems, and will improve background rejection for heavy flavor analyses [2]. High-speed readout and processing allows SVX II data to be used in the Level 2 trigger. This ability to *trigger* on secondary vertices is important for all analyses with heavy flavor signatures.

†Representing the CDF Collaboration

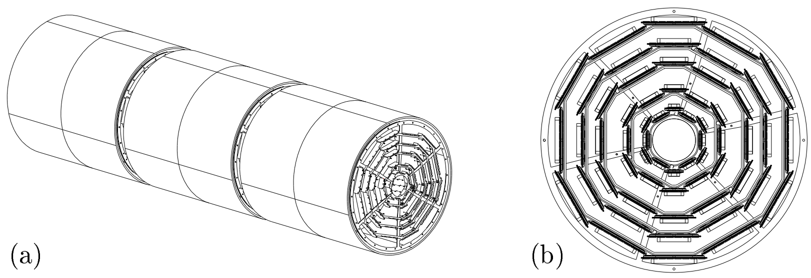

Figure 1: The SVX II consists of three barrels placed end-to-end (a). The bulkheads (b) provide structural support for the detector.

2 Mechanical Design

The SVX II is segmented into three barrels, each 29 cm long. Each barrel end contains 12 wedges in ϕ, with each wedge comprised of 5 layers of silicon sensors placed radially from 2.45 cm to 10.65 cm. The silicon is mounted in structural units, or ladders, of four sensors. These ladders are fixed to a beryllium bulkhead at the end of each barrel which also contains cooling channels for the electronics. Both the barrel and bulkhead layouts can be seen in Figure 1.

The SVX II ladders are formed of boron-carbon fiber with a Rohacell foam core. This composition has the same thermal expansion coefficient as silicon, to minimize thermal stresses. The sensors on each ladder are wire bonded in pairs and read out near the ends. These pairs form electrical units that are bonded to the readout chips on an electrical hybrid.

The bulkheads serve as heat sinks for electrical components mounted nearby and provide precision alignment of the ladders. A cooling channel for each layer is machined directly into each bulkhead to improve thermal conductivity. Coolant circulated in this channel should maintain the silicon sensors near 13 °C (based on a thermal load of 425 mW per readout chip set) [3]. An open half-cylinder support is provided to hold and align all three barrels. This support, or spaceframe, allows position adjustability in (r, θ, z) within (± 100 μm, ± 250 μrad, ± 1 mm).

3 Silicon Sensors

Double sided AC coupled strip sensors are being used for all 5 layers of the SVX II. There are three layers of 90° stereo sensors (Layers 0, 1, and 3) and two layers of small-angle sensors (Layers 2 and 4). Hamamatsu Photonics supply

Property	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
stereo angle (deg.)	90	90	+1.2	90	−1.2
$r\phi$/Z strips	256/512	384/576	640/640	768/512	896/896
$r\phi$/Z chips	2/2	3/3	5/5	6/4	7/7
$r\phi$/Z strip pitch (μm)	60/141	62/125.5	60/60	60/141	65/65
total width (mm)	17.140	25.594	40.300	47.860	60.170

Table 1: Mechanical specifications of the sensors.

the Layer 0, 1, and 3 sensors, and Micron Semiconductor provide Layers 2 and 4 [4]. All sensors are made from high-resistivity n-type silicon. The nominal silicon thickness is 300 μm for 90° sensors and 275 μm for the small angle sensors.

Readout is accomplished by aluminum strips AC coupled to the implant strips, with the p-side measuring $r\phi$ (longitudinal) and the n-side measuring z (or $r\phi'$). The sensors are biased through polysilicon resistors on each side. Isolation on the n-side is maintained by a modified common p-blocking implant between the readout strips. Properties of the sensors can be found in Table 1. On the n-side of the 90° stereo layers, several strips are multiplexed together and read out through one channel. Multiplexing varies by layer to eliminate ghost tracks. Layer 2 and 4 sensors are directly read out at the ladder ends.

The geometric features and materials have been chosen to maximize the radiation hardness of the sensors. Inner layers, however, are expected to undergo type inversion and will need to be replaced after ~ 1.5 Mrad (2 to 3 fb^{-1}).

4 Data Acquisition

Readout of the silicon sensors is accomplished through readout chip sets (SVX3) on electrical hybrids mounted on the ladders. For each wedge (44 SVX3 chips), copper/Kapton laminate cables (high density interconnects – HDI) from the hybrids carry signals to a single port card (PC). The PC converts the digital output of the SVX3 chips to an optical signal that is carried to VME crates located outside the CDF detector. Optical signals are generated in the PC by dense optical interface modules (DOIMs) operating at 53 MHz. At the VME crates, a fiber interface board (FIB) serializes the data from the DOIMs onto a high speed optical link (HP G-link) operating at 1.5 GHz. In addition, the FIBs sends control and clock signals to the PCs. From the FIB, data travel 80 m to the counting house where it is optically split and sent not only to VME readout buffer cards (VRBs) to await readout, but also to a separate

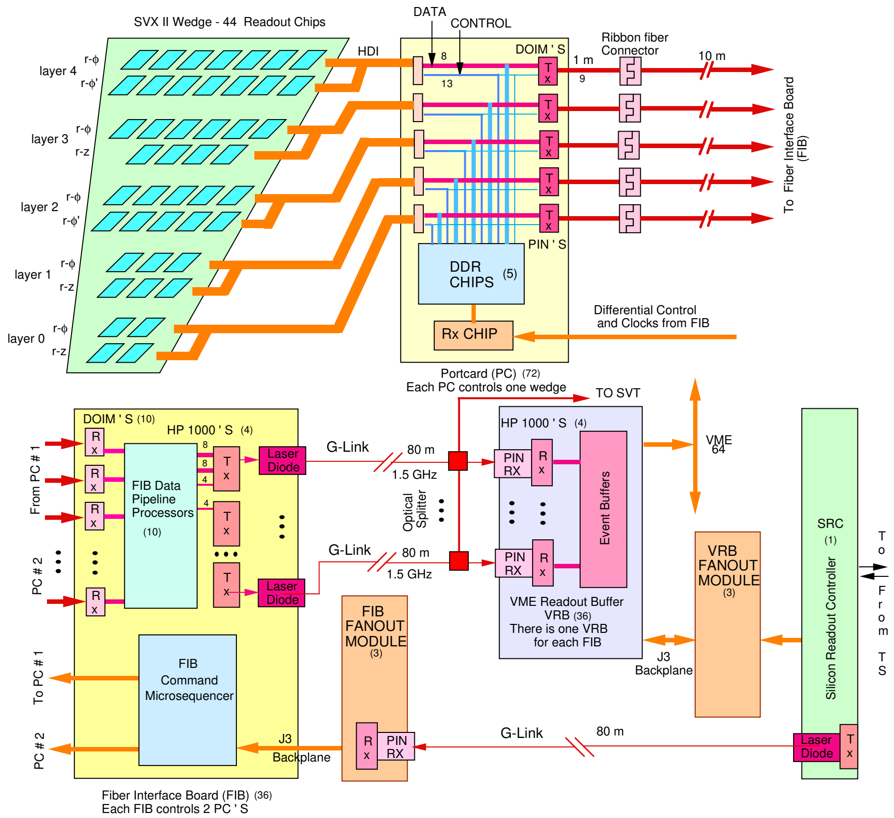

Figure 2: SVX II data acquisition system.

trigger processor that prepares SVX II data for use in the trigger. Control of this system is accomplished by a silicon readout controller (SRC) which sends commands to the VRBs and FIBs. The FIBs in turn control the PCs. The entire readout architecture can be seen schematically in Figure 2.

The SVX3 chip set [5] consists of a pair of radiation hardened CMOS chips. The front end chip acts as a 128 channel dual-ported analog pipeline with skip logic (42 cell depth) and allows up to 4 cells to be reserved for digitization. The back end chip provides an 8 bit ADC, data sparsification, and multiplexing features. By dual porting the pipeline and separating analog and digital functions into two concurrently functioning chips, readout deadtime is essentially eliminated for trigger rates below 50 kHz ("deadtimeless" operation). The RMS noise of the SVX3 is expected to be around 1700 electrons (assuming 20 pF sensor input capacitance and a chip optimized for 132 ns crossing times).

5 Conclusion

The CDF SVX II, designed for the high luminosity environment of Run II, will provide tracking and vertex reconstruction in three dimensions and to $|\eta| < 2$. Advances in data acquisition allow events reconstructed in the SVX II to be processed for use in the Level 2 trigger. These features will significantly enhance the heavy flavor physics program at CDF.

References

1. "CDF Upgrade Technical Design Report" D. Amidei, Ed., CDF Internal Note Number 3777.
2. "SVXII Simulation Study And Upgrade Proposal", CDF Internal Note Number 1922 (1992).
3. "Thermal Analysis of the CDF SVX II Silicon Vertex Detector", P. Ratzmann, FERMILAB-PUB-96/031-E (1996). To be published in *Nuclear Instruments and Methods*.
4. Hamamatsu Photonics KK, Solid State Divison, Hamamatsu, 435 Japan, and Micron Semiconductor Limited, Lancing, Sussex BN15 8UN, UK.
5. Operational details found in "A Beginner's guide to the SVX2", Ray Yarema *et al.*, FERMILAB-TM-1892 (1994). SVX3 specifications are found in "Device Specifications for the SVX 3 Readout Chip Set", R. Strohmer and W. Knopf, FERMILAB-ESE-SVX-950703.