The Silicon Tracking Upgrade at CDF

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Abstract

The Collider Detector at Fermilab (CDF) is scheduled to begin recording data from Run II of the Fermilab Tevatron in early 2000. The silicon tracking upgrade constitutes both the upgrade to the CDF silicon vertex detector (SVX II) and the new Intermediate Silicon Layers (ISL) located at radii just beyond the SVX II. Here we review the design and prototyping of all aspects of these detectors including mechanical design, data acquisition, and a trigger based on silicon tracking.

[1] Representing the CDF collaboration

1 Introduction

CDF is a general purpose experiment for the study of $p\bar{p}$ collisions at a centre-of-mass energy, $\sqrt{s} = 1.8\,\mathrm{TeV}$. In July 1995 Run I ended with a total integrated luminosity of $110\,\mathrm{pb}^{-1}$ and with typical instantaneous luminosities of $\sim 2 \times 10^{31}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In Run II, to begin in 2000, the goal is to accumulate about $2\,\mathrm{fb}^{-1}$ of data (20 times that of Run I) with typical luminosities of $2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The Run II centre-of-mass energy will increase to 2.0 TeV, and the bunch spacing will ultimately be 132 ns, significantly shorter than the $3.7\,\mu\mathrm{s}$ in Run I. The Run II Tevatron environment therefore provides significant challenges to designing the silicon tracking detectors, in addition to its three dimensional readout and deadtimeless data acquisition (DAQ) system.

In the latter part of Run I the silicon vertex detector (SVX′) consisted of 4 layers of single-sided silicon sensors with AC coupled strips and radiation hard readout chips [1]. This succeeded its rad-soft DC coupled version about $20\,\mathrm{pb}^{-1}$ into Run I [2]. Both silicon vertex detectors were 51 cm in length, consisting of 2 barrels partitioned in the transverse plane into 12 30° *wedges*, with the 4 layers ranging in radii from 3.0 cm to 7.8 cm.

The CDF upgrade for Run II [3] will include two mechanically separate silicon devices; SVX II, the successor of SVX′, and ISL, Intermediate Silicon Layers at radii in between the SVX II and the Central Outer Tracker (COT). The addition of the ISL to SVX II will allow precision standalone three dimensional tracking with up to 7 stereo and 7 axial measurements out to a pseudorapidity of $|\eta| < 2.0$, and a P_T resolution of $\frac{0.4\%}{P_T^2}$. With an expected radiation dose of $0.5\,\mathrm{Mrad/fb}^{-1}$ for the innermost SVX II layer, the SVX II will be radiation hard to an integrated luminosity of approximately $3\,\mathrm{fb}^{-1}$. A deadtimeless DAQ system will allow SVX II information to be used to trigger on secondary vertices, a tremendous asset for all analyses involving heavy flavour signatures.

2 Mechanical Design

The SVX II is composed of three identical barrels, each with an active length of 29 cm, with the nominal interaction point being in the centre of the middle barrel. A barrel is segmented,

Table 1: Mechanical specifications of the SVX II sensors.

Property	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
Radial distance (cm)	2.45	4.67	7.02	8.72	10.6
Stereo angle (degrees)	90	90	+1.2	90	-1.2
$r\phi/z$ readout channels	256/512	384/576	640/640	768/512	896/896
$r\phi/z$ readout chips	2/2	3/3	5/5	6/4	7/7
$r\phi/z$ strip pitch (μm)	60/141	62/125.5	60/60	60/141	65/65
Total width (mm)	17.14	25.59	40.30	47.86	60.17
Total length (mm)	74.3	74.3	74.3	74.3	74.3

in the plane transverse to the beam direction, into 12 wedges each spanning 30° in ϕ. Each barrel comprises 5 layers of silicon sensors placed radially from 2.45 cm to 10.6 cm. The geometry in the transverse plane is shown in Figure 1.

The ISL is composed of 3 layers, the radial positions and z ranges of which are shown in Figure 2. The layers lie at radii of 20 cm, 22 cm, and 28 cm respectively, and extend to a pseudorapidity of $|\eta| \sim 1.9$. The central layer ($|\eta| < 1.0$) covers the same η range as the CDF Central Outer Tracker (COT), a large open cell drift chamber for tracking at large radii ($40 < r < 137$ cm).

The basic structural unit for the SVX II and ISL is the *ladder*, though for each detector they are of somewhat different design. An SVX II ladder consists of 4 double-sided silicon microstrip sensors, with width and number of readout channels depending on the layer. A schematic of an SVX II half-ladder is shown in Figure 3. A full ladder is read out from both ends. The ladders are supported and aligned on both ends by precision machined beryllium bulkheads (see Figure 1), which have cooling channels (rectangular 1 mm $\times$ 8 mm) integral to them for the removal of heat generated by the frontend electronics (see below for a description of the cooling system). Some mechanical properties of the SVX II sensors for each layer are given in Table 1.

The ISL ladders will all be identical, comprising 6 silicon sensors (each with an active length of 72.4 mm and an active width of 56.3 mm), 3 of which will be read out at either end. All ISL sensors have a p-side and n-side strip pitch of 110 μm. The forward ISL ladders are also arranged in the 30° wedge geometry, however, to achieve sufficient arc coverage per wedge, 2 are needed for the layer at 20 cm, and 3 for the layer at 28 cm. Due to overlap requirements, the central ISL ladders, at 22 cm, are arranged with smaller ($\sim$ 13°) segmentation.

Details of the SVX II silicon microstrip sensors, together with design and test results (including irradiation tests), are the subject of 2 separate presentations in these proceedings [4, 5], and so only a cursory overview will be given here. Double sided AC coupled microstrip sensors are being used for all layers of the SVX II and ISL. SVX II layers 0, 1 and 3 are composed of 90° stereo sensors, while SVX II layers 2 and 4, and the ISL layers are made from small angle (1.2°) stereo sensors. All sensors are made from high-resistivity n-type silicon, with nominal thicknesses of 300 μm for the 90° stereo sensors and 275 μm for the small angle stereo sensors. Readout of the strips from the end of the sensors is achieved through aluminium strips AC coupled to the implant strips with the p-side measuring the r-ϕ position, and the n-side measuring the z position (or r-ϕ' for the small angle stereo sensors). Readout of the r-z strips at the end of the sensor requires the double metal layer technology. These 90° stereo sensors (layers 0, 1 and 3) are manufactured by Hamamatsu Photonics using 4" silicon wafers. The SVX II sensors for layers 2 and 4, and the sensors for the ISL outer layers (all small angle stereo) are manufactured by Micron Semiconductor using 6" wafers. (The inner ISL layer uses 4" wafers with the vendor as yet not determined.) For both the SVX II and the ISL the strip pitch equals the readout pitch. The total number of SVX II readout channels is 405,504 (211,928 from the p-side (r-ϕ) and 193,536 from the n-side (z or r-ϕ')). The ISL adds a total of 307,200 readout channels.

3 Cooling and Interlocks

Supplying adequate cooling to the SVX II is crucial for its survival. Cooling issues are less of a concern for the ISL due its larger radius from the beam line and the fact the readout chips are mounted off the silicon, however for convenience the ISL cooling system will be very similar to that for the SVX II. The cooling system is designed to keep the silicon temperature less than $\sim 15^\circ$C for nominal operating conditions, and to prevent thermal runaway in the innermost layer at the maximum expected chip power dissipation for $2\,\mathrm{fb}^{-1}$ of integrated luminosity (corresponding to a 1.0 Mrad dose).

The SVX II (ISL) heat load is about 1.4 kW (1.0 kW) from the SVX3 chips, and 1.0 kW (0.4 kW) from the port cards, giving a total of 4.0 kW for the entire silicon tracking system. Simulation and test stand studies have shown that the SVX II cooling system design requirements can be met by flowing a 30% glycol/water mixture at a rate of ~ 23 kg/min. The minimum temperature at the chiller is -10°C which translates to a bulkhead ledge temperature of $\sim 0^\circ$C, and a silicon temperature of $\sim 12^\circ$C.

All power to the SVX3 chips, silicon ladders and port cards will be provided by custom power supplies from CAEN (one power supply per wedge). Monitoring of silicon and bulkhead temperatures, cooling system variables (flows and pressures), and the power supplies, will be done using a programmable logic controller (PLC) and commercial monitoring software. Interlocking of the power supplies will occur if the monitored temperatures and/or cooling system pressures fall outside some preset ranges.

4 Data Acquisition System

Signals from the silicon sensors are read out by "SVX3" chips [6], which perform signal integration, analog pipelining to provide the delay required by the Level 1 trigger, digital conversion, and data sparsification for each of the 128 channels per chip. The SVX3 chip is designed for fabrication in the Honeywell 0.8 micron radiation hard process and is shown schematically in Figure 4. The SVX3 has been divided into a "front end" (SVX3FE) and a "back end" (SVX3BE). The SVX3FE contains an integrator, a dual ported analog pipeline, and the logic necessary for removing cells from the pipeline (42 cells deep) that are flagged by triggers and queuing them for digitization. Up to 4 cells can hold data for later processing. The pipeline also contains a reference cell, giving 47 pipeline cells per channel in total. The maximum delay length of the pipeline is 42 cells, which, at 132 ns beam crossings corresponds to $5.5\,\mu$s. The SVX3BE provides digitization, sparsification and readout functions.

The SVX3 has the distinct capability to continuously perform the analog data acquisition during digitization and readout. This allows deadtimeless operation for Level 1 trigger rates up to 50 kHz. Complete readout of SVX II (both r-ϕ and r-z sides) by the SVX3 chips is expected to take about 10 μs. The equivalent noise charge (ENC) has been measured to be $500 + 60$e/pF rms, which for a typical sensor with a 20 pF input capacitance, gives an rms noise of 1700 ENC. This can be compared to an expected signal of $\sim$ 24000 electrons for a 90° track. Radiation hardness has been demonstrated with the SVX3 chips working within specifications after doses of 2 Mrad. Production SVX3 chips are expected to be ready from Honeywell by the middle of 1998.

The SVX3 readout chips are mounted on electrical hybrids that process detector signals for the port card (see below). The ISL DAQ system is essentially identical to that for SVX II, the major difference being in the hybrid design and placement. The SVX II hybrids are constructed of thick film on BeO ceramic (500 μm), and are mounted directly on the ladders. For the ISL the hybrids are thick film on Aluminium Nitride and are mounted off the ladders.

From the port cards out, the ISL DAQ is the same in design as that for SVX II, and so for brevity only the latter will be discussed further. For each SVX II wedge of 44 SVX3 chips, high density interconnects (HDI's, Copper/Kapton laminate cables) from the hybrids carry signals to a single port card (PC). One function of the PC is to convert the digital output of the SVX3 chips to an optical signal by way of 5 dense optical interface modules (DOIM's) operating at 53 MHz. There is one DOIM and one HDI per layer of a wedge. These optical signals are carried to the rest of the DAQ, beginning with the fibre interface board (FIB), which serializes the data from the low speed fibre system (DOIM's) onto a high speed optical link (G-Link) operating at 1.5 GHz. One FIB multiplexes the readout data from 2 PC's. The G-Links carry data to VME readout buffer cards (VRB's) which hold the data until a Level 2 trigger decision is received. The VRB (one per FIB) then sends the data off to Level 3 if a Level 2 accept was received. The data from the FIB is also optically split to the Silicon Vertex Tracker (SVT), a level 2 trigger processor (see below). The master controller for the SVX II is the silicon readout controller (SRC), which communicates with the CDF trigger supervisor (TS). The FIB generates control signals for the PC based on commands sent from the SRC. The PC relays these control signals to the SVX3 chips through the HDI's. In addition the PC's provide power to the chips through the HDI's. The entire DAQ architecture is schematically shown in Figure 5. A complete prototype DAQ system, which used a test stand version of the port card and copper interfaces instead of DOIM's, was successfully used under test beam conditions.

5 Silicon Vertex Trigger

The SVT trigger mentioned above uses the SVX II data (with each wedge read out in parallel) to obtain impact parameter [2] information to be used in a level 2 trigger. The SVX II is read out after each level 1 trigger ($\sim 40\,$kHz accept rate). The SVT combines r-ϕ SVX II data (read out in $\sim 6\,\mu s$) with tracking information from the COT, with a total execution time of $\sim 15\,\mu$s (including readout). The CDF level 2 trigger has an accept rate of $\sim 300\,$Hz ($\sim 20\,\mu$s processing time) giving a deadtime $\leq 10\%$. The level 3 trigger writes events to tape at a rate of $\sim 50\,$Hz. The impact parameter resolution of the SVT track fits are nearly as good as offline reconstruction. The expected impact parameter resolution (at $P_T = 2\,$GeV) is $\sigma_d = 35\,\mu$m, and the azimuthal and P_T resolutions are $\sigma_\phi = 1\,$mrad and $\sigma_{P_T} = 0.3\% P_T^2$ (where P_T is in GeV) respectively. Applying impact parameter cuts at level 2 will drastically increase the efficiency for heavy flavour physics processes.

6 Conclusion

The CDF silicon tracking upgrade, comprising the SVX II and ISL detectors, will provide standalone 3 dimensional silicon tracking in the very challenging Run II Tevatron environment. Both detectors are making encouraging progress towards their readiness for Run II scheduled to begin in 2000. The ability to trigger on impact parameter information from the SVX II will greatly enhance the physics reach, particularly for heavy favour analyses, in what promises to be an exciting Run II physics program at CDF.

[2] Impact parameter is defined as the perpendicular distance from the interaction point to the track in the transverse plane.

References

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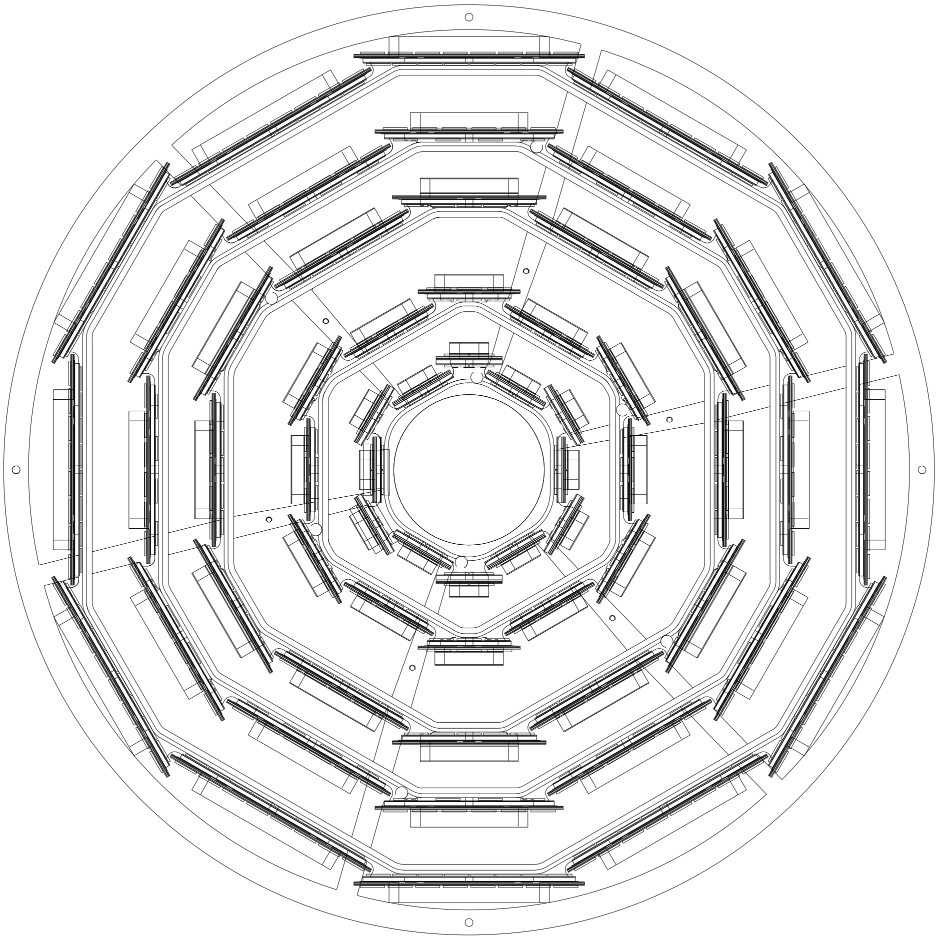

Figure 1: End view of an SVX II bulkhead providing structural support for the ladders.

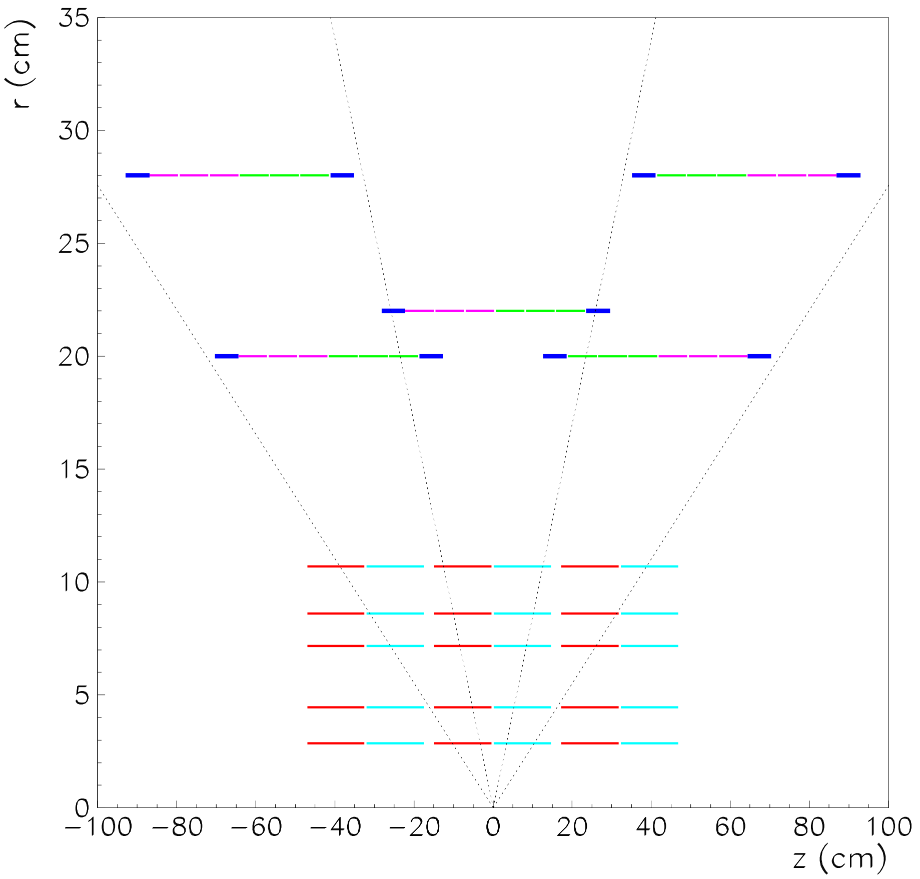

Figure 2: View of the SVX II and ISL detectors in the r-z plane. The z direction is along the beamline. The lines from $z = 0$ represent pseudorapidities, $\eta = -\ln(\tan\frac{\theta}{2})$, of 1 and 2.

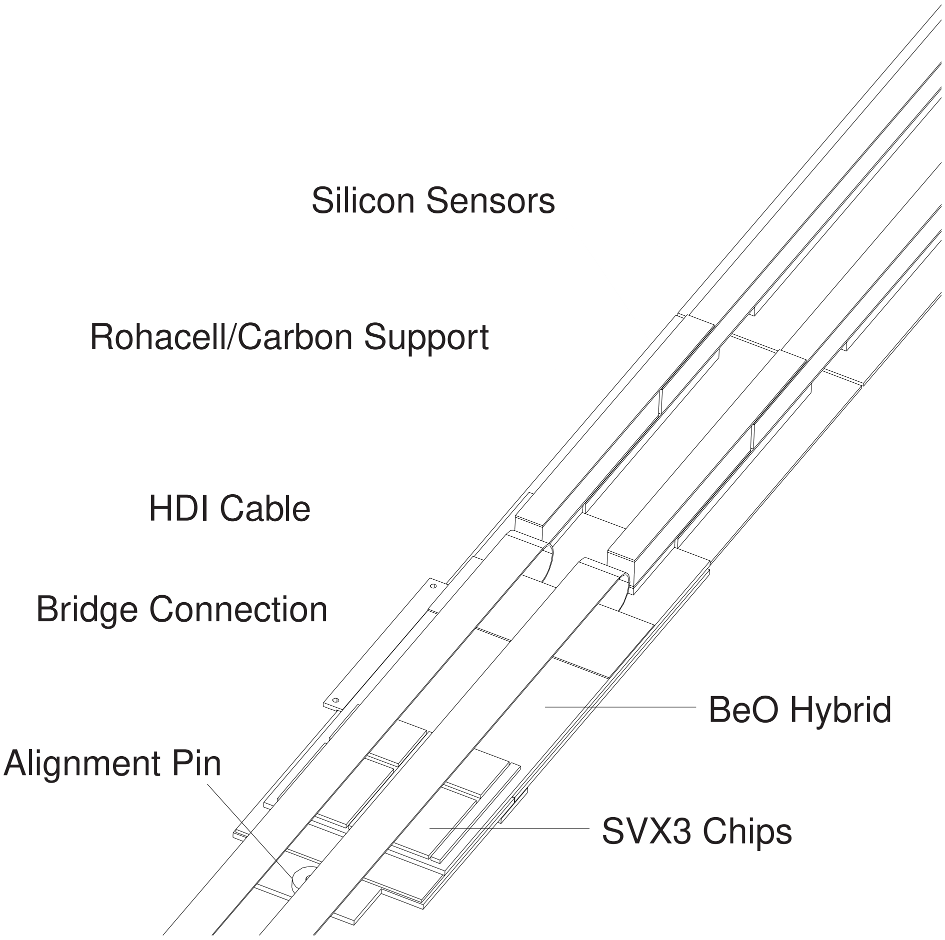

Figure 3: Schematic of an SVX II layer 0 half-ladder consisting of 2 silicon sensors. Electronics for the readout are mounted on the first sensor. The z-side SVX3 chips are on the underside and are not visible.

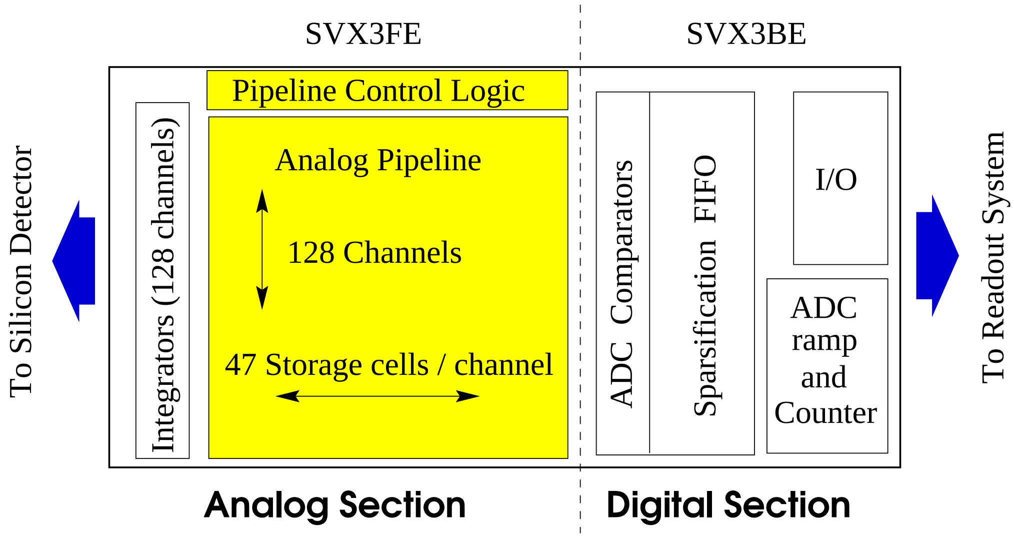

Figure 4: Schematic of the SVX3 readout chip. The approximate chip size is $6.26 \times 12.0\,\mathrm{mm}^2$. A single chip reads out 128 silicon microstrips.

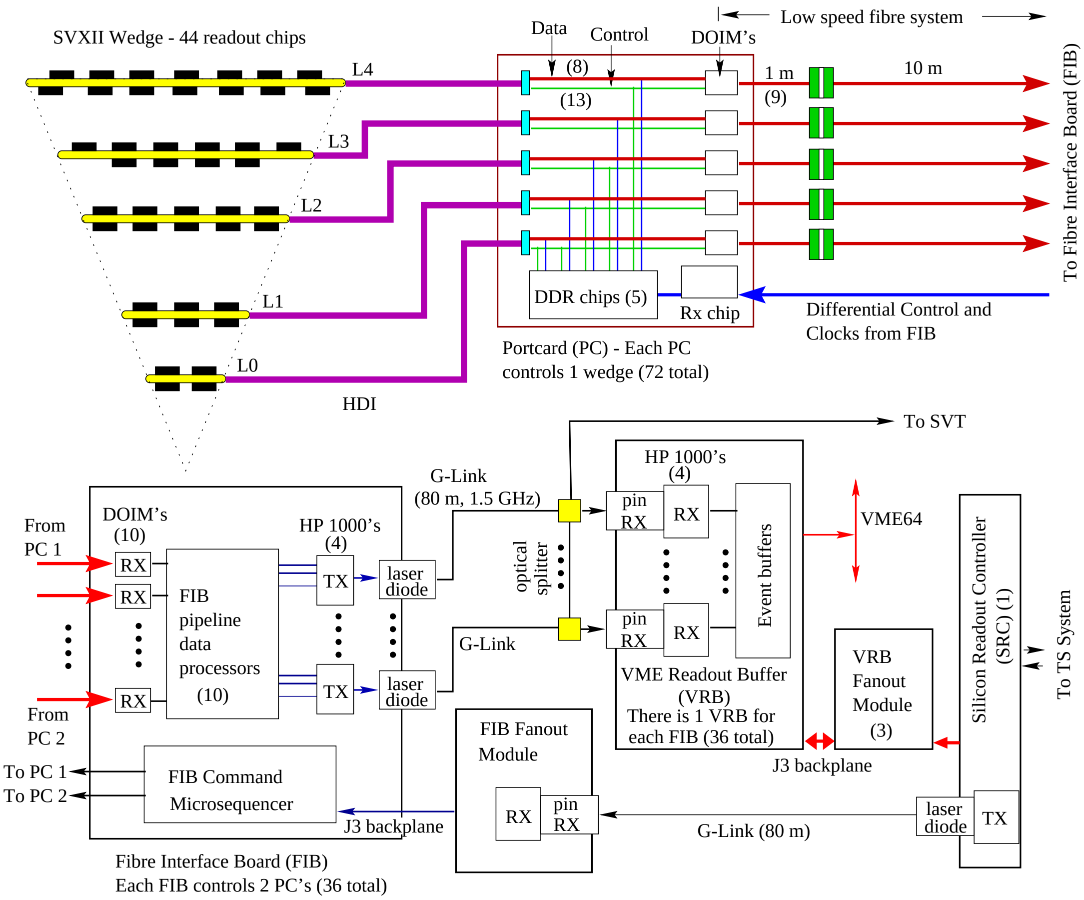

Figure 5: Schematic of the SVX II data acquistion system. The upper half shows the frontend readout mounted on or near the SVX II. The FIB system is in VME crates on the sides of the CDF detector, and the VRB system and SRC are in the counting room.